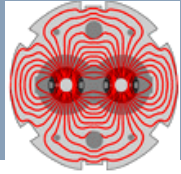
FGClite communication failures



- With FGClite the PC regulation moves from the FGC to the gateway (minimize radiation sensitive elements).
  - *The regulation loop is running in the gateway, transmitting new voltage references (not current !) to the PC over the WorldFIP bus.*
  - *References are sent at 50 Hz (previously 1 kHz).*
    - This renders the regulation more difficult and delicate, see the case last weekend when a noisy BPM led to a PC failure through the regulation levels.
- An obvious new failure is the loss of communication between FGClite PCs and their gateway (one, two … all) due to a gateway, WorldFIP etc issue.
  - *The PC will not even be able to maintain a constant current since it will keep the last voltage reference.*
  - *In the event of a communication loss reboots of the affected converters are initiated after 10 seconds (+ some time staggering of the PCs).*

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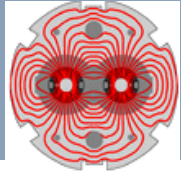

- SIS ignored communication failures for FGC2 because it was difficult to separate transient CMW issues from real faults (for example due to radiation).
  - *A beam dump is triggered only when a 60A state is changing to fault.*
- A separate interlock logic was setup to react on communication faults.
  - *The SIS acquisition buffer bridges 4 seconds in case of missing data.*
  - *After that timeout communication faults are recorded.*
  - *After three consecutive evaluations (3 x 2 seconds) where at least one comm. fault is present and the sum of the kicks (absolute values) is > 6 urad, SIS will trigger a beam dump.*
    - Separate logic for B1 and B2.
  - *Interlock is already active.*
- The interlock was tested and tuned by cutting the incoming communication to SIS. A real test of a gateway communication problem will be organized ~next week with EPC.