Circuits description and requirements
- Closed Session-

Félix Rodríguez Mateos
(on behalf of the HL-LHC Magnet Circuit Forum)

HL-LHC Cold Powering Review – 4th July 2017

A recap on the definition of voltage withstand levels from previous Reviews:

Test voltage procedure

Acceptance /Reception

Manufacturer & 1st test at arrival to test bench

300 K, 1 bar , AIR

$V2$

$V2 = 2 * V1$

1st test at cold in the test bench

Nominal operating conditions

$V1$

$V1 = 2 * U_{Coil\ to\ gnd} + 500$

Installation

1st test after cold test in air but possibly with He gas

300 K, 1 bar , He (gas)

$V3$

$V3 = \frac{V1}{5}$

Test at cold after acceptance or reception test

Nominal operating conditions

$V4$

$V4 = 1.2 * U_{Coil\ to\ gnd}$

Harmonizing strategies for HV levels definition

Felix Rodriguez Mateos, TE-MPE-EE

HVWL Discussion Group, 30 September 2015

Reference documents

1. “Voltage withstand levels for electrical insulation tests …” EDMS 90327
2. “ELQA Qualification of the superconducting circuits during hardware commissioning” EDMS 788197

Strategy for LHC (initially) -1

- The max quench voltage was calculated to ground [and to heaters, see later], lets call it **Uq-g** (worst case value in case of a quench, to ground, including realistic failure scenarios)
- This voltage was obtained from simulations and tests and is composed of three terms:
  - Uq-g= U max coil + U ee + U overshoot
  - (e.g. for dipoles is Uq-g = 700 V+ 500 V+ 0.2*500 V= 1300 V)
- The minimum withstand voltage at working cryogenic conditions is
  - **Uq-g, test= 2*Uq-g+500 [V]** from the IEEE standard 95-177, or 2*1300+500= 3100 V

Strategy for LHC (initially) -2

- For heaters, the voltage was calculated assuming different polarity in coil and heater itself. At that moment we were expecting to power heaters with ±400 V, hence
  - Uq-h= 700V +400V = 1100V
  - Uq-h, test= 2*1100V+500V= 2700V

- These voltages (to-ground and to-heater) are defined levels for components during **cryogenic tests** (nominal working conditions) after production and prior to installation in the tunnel

Strategy for LHC (initially) -3

How to translate these values to the following:

- Tests at warm after cold testing?
  - It was assumed that tests at warm at reception at CERN premises, prior to cold testing, be done at the same level as the final test at factory under same conditions (T, p, humidity, etc)
  - It was decided that in order to get the levels to be applied at warm, lower by a **factor of 5** the levels at cold (i.e. **Uq-g, test**)

- Tests at cold in the machine?
  - In general a **factor of 1.2** was applied to **Uq-g**, with the exception of the dipoles where a worst case value considering a short to ground was directly taken:

RB (1900 V = 700 V+ 600 V+ 600 V)
RCS (1.2*400 V= 480 V)

Revision in 2012 by R Mompo et al

- A review of the reference values was conducted:
  - RB test level at cold was 2100V instead of 1900V
  - Full ElQA
    - RQs alone 500V
    - Spools 1000V
  - Partial qualification RQs (incl. to spools) 800V
  - Nested magnets
    - 1.2*__2__*Uq-g
  - New proposed values for TP4 and MIC

Underlined was to consider “cross talk” between circuits

Are we proposing less for HL-LHC?

- Taking the present inner triplets in LHC as example:

Values applied today to LHC's inner triplets during ElQA

CIRCUIT	Maximum Discharge voltage to ground [V]	Maximum expected voltage to ground at quench [V]	Min. Design withstand voltage at working cryogenic conditions [V]		Test voltage to ground [V] for system warm	Test voltage to ground [V] for system cold (1.2*Umax)
			To ground	To heaters		
LowBeta Quads (KEK)	0	350	1200	1400	240	420
LowBeta Quads (FNL)	0	350	1200	1400	240	420

Tests on LHC's Bus Bars and DFBs

3 - Test of the bus bars after installation in the DFB, the current leads not connected, in air at T=300K and P=1bar; leakage currents given per double length

Circuit rating (A)	U (V)	I (μ A)	Duration (s)
120	4000	1	120
600	4000	1	120
6000	3000	10	120
13000	5000	40	120

V2

4 - Test of all DFB electrical circuits, the current leads connected, in gaseous helium at t=300K and P=1bar; leakage currents given per double length

Circuit rating (A)	U (V)	I (μ A)	Duration (s)
120	300	1	30
600	300	1	30
6000	260	10	30
13000	620	40	120

V3

"Voltage withstand levels for electrical insulation tests …" EDMS 90327

- Subsequent tests at cold follow the values for circuit as specified
- NB. LHC dipoles have 1000 V of energy extraction at both extremities, HL-LHC inner triplets don't

Electrical insulation test levels for link and bus bars

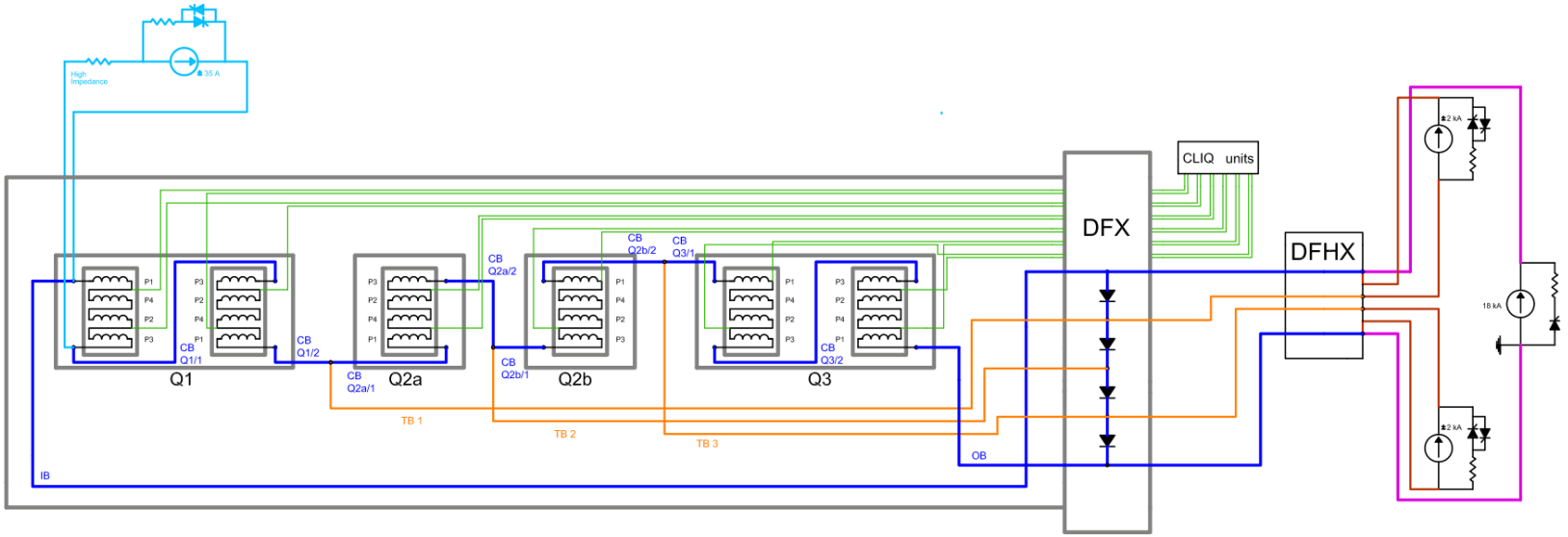
Rating (kA)	Worst case voltage to ground during operation (V)	Acceptance tests of components to ground (V)		Insulation test voltage of system to ground (V)		Leakage current per component (µA)	Test duration (s)
		RT	NOC	RT	NOC		
18	900	4600	2300	460	1080	≤10	30
7	900	4600	2300	460	1080	≤10	30
2	540	3160	1580	316	648	≤10	30
0.2	540	3160	1580	316	648	≤10	30
0.12	40	1160	580	220	360	≤10	30
0.035	900	4600	2300	460	1080	≤10	30

Table: Test voltage of leads and cables and calculated highest voltage to ground during operation. For the 18 kA and 7 kA cables, the highest voltage is estimated to be 700 V (across the high resistance of Q1a trim) + 100 V (sum of voltages across crowbar and cables resistances) + 100 V (superconducting cable in the link resistive along the full length). For the 2 kA and 0.2 kA cables, an energy extraction of 500 V is considered (worst case scenario). For the 0.12 kA circuits the crowbar voltage across the power converter is taken into account for the calculations.

RT: Room temperature
NOC: Nominal operating conditions

Cold diodes option

- The Internal Review Panel (March 2017) recommended to carry out studies related to the integration of cold diodes in a way to further optimize the circuit as cold diodes would bring in clear advantages:
  - Decoupling of warm and cold parts of the circuit
  - Avoiding the large current unbalances flowing through the sc link
  - Making the circuit more robust with respect to variability of scattering of quench resistances in the different magnets due to delays in protection actions and/or inherent magnet properties (RRR, Cu/non-Cu, strand diameter, quench location, etc)
- But diodes have to be qualified with respect to:
  - Integration in the cold environment (bus bar section for options being studied at present)
  - withstand the current pulses according to the circuit time constants
  - tolerate with margin the radiation doses expected at their final position (roughly 1 order of magnitude above LHC)



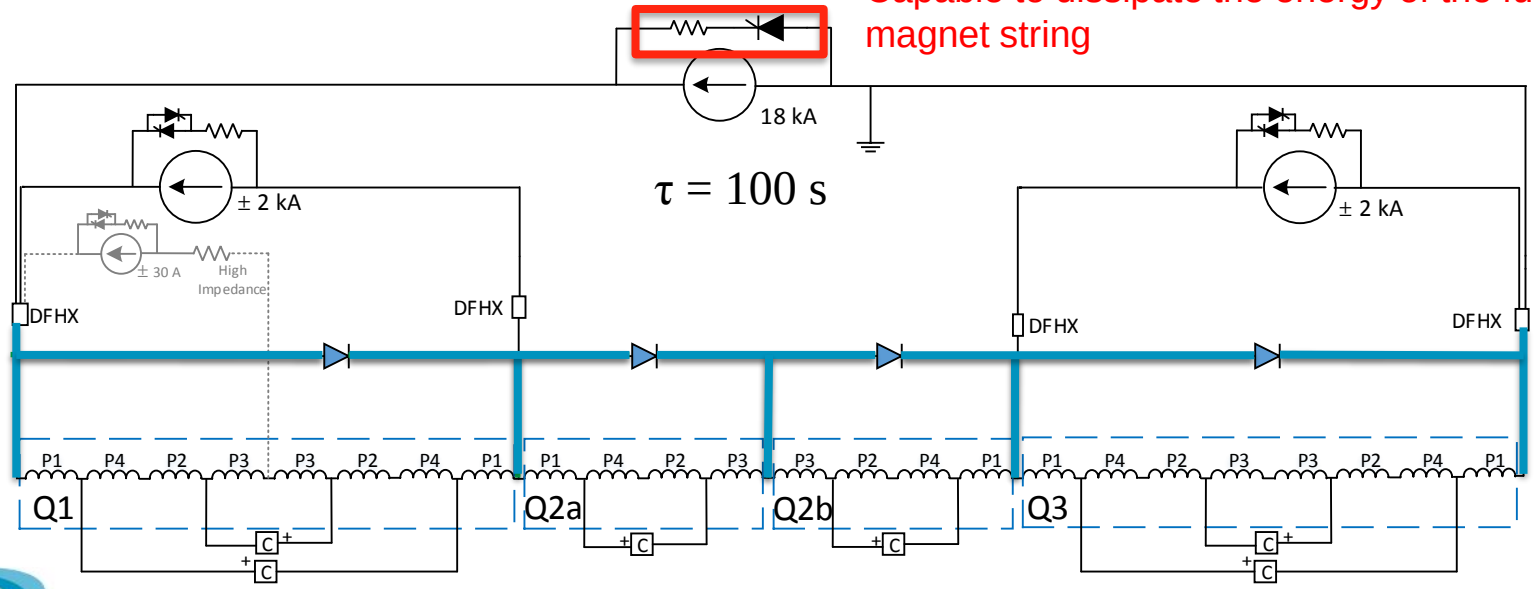
Optimization: Cold Diodes

2 options

- τ = 100ms
- τ = 100 s

- 7 kA
- 18 kA

Capable to dissipate the energy of the full magnet string



Conclusions

- The HL-LHC circuits baseline in terms of powering and protection has been consolidated through two Reviews and the teamed work within the Magnet Circuit Forum where all the relevant WPs are represented
- Inputs to the design of cold powering have been defined and are documented
- Optimization in the case of the inner triplet main circuit is ongoing and should not have a major impact into the cold powering baseline (provided decisions are taken with sufficient anticipation)
- A few open points require a follow-up but there is no showstopper identified as of today

Thank you very much for your attention