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and related detectors

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Development of a new Front-End electronics in Si and Si-Ge technology for the Resistive Plate Chamber (RPC) detector for high rate experiments

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Summary

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- ***The new Front End Electronics***
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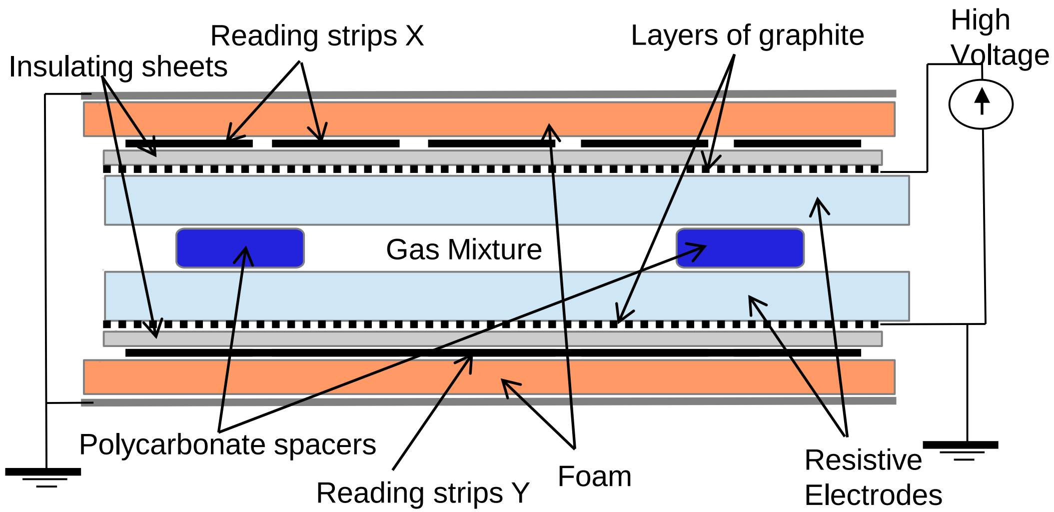
RPC rate capability and improvements for high rate experiments

The **RPC rate capability** is mainly limited by the current that can be driven by the high resistivity electrodes. It can be improved working on a number of highly interconnected parameters.

$$V_{gas} = V_a - R \cdot I$$

$$V_{gas} = V_a - \rho \cdot \frac{d}{S} \cdot \langle Q \rangle \cdot S \cdot \Phi_{particles} = V_a - \rho \cdot d \cdot \langle Q \rangle \cdot \Phi_{particles}$$



There are several possible ways to increase the detectable particle flux:

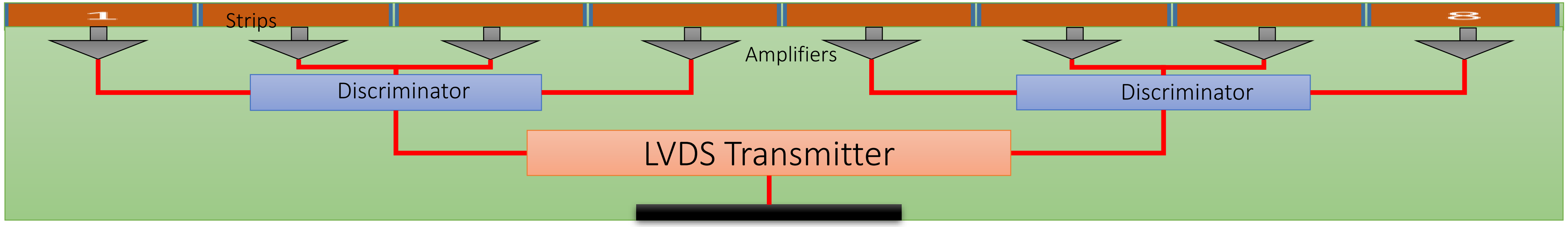
1. Decrease the electrode resistivity; large technological effort, with the risk of increasing its operating current, causing a possible ageing problems due to the more current driven.
2. Reduce the electrode thickness; similar effect obtained with the reduction of the resistivity.
3. **Reduce the average charge per count Q. This method is the only one that permits to increase the rate capability while operating the detector at fixed current.**

This last approach requires:

- Very sensitive FE electronics with an excellent signal to noise ratio
- High suppression of the noise induced inside the detector by the electronics and by external sources
- Very careful optimization of the chamber structure as a Faraday cage.

The new Front-End final design

8-channels Front-End Board composed by the new Amplifier, the full-custom ASIC Discriminator and the LVDS transmitter

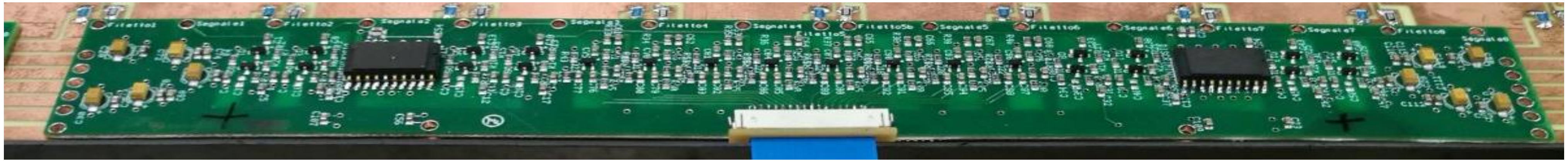


Amplifier Properties

- Si standard component
- Amplification factor: 2-4 mV/fC
- Power Consumption: 3-5 V 1–2 mA
- Bandwidth: 100 Mhz

Discriminator Properties

- SiGe full custom
- Power Consumption: 2-3 V 4-5 mA
- Threshold: 0.5 mV
- Bandwidth: 100 MHz



Full-Custom Amplifier

The Amplifier developed in Rome Tor Vergata for the RPCs is made in **Silicon Bipolar Junction Transistor** technology. The main feature of this new kind of amplifier is a fast charge integration with the possibility to match the input impedance to a transmission line. The working principle of this amplifier is shown in Figure 3. The performance of the silicon BJT amplifier are shown in the following table.

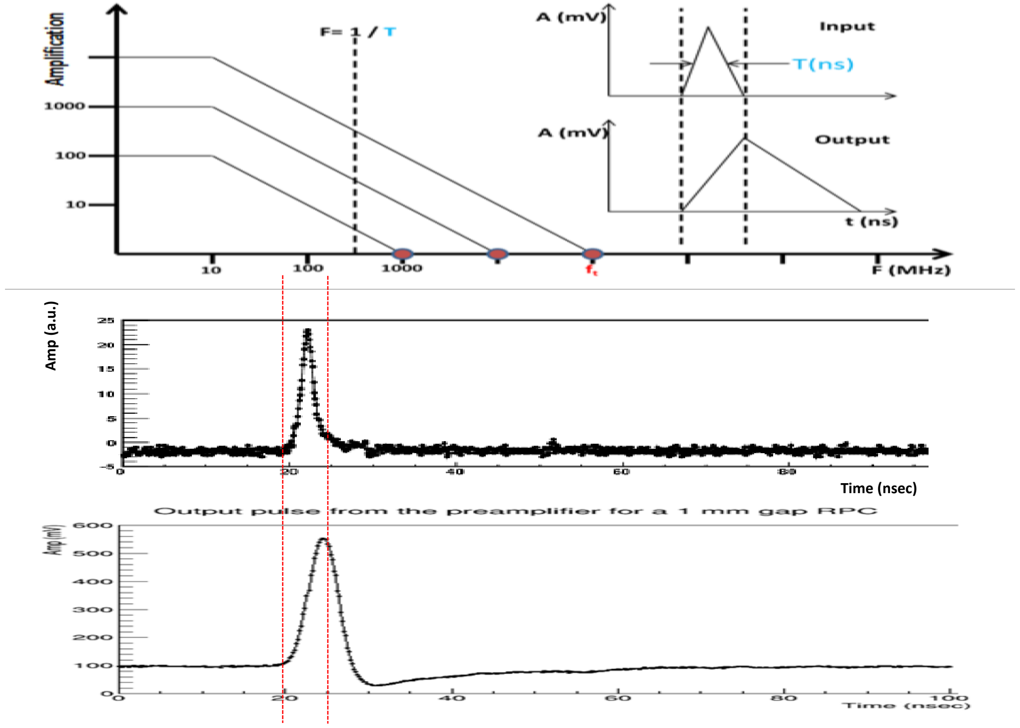


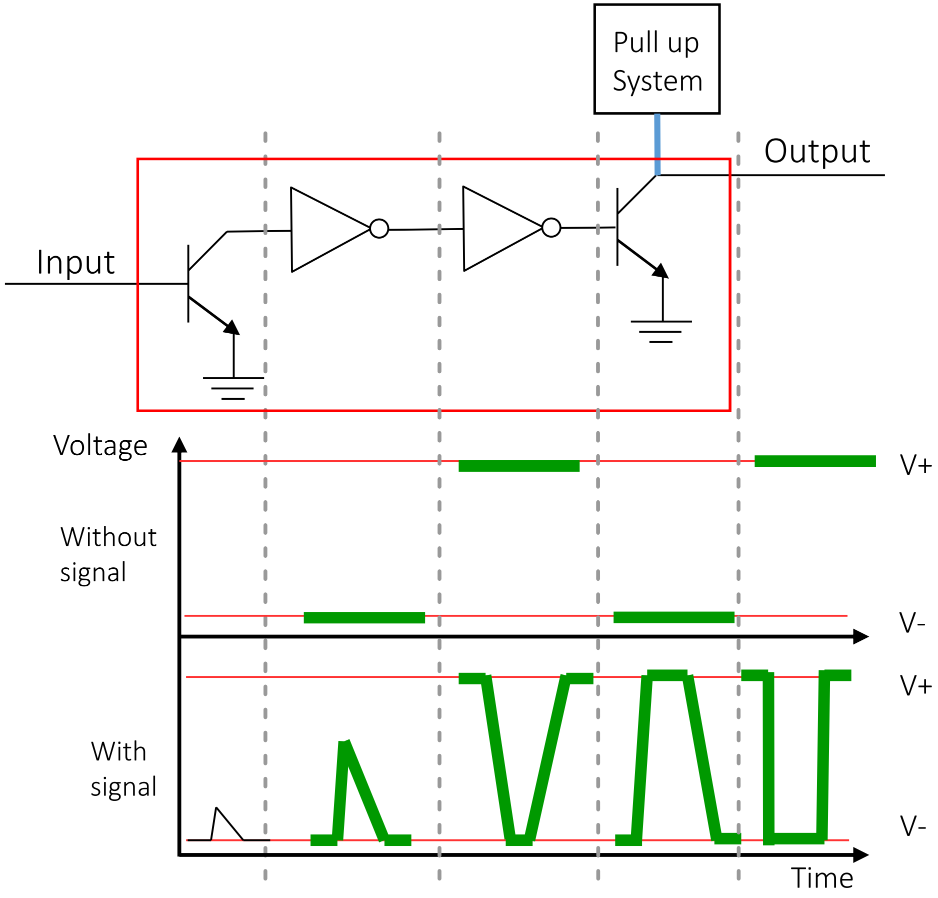
Figure 3: Operating principle of custom charge amplifier in Silicon technology

Voltage supply	3–5 Volt
Sensitivity	2–4 mV/fC
Noise (independent from detector)	4000 e^- RMS
Input impedance	100–50 Ohm
B.W.	10–100 MHz
Power consumption	10 mW/ch
Rise time $\delta(t)$ input	300–600 ps
Radiation hardness	1 Mrad, 10^{13} n cm^{-2}

Table 2: Performance of custom charge amplifier in Silicon BJT technology

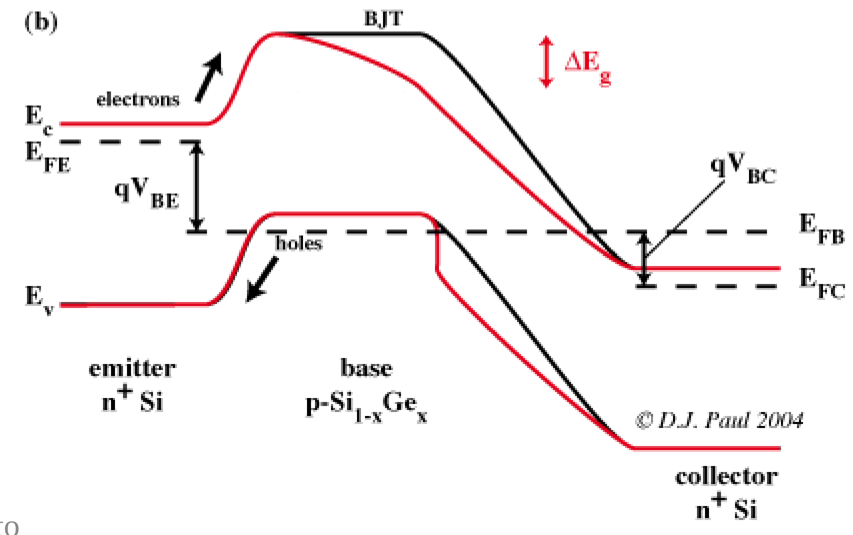
With this amplifier it is possible to anticipate the efficiency curve of around 400 V respect to the previous ATLAS amplifier.

Full-Custom ASIC Discriminator



The new full-custom Discriminator circuit dedicated to the RPCs for high rate environment is developed by using **the Silicon-Germanium HJT technology.** The main idea behind this new discriminator is the limit amplifier. If the signal surpasses the threshold, it will be amplified until saturation giving as output a square wave.

The principle of SiGe heterojunction bipolar transistor (HJT) is to introduce a Silicon-Germanium impurity in the base of the transistor. The advantage of this device is that the band structure introduces a drift field for electrons into the base of the transistor, thus producing a ballistic effect that reduces the base transit time of the carriers injected in the collector. The net effect is to improve the transition frequency and to introduce a directionality in the charge transport allowing a much lower value of B-C capacitance; hence a much higher charge amplification can be achieved.



Full-Custom ASIC Discriminator

The main features are:

- Optimal characteristic function with the possibility of an easy regulation of the threshold from a minimum value of few mV (see Fig. 4)
- Very small transition region of around 300 μV, practically negligible when the discriminator is used within the RPC (see Fig 4).
- Time-over-threshold measurement directly with the discriminator (see Fig 5).
- Minimum pulse width of 3 ns ; for shorter signal the discriminator goes into a charge regime with a threshold in charge (see Fig 6).

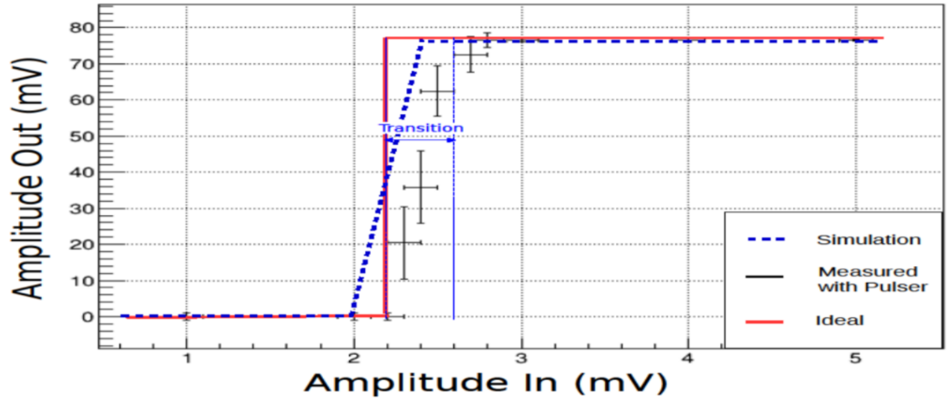


Figure 4: Characteristic function of the discriminator in Si-Ge HJT technology

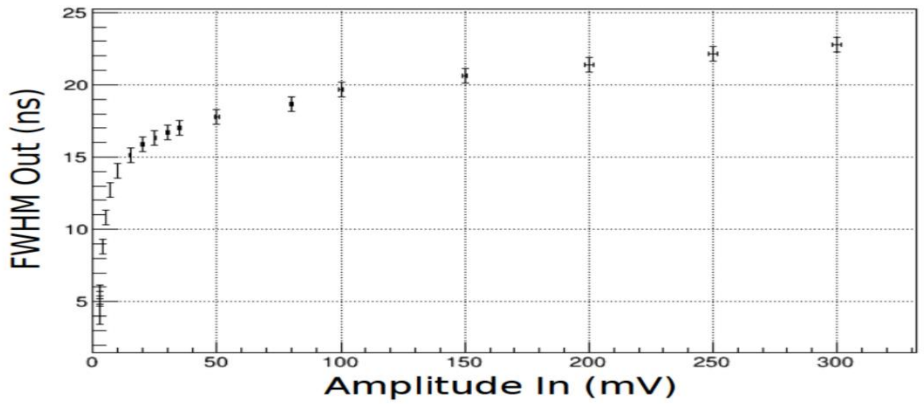


Figure 5: Dynamic of the time-over-threshold of the discriminator prototype in SiGe HJT technology.

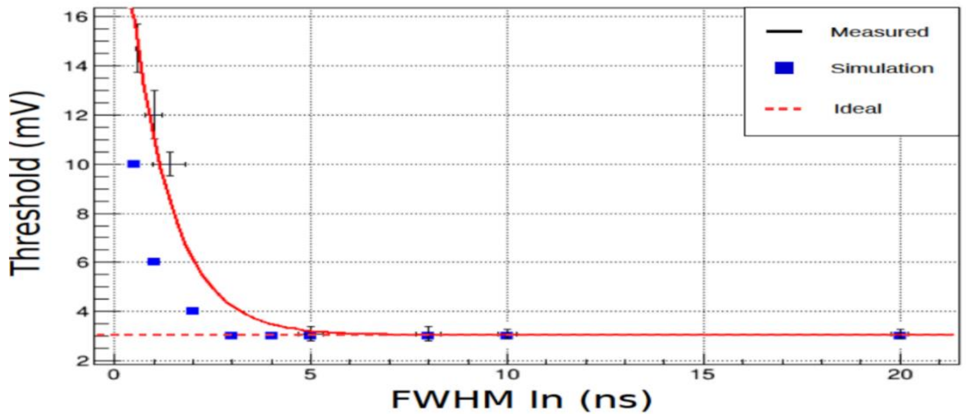


Figure 6: Minimum pulse width of the new Si-Ge prototype with the simulated and the ideal behavior of a discriminator compared

Testbeam at the H8 beamline

This Test beam was realized inside the North Area of CERN, precisely at the H8 beamline. The H8 beam is a secondary particle beam that provides hadrons, electrons or muons of energies between 10 and 400 GeV/c, as well as 450 GeV/c (primary) protons and up to 400 GeV/c per charge primary Pb ions. Only the muon beam was used for this test.

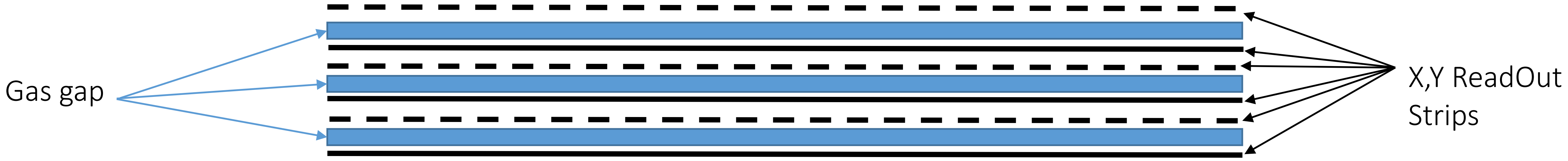
Measurement realized:

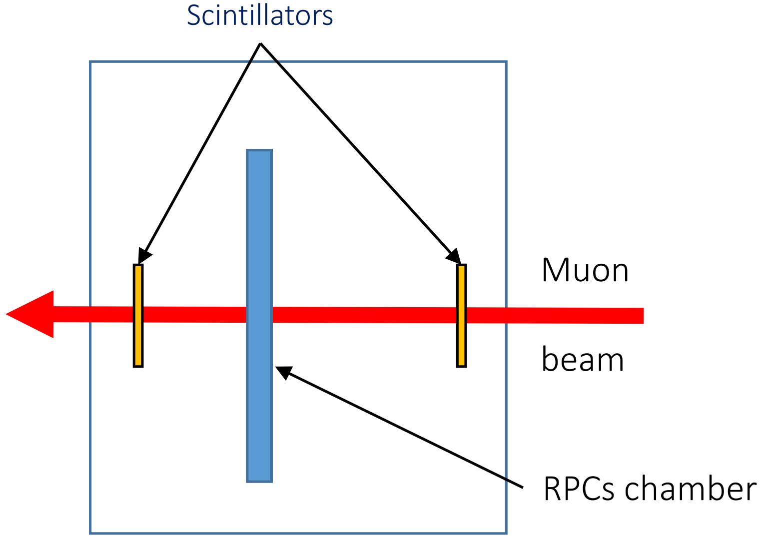
a) RPC overall test
   - The aim of this test was to ensure that the whole system was working correctly

b) Parameters ”phase space” scans
   - The aim of these scans is to find out all the possible electronics working points and their properties

Testbeam at H8 experimental setup

The RPCs chamber is composed by 3 mono-gap equipped with the new Front-End.
The gas gap is 1 mm thick and the electrodes are 1.2 mm thick each. The mixture used was 95% TFE, 4.7% I-C4H10, 0.3% SF6.





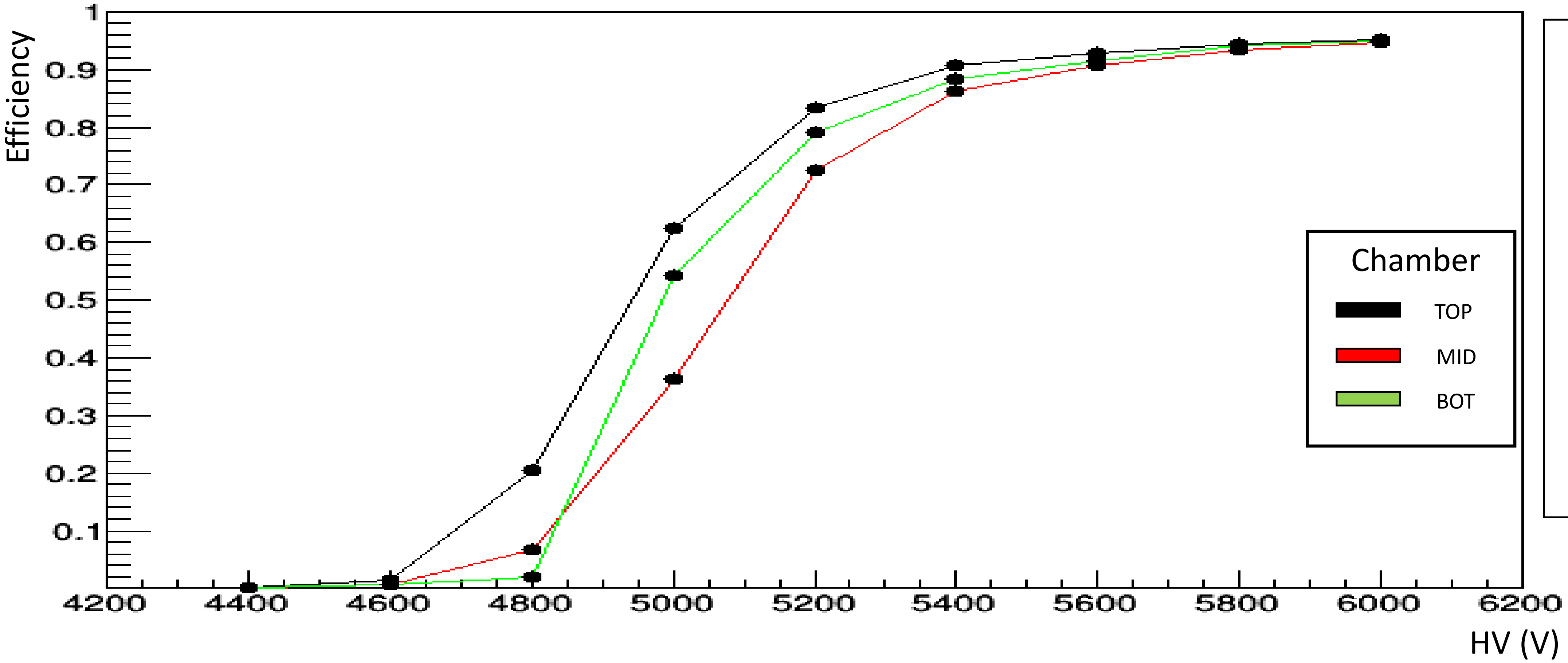
The trigger system was composed by two scintillators of around 10cm x 10cm.
The data acquisition was realized by using a CAEN TDC.

The low voltage system was realized in such a way to have the possibilities to regulate each parameter individually, allowing a deep parameters regulation for each Front-End board.
The Front-End board low voltages studied:

1. Pull Up & Discriminator → The stability of the system
2. Threshold & Amplifier → The effective threshold applied on the signals

Experimental Results

Chambers efficiency in ‘’and’’ configuration



LV parameter

Vth = 1.6 V

Vpu = 0.4 V

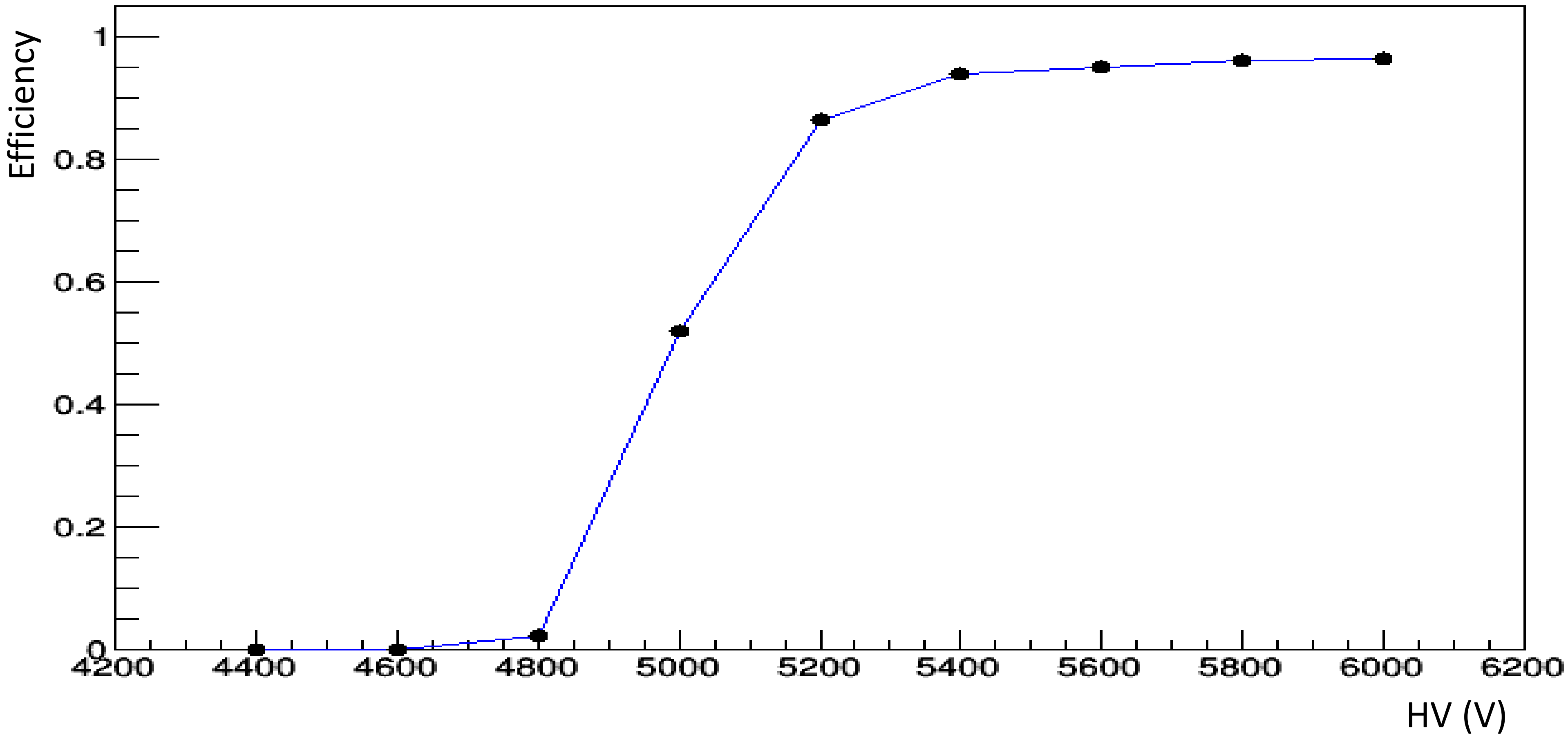
Vamp= 1.5 V

Vdis = 2.5 V

Vtras= 3.5 V

Experimental Results

Triplet efficiency 2 on 3



LV parameter

Vth = 1.6 V

Vpu = 0.4 V

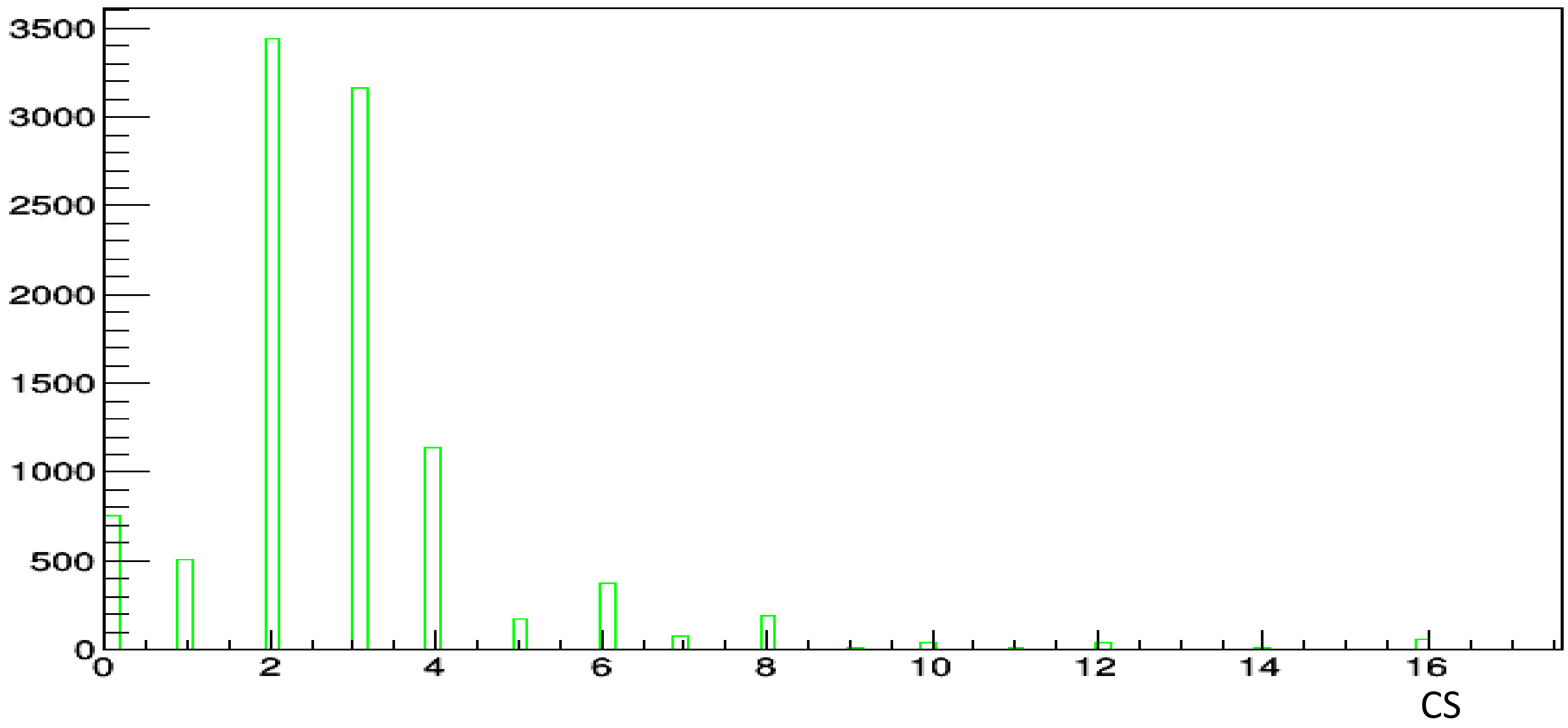
Vamp= 1.5 V

Vdis = 2.5 V

Vtras= 3.5 V

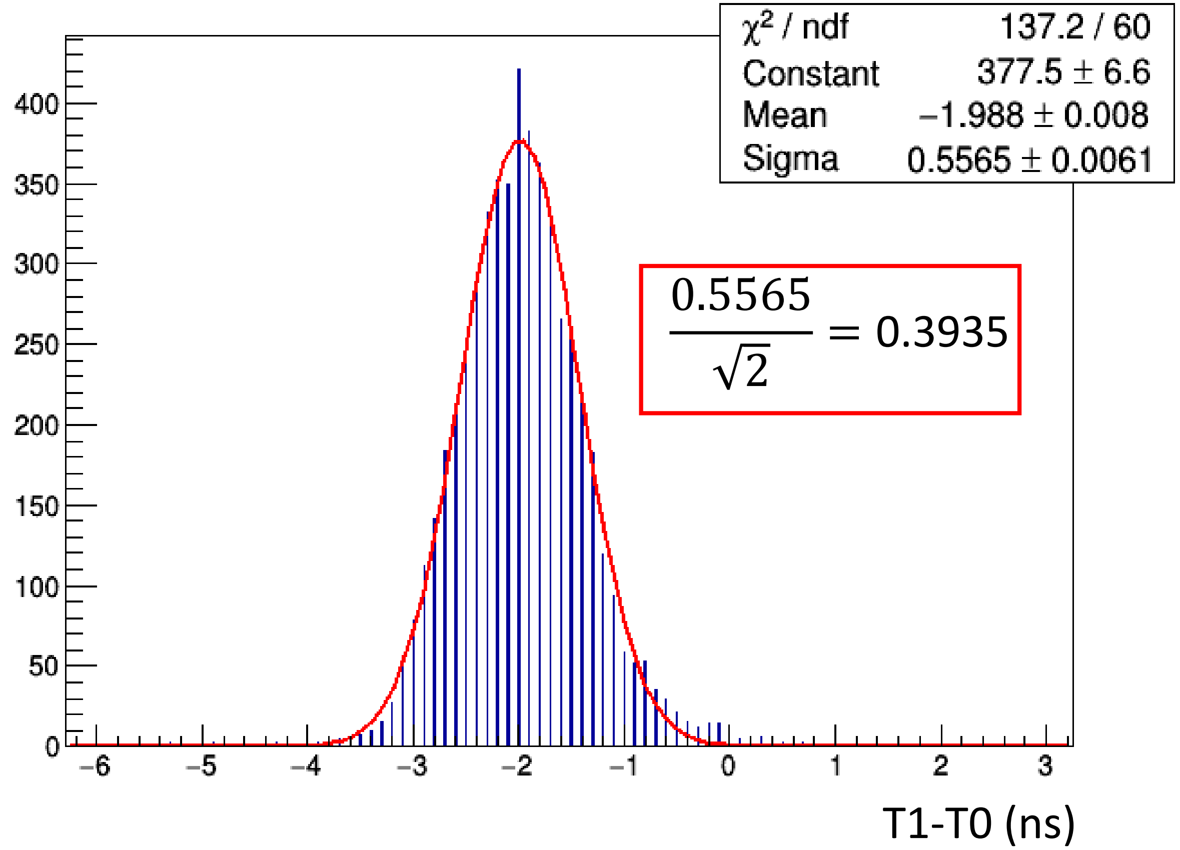
Experimental Results

Average Cluster Size of the chamber



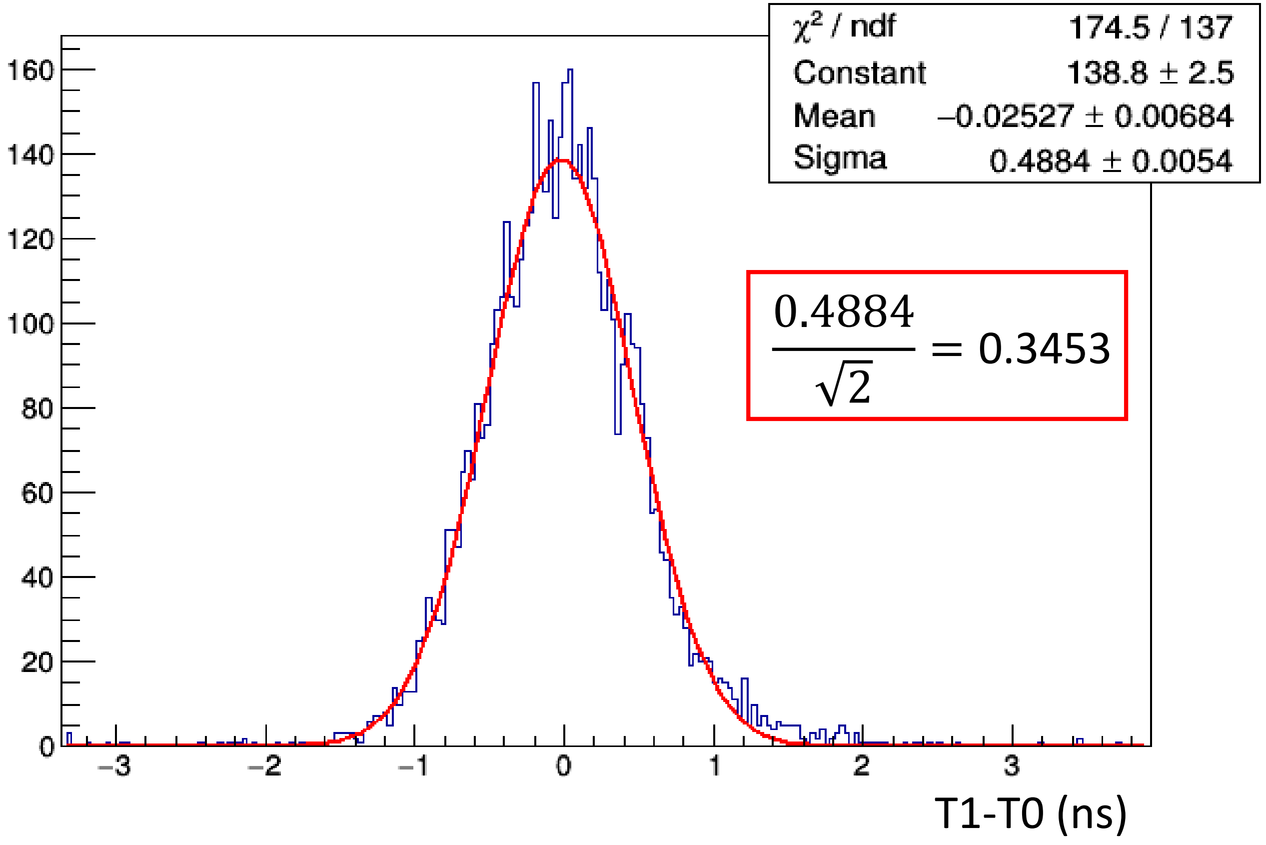
Experimental Results

Time Resolution



$$\frac{0.5565}{\sqrt{2}} = 0.3935$$

Time Resolution with time walk correction



$$\frac{0.4884}{\sqrt{2}} = 0.3453$$

Conclusions

The new Front-End developed achieved the following performances:

1. Minimum Threshold value of 1 mV of the amplified signal

2. Time-over-threshold measurement achievable directly with the FE

3. Along with 1mm gap RPC, a Time Resolution of around 350 ps

The developed Front-End, with the full-custom ASIC Discriminator in SiGe technology and the new Amplifier in Si technology, is able to detect signals of around 1 fC allowing the use of the RPC in high rate experiments

Thank you

Back up

Full-Custom Amplifier

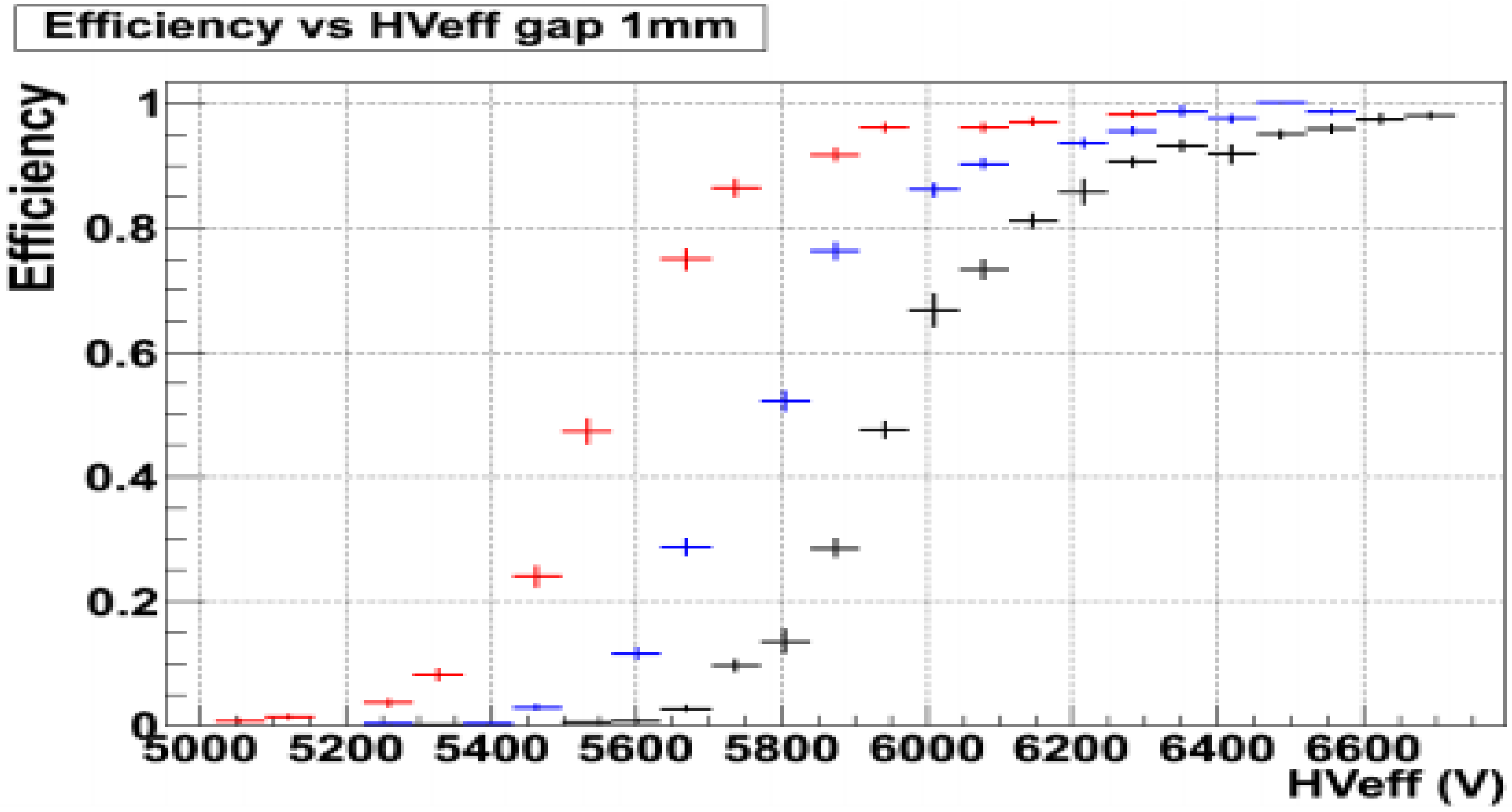


Figure 3. Efficiency curves RPC 1mm gap. In red SiGe FE; in blue Si FE; in black oscilloscope analysis with 1.5mV threshold.

Rate Capability results