Development of semiconductor solid-state detectors with sub-100ps time resolution.

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On behalf of the TT-PET collaboration
The fast silicon pixel detector

• At the beginning of the LHC era, the RPC was the only detector capable of sub-100ps time resolution.

• Silicon pixel technology was focusing on tracking, power consumption and radiation hardness, with a time resolution in the range from few ns to some tens of ns.

• The roadmap for the development of silicon pixel detectors with a 100ps (or better) time resolution will be described through the experience of the TT-PET collaboration.
The TT-PET project

A 3-year project financed by SNSF to produce a PET Scanner for small animals **based on silicon detector technology**, insertable in an MRI machine and with 30ps RMS time resolution. The project started in March 2016.

The TT-PET collaboration:

- University of Geneva
- University of Bern
- Hôpital cantonale de Genève
- INFN of Roma Tor Vergata
- CERN
- Stanford University

Other collaborators:

- IHP Microelectronics
Targets of the TT-PET project

1. Make a 30ps time resolution detector for 511 keV photons and...

What are the main parameters to improve for the time resolution of semiconductor detectors?

- Read out geometry.
- Electronics noise.
- Charge collection noise.

\[ I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i} \]
Read out geometry

The “parallel plate” read out is fundamental to guarantee the uniformity of the weighting and the electric field.

\[ I_{ind} = \sum_{i} q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i} \approx v_{drift} \frac{1}{D} \sum_{i} q_i \]

Scalar, possibly saturated
Scalar, uniform

**Drawback:**

Increase of the pixel capacitance

Larger equivalent noise from the amplifier.
Electronics noise

Detector time resolution depends mostly on the amplifier performance!

\[ \sigma_t = \frac{\sigma_V}{dV/dt} \cong \frac{\text{Rise Time}}{Q/\text{ENC}} \]

\[ I_{\text{ind}} = v_{\text{drift}} \frac{1}{D} \sum_i q_i \]

1. Fast, low noise electronics: 1 ns rise time, < 1000 $e^{-}$ ENC on 1 pF capacitance.

   High $f_t$, single transistor preamplifier. \( \rightarrow \) SiGe HBT technology.

2. Gain...?
Intrinsic limit to the time resolution for a semiconductor detector.

Can be reduced by reducing the sensor thickness.
 Targets of the TT-PET project

1. Make a 30ps time resolution detector for 511 keV photons and...

2. ... make it monolithic.

Both sensor and electronics **integrated in the same chip**, in a commercial microelectronics process.

**Advantages:**

- Simplified interconnections.

- Integrated front end, TDC, logic, serializer.

- Cost reduction
# The TT-PET ASIC

A monolithic silicon pixel detector:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIC length</td>
<td>24 mm</td>
</tr>
<tr>
<td>ASIC width</td>
<td>7, 9, 11 mm</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>500 × 500 μm²</td>
</tr>
<tr>
<td>Pixel Capacitance (comprised routing)</td>
<td>750 fF</td>
</tr>
<tr>
<td>Preamplifier power consumption</td>
<td>200 μW/channel</td>
</tr>
<tr>
<td>Preamplifier E.N.C.</td>
<td>600 e⁻ RMS</td>
</tr>
<tr>
<td>Preamplifier Rise time (10% - 90%)</td>
<td>800 ps</td>
</tr>
<tr>
<td>Time resolution for MIPs</td>
<td>100 ps RMS</td>
</tr>
<tr>
<td>TDC time binning</td>
<td>20 ps</td>
</tr>
<tr>
<td>TDC power consumption</td>
<td>&lt; 1 mW/channel</td>
</tr>
</tbody>
</table>
Results from the R&D
Proof of principle

Test of external sensor and custom SiGe HBT preamplifier at H8 beam line at SPS (CERN).

180 GeV/c pions
Proof of principle

\[ \sigma_t = \frac{(150 \pm 1)\, ps}{\sqrt{2}} = (106 \pm 1)\, ps. \]

100ps time resolution measured with MIPs
1\textsuperscript{st} monolithic prototype

- Two pixels + amplifier + discriminator in standard IHP SG13S process.
- Pixel size: $900 \times 900 \, \mu m^2$ and $900 \times 450 \, \mu m^2$.
- Higher wafer resistivity (1 kOhmcm)
- No thinning, no backplane metallization.
1st monolithic prototype

Test of the 1st monolithic prototype at H8 beam line at SPS (CERN).

- Events triggered by the Geneva telescope.
- Typical signal charge: 1.6 fC.
1\textsuperscript{st} monolithic prototype

- Efficiency 99.8%.

- Amplifier ENC $< 600$ electrons RMS.

- Amplifier power consumption: $< 350\ \mu\text{W/\ channel}$
1\textsuperscript{st} monolithic prototype

Time resolution $\sim 220$ ps RMS

(Strongly affected by the absence of fundamental backside processing steps.)
2\textsuperscript{nd} monolithic prototype

- $3 \times 10$ matrix, $500 \times 500 \mu m^2$ pixels.
- Preamplifier, discriminator, 20 $ps$ time resolution TDC, logic, serializer integrated in chip.
- Thinned to 100 $\mu m$.
- Full backside processing.
- **Back from foundry next month.**
Is it possible to go below 100 ps?

Possible approaches:

1. Reduce pixel size and sensor thickness.

   New monolithic design (under study)

2. The Low Gain Avalanche Diode (LGAD).

   See next slide
The LGAD

- Proposed as timing detector for the new ATLAS HGTD.
- The is kept low: $G \lesssim 20$
Our discrete-component SiGe amplifier was coupled to a LGAD produced by CNM and kindly provided by Sebastian Grinstein (IFAE Barcelona)

Thickness: $\sim 45 \mu m$
PAD size: $1.3 \times 1.3 \ mm^2$

**Test beam with CNM LGAD sensors**

Performance (bias 220V):

\[
\frac{S}{N} = 124 \\
\text{rise,20\%-80\%} = 600 \ \text{ps} \\
\frac{\sigma_v}{dV/dt} = 8 \ \text{ps}
\]

**Expected electronics contribution to the time resolution.**
Test beam with CNM LGAD sensors

LGAD time resolution with MIPs measured at H8 beam line at SPS (CERN).

Compatible with expectations from charge collection noise.
Conclusions

• Silicon pixel technology is now able to combine its sub-millimetre space resolution, very high counting rate capability and excellent radiation hardness with a 100 ps time resolution.

• The TT-PET collaboration is implementing this fast pixel detector in a monolithic structure in a SiGe BiCMOS process.

• Even better time resolution is possible introducing a gain layer in the sensitive volume.

• An important part of the expertise at the base of this development comes from the experience obtained on the development of the Resistive Plate Chambers and their front-end electronics.
Extra Material
Minimization of ENC for a fast integrator

\[ \text{ENC}^2 \propto \left( 2q_e I_C + \frac{4kT}{R_P} + i_{na}^2 \right) \cdot \tau + \left( 4kT R_S + e_{na}^2 \right) \cdot \frac{C_{in}^2}{\tau} + 4A_f C_{in}^2 \]

Dominating term

Excellent performance in terms of series noise for fast shaping are achievable with the BJT technology

\[ \text{ENC_{series noise}} \propto \sqrt{2kT \langle SNI \rangle \left[ (C_{in})^2 \frac{h_{ie}}{\beta} + R_{bb} C_{in}^2 \right]} \]

Transistor ENC contribution depends on current gain and base spreading resistance
SiGe technology for very low noise and fast amplifiers

Amplifier current gain can be expressed as (NPN BJT)

\[
\beta = \frac{i_C}{i_B} = \frac{\tau_p}{\tau_t}
\]

\(\tau_p\) = hole recombination time in base
\(\tau_t\) = electron transit time (E to C)

Need to minimize electron transit time in the base

Increase gain \(\rightarrow\) Reduce base width \(\rightarrow\) Reducing base doping

Spreading resistance increases!
SiGe technology for very low noise and fast amplifiers

A possible approach: changing the charge transport mechanisms in the base from diffusion to drift.

Equivalent to introducing an electric field in the base.

SiGe heterojunction bipolar transistor technology.

The technology we have chosen is SG13S from IHP:

\[
\beta = 900 \\
f_t = 250 \text{ GHz}
\]