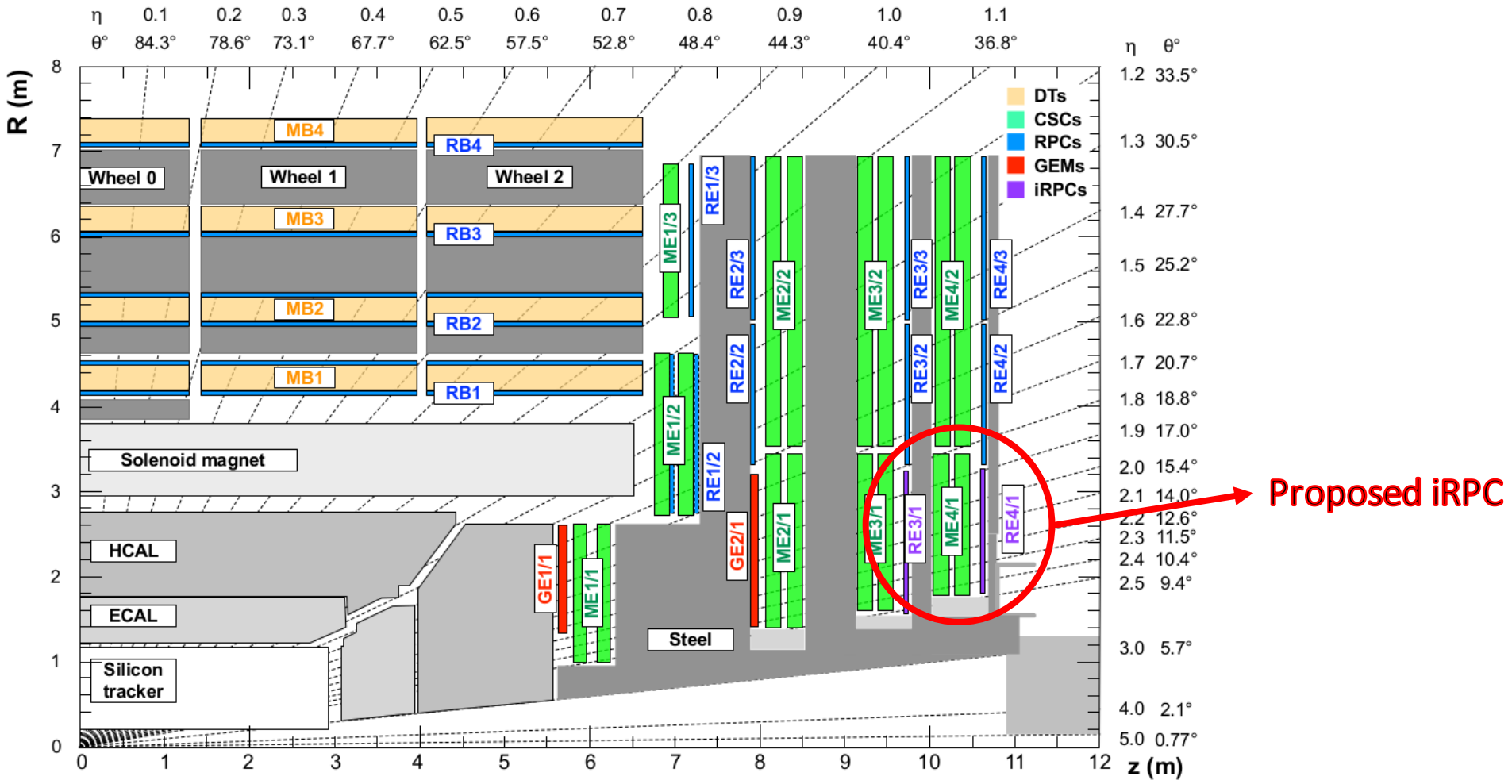
Fast timing measurement for CMS RPC Phase II upgrade

Christophe COMBARET, IPNL – CNRS IN2P3
On behalf of the CMS Muon Group

XIV Workshop on Resisitive Plate Chambers and Related Detectors

72 chambers to equip area with 1.8 < |η| < 2.4
→ Add track hits in muon reconstruction
→ Search for Heavy Stable Charge Particle



Strip board :

96 strips per chamber (1cm strip width at η = 2.8) between double gap RPC detectors

Front-end :

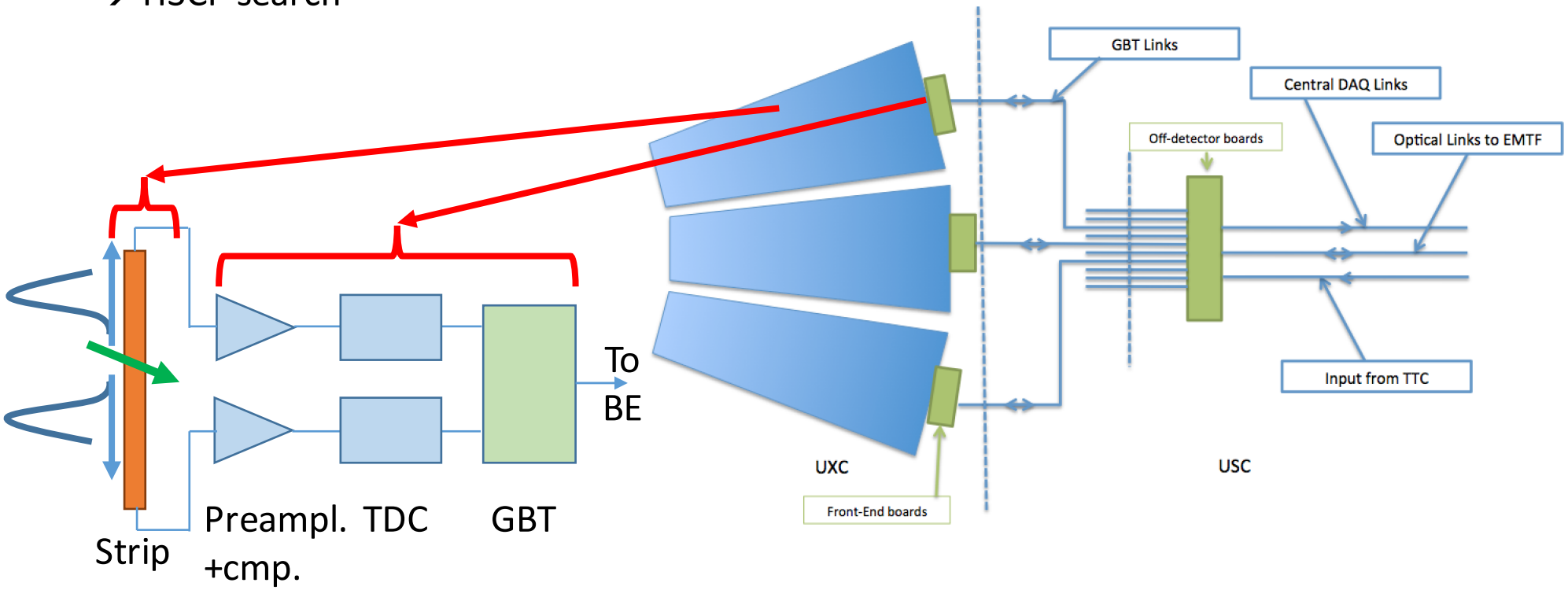
Readout on both sides of the strip

Relative timing between both channels of same strip (σ<100ps)

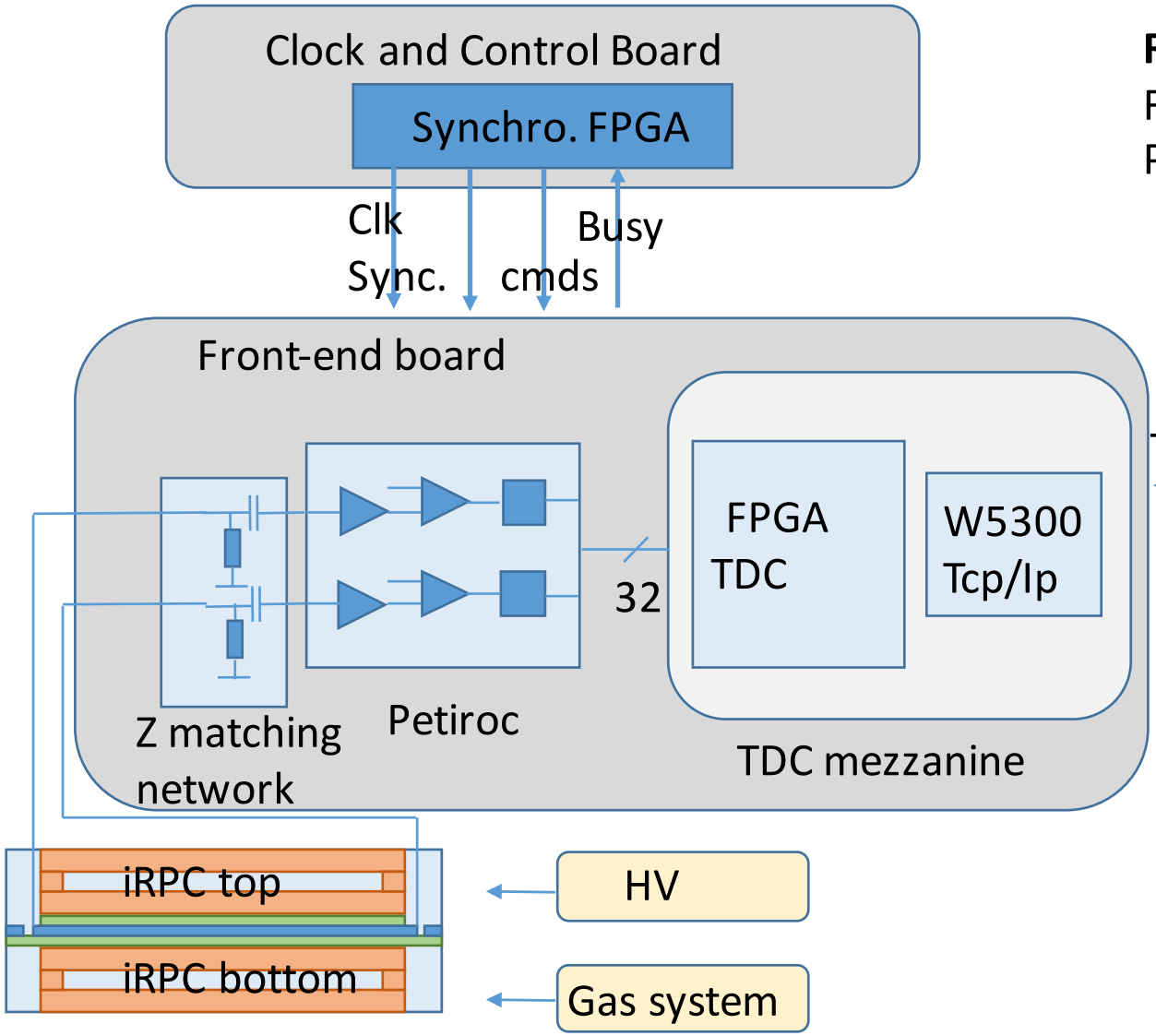
→ Position along the strip (σ = 1.8 cm) $Y = \frac{L}{2} - V.\frac{T2-T1}{2}$

Absolute timing (σ << 1ns)

→ HSCP search



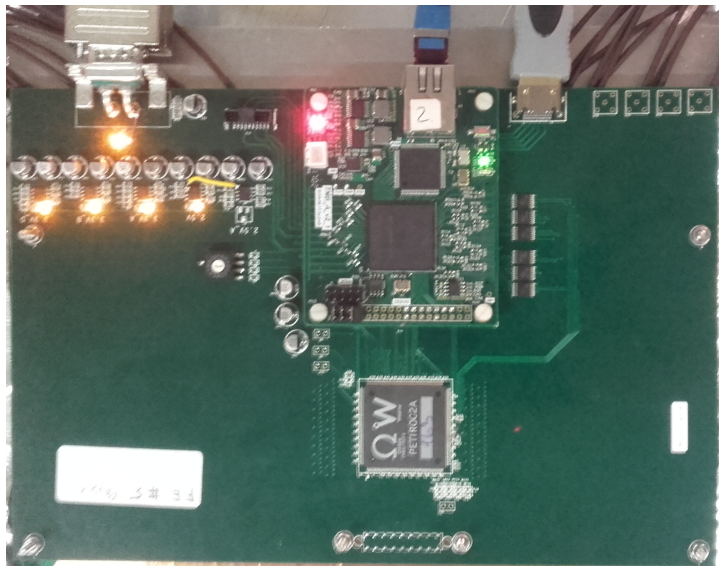
Global prototype measurement chain



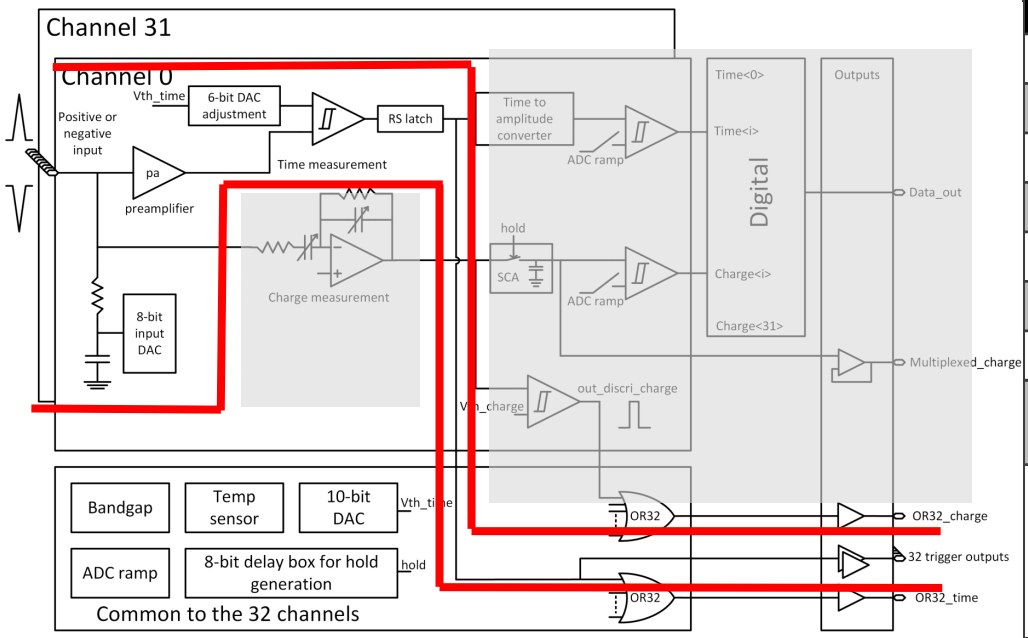
Requirements :
Fast preamp. : Petiroc ASIC
Precise TDC : Wave union TDC

TCP-IP

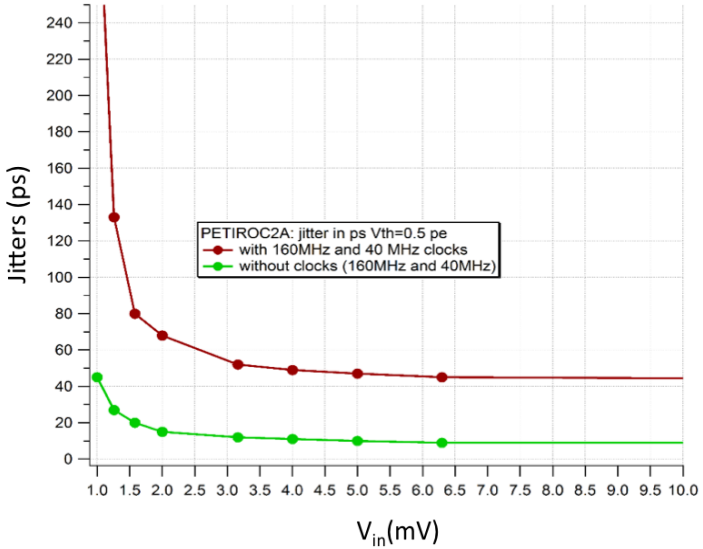
ZDAQ acquisition software
cf. Laurent Mirabito's talk

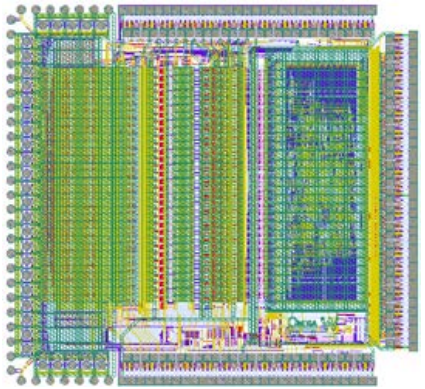


Petiroc ASIC



Parameter	Value
Number of Channels	32
Signal Polarity	positive or negative
Sensitivity	Voltage input amplifier, 200 Ohm matching
Timing Resolution	~ 18 ps RMS on trigger output (4 photoelectrons injected)
Dynamic Range	160 fC up to 400pC
Packaging & Dimension	TQFP 208 (28x28x1.4 mm) TFBGA 353 (12x12x1.2mm)
Power Consumption	6 mW/channel
Inputs	32 analogue inputs, No external component required Inputs DC level adjustable
Outputs	32-channel trigger outputs ASIC level general trigger (OR of all channel) ASIC level second level general trigger (OR of all channels) Charge measurement (10 bits) Time measurement (10 bits)
Internal Programmable Features	Common trigger threshold adjustment and 6bit-DAC/channel Shaping time & gain of the charge shaper 32 x 8bit-input DAC over 1V span



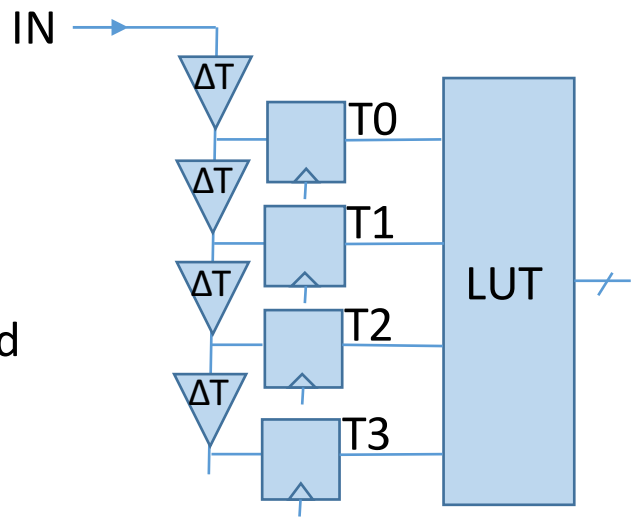


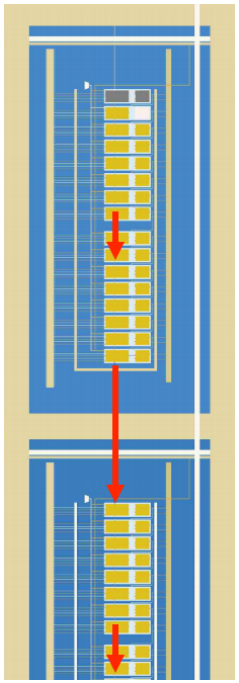
Principle :

Input signal is propagated into a chain of identical delays (bins)

All delays output are latched on the system clock

Fine delay to clock edge is measured by position of last crossed delay element.





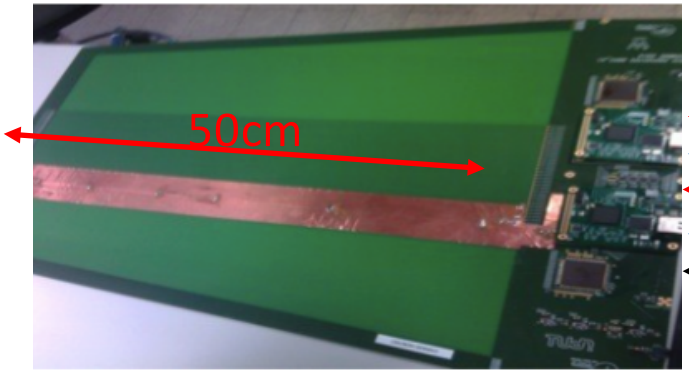
Implementation of carry chain TDC in FPGA :

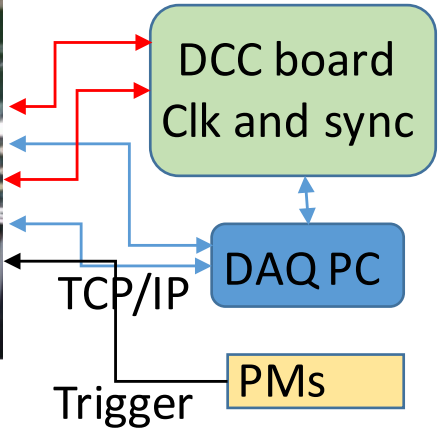
Width of bins are different (Vcc and temperature). Typ. 60ps for Altera Cyclone II
Some ultra-wide bins (LAB boundary crossing). Typ. 165ps for Altera Cyclone II

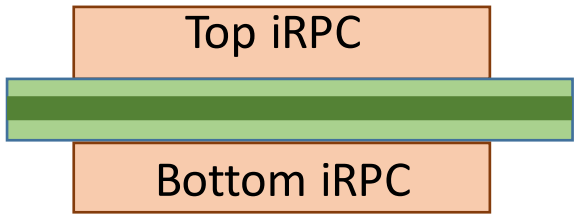
Wave union TDC solves this problem by splitting the input signal in 2 edges and ensuring that in any case, at least one edge is not in the ultra-wide bin.

Details in : QI Ji, DENG Zhi, Liu Yi-nong. Nuclear Electronics &Detection Technology, 2011, 31(4): 378-381.

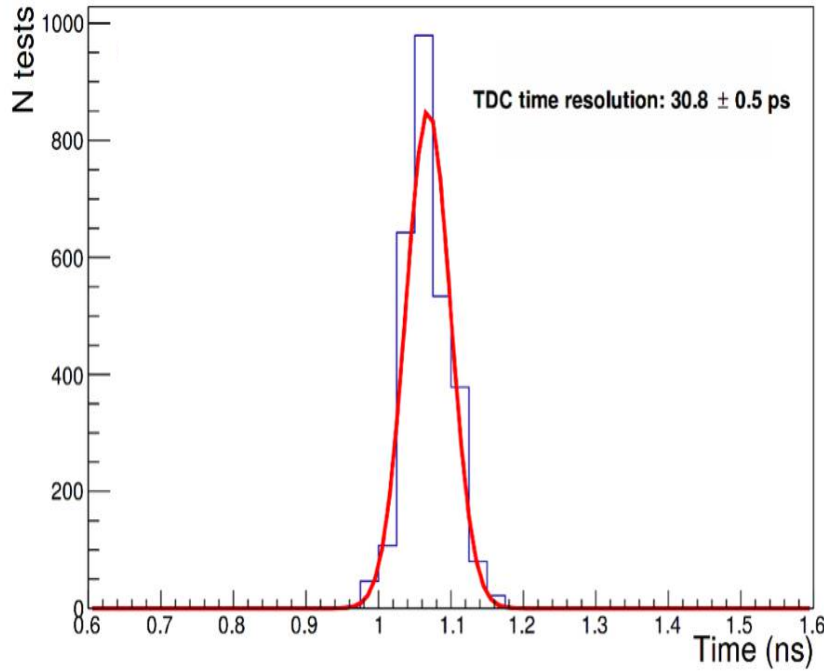
- 32 x 50cm strips (3,5mm pitch) and 32 off detector return lines (1mm wide)
- 2 iRPC chambers : 1.4/1.4 mm and 1.6/1.6 mm
- 2x Petiroc ASIC and 2x Wave union TDC mezzanine





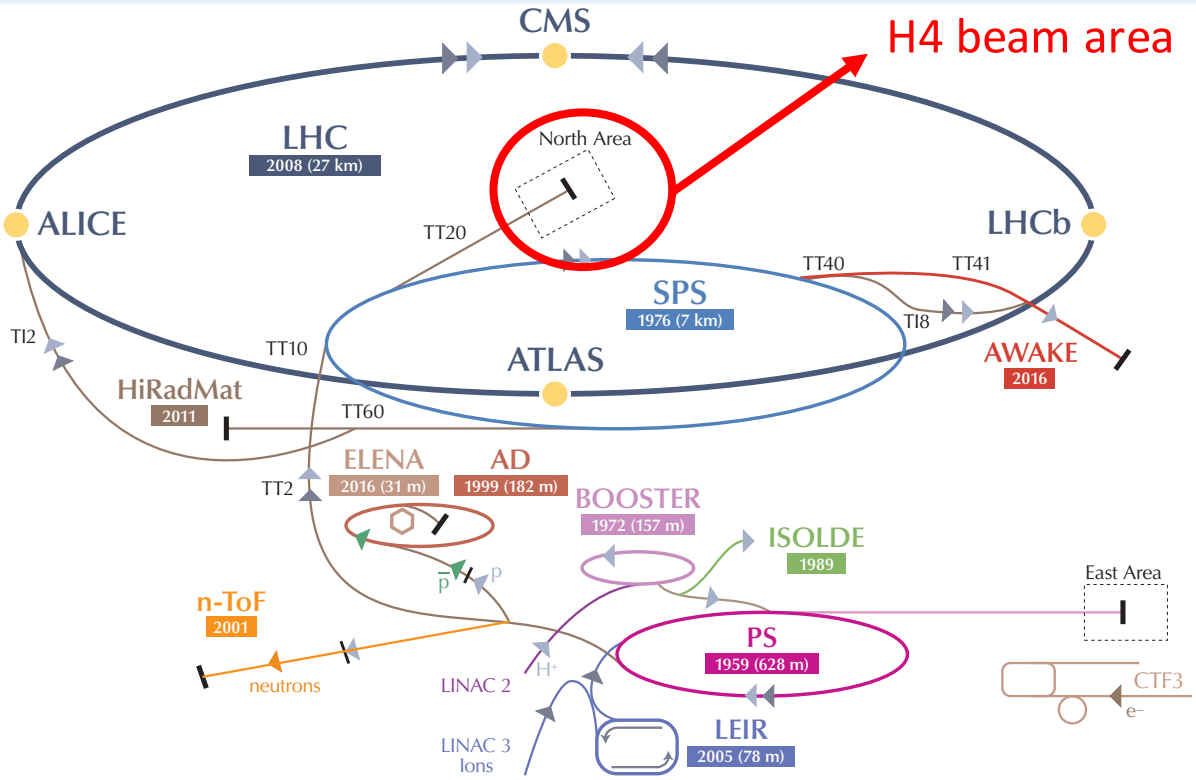


Pcb with buried strips, readout on both sides

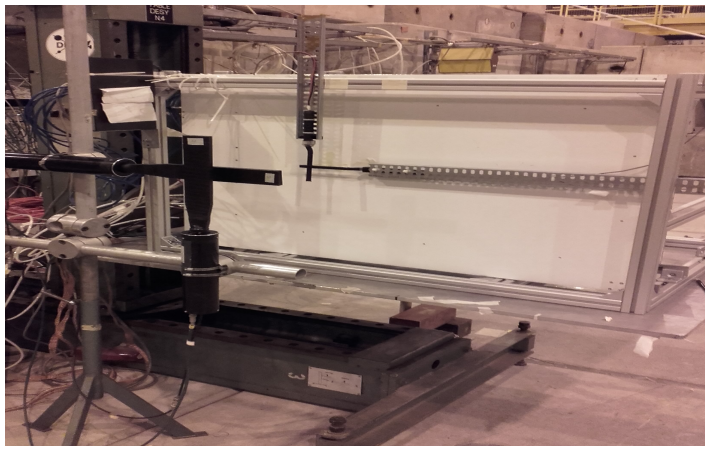


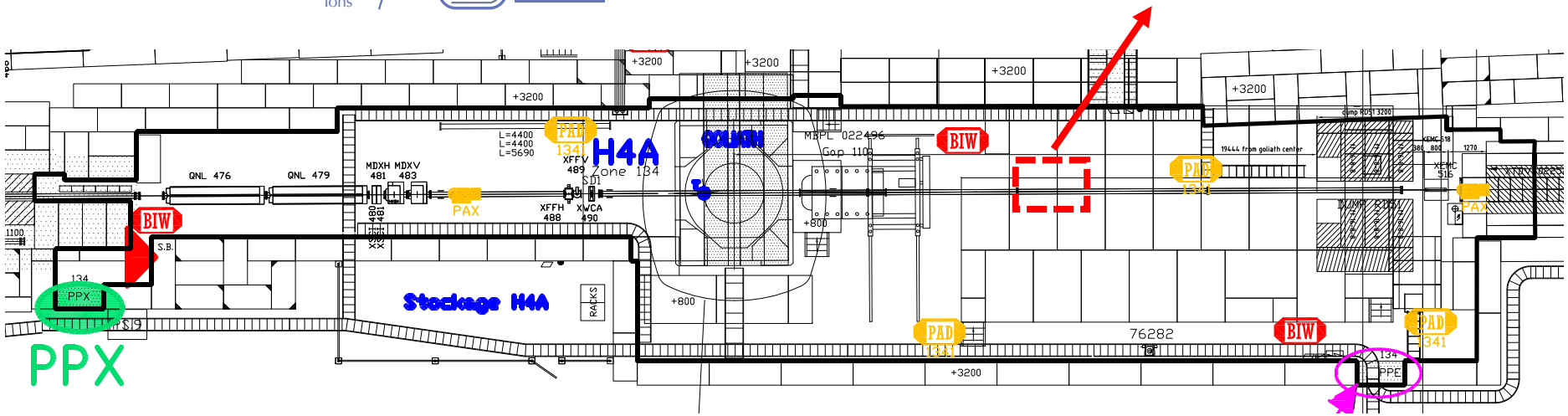
Time resolution with 5pC injection

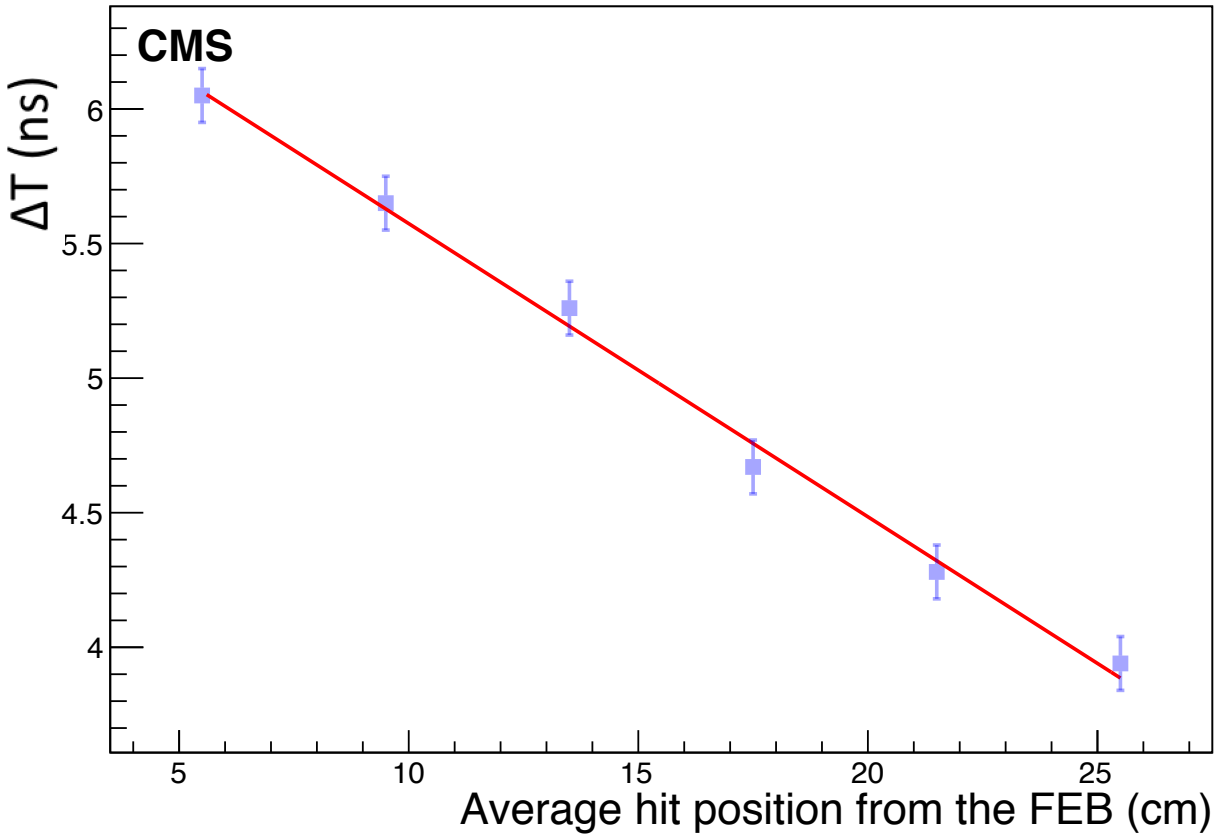
May 2017 beamtest at CERN (H4) : setup



- Muon beam (150GeV)
- Tiny scintillators (1cm width)
- Scan studies were performed using moving tables (< 1mm resolution)







$$Y = \frac{L}{2} - \mathrm{V}.\frac{T2 - T1}{2}$$

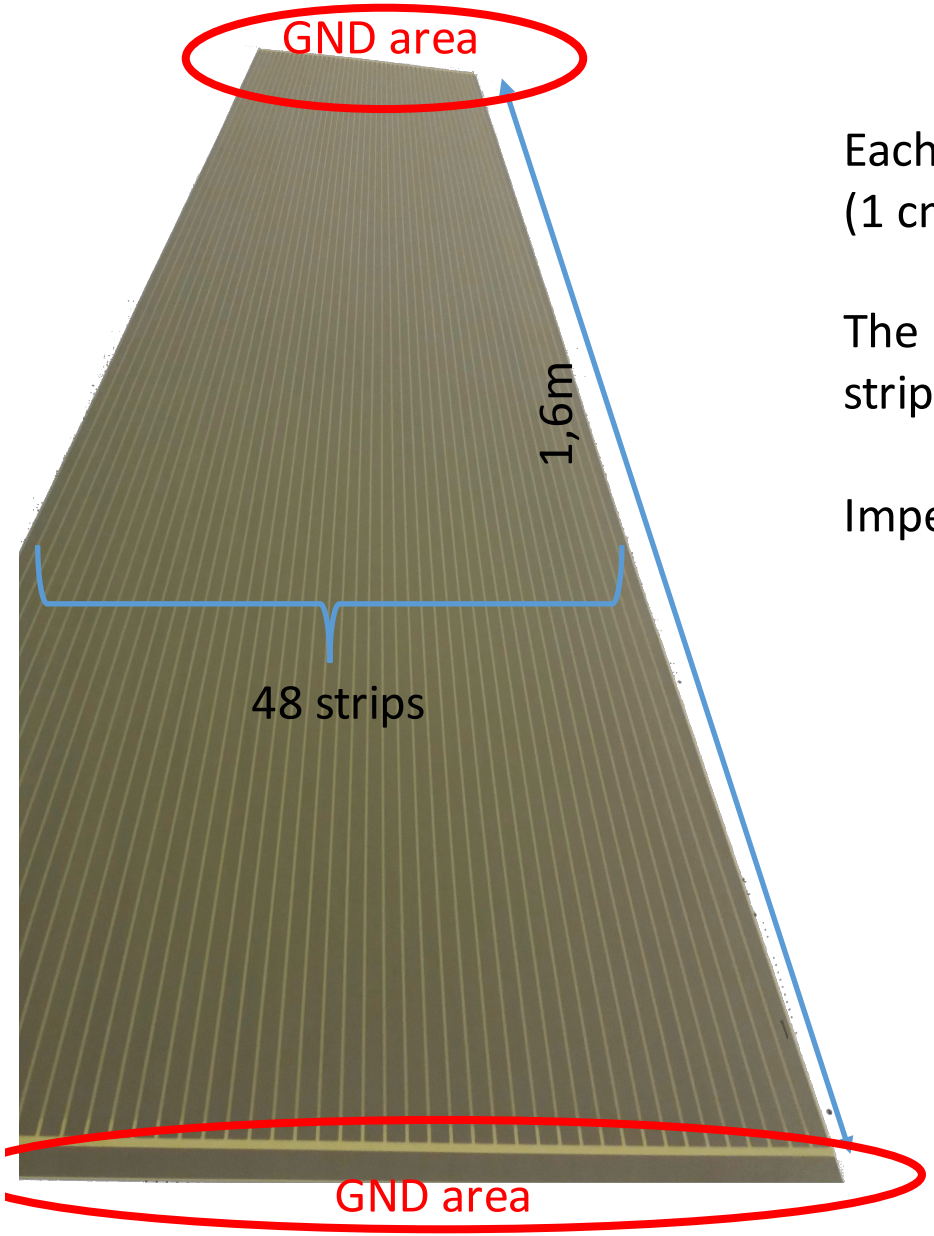
$$\rightarrow \quad \sigma(Y) = V.\,\sigma\left(\frac{T2-T1}{2}\right)$$

Signal Propagation Speed :
V ~2*1 cm/0.11 ns ~18 cm/ns

σ(T2-T1) ~100 ps

$$\sigma(\gamma) \sim \frac{1{,}8cm}{\sqrt{strip\ multiplicity}}$$

Real size strip PCB



Each strip PCB covers half of a cassette with 48 strips (1 cm each)

The strip, both gaps and cassette behave as a stripline where the cassette is the ground planes

Impedance of the strip is defined by :

$$Z_c = \sqrt{\frac{R_s + j.L_s.\omega}{G_p + j.C_p.\omega}}$$

Where :
R_s : Resistance
L_s : Inductance
G_p : Conductance
C_p : Capacitance

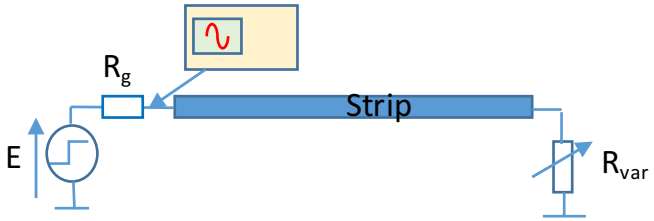
To minimize signal reflections, the stripline impedance must be controlled up to the asic.
3 methods were used to measure strip impedance :

- **Direct measurement of line parameters with a RLC meter (at 2MHz)**

Side	C_p (pF)	G_p (µS)	L_s (nH)	R_s (mΩ)	Z_c (Ω)
Wide	244	934	482	467	**43,5**
Narrow	244	934	487	461	**44**

- **Direct measurement with potentiometric line adaptation**

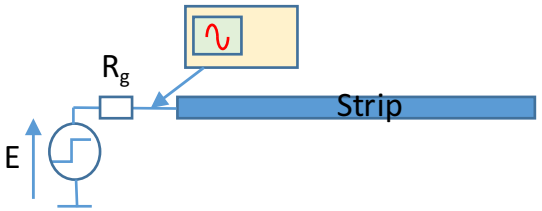
Z_c= 46 Ω



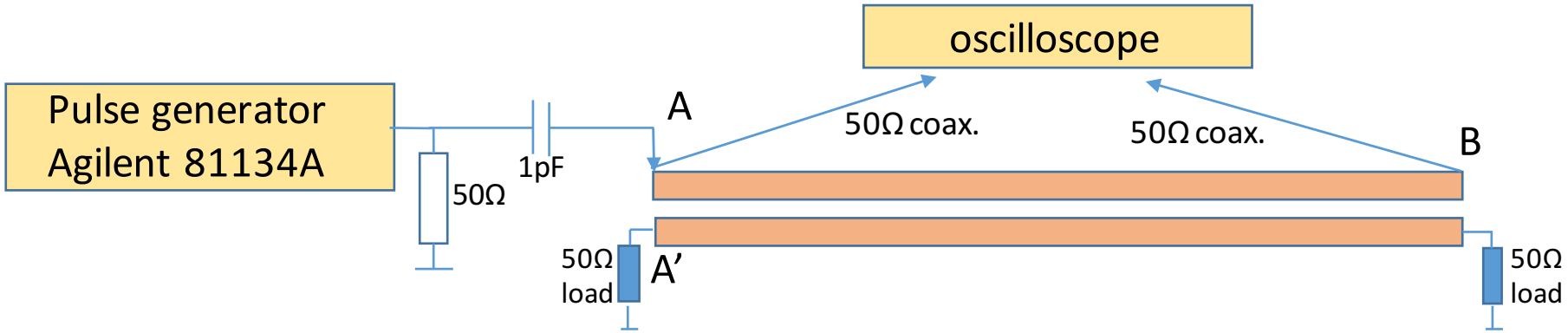
- **Reflection Method**

$$Z_c = \frac{R_g . Vs}{E - Vs}$$

Z_c=41Ω



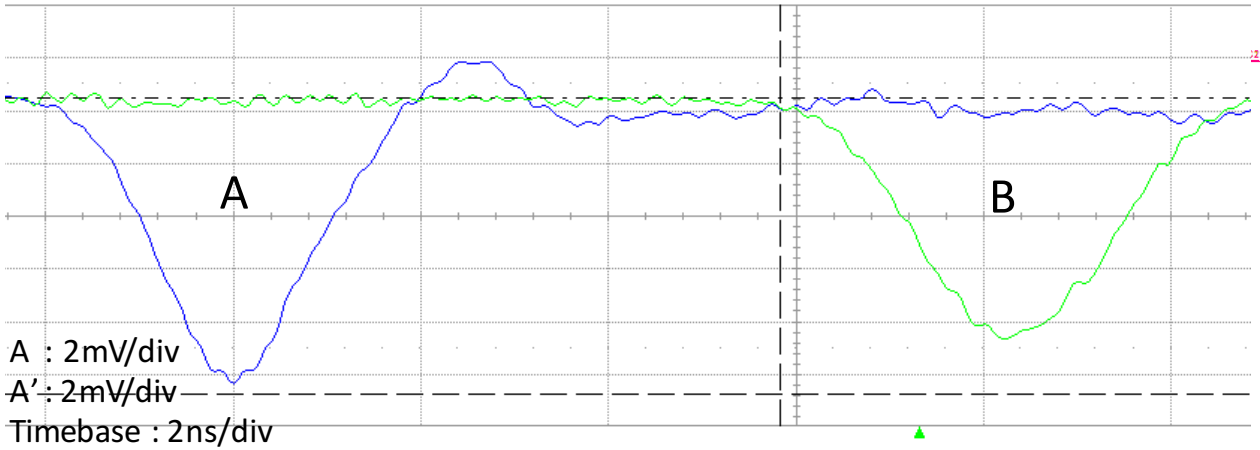
Calibrations (2) : injection on the PCB - principle



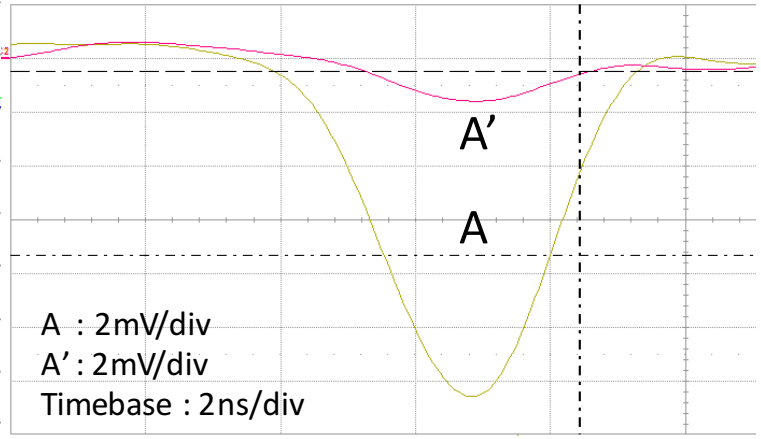
Change is injected on one side (point A)

Charge is divided in two equal halves, each propagates in one direction of the strip

Cross talk is measured on adjacent strip



Injected charges measured at both ends of the strip

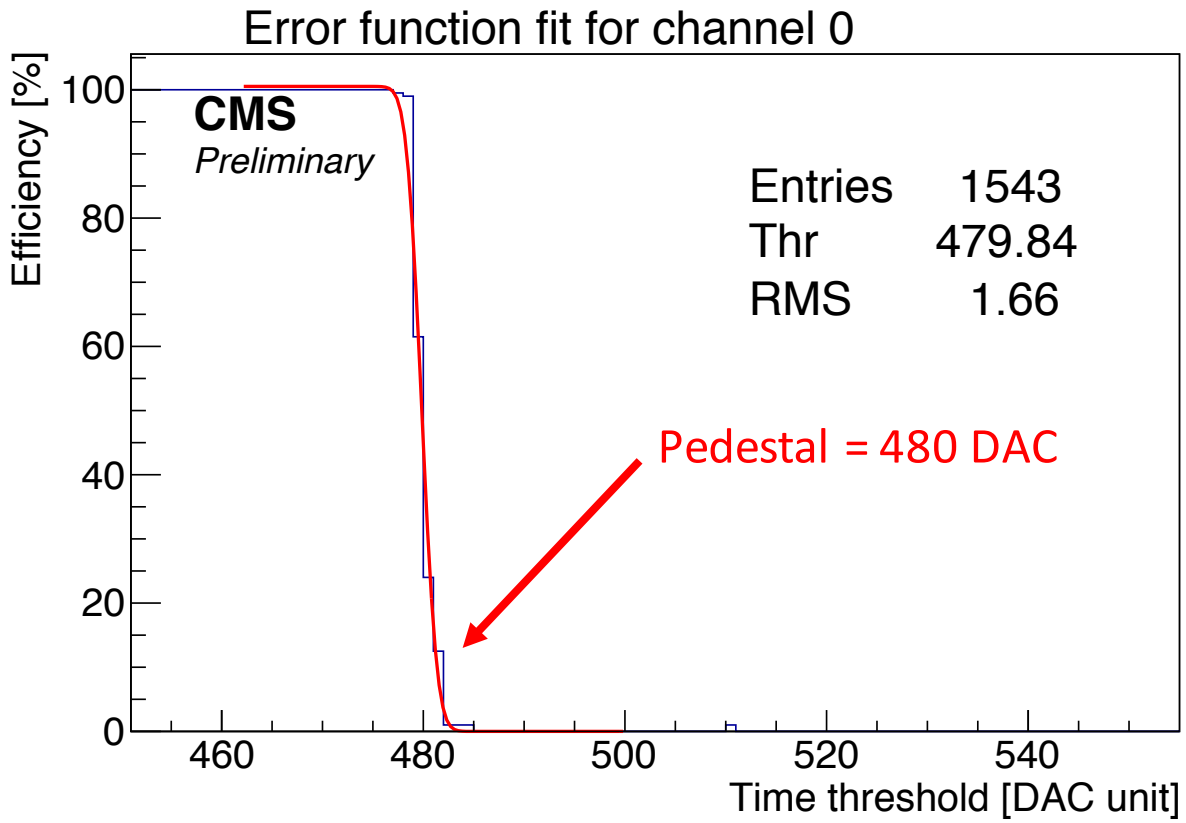


Cross talk on two adjacent strips

FE Calibration method :

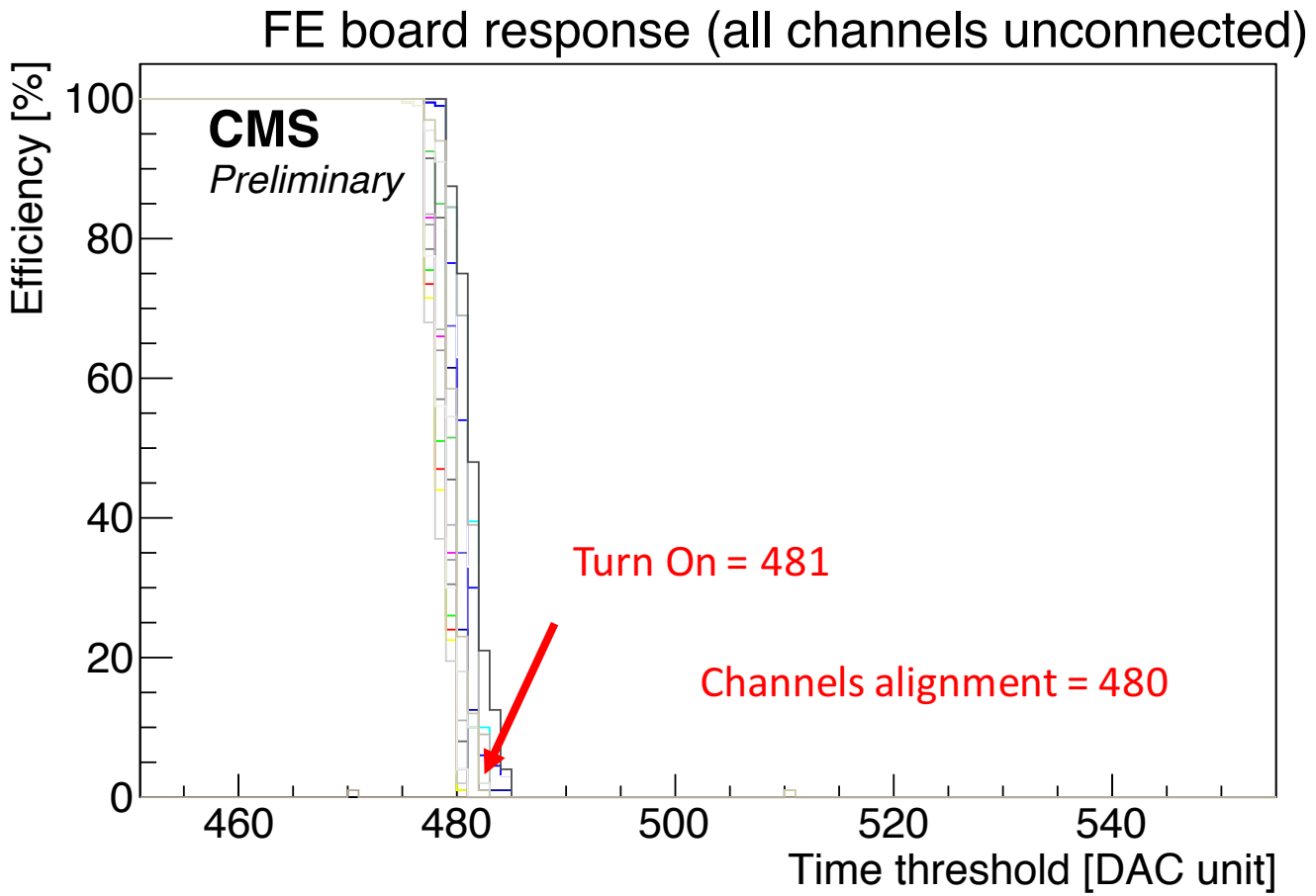
- With only one channel activated at once in the Petiroc ASIC :
  Threshold of comparator lowered step by step with short acquisition window

- Alignment of all channels pedestal to the same value (individually saved in configuration database) . Erf fit function is used to compute pedestal value



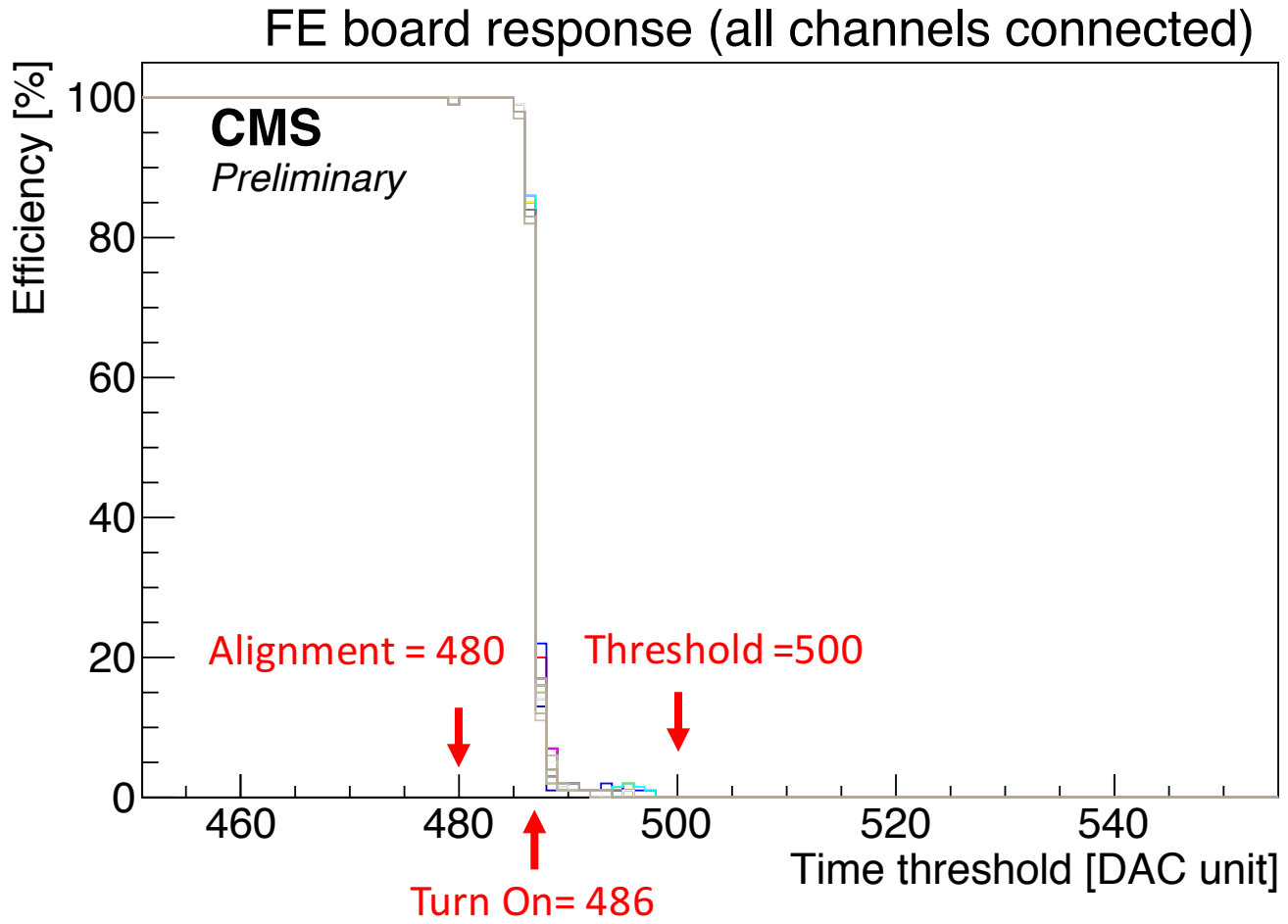
FE Calibration method :

- With all Petiroc channels activated together :
  Threshold of comparator lowered step by step with short acquisition window (alignment check)

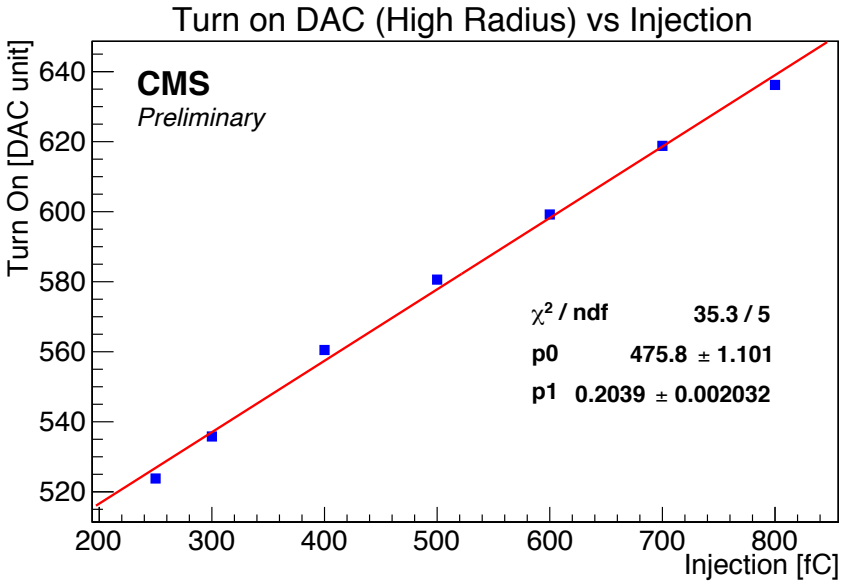


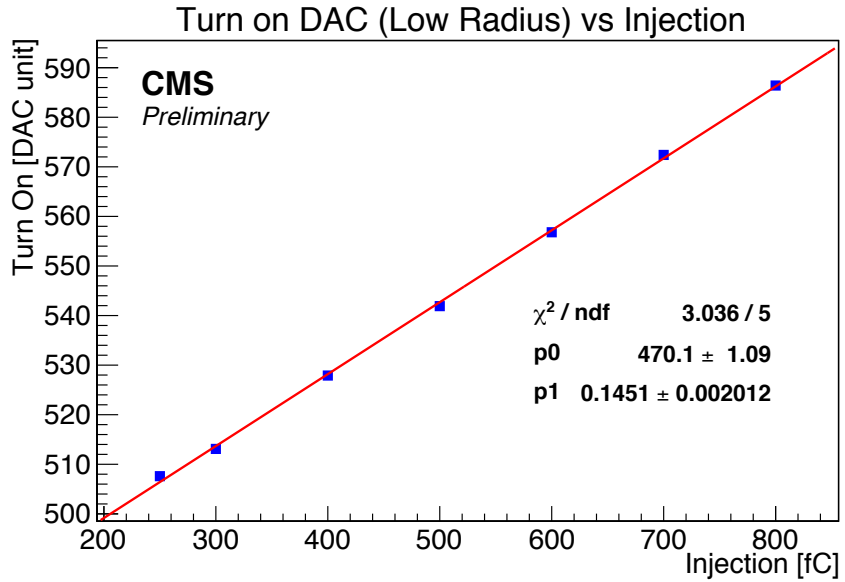
FE Calibration method :

- With all channels activated together and strips connected to the FE board :
  Threshold of comparator lowered step by step with short acquisition window
  (alignment check and noise sources hunt)



Calibrations (3) : injection on the PCB – results (for FE#2)





For this FE Board :

1pF injection capacitance used on high radius

For high radius :

Pedestal from fit = 476 DAC

Threshold set to 500 DAC

→ Minimal charge that can be seen is

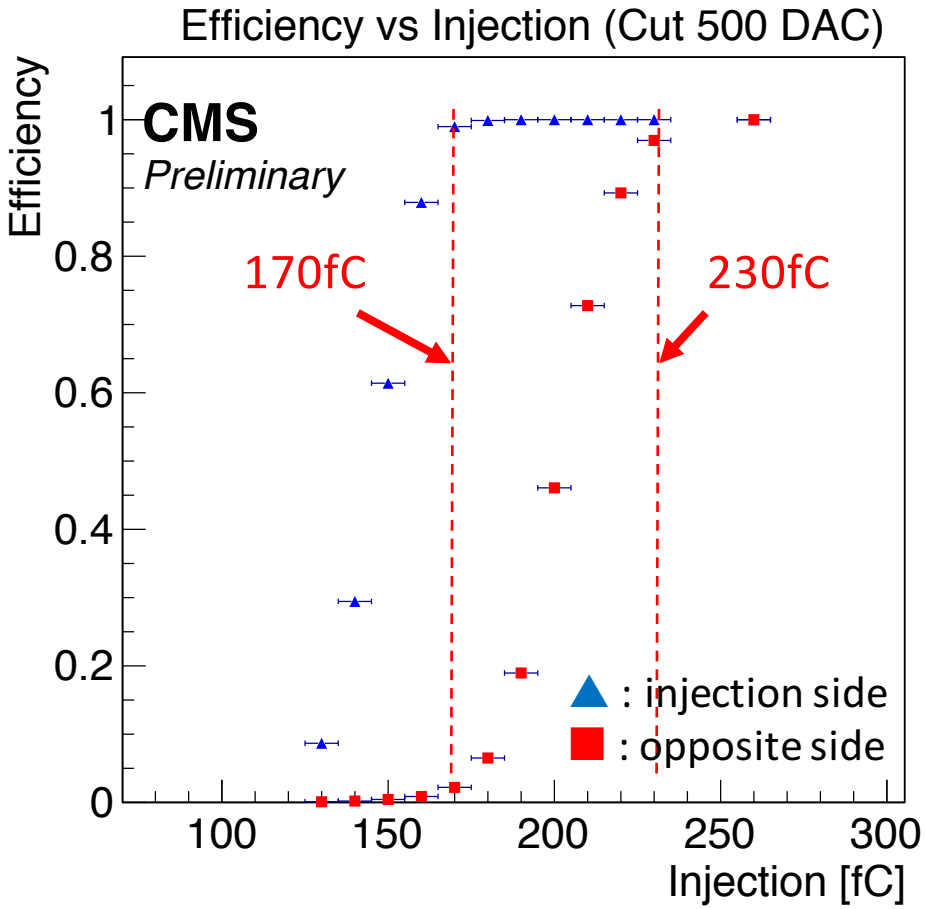
$\frac{500-476}{0,2039}$ = 117 fC for the strip

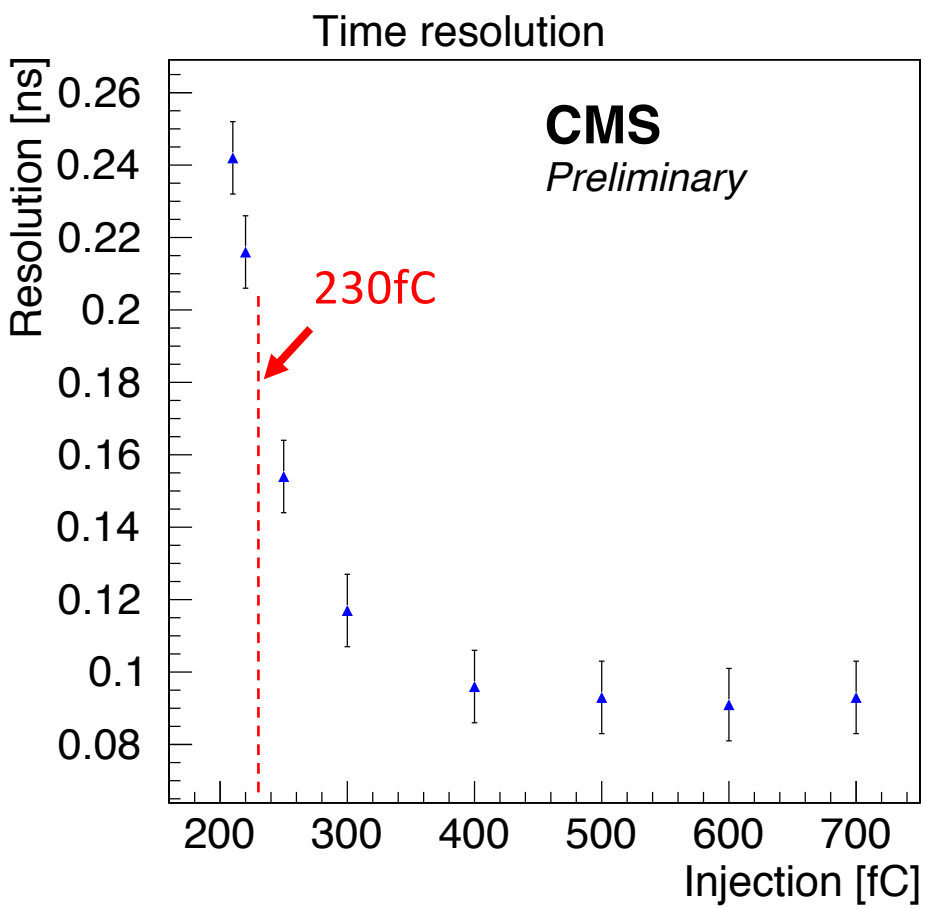
→ 59 fC per channel on injection side

On Low radius side, $\frac{500-470}{0,1451}$ = 206 fC for the strip

→ 103 fC per channel on other side

Calibrations (4) : injection on the PCB – results (for FE#2)





Full efficiency on injection side : 170 fC (85 fC seen on each side)

Full efficiency on both sides : 230 fC (115 fC seen on each side), less than 200 ps resolution (3,6 cm)

- Longitudinal position on the strip measured by difference of signals time arrival on both sides achieved with good resolution

- Long Strip PCB behavior and impedance understood and under control

- Wave union TDC used with Petiroc ASIC

Next steps and prospects :

- FE board version 2 : 64 channels embedded in cyclone V GT FPGA
- Petiroc3 ASIC (lower threshold and improved noise immunity)
- Time over Threshold (ToT) to measure charge and correct time-walk effects
- Integration in CMS central DAQ (GBT data link)