Fast timing measurement for CMS RPC Phase II upgrade

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On behalf of the CMS Muon Group

XIV Workshop on Resistive Plate Chambers and Related Detectors
CMS muon upgrade at high eta

- 72 chambers to equip area with $1.8 < \eta < 2.4$
- Add track hits in muon reconstruction
- Search for Heavy Stable Charge Particle

C. Combaret
Proposed iRPC and front end electronics for RE3/1 and RE4/1

**Strip board:**
96 strips per chamber (1cm strip width at \( \eta = 2.8 \)) between double gap RPC detectors

**Front-end:**
Readout on both sides of the strip
Relative timing between both channels of same strip (\( \sigma < 100 \text{ps} \))

- Position along the strip (\( \sigma = 1.8 \text{ cm} \))
  \[ Y = \frac{L}{2} - V \cdot \frac{T_2 - T_1}{2} \]

Absolute timing (\( \sigma << 1 \text{ns} \))

- HSCP search

![Diagram of iRPC and front end electronics](image)

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- **Absolute timing (\( \sigma << 1 \text{ns} \))**

- **HSCP search**
Global prototype measurement chain

Requirements:
Fast preamp.: Petiroc ASIC
Precise TDC: Wave union TDC

Clock and Control Board
- Synchro. FPGA
- Clk
- Sync.
- Busy
- cmds

Front-end board
- Z matching network
- Petiroc
- FPGA TDC
- TDC mezzanine
- W5300 Tcp/Ip

TCP-IP

ZDAQ acquisition software
cf. Laurent Mirabito’s talk

iRPC top
- HV
- Gas system

iRPC bottom

32
The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing and whole crystal light charge. The ASIC is PET time flight but it can also be used for any application requiring both accurate time resolution and precise energy measurement.

### Table: Petiroc ASIC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Channels</td>
<td>32</td>
</tr>
<tr>
<td>Signal Polarity</td>
<td>positive or negative</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>Voltage input amplifier, 200 Ohm matching</td>
</tr>
<tr>
<td>Timing Resolution</td>
<td>~ 18 ps RMS on trigger output (4 photoelectrons injected)</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>160 fC up to 400pC</td>
</tr>
<tr>
<td>Packaging &amp; Dimension</td>
<td>TQFP 208 (28x28x1.4 mm) TFBGA 353 (12x12x1.2mm)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>6 mW/channel</td>
</tr>
<tr>
<td>Inputs</td>
<td>32 analogue inputs, No external component required</td>
</tr>
<tr>
<td></td>
<td>Inputs DC adjustable to</td>
</tr>
<tr>
<td>Outputs</td>
<td>32-channel trigger outputs</td>
</tr>
<tr>
<td></td>
<td>ASIC level general trigger (OR of all channel)</td>
</tr>
<tr>
<td></td>
<td>ASIC level second level general trigger (OR of all channels)</td>
</tr>
<tr>
<td></td>
<td>Charge measurement (10 bits)</td>
</tr>
<tr>
<td></td>
<td>Time measurement (10 bits)</td>
</tr>
<tr>
<td>Internal Programmable</td>
<td>Common trigger threshold adjustment and 6bit-DAC/channel</td>
</tr>
<tr>
<td>Features</td>
<td>Shaping time &amp; gain of the charge shaper</td>
</tr>
<tr>
<td></td>
<td>32 x 8bit-input DAC over 1V span</td>
</tr>
</tbody>
</table>

**Diagram:**

- **Channel 31**
  - Positive or negative input
  - 6-bit DAC adjustment
  - Time to amplitude converter
  - Charge measurement
  - 8-bit input DAC
  - 8-bit delay box for hold generation
  - Common to the 32 channels

**Figure 5.23:** The PETIROC schematics.

**Figure 6.17:** The PETROD2A: jitter in ps Vth=0.5 pe with 160MHz and 40 MHz clocks without clocks (160MHz and 40MHz).

**Contact:**

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www.weeroc.com/products/

**Learn more about:**

Petiroc 1 & 2

**Layout:**

P.R.C. Combaret

**RPC2018**, Feb 19-23rd 2018
Wave union TDC

**Principle:**
Input signal is propagated into a chain of identical delays (bins)

All delays output are latched on the system clock

Fine delay to clock edge is measured by position of last crossed delay element.

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**Implementation of carry chain TDC in FPGA:**
Width of bins are different (Vcc and temperature). Typ. 60ps for Altera Cyclone II
Some ultra-wide bins (LAB boundary crossing). Typ. 165ps for Altera Cyclone II

Wave union TDC solves this problem by splitting the input signal in 2 edges and ensuring that in any case, at least one edge is not in the ultra-wide bin.

Small size Electronics prototype

- 32 x 50cm strips (3,5mm pitch ) and 32 off detector return lines (1mm wide)
- 2 iRPC chambers : 1.4/1.4 mm and 1.6/1.6 mm
- 2x Petiroc ASIC and 2x Wave union TDC mezzanine

Pcb with buried strips, readout on both sides

Time resolution with 5pC injection
May 2017 beamtest at CERN (H4): setup

- Muon beam (150GeV)
- Tiny scintillators (1cm width)
- Scan studies were performed using moving tables (<1mm resolution)
May 2017 beamtest at CERN (H4): Results

![Graph showing the relationship between ΔT (ns) and Average hit position from the FEB (cm).]

\[ Y = \frac{L}{2} - V \cdot \frac{T2 - T1}{2} \]

\[ \Rightarrow \sigma(Y) = V \cdot \sigma\left(\frac{T2 - T1}{2}\right) \]

Signal Propagation Speed:
V \sim 2*1 \text{ cm/0.11 ns} \sim 18 \text{ cm/ns}

\[ \sigma(T2-T1) \sim 100 \text{ ps} \]

\[ \sigma(\gamma) \sim \frac{1.8 \text{ cm}}{\sqrt{\text{strip multiplicity}}} \]
Each strip PCB covers half of a cassette with 48 strips (1 cm each)

The strip, both gaps and cassette behave as a stripline where the cassette is the ground planes

Impedance of the strip is defined by:

\[ Z_c = \frac{R_s + jL_s \omega}{\sqrt{G_p + jC_p \omega}} \]

Where:
- \( R_s \): Resistance
- \( L_s \): Inductance
- \( G_p \): Conductance
- \( C_p \): Capacitance
To minimize signal reflections, the stripline impedance must be controlled up to the asic. 3 methods were used to measure strip impedance:

- **Direct measurement of line parameters with a RLC meter (at 2MHz)**

<table>
<thead>
<tr>
<th>Side</th>
<th>( C_p ) (pF)</th>
<th>( G_p ) (( \mu )S)</th>
<th>( L_s ) (nH)</th>
<th>( R_s ) (m( \Omega ))</th>
<th>( Z_c ) (( \Omega ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wide</td>
<td>244</td>
<td>934</td>
<td>482</td>
<td>467</td>
<td>43,5</td>
</tr>
<tr>
<td>Narrow</td>
<td>244</td>
<td>934</td>
<td>487</td>
<td>461</td>
<td>44</td>
</tr>
</tbody>
</table>

- **Direct measurement with potentiometric line adaptation**

  \[ Z_c = 46 \, \Omega \]

- **Reflection Method**

  \[ Z_c = \frac{R_g \cdot V_S}{E - V_S} \]

  \[ Z_c = 41 \, \Omega \]
Calibrations (2): injection on the PCB - principle

Change is injected on one side (point A)
Charge is divided in two equal halves, each propagates in one direction of the strip
Cross talk is measured on adjacent strip

Injected charges measured at both ends of the strip
Cross talk on two adjacent strips
FE Calibrations: noise response, no injection

FE Calibration method:

- With only one channel activated at once in the Petiroc ASIC:
  - Threshold of comparator lowered step by step with short acquisition window

- Alignment of all channels pedestal to the same value (individually saved in configuration database). Erf fit function is used to compute pedestal value

![Error function fit for channel 0](image)

Error function fit for channel 0

- CMS Preliminary
  - Entries: 1543
  - Thr: 479.84
  - RMS: 1.66

Pedestal = 480 DAC
FE Calibration method:

- With all Petiroc channels activated together:
  
  Threshold of comparator lowered step by step with short acquisition window (alignment check)

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FE board response (all channels unconnected)

![Graph showing CMS Preliminary data with Efficiency [%] on the y-axis and Time threshold [DAC unit] on the x-axis. The graph indicates a threshold of 480 for channels alignment and 481 for Turn On.]
FE Calibrations: noise response, no injection

**FE Calibration method:**
- With all channels activated together and strips connected to the FE board:
  - Threshold of comparator lowered step by step with short acquisition window (alignment check and noise sources hunt)

![Graph of FE board response](image)

- CMS Preliminary
- Alignment = 480
- Threshold = 500
- Turn On = 486
- Efficiency [%]
- Time threshold [DAC unit]
- Efficiency [%]
- Time threshold [DAC unit]
Calibrations (3): injection on the PCB – results (for FE#2)

For this FE Board:
1pF injection capacitance used on high radius

For high radius:
Pedestal from fit = 476 DAC
Threshold set to 500 DAC

→ Minimal charge that can be seen is
\[
\frac{500 - 476}{0.2039} = 117 \text{ fC for the strip}
\]

→ 59 fC per channel on injection side

On Low radius side, \[
\frac{500 - 470}{0.1451} = 206 \text{ fC for the strip}
\]

→ 103 fC per channel on other side
Full efficiency on injection side: 170 fC (85 fC seen on each side)
Full efficiency on both sides: 230 fC (115 fC seen on each side), less than 200 ps resolution (3.6 cm)
Conclusions and prospects

• Longitudinal position on the strip measured by difference of signals time arrival on both sides achieved with good resolution

• Long Strip PCB behavior and impedance understood and under control

• Wave union TDC used with Petiroc ASIC

**Next steps and prospects :**

• FE board version 2 : 64 channels embedded in cyclone V GT FPGA
• Petiroc3 ASIC (lower threshold and improved noise immunity)
• Time over Threshold (ToT) to measure charge and correct time-walk effects
• Integration in CMS central DAQ (GBT data link)