Design a TDC in SiGe for the Front-end electronics used in the RPCs for high-rate experiment

Section
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Key motivation for using a new ASIC Front-end

The RPC is a detectors that it has a optimal time resolution. For this reason is a good idea to use a Time-to-digital-Converter (TDC) for each channel.

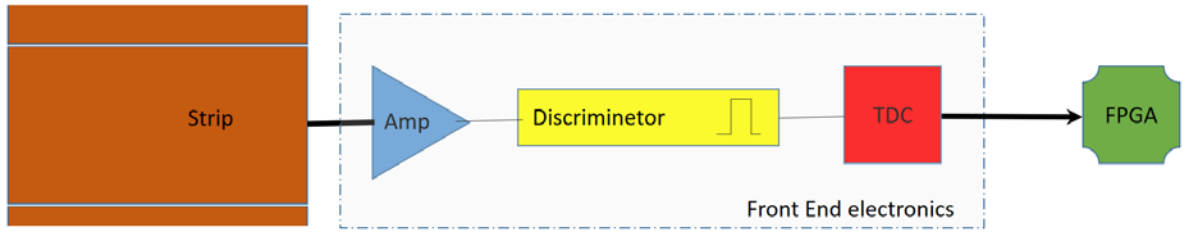
Request for Front-end

- Decrease the noise for short shaping;
- Decrease the rise time, to improve time-of-flight capability;
- Improve the performance of the discriminator and the time-to-digital converter;
- Minimize complexity in order to achieve high reliability and low cost;
- Minimize the power consumption to avoid the need for active cooling;
- Employ radiation-hard technology, since the front-end electronics can’t be replaced.

To solve this problem, we have thought to insert all read-out chain in a front-end ASIC, using a SiGe BiCMOS tecnology at 130nm [1][2] by innovations for High Performance Microelectronics (IHP) [3]

Read-out chain in SiGe Tecnology

The read out chain includes: Amplifiare, Discriminator and TDC.



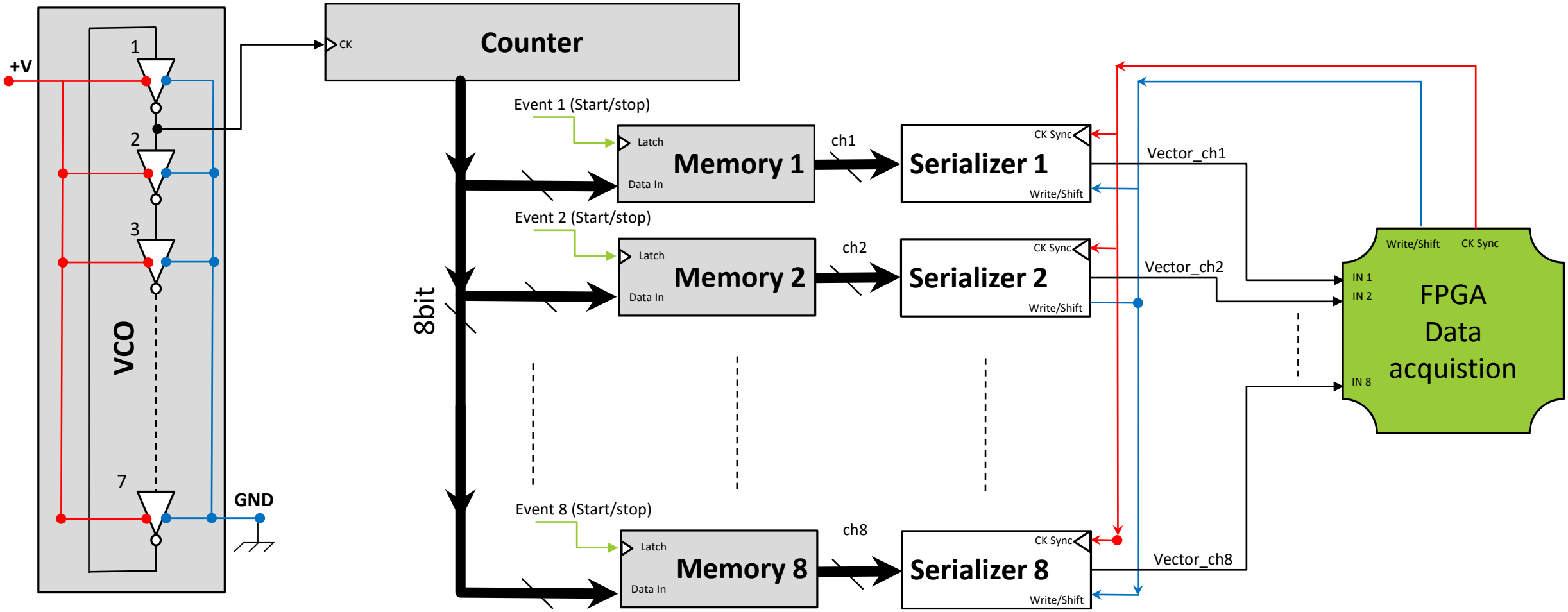
Block Diagram of a single channel chain.The front-End inserted within the same chip using the SiGe Technology.

The integration of these blocks, within the same chip, permit to use the advantages of the SiGe technology, to improve the front-end performance.

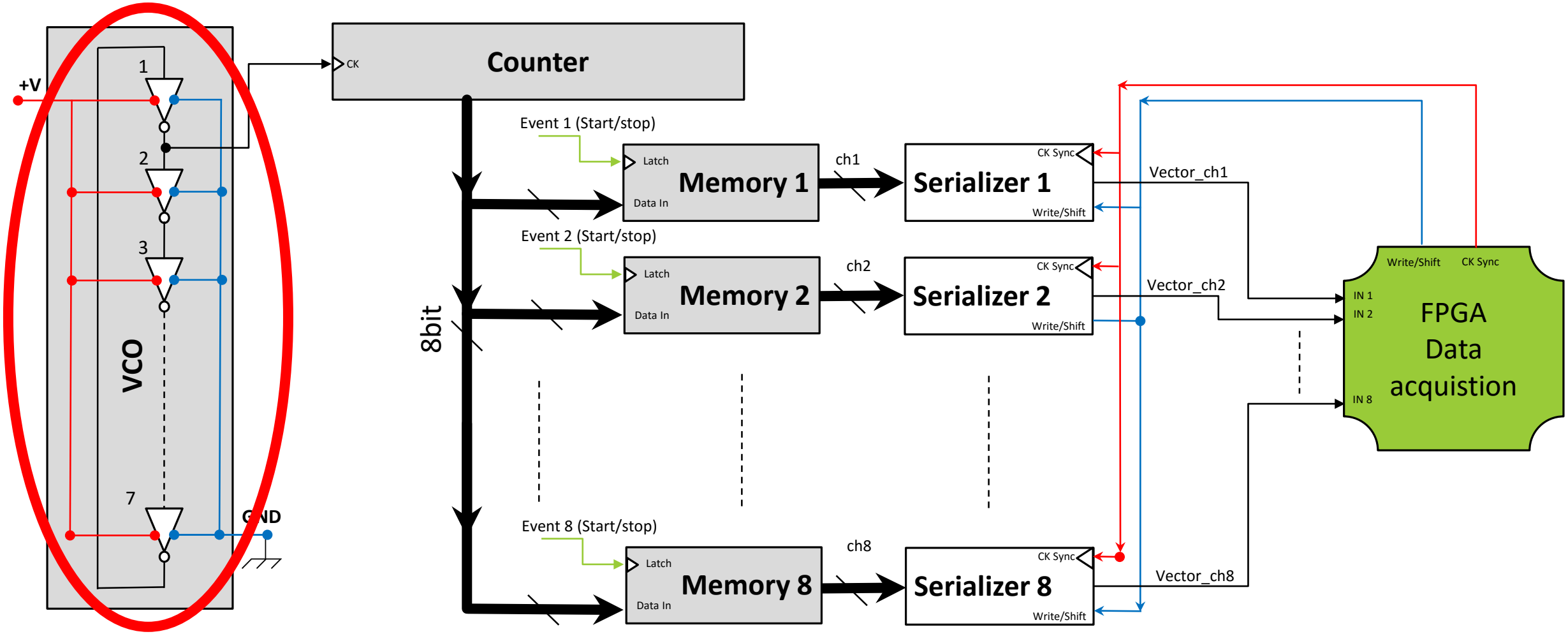
- Lower cost of production of all electronics read-out chain;
- Better time resolution than a TDC compared to the commercial TDC;
- Low power consumption of digital part (around 10- 90 µW / channel);
- Intrinsic radiation-hardness and better radiation tolerance than the classic Si BJT[4]

Future TDC *(time to digital convert)*

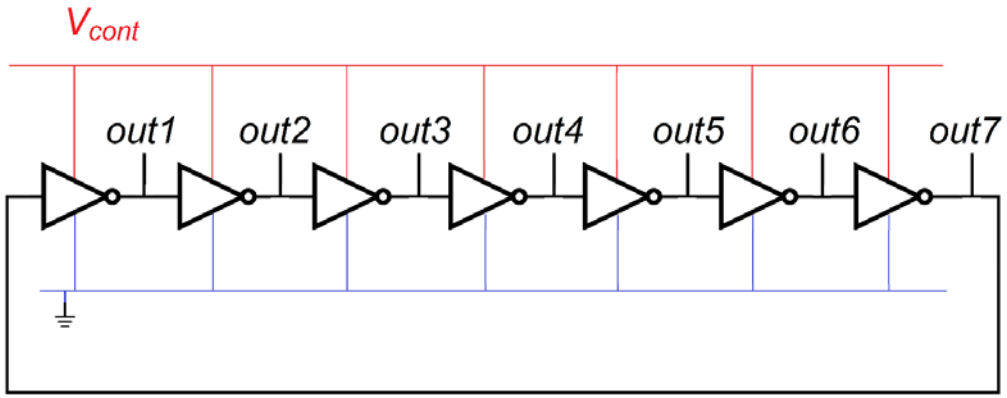
A high-performance and very-low-power TDC with a time resolution of 100 ps. It consists of four functional blocks: an internal oscillator (VCO), a counter , a memory and a serializer. The TDC logic is designed to work both on the rising and falling edge of the event.



Design and result of a VCO



Local oscillator VCO

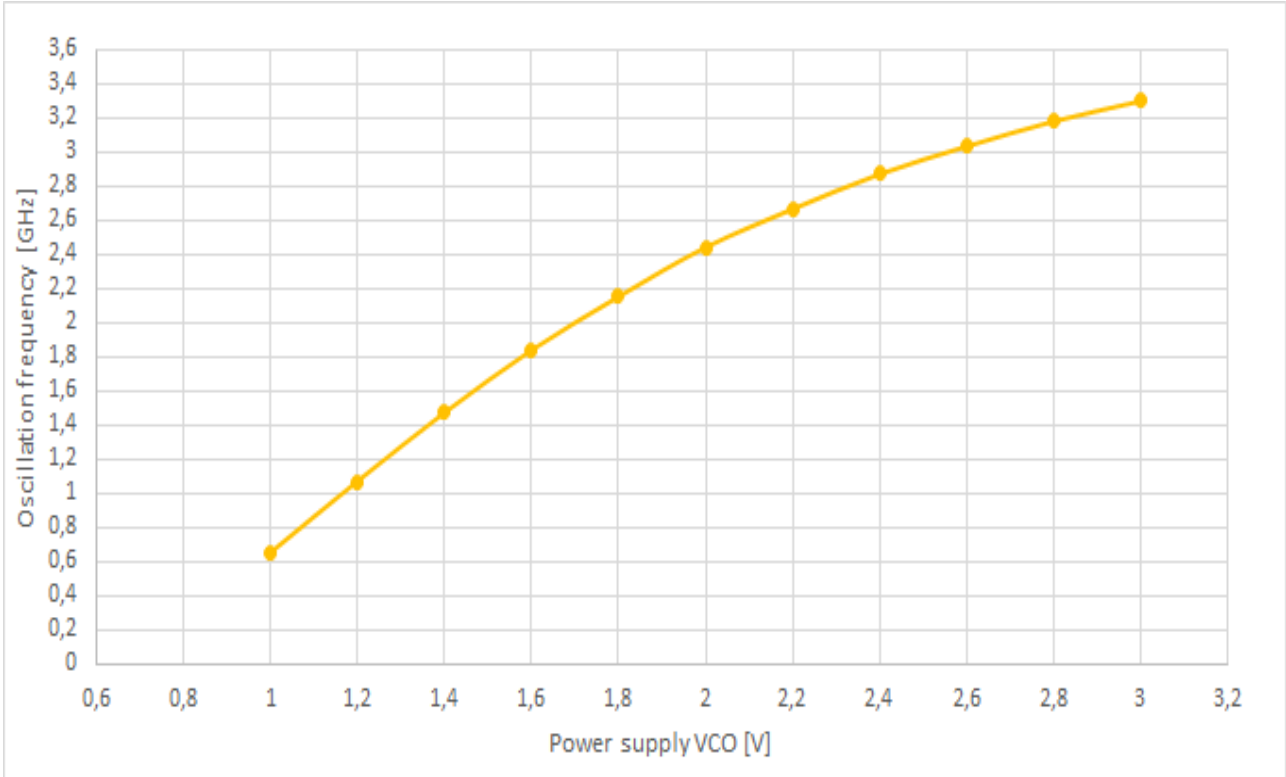


Logic diagram of a Voltage control oscillator (VCO)

- The VCO is realized by a series of 7 NOT gates with a feedback connection.

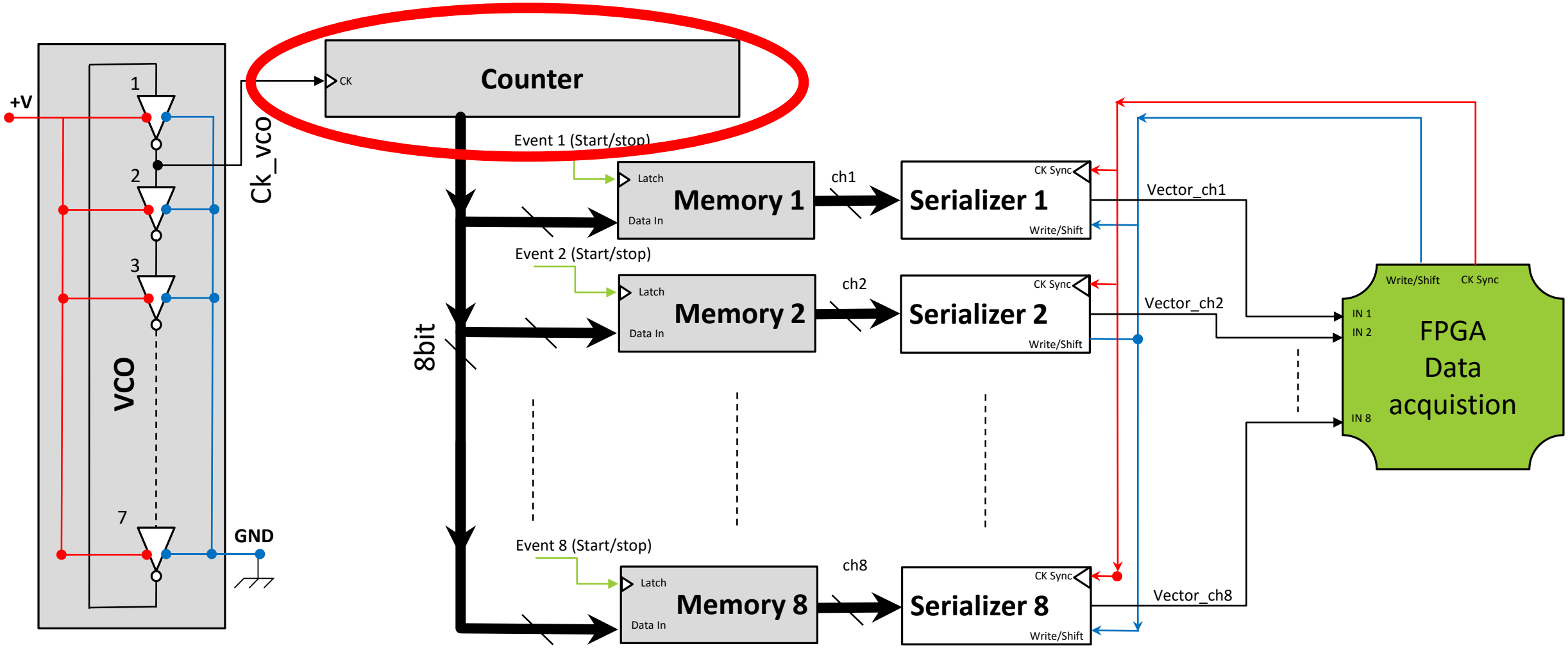
- By varying the VCO voltage supply (0.7 ÷ 3V), we have oscillations between 600MHz and 3.2GHz.

- We have obtained the same results in different mesurement made in different environment conditions.

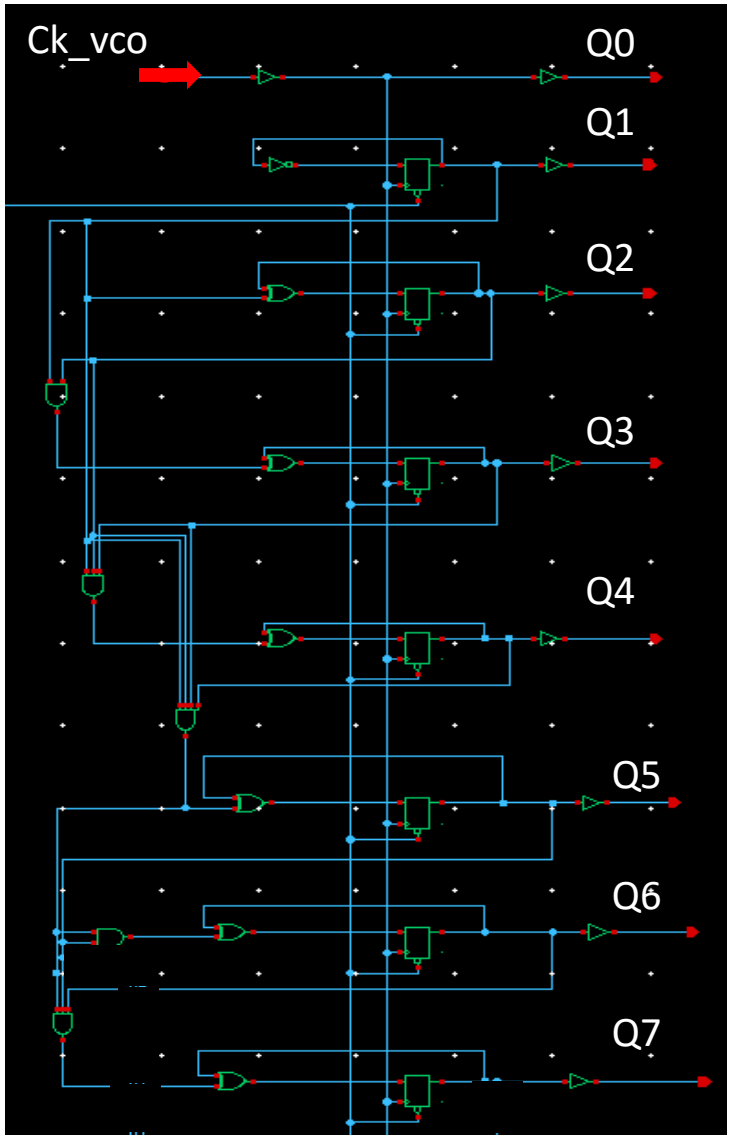


Result obtained during the test of the first prototype

Design of a Counter



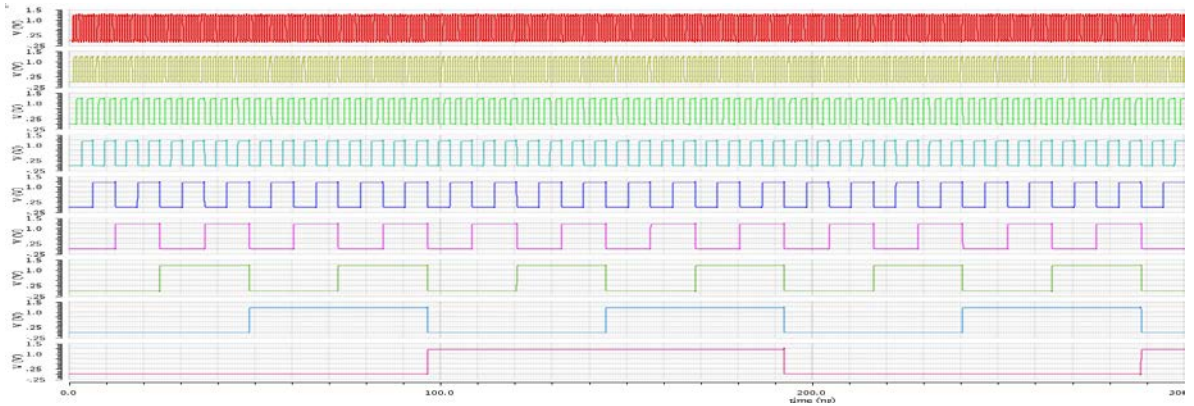
Counter, 8bit



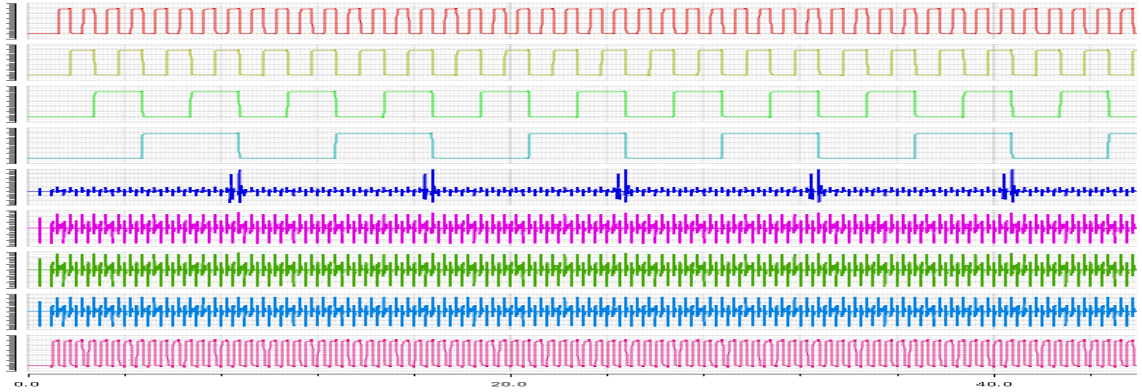
Electric circuit of the Counter at 8 bits

- This counter is called sync because the signal of counting is applied simultaneously at all flip-flop that switch in the same time. This configuration allows to not depending of the switch time.

Ck_vco = 2 GHz



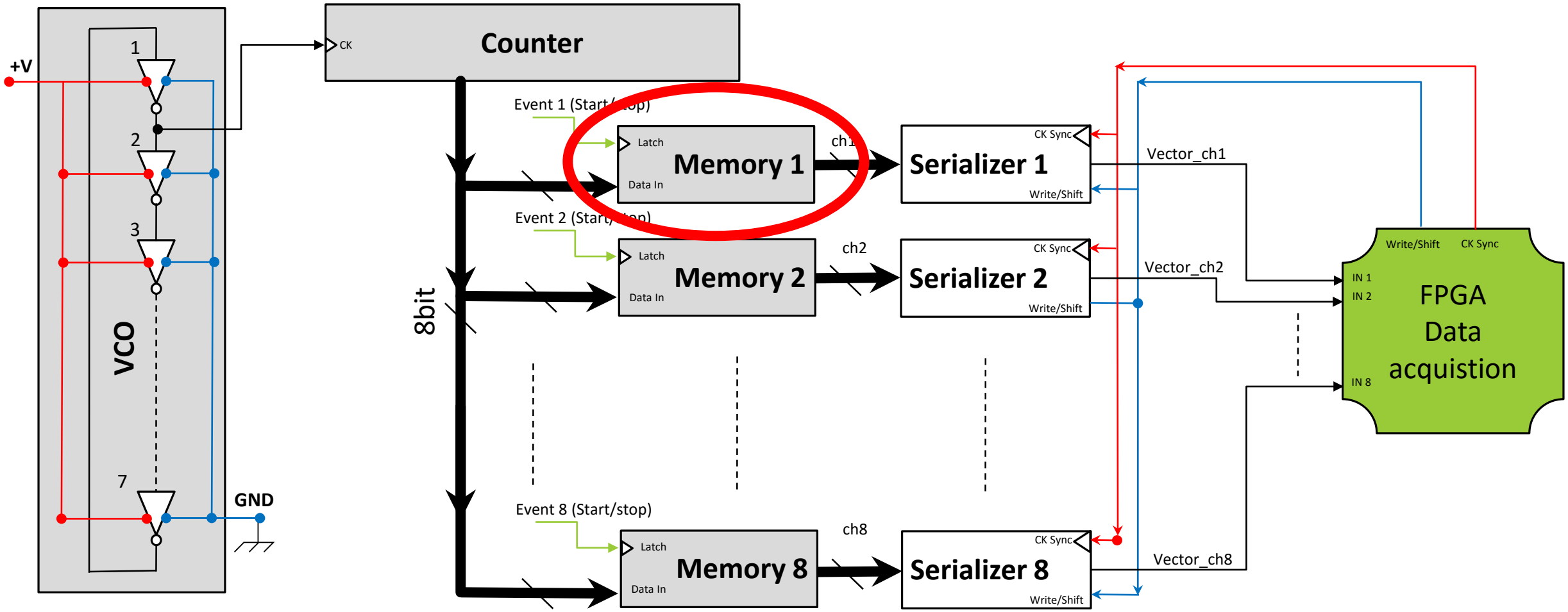
Ck_vco = 2.5 GHz



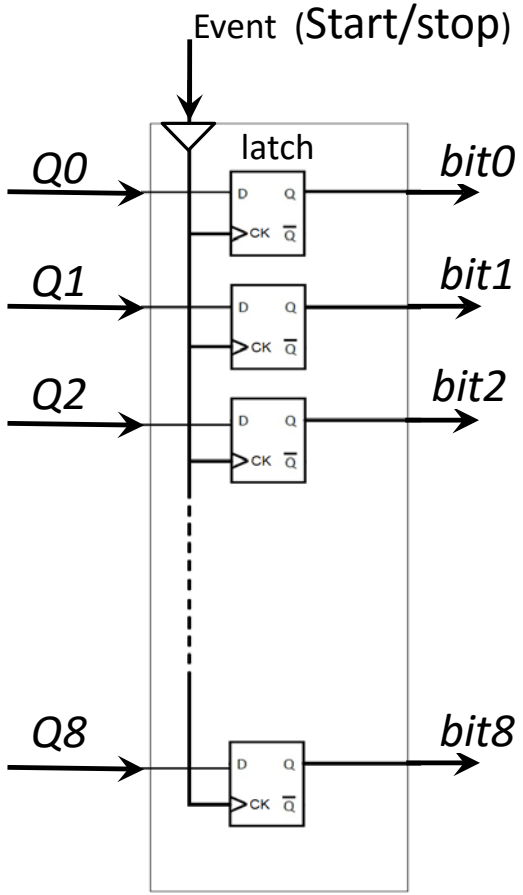
Simulation of the counter at 8 bit, obtained by Cadence software

- This counter works with a signal of counting until a 2 GHz of frequency. This permits a resolution time of 100ps.

Design of a single block Memory/latch

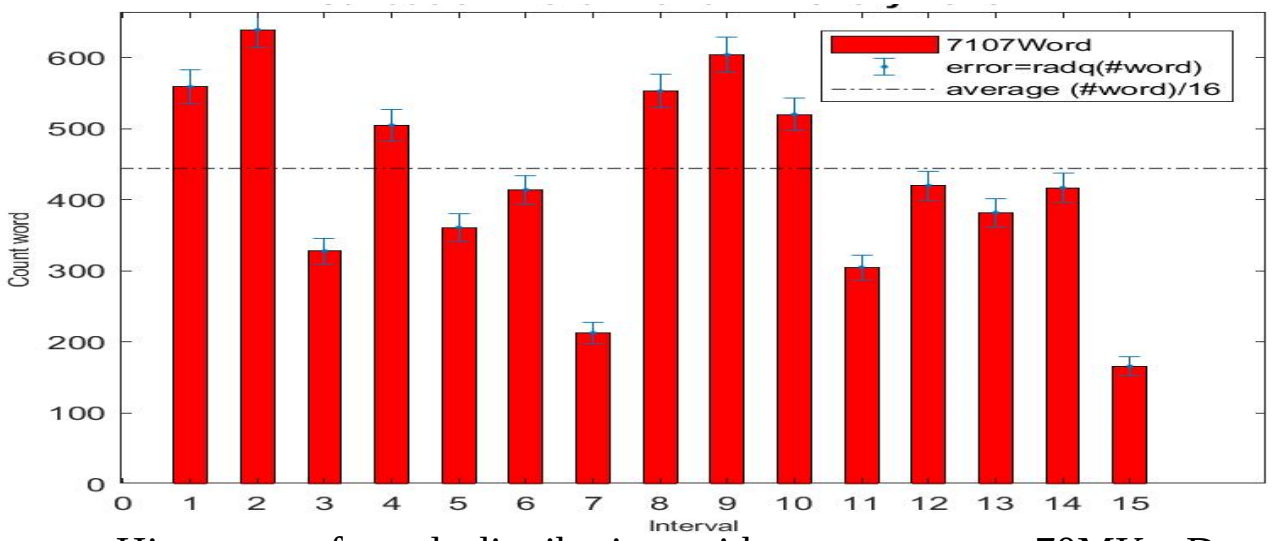


Memory/latch block



Electric schema of the block memory

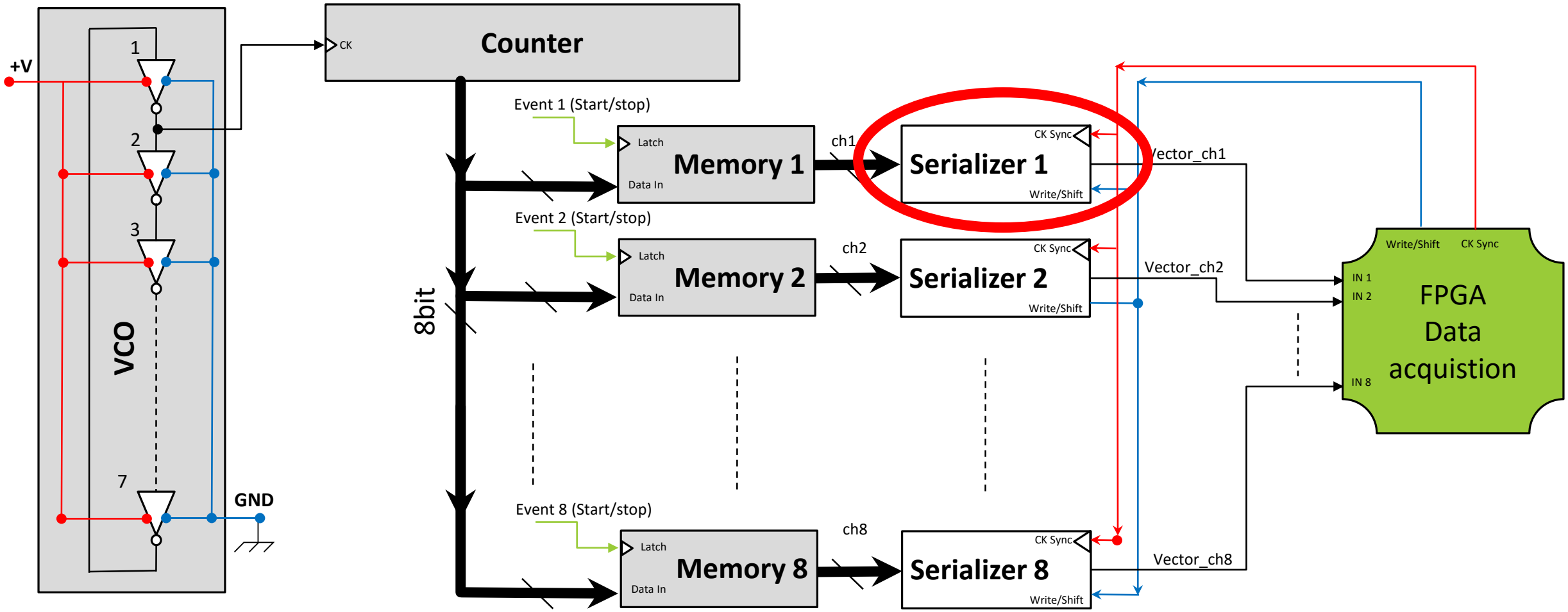
- When the rising edge of the Event (start/stop) arrives, this block takes and saves a picture at the counter's state, which is stored in the counter's output until a new event arrives.
- From the test, we have obtained that this block works correctly up to a rate ~ $100MHz$ of event. Result compatible with the simulations.



Histogram of words distribution, with an event every 70MKz. Data obtained from the prototype test made with 4 bits.

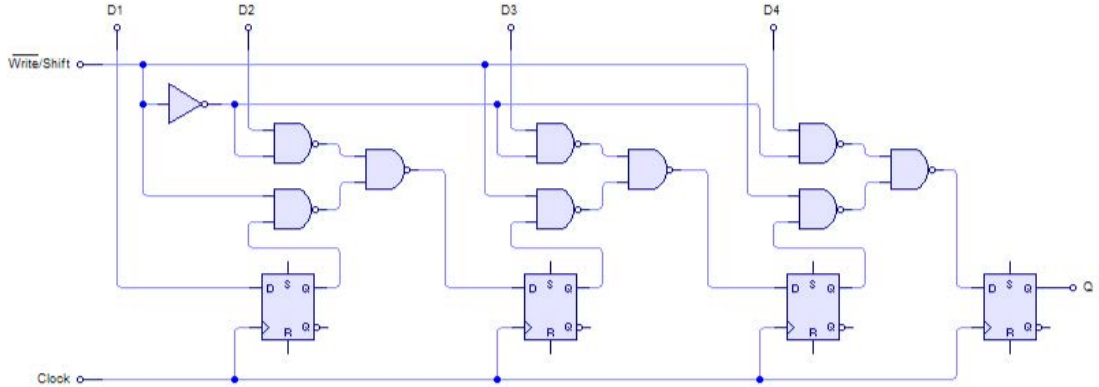
- The words' distribution isn't perfectly uniform because the event was produced by a stimulator that realizes periodic waves. I In order to have a uniform distribution, we should use a casual event.

Study and Design of a single Serializer

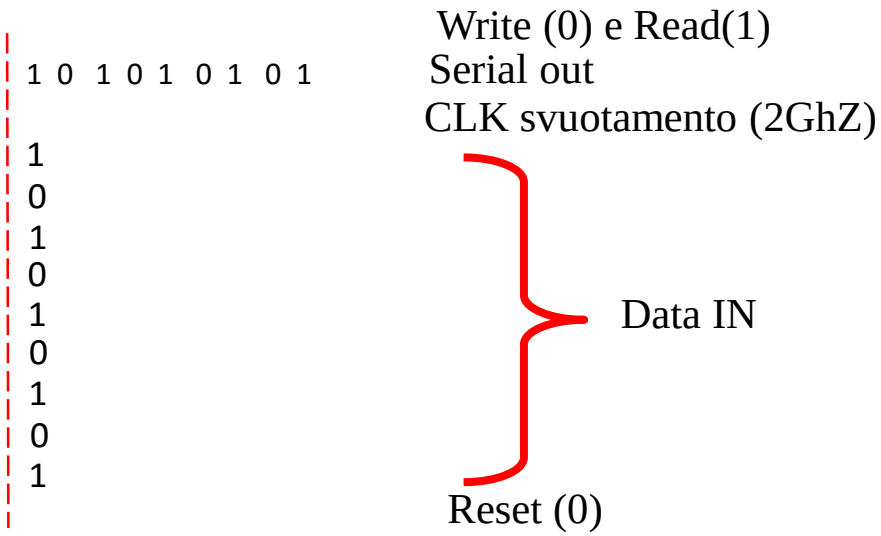


Serializer- PISO (parallell in Serial Out)

Principle of operation



Schema of a serializer at 4 bits.

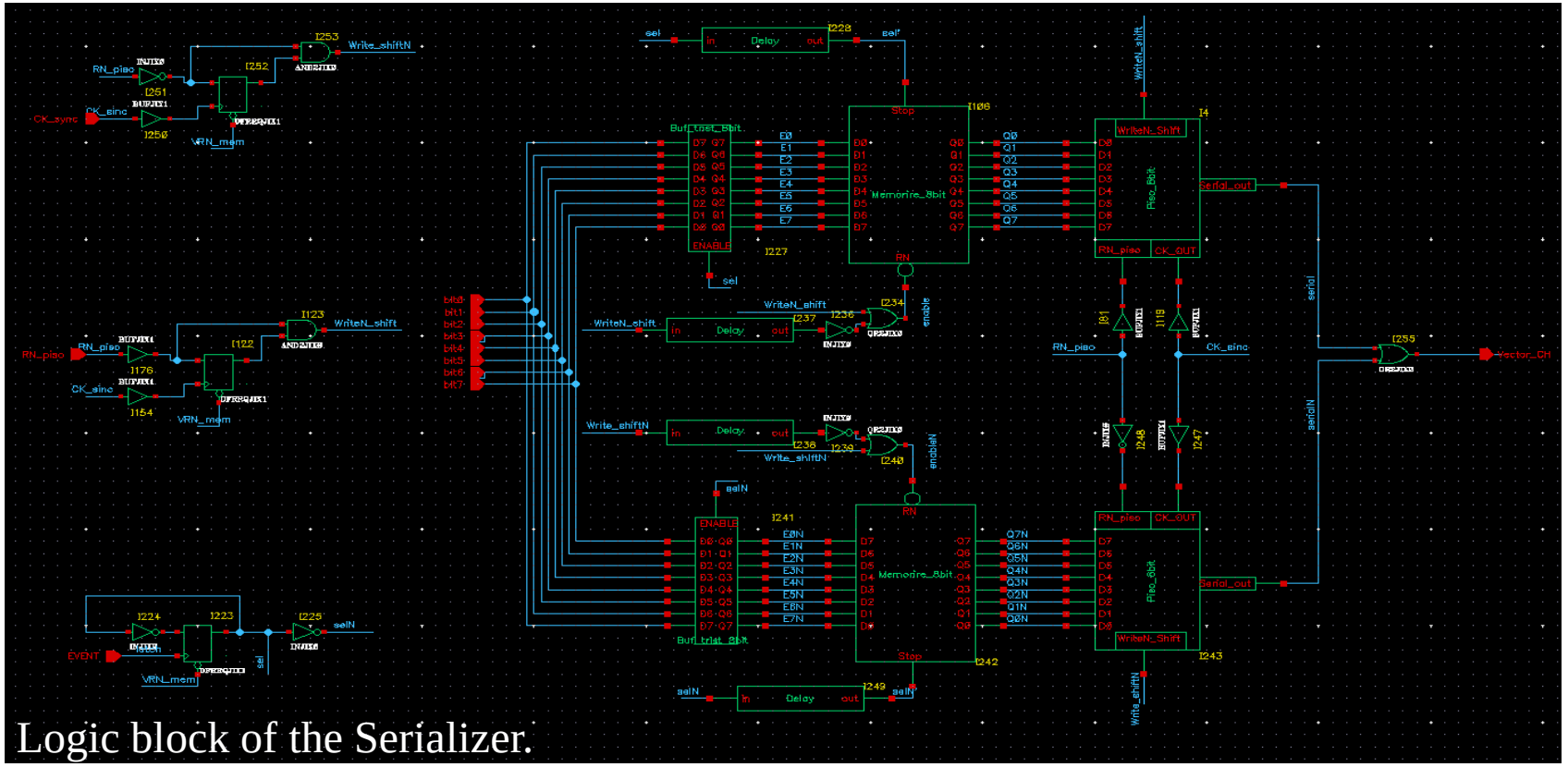


Funzionality test of a Piso

- This device converts the parallel input into a serial output. This operation is managed by a FPGA signal that gives the habilitation to write or read.
- When the signal write_read has a transition, the serializer starts the data transmition.
- The whole process is managed by a clock that it is given at the PISO by the FPGA. This Clock is utilized to synchronize the TDC with the data acquisition system.
- This devices work until 2 GHz of the synchronism clock; this determines the speed of downloading data and consequently also the dead time of the device. We will choose the download speed according to the specifications of the FPGA and the experiment that we will use.
- After each data transfer the serializer must be resetted (0) for a short time.

Improve of the Serializer

To reduce the pill-up of events, caused by the data transmission to the FPGA, we have decided to divide the output of the latch in two different serializer channel (one for "even" events and one for "odd" events). In this way the TDC has the capability to receive a biggest event rate because it will have always a free serializer channel where to save the data and send it to the FPGA when it is free to receive.

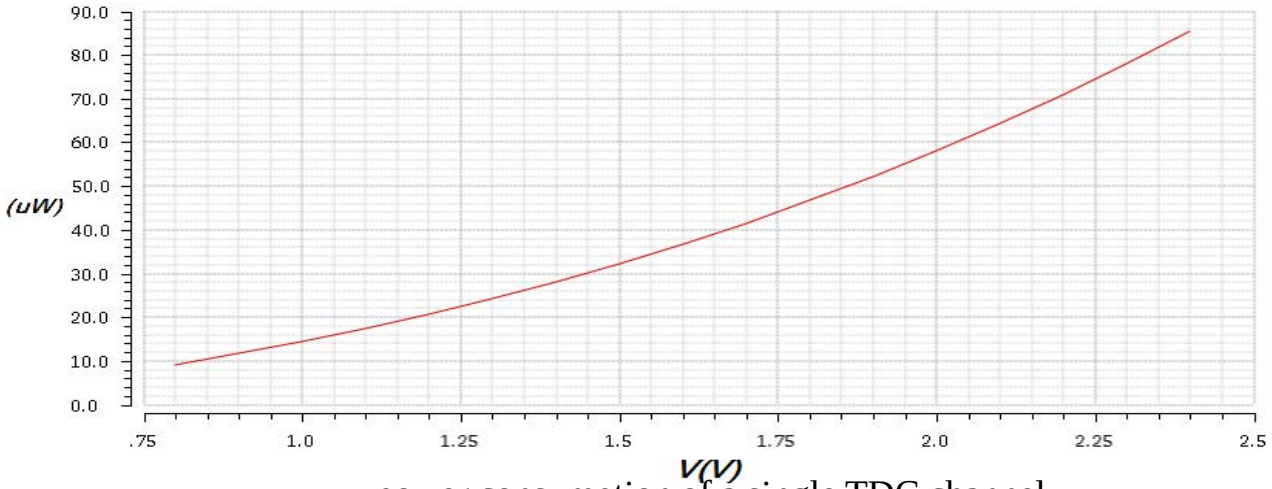


Logic block of the Serializer.

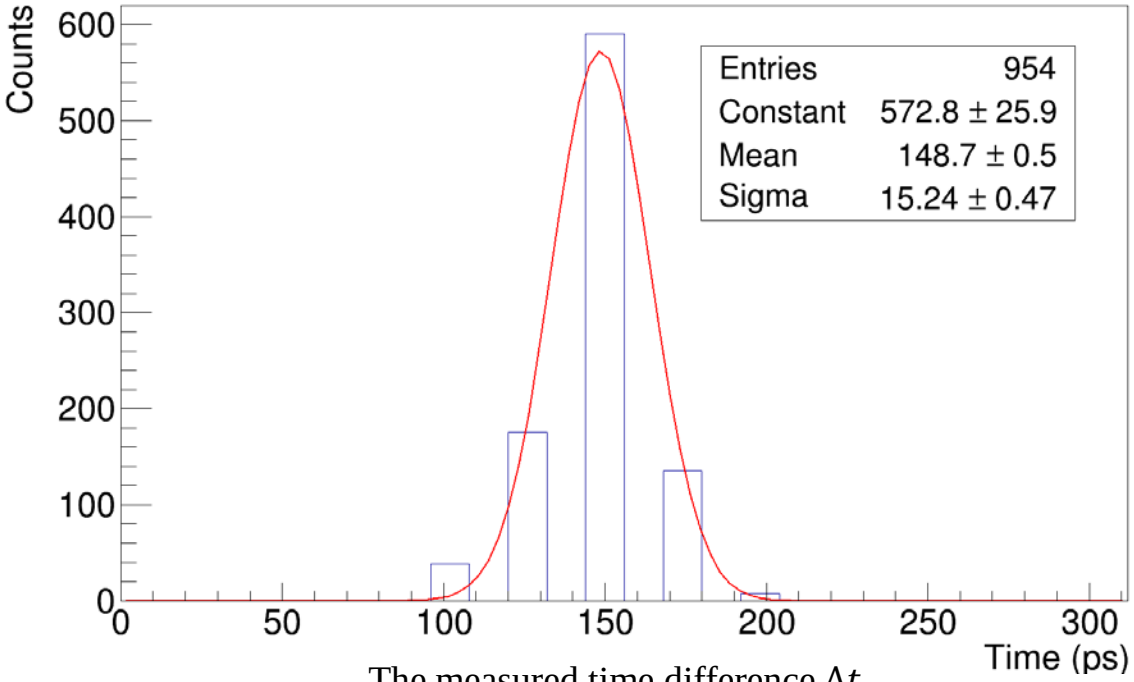
The serializer upgrade permits to arrive at a rate of event up to the same of the frequency synconism clock. Now, this paramiters depend on the FPGA used and on the experiment's requests.

Test's Result of the prototype

The device has a low power consumption, thanks to the BiCMOS technology features.
We can see the lower power consumption of a single TDC channel at a signal rate of 100 MHz for different supply voltages, ranging from $ $10 \div 90\ \mu W$ per channel.



power consumption of a single TDC channel



The measured time difference Δt.

An important test of the TDC consisted in measuring the intrinsic jitter of the VCO, which represents the ultimate limit of the TDC precision. This was done by measuring time interval in-between the rising edges of two consecutive pulses produced at 100 MHz rate with a precision of 5 ps. The intrinsic jitter of the VCO is:

$$\sigma_{vco} = \frac{\sigma}{\sqrt{2}} = 10.77$$

This result also includes the internal jitter of pulse generators.

Next stap

- Accurate and systematic tests on the current prototype, march – august 2018;
- Optimization and layout design of the serializer for the next prototype, run foudry August 2018;
- Desing, Optimization and layout for the coupling of the discriminator and the TDC, foundry run August 2018;

Conclusions and observations

- The study of SiGe technology at 130nm has given good results, that allows to apply them to the SiGe technology on the future PRC front-ends.
- We have understood the feasibility of the a full-custom TDC.
- The results obtained on the prototype are consistent with the simulation.
- The intrinsic jitter of the VCO gives the possibility to realize TDC with precision below 100ps.

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BIBLIOGRAPHY

[1] John D Cressler. Sige hbt technology: A new contender for si-based rf and microwave circuit applications. IEEE Transactions on Microwave Theory and techniques, 46(5):572589, 1998.

[2] Lawrence E Larson. Sige hbt bicmos technology as an enabler for next generation communications systems. 2004.

[3] Ihp - innovations for high performance microelectronics. https://www.ihpmicroelectronics.com/en/start.html. Accessed: 07-09-2017.

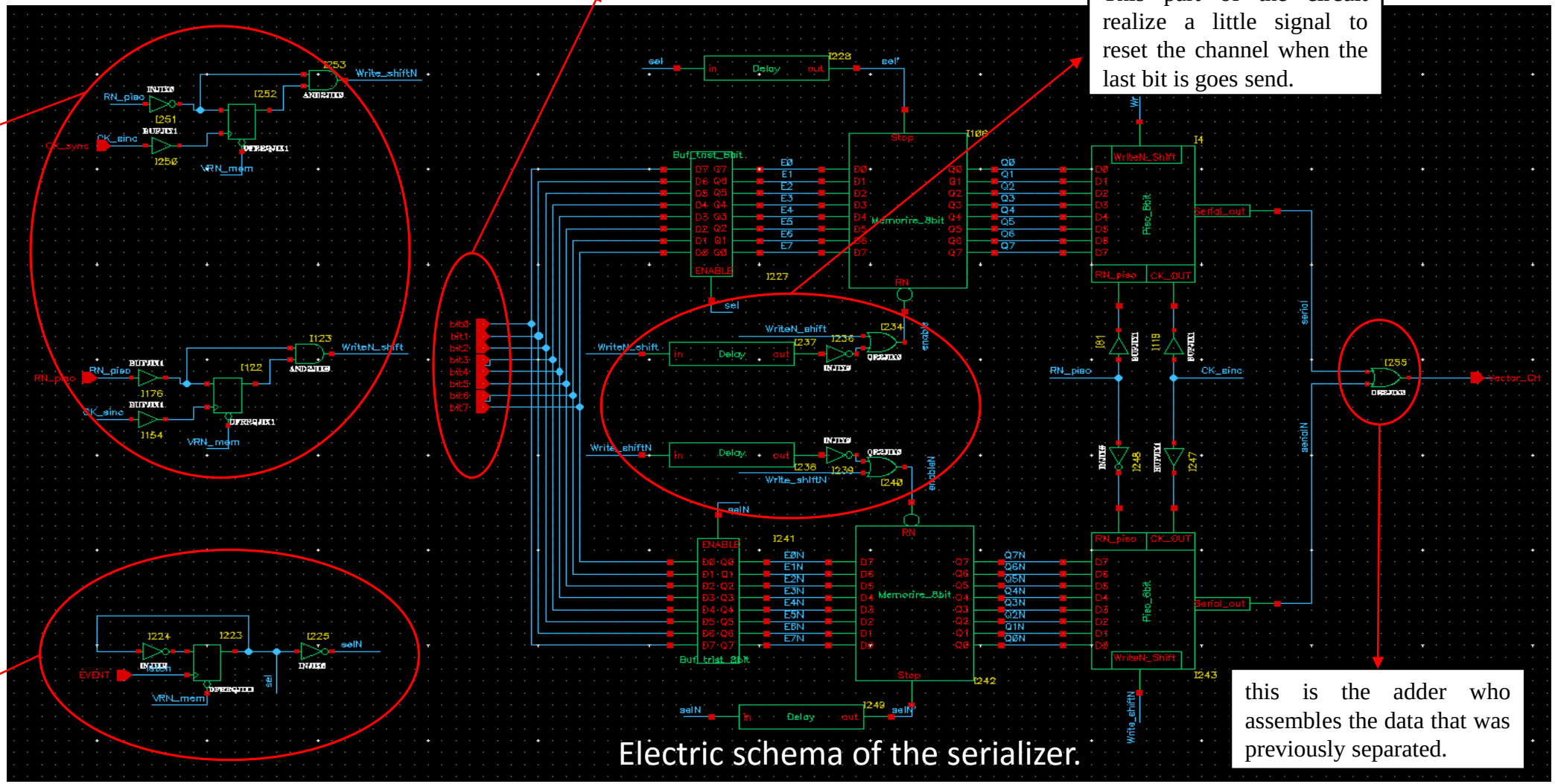
[4] M. Ullan et al. Radiation hardness evaluation of sige hbt technologies for the front-end electronics of the atlas upgrade. Nuclear Instrument s and Methods in Physics Research, 2007.

Improve of the Serializer

This circuit , through the clk_sync and reset of the piso coming of the FPGA, produce a write or read signal for download the data present in one of the serializer.

Input of the data that is stored in the latch block.

This part of the circuit realize a little signal to reset the channel when the last bit is goes send.



Electric schema of the serializer.

This simple divider discriminates odd and even Events. The output of this block is send to the buffer tri state which permit the passage of the data.

this is the adder who assembles the data that was previously separated.