Trigger System

Production Readiness Review

July 2017

D. Evans[1], A. Jusko[1], M. Krivda[1], R. Lietava[1], L. A. Pérez Moreno[2], J. Špalek[3], O. Villalobos Baillie[1]

[1]*School of Physics and Astronomy, University of Birmingham, Birmingham, UK*

[2]*Benemérita Universidad Autónoma de Puebla, Puebla, Mexico*

[3]*Institute of Experimental Physics, Slovak Academy of Sciences, Kosice, Slovakia*

Version 1.0

June 2017

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Document History

Version	Date	Editor	Comments
1.0	12/06/17	R. Lietava	First draft
1.1	27/06/17	A.Jusko, M.Krivda	Comments
1.2	29/06/17	O. Villalobos-Baillie	Comments
1.3	03/07/17	D. Evans	Comments

Definitions and acronyms

BC Bunch Crossing (clock) - the 40.08 MHz clock, locked to the LHC machine cycle, used to synchronise the pipeline processing system.

BUSY Signal generated by a detector to indicate that it cannot accept another trigger.

CRU ALICE Common Readout Unit.

CTP Central Trigger Processor - electronic board that receives inputs from ALICE trigger detectors and generates **LM**, **L0** and **L1** trigger decisions for all detectors.

DAQ (ALICE) Data Acquisition system.(Run2).

DCS (ALICE) Detector Control System.

ECL emitter-coupled logic connector**FLP** First Level Processor (PC in which CRUs are connected).

FMC FPGA Mezzanine Card standard connector.

GBT GigaBit Tranceiver.

HLT (ALICE) High Level Trigger system.

LEMO push-pull connectors made by LEMO.

LM Level-minus trigger.

L0	Level-0 trigger.
L1	Level-1 trigger.
LED	Light Emitting Diode (indicator).
LTU	Local Trigger Unit (board).
LVCMOS	Low voltage CMOS
LVDS	*Low Voltage Differential Signalling* - a standard differential signal format.
O2	Data acquisition system (Run3).
PLL	Phase locked loop.
TTC-PON	TTC 10G-PON.
TTC	Timing, Trigger and Control (system).
TTCex	TTC Encoder/Transmitter (board).
U	Unit of height in the standard 19" rack (1U = 4.36 cm).

1. Introduction

This document describes the tests carried out on the universal ALICE trigger board, the so called CTP/LTU board. The purpose of the document is summarise information for the Production Readiness Review (PRR). The overview of the full system can be found in Trigger System Design Review [1]. This document is divided into sections as follows: Section 2 summarises the ALICE trigger update. Section 3 describes the interface tests of the universal trigger board, the so called CTP/LTU board, performed on two prototypes produced at the beginning of 2017. In section 4, qualification of the optical component for the GBT system is presented. Section 5 summarises the TTC-PON firmware and its tests. Section 6 provides information on the general LVDS input/output FMC card being designed for CTP inputs. Section 7 presents the option for providing LTUs, with power supplies, as independent standalone units. The software is described in section 8. The milestones are listed in the last section.

2. The ALICE Trigger Upgrade

The ALICE Upgrade will require a very different triggering strategy from the current one and hence a new Central Trigger Processor (CTP) is needed. The CTP will manage a system of detectors with markedly different properties. The majority of detectors, which will read out at the nominal interaction rate, are dead-time free. However, in order to provide backwards compatibility for detectors not being upgraded, the trigger system must cope with detectors which will have dead-time during the read-out.

The strategy for selecting events for readout will also be different from that employed in previous runs. Previously, despite the fact that ALICE events are highly complex, the trigger strategy was to combine a Minimum Bias sample with one selected according to thresholds in high E_T (calorimeter triggers), high p_T, or high multiplicity. The strategy for the ALICE upgrade system is to read out *all* interactions and apply an online filtering in the high level trigger (HLT).

In Run 3 the interaction rates will increase to ~ 50 kHz for Pb-Pb, and 200 kHz for p-p and p-A (and where feasible a safety margin of two is applied in the system design). The aim of the ALICE trigger system is to select essentially all of these interactions; the events are then read out and the event records are sent to the HLT farm for further filtering. To achieve this, a combination of continuous readout detectors and a minimum bias trigger based on the new forward Fast Interaction Trigger (FIT) detectors is used, with a few additional inputs to allow for cosmic triggers and calorimeter based triggers to enhance rates for some types of events where the minimum bias trigger is inefficient.

2.1 Trigger Architecture

The overall trigger architecture is shown in Figure 2.1. For Run 3 we will keep the concept of a Central Trigger Processor and Local Trigger Units as detector interfaces but advances in FPGA technology mean it is now possible to have all the functionality of the CTP on a single 6-U board. Figure 2.1 shows the six detectors that will deliver trigger inputs to the CTP and the three ways the trigger data will be distributed to the detector Front End Electronics (FEE).

Detectors not upgrading their FEE will have trigger data sent via the TTC system [2], directly to their FEE. Most of the detectors being upgraded will receive trigger data via a TTC 10G-PON (TTC-PON) optical link [3][4] to their Common Readout Units (CRUs) but some will require a direct link via GBT [5]. Trigger inputs are collected to satisfy three different latencies, giving hardware triggers at three different latencies known as LM, L0 and L1.

The trigger system itself will consist of a CTP board and a Local Trigger Unit (LTU) board for each detector. The interface between CTP and LTU boards is PON. The schematic layout of the system is shown in Figure 2.2. All boards will be 6U VME type boards but the VME connectors will be used for power only due to the limited speed of the VME backplane.

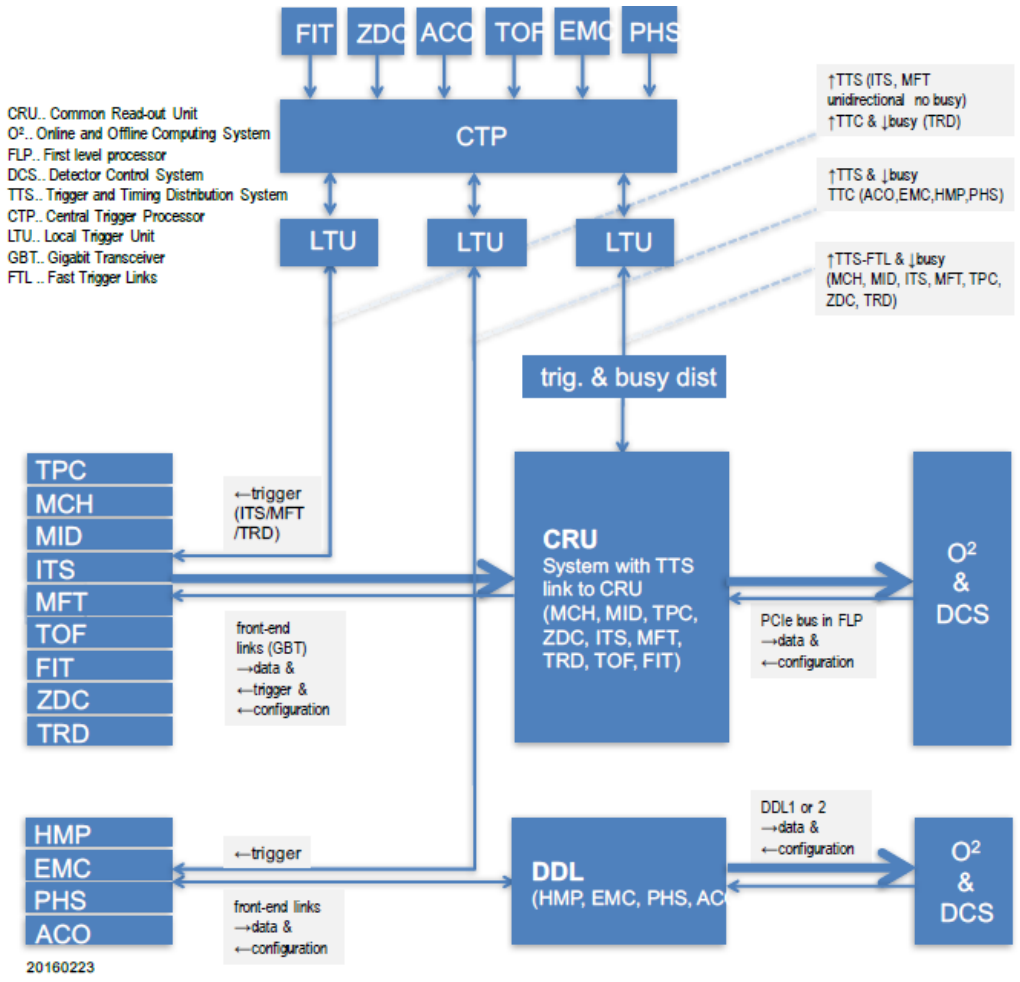

Figure 2.1 Summary of trigger distribution

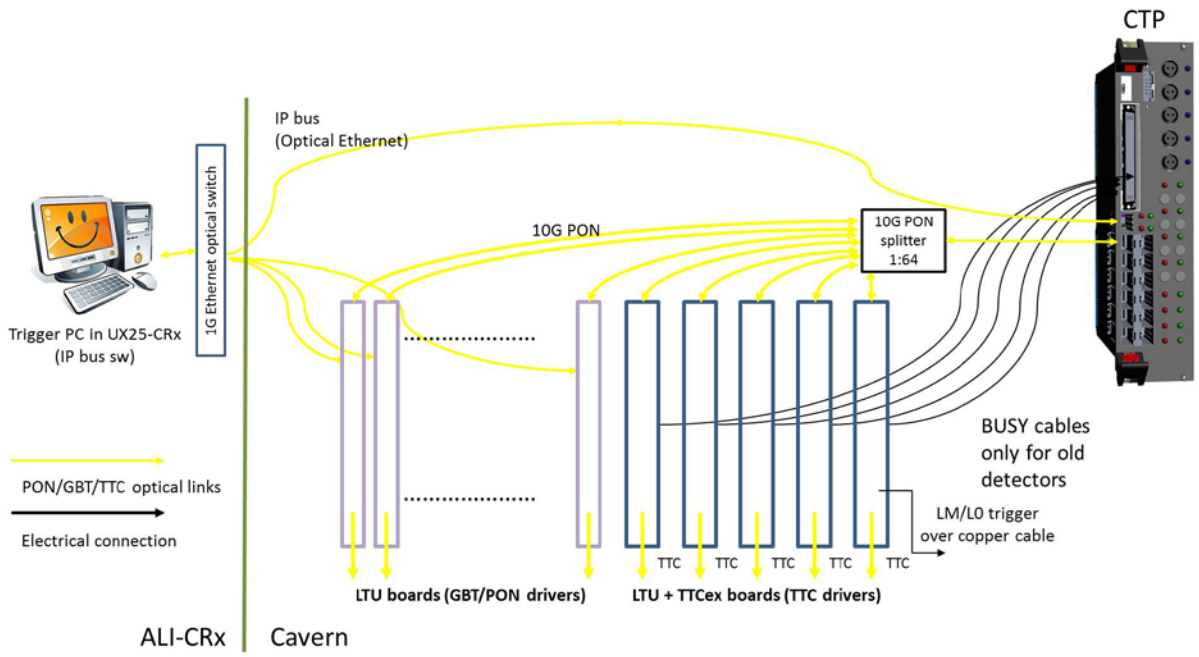

Figure 2.2 Schematic layout of the Trigger System

3. ALICE CTP/LTU trigger board tests

3.1 Introduction

In this section the results of the universal board tests are presented. The board is a 6U VME-type board and uses the existing CTP/LTU VME crates for power only. Photographs a prototype trigger board are shown in Figure 3.1.

The board is provided with:

- a new XILINX series KINTEX Ultrascale (XCKU040-1FFVA1156C) FPGA with sufficient frequency range to implement PON and GBT, thus keeping flexibility to use TTC-PON or GBT,
- 2 GB of DDR4 memory, partitioned so as to allow adequate storage of snapshot data, with reserved space for future applications,
- a universal FMC connector (connected to a simple mezzanine card for 70 LVDS inputs/outputs in the CTP case or to a mezzanine card with an additional seven optical connections in the LTU case),
- a 12 slot cage for optical input/output GBT or TTC-PON. These inputs/outputs will be populated in accordance with the board's given role (CTP/LTU) and detector (number of outputs),

- an optical SFP+ link to a O2 (or dedicated Trigger) PC using IP-BUS protocol for monitoring and control. An electronic Ethernet SFP+ module, instead of an optical module, will be used for IP-BUS communications when using the CTP/LTU in the lab.

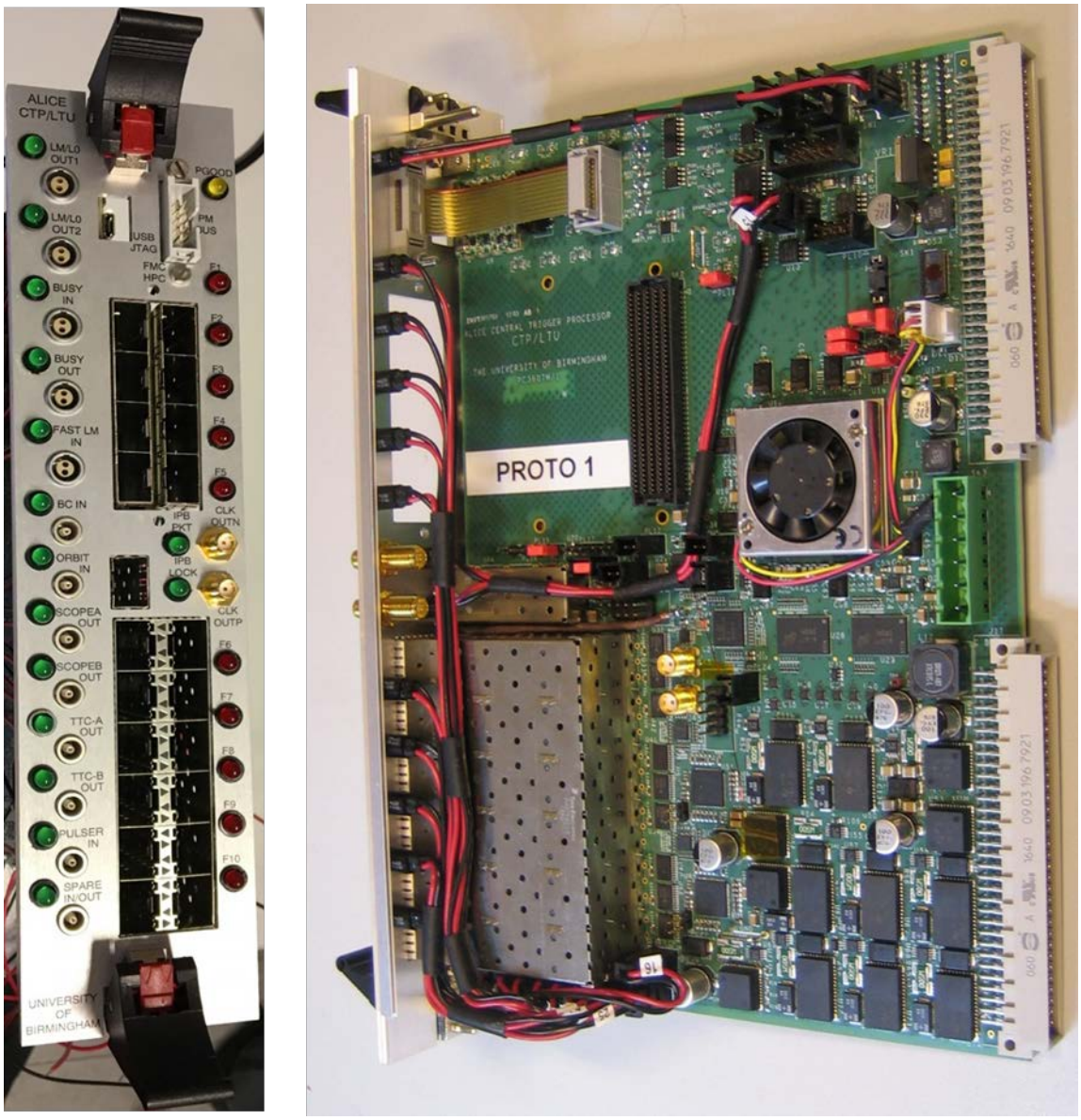

Figure 3.1 Trigger board

3.2 Board Interfaces

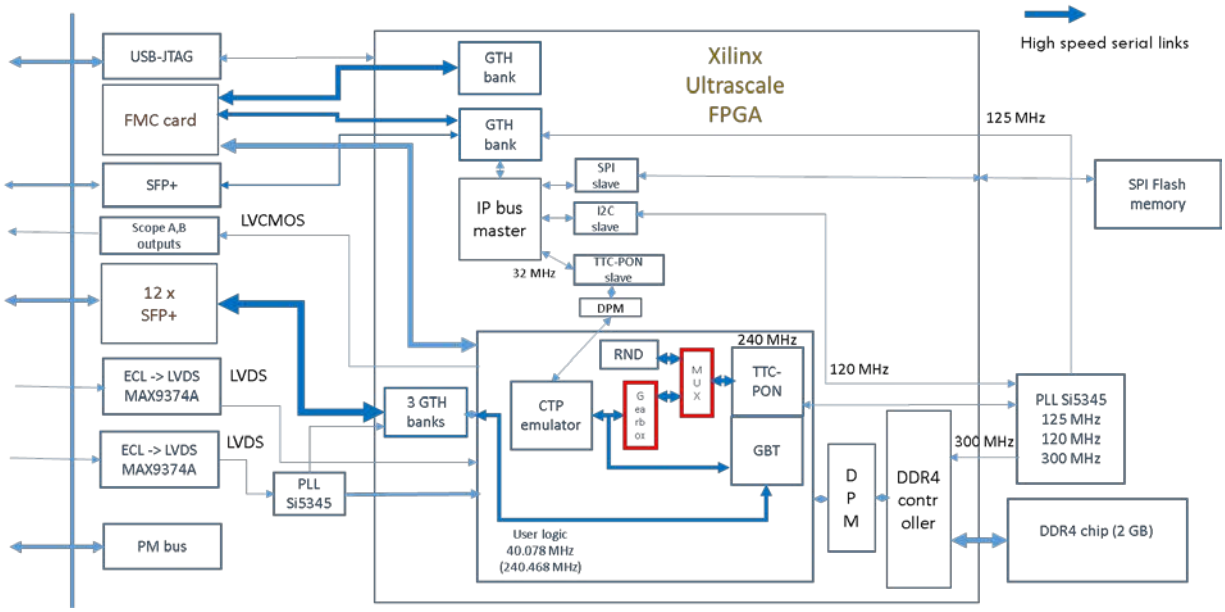

Figure 3.2 CTP/LTU board interfaces

All inputs/outputs to/from the board will be performed via the front panel. The I/O connections are as follows (see Figure 3.1 Trigger board):

1. A PM bus connector for voltage and temperature monitoring
2. A USB-JTAG connector for configuring the Kintex-Ultrascale FPGA. In the ALICE cavern, the JTAG will be connected to the Trigger PC located on surface via a USB to Ethernet module (Anywhere© USB) which makes an interface between USB and Ethernet protocols.
3. A FMC connector: 70 LVDS I/O connector on the mezzanine FMC board for trigger inputs, BUSY inputs (via LTUs), and a special fast LM trigger output for the TRD detector.
    a. Note the current number of trigger inputs is expected to be 31, the number of BUSY inputs is 6 (one per detector using current TTC system), and one output is reserved for the fast LM (pre-trigger) signal to the TRD. This leaves a total of 34 spare I/Os.
    b. An adaptor cable, known as the spider, has a 200 pin Molex connector on one end and LVDS LEMO connectors on the other end so that the connectors for trigger and BUSY inputs will remain the same as for Runs 1 and 2.
4. A SFP+ optical connector for the control and monitoring interface to the O2 (or dedicated Trigger PC).

    a. Note the optical connector unplugs and can be replaced by an electrical Ethernet SFP+ connector for control and monitoring in the lab.
5. Two LEMO LVCMOS outputs for an oscilloscope
6. Five LVDS LEMO B connectors
7. Eight LEMO 00 b ECL connectors
8. 12 optical connections

The CTP/LTU board interfaces are schematically shown in Figure 3.2. They are discussed in detail in the following subsections.

3.2.1 Power tests (1)

After careful visual inspections and short circuit measurements, the PM bus was activated. A problem with the MON5 input was detected involving, the missing monitoring of VIN. It has since been fixed.

In Table 3.1, the results of voltage measurements, using two different methods, are presented for both prototype trigger boards. The first method involves measurements using a multimeter at testing points. The second method is using the Fusion Digital Power Designer package, which can also be used in command line mode, as demonstrated in Figure 3.3. The various columns in Table 3.1 are as follows: 1st column: voltage name; 2nd column: required voltage; 3rd column: Test Point; 4th column: voltage measured by multimeter; 5th column: the deviation of measured value from required value in percentage; 6th column: voltage measured by fusion digital power designer (part of Power Management); 7th column: the deviation of measured value from required value in percentage.

Figure 3.4 shows an example of temperature and voltage measurements, measured in the FPGA and displayed by VIVADO software [6]. Vivado Design Suite is software suite produced by Xilinx for synthesis and analysis of HDL designs.

3.2.2 FPGA programming tests (2)

A USB-JTAG interface [7] and VIVADO software were used to program the FPGA. One of the first tests was uploading the IPbus firmware, which is used as the main board control interface (see also 3.2.4).

3.2.3 FMC tested (3)

The FMC loopback tester board (see Figure 3.5) enables enabled us to test and characterize the FMC carrier board interfaces. The board features full differential loopbacks on all FMC high pin count connector interfaces including LA, HA, HB, DP and CLK. It also provides a 125 MHz transceiver LVDS reference clock on GBTCLK signals.

Table 3.1Voltage system on trigger prototype boards

	Proto 1						Proto 2					
Name	Required V	Test Point	Measured		Measured		Required V	Test Point	Measured		Measured	
		(TP)	Multimeter		Fusion			(TP)	Multimeter		Fusion	
	[V]		[V]	[%]	[V]	[%]	[V]		[V]	[%]	[V]	[%]
VCCINT	0.95	(RS1)	0.959	0.9%	0.947	-0.3%	0.95	(RS1)	0.9738	2.5%	0.95	0.0%
MGTAVCC	1	(RS3)	0.998	-0.2%	0.986	-1.4%	1	(RS3)	1.013	1.3%	0.991	-0.9%
VCCBRAM	0.95	(RS5)	0.953	0.3%	0.942	-0.8%	0.95	(RS5)	0.9657	1.7%	0.948	-0.2%
MGTAVTT	1.2	(RS2)	1.197	-0.2%	1.184	-1.3%	1.2	(RS2)	1.211	0.9%	1.19	-0.8%
VCCAUX	1.8	(RS6)	1.809	0.5%	1.787	-0.7%	1.8	(RS6)	1.851	2.8%	1.802	0.1%
VCC1V8	1.8	(RS8)	1.811	0.6%	1.795	-0.3%	1.8	(RS8)	1.848	2.7%	1.787	-0.7%
VADJ1V8	1.8	(RS7)	1.817	0.9%	1.79	-0.6%	1.8	(RS7)	1.856	3.1%	1.788	-0.7%
VCC1V2	1.2	(RS10)	1.2	0.0%	1.187	-1.1%	1.2	(RS10)	1.21	0.8%	1.18	-1.7%
MGTVCCAUX	1.8	(RS9)	1.809	0.5%	1.794	-0.3%	1.8	(RS9)	1.845	2.5%	1.784	-0.9%
3V3	3.3	(RS4)	3.325	0.8%	3.306	0.2%	3.3	(RS4)	3.422	3.7%	3.371	2.2%
UTIL_3P3V	3.3	(C129)	3.318	0.5%			3.3	(C129)	3.403	3.1%		
DDR4_VTT	0.6	(C70)	0.608	1.3%			0.6	(C70)	0.605	0.8%		
VCC5V0	5	(TP4)	4.962	-0.8%			5	(TP4)	4.94	-1.2%		
2V5	2.5	(C94)	2.524	1.0%			2.5	(C94)	2.53	1.2%		
-3V3	-3.3	(C1)	-3.398	3.0%			-3.3	(C1)	-3.394	2.8%		

```
Select Command Prompt
C:\Program Files (x86)\Texas Instruments\Fusion Digital Power Designer\bin>FusionParamReader --scan READ_VOUT
PartID  AddressDecimal  CmdIDWithPhase  PageHex SAAStatus       Decoded DecodedNumeric  EncodedHex
UCD90120A       101     READ_VOUT       0x00    ACK     0.950 V 0.95    0x3CD4
UCD90120A       101     READ_VOUT       0x01    ACK     0.993 V 0.993   0x3F90
UCD90120A       101     READ_VOUT       0x02    ACK     0.949 V 0.949   0x3CC0
UCD90120A       101     READ_VOUT       0x03    ACK     1.190 V 1.19    0x4C24
UCD90120A       101     READ_VOUT       0x04    ACK     1.802 V 1.802   0x39AE
UCD90120A       101     READ_VOUT       0x05    ACK     0.000 V 0       0x0000
UCD90120A       102     READ_VOUT       0x00    ACK     1.787 V 1.787   0x392C
UCD90120A       102     READ_VOUT       0x01    ACK     1.789 V 1.789   0x3940
UCD90120A       102     READ_VOUT       0x02    ACK     1.180 V 1.18    0x4B84
UCD90120A       102     READ_VOUT       0x03    ACK     1.785 V 1.785   0x391C
UCD90120A       102     READ_VOUT       0x04    ACK     3.231 V 3.231   0x33B4
```

Figure 3.3 Fusion Digital Power Designer – command line measurement

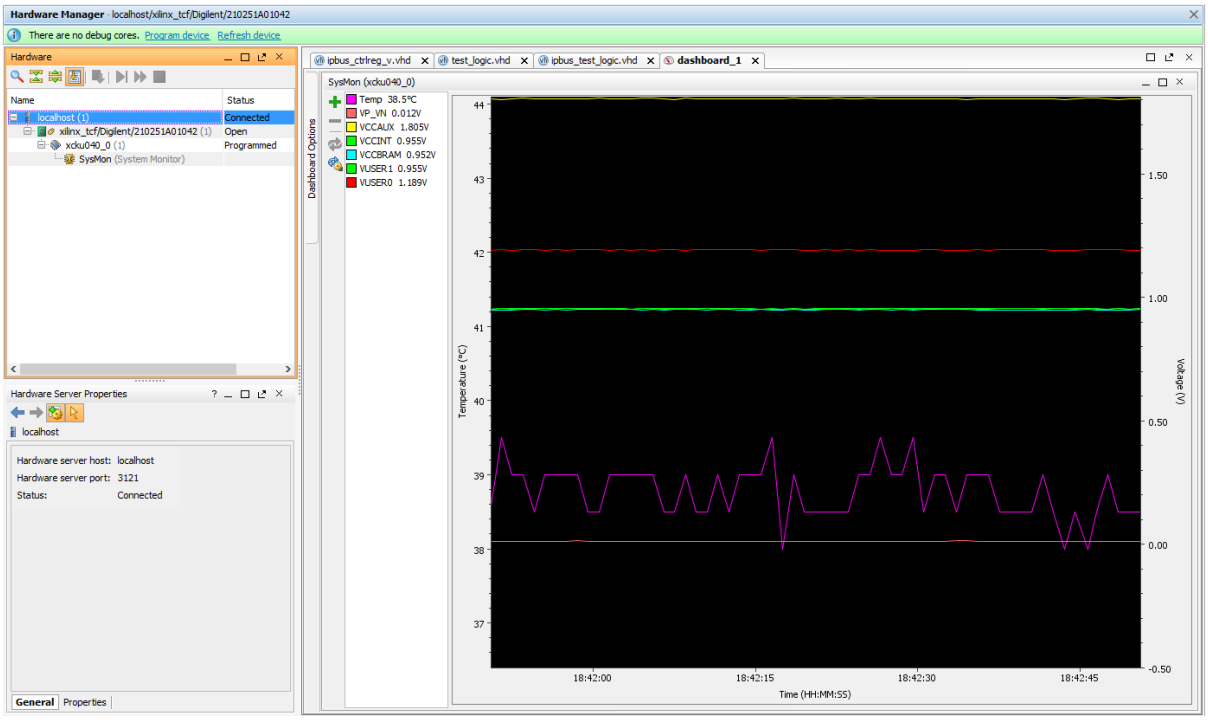

Figure 3.4 Temperature and FPGA core voltages

Figure 3.5 FMC loopback test board

3.2.4 SFP+ tested (4)

The IP bus control protocol was already tested and used on the evaluation boards. No problems were encountered when implemented on CTP/LTU board. IP bus access via I2C was tested to all SFP+ modules (12+8) by reading the manufacturer ID and serial number of the SFP+ module.

3.2.5 Front panel tests (5,6,7)

The output connectors were tested by connecting an internal clock to each output and monitoring it via a high-performance oscilloscope connected to the output.

The input connectors were tested by loop internal clock -> output connector –> cable -> input connector -> scope output.

3.2.6 SFP links (8)

3.2.6.1 IBERT test

IBERT tests (scan, sweep, BER) with 20 active high speed links/SFP+ modules using an AFBR-709DMZ 1G/10G Ethernet optical module were carried out. A FMC S-18 card was used for 10G serial links. The SFP+ connections are described onFigure 3.6. The results of the eye scan test are in Table 3.2 and Figure 3.7. In Table 3.2 the 1st column shows the name of high speed bank (Multi Gigabit Transceiver - MGT_LINK). The following columns show:

TX_DIFF amplitude of Gigabit Transceiver (GTH) output of high speed data sent to SFP. The measured values are the horizontal width of the eye scan open area.

The Eye scan tests indicate that two links on the FMC card – X0Y12, X0Y13 – have high attenuation. The producer of the board has been contacted. Bit Error rates were measured for 36 hours without any errors being detected. This provides an estimated bit error rate of less than 10^{-15} (see Figure 3.7).

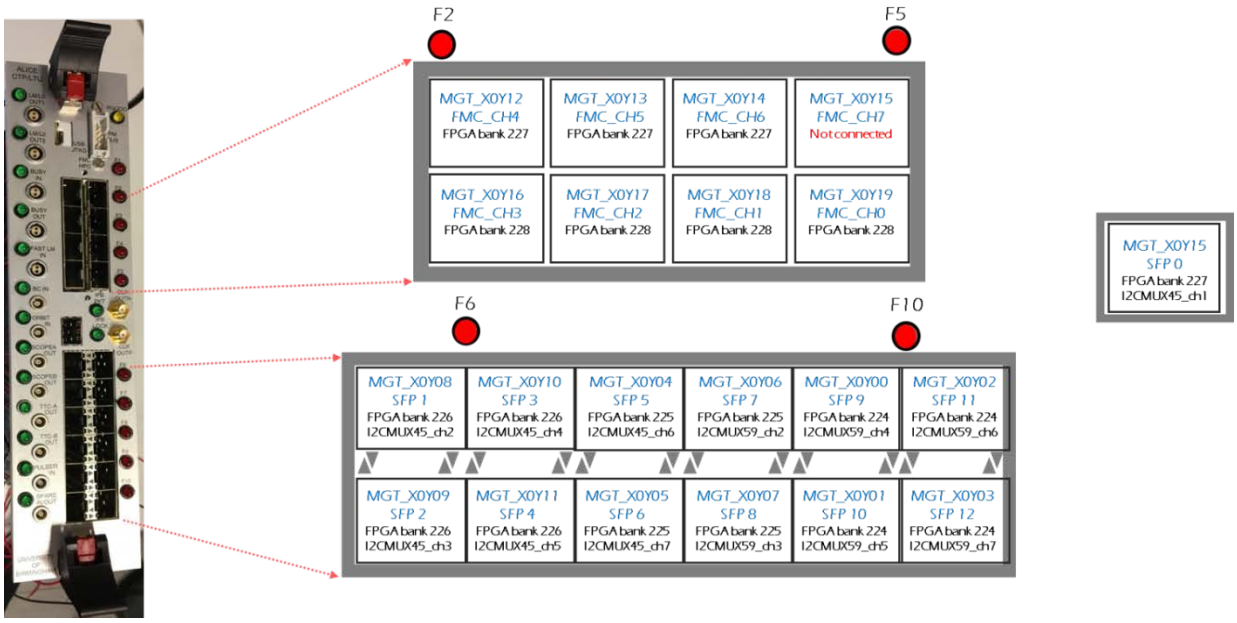

Figure 3.6 SFP+ connections

Table 3.2 Eye scan tests results

	Eye Scan Open Area (UI) 10Gbps							Eye Scan Open Area (UI) 9.6Gbps			
MGT_LINK	TX_DIFF 1080 mV	TX_DIFF 1080 mV FMC	TX_DIFF 840 mV	TX_DIFF 840 mV FMC	TX_DIFF 660 mV	TX_DIFF 660 mV FMC	TX_DIFF 390 mV	TX_DIFF 1080 mV	TX_DIFF 840 mV	TX_DIFF 660 mV	TX_DIFF 390 mV
X0Y19	2304	4352	2176	3392	2176	2240	2112	2688	2880	2496	2240
X0Y18	1344	3200	1408	2752	1408	1664	1280	1600	1600	1920	1472
X0Y17	1152	3136	1088	2560	960	4544	896	1408	1216	1024	832
X0Y16	1984	4288	1856	3456	1728	2560	1408	2176	1984	1792	1216
X0Y15	2112		2112		2176		2048	2176	2048	1856	1728
X0Y14	2432	2944	2112	2048	1536	2240	1216	1920	1408	1088	832
X0Y13	960	6592	1024	5632	1024	2624	1024	1024	1024	960	960
X0Y12	1088	7360	1152	7040	1088	5824	704	1344	1344	1408	832
X0Y11	2496		2432		2560		2304	2176	2112	1984	1920
X0Y10	2488		4416		4288		4352	3776	3648	3648	3648
X0Y9	2688		3008		3072		3008	1164	1792	1728	1664
X0Y8	3200		3136		2944		3008	3456	3008	2624	2496
X0Y7	4096		4352		4544		4480	3136	3392	3648	3648
X0Y6	4096		4672		4992		5120	2624	3008	3072	3072
X0Y5	2368		2240		2176		2112	2944	3072	3008	3008
X0Y4	3008		3392		3456		3392	2304	2304	2048	1984
X0Y3	1664		1792		1920		1984	1408	1536	1472	1728
X0Y2	3712		3904		3968		4160	3456	3776	3776	3776
X0Y1	1728		2112		2112		2240	1472	1164	2112	1856
X0Y0	2496		2752		2880		2280	1600	1728	1984	1856

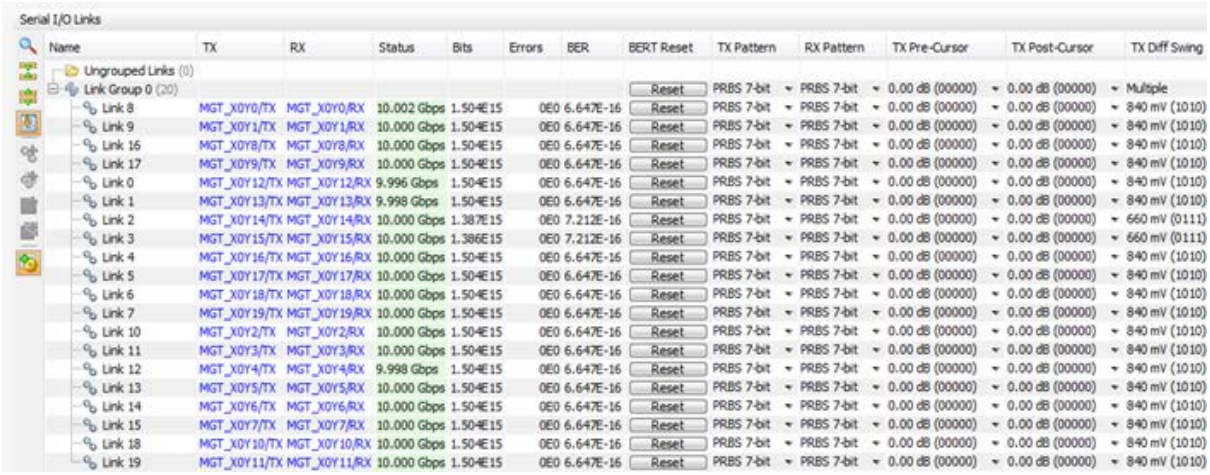

Figure 3.7 BER test 10 Gbs

3.3 Flash memory

Access to the bank 0 pins of the Xilinx Ultrascale FPGA is possible only through special primitives, e.g. ICAPE3. Figure 3.8 shows a schematic diagram of how bank 0 is accessed.

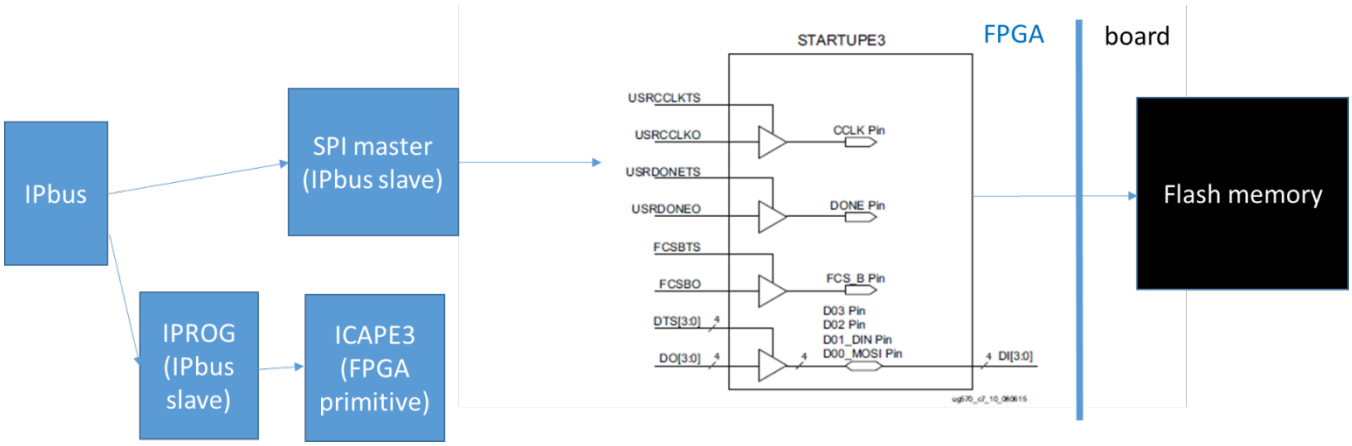

Figure 3.8 Flash memory tests

Flash memories are connected over SPI bus protocol. Several sectors (64kB) were tested (write/read/check) in both flash memories. The writing rate is 0.12 second/kB. When using a ‘counter pattern’ no errors were found but with a ‘random pattern’ writing errors were detected, i.e. the same data were read in repetitive reads. This is still being investigated. At present, we know that this is not a problem of the connection between the FPGA and the Flash Memory as a connection via JTAG works

3.4 DDR4 memory

DD4 memory tests are being performed at the time of writing this document.

3.5 Clocks/PLLs

The PLL Si5345 was successfully programmed via a USB Silicon Labs adapter using both I2C and SPI interfaces. The corresponding clock outputs were measured by scope and found to be consistent with programmed values. We have tested also access to Si5345 via I2C IPbus.

4. AFRB-709DMZ qualification for GBT system

The requirements for SFP+ modules for the GBT system are given in EDMS document 1146246 [8]. Measurements carried out by Csaba Soos (PH-ESE) using an Agilent JBERT digital attenuator. The results are summarised in Table 4.1 and meet the qualification for the GBT system.

Table 4.1 GBT qualification

Vindiff[mV]	Ref	200	400	800	1000
OMA[mW]	> 479	670	680	664	676
Eye Height[mV]	>400	492	490	494	484
Extinction Ratio [dB]	>3	5.31	5.43	5.36	5.51
Rise time[ps]	<40	36.21	37.77	37.66	38.65
Fall time[ps] (not used)	<40	44.85	47.37	43.99	46.75
Total jitter [ps]	<52	23.24	21,79	21.57	22.95
Deterministic jitter[ps]	<28	11.74	11.79	10.88	11.96

5. TTC-PON tests

TTC-PON firmware was developed and tested in several stages. In the first stage, evaluation boards KC705 (Kintex 7) and KCU105 (Kintex Ultrascale) were used. Later the evaluation boards were replaced by the prototype CTP/LTU boards where appropriate and available. The default interface for control and setting is IPbus. However, in the first stage of tests, the MicroBlaze interface [9] provided by TTC-PON developers was used. The KCU and ARIA 10 evaluation boards were used to represent a CRU in these tests.

The Trigger board, in the role of LTU, needs one ONU (Optical Network Unit) and several OLTs (Optical Line Terminal). The fast bank programming restriction limits the number of OLTs to eight which is enough for the ALICE system.

5.1 Tests with evaluation boards

Parallel with Trigger board testing and development, TTC-PON firmware was tested on the evaluation board KCU105. The firmware scheme is shown in Figure 5.1.

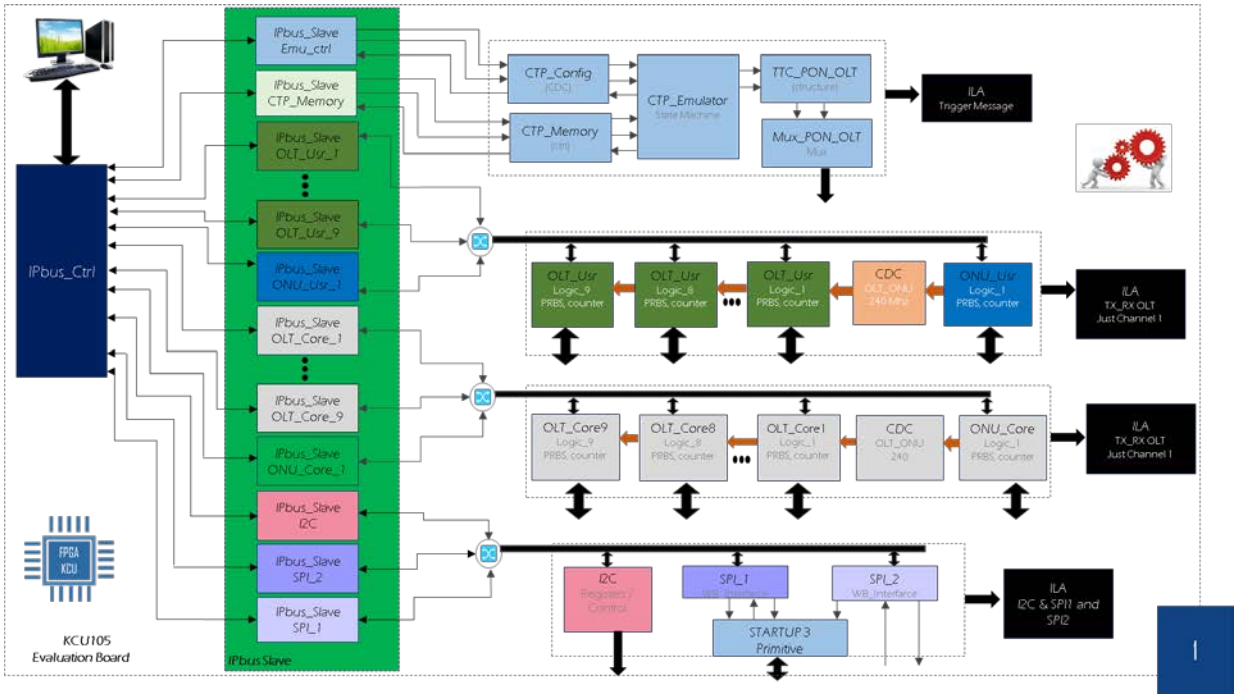

Figure 5.1 Firmware structure KCU 105

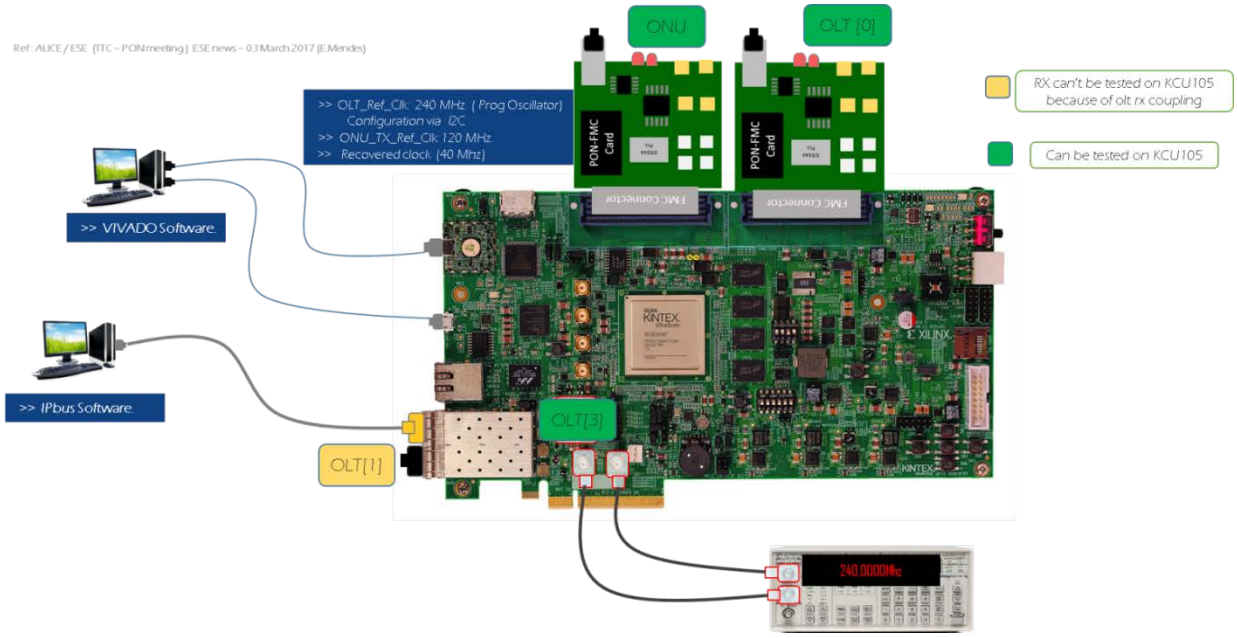

Figure 5.2 Evaluation board configuration for lab tests

Figure 5.2 shows the KCU105 evaluation board, with two PON-FMC cards, available for tests in the lab. The actual setup, used for bit error tests and latency measurements, is shown in Figure 5.3. It uses an OLT connected via a FMC-PON board and three ONUs – two on KC705 boards, controlled by MicroBlaze, and one on a KCU105 board connected via a FMC-PON board. The downstream BER from about 6 hours of tests (see Figure 5.4) shows

no errors, providing estimate of error rate lower than $3x10^{-15}$. The upstream BER measured for about 2 hours with no errors provides the estimate of error rate lower than $5x10^{-12}$.

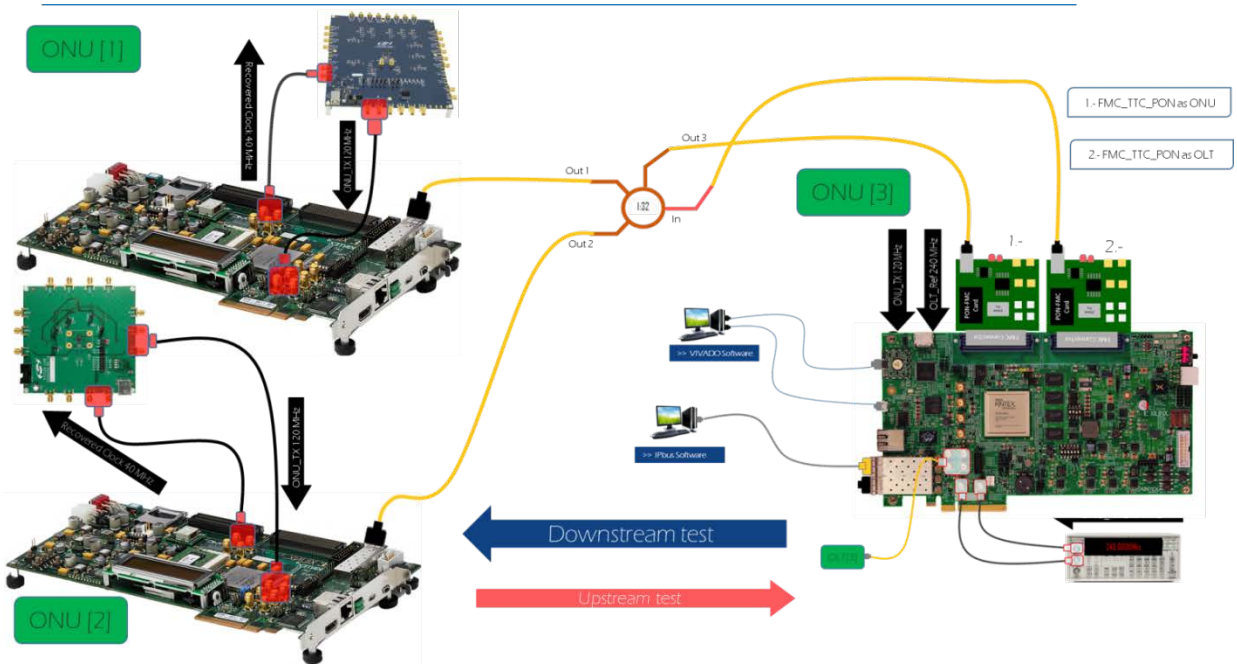

Figure 5.3 Test set up with valuation boards

```
ONU1 BERT latch...
ONU1 bits: 3331459424 36215 errs: 0 0 errs/bits: 0.000e+00
ONU2 BERT latch...
ONU2 bits: 2963755968 36216 errs: 0 0 errs/bits: 0.000e+00
ONU5 BERT latch...
ONU5 bits: 2910575872 36217 errs: 0 0 errs/bits: 0.000e+00
>
```

Figure 5.4 Downstream Bit error rate for setup in Figure 5.3

Latency was measured using the same setup, with measured points as indicated in Figure 5.5. The screenshot of the signals is shown in Figure 5.6. The results are a latency of 116 ns for the KC705 boards, i.e. ONU[1], ONU[2] and 100 ns for the KCU105 board, i.e. ONU[3] The difference is caused by different FPGAs and firmware versions.

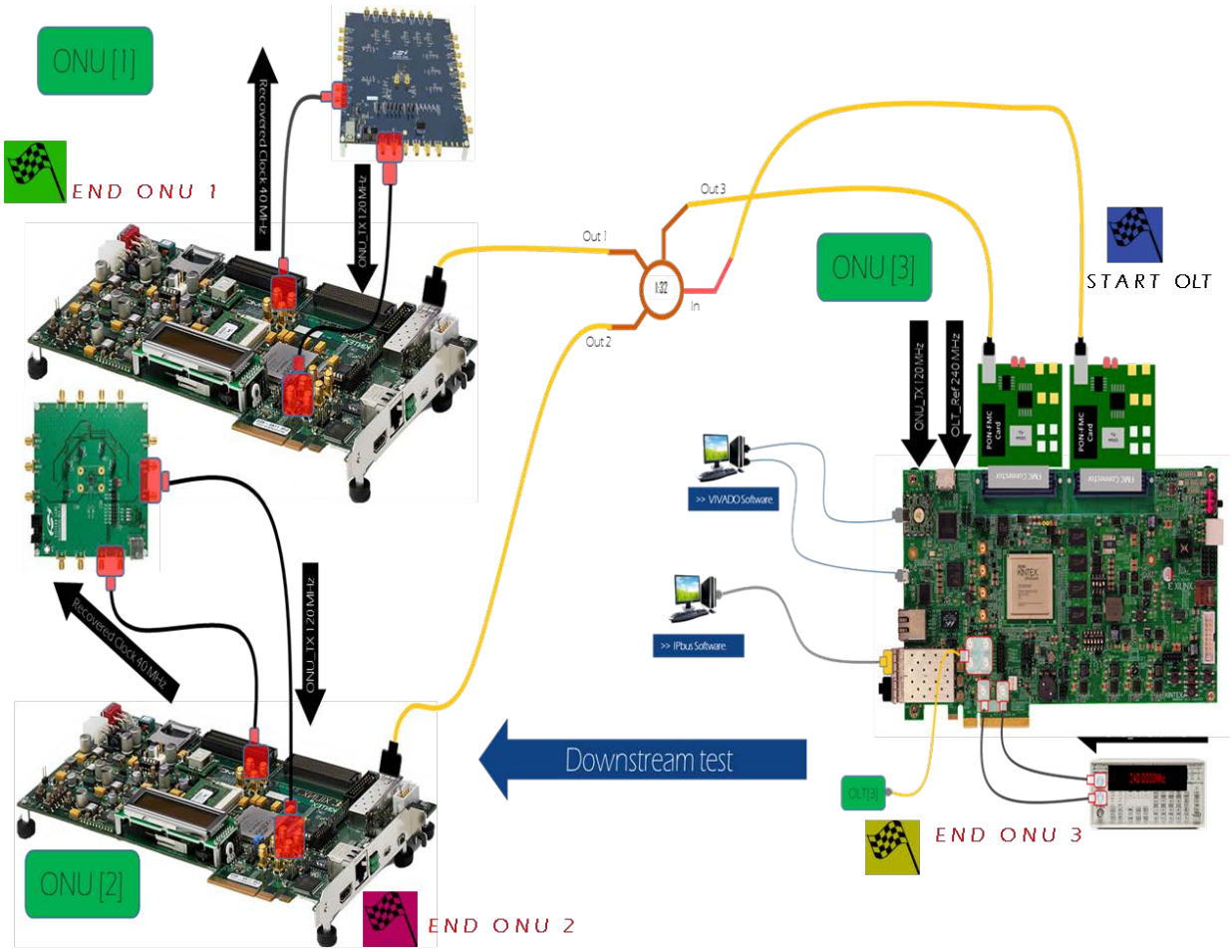

Figure 5.5 Latency measurement

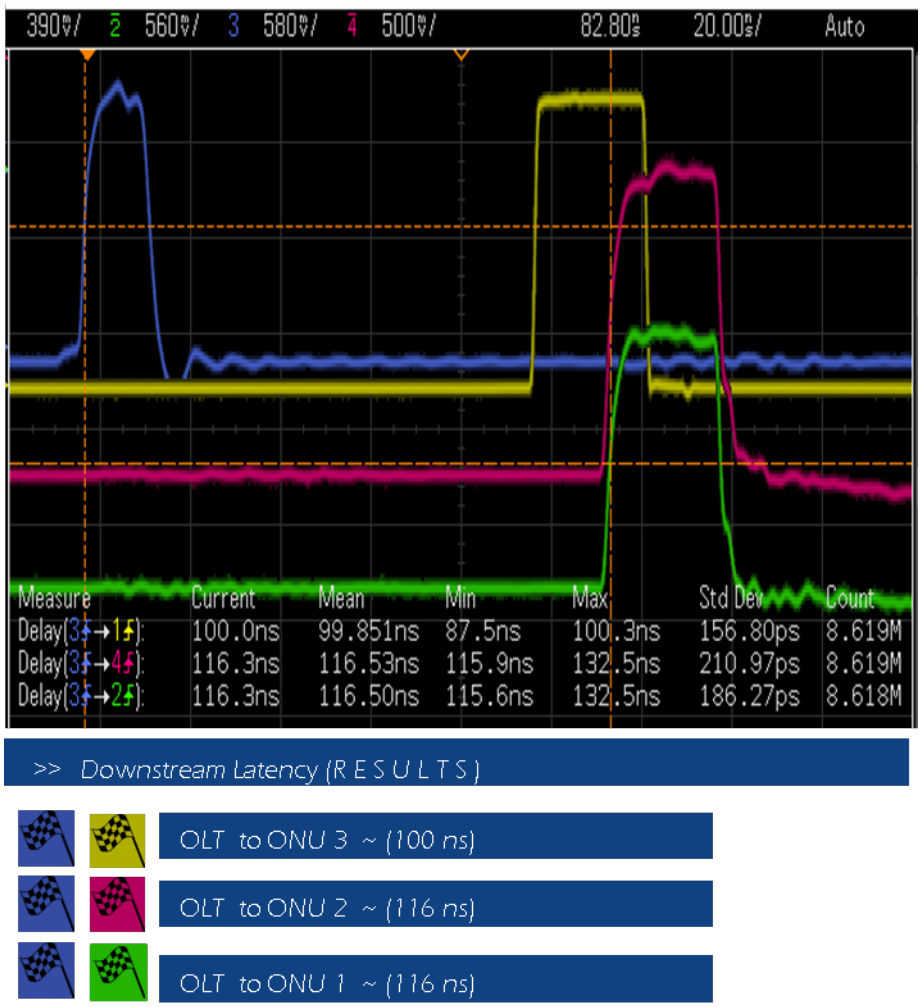

Figure 5.6 Latency measurement results.

5.2 Tests with the ALICE CTP/LTU boards

The block scheme of the firmware is shown in Figure 5.7; it contains:

- 25 IP bus slaves
- 9 OLTs
- 1 ONU
- 2 SPI ctrl
- 1 I2C ctrl
- The CTP emulator
- 8 ILAs (Logical analysers)

The test setup is shown in Figure 5.8 and allows testing of the full chain of CTP-LTU-CRU.

The BER test carried out under the setup shown in Figure 5.8, with Pseudorandom Bit Stream with 7 bits (PRBS7) at LTU and a KCU105 board acting as a CRU, gave no errors after 2.6 hours of testing. This corresponds to a BER of less than 1 in 2×10^{13}.

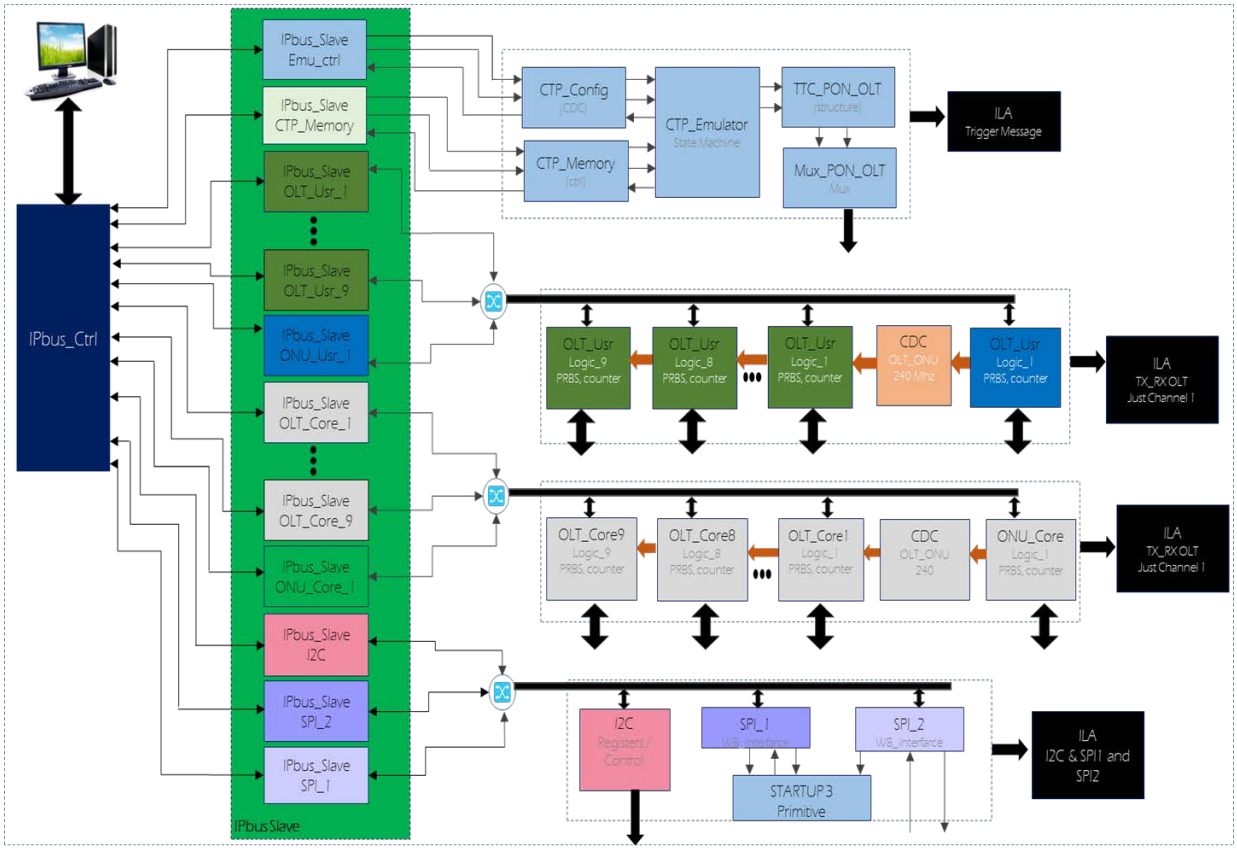

Figure 5.7 Firmware version V1 for trigger board

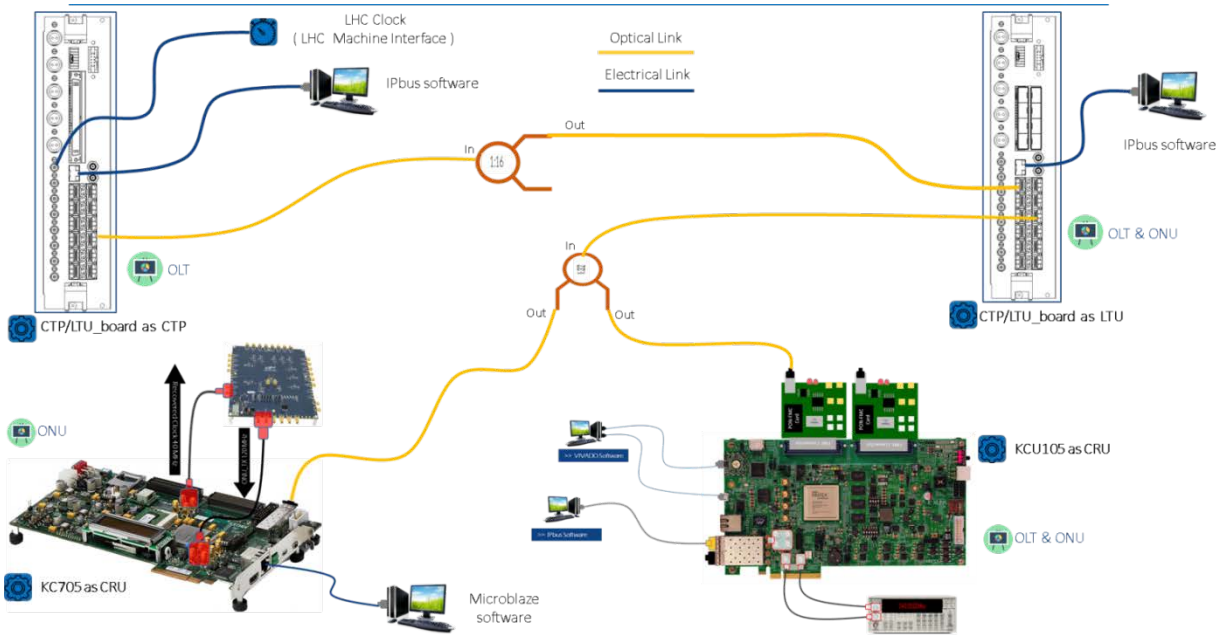

Figure 5.8 LAB test up

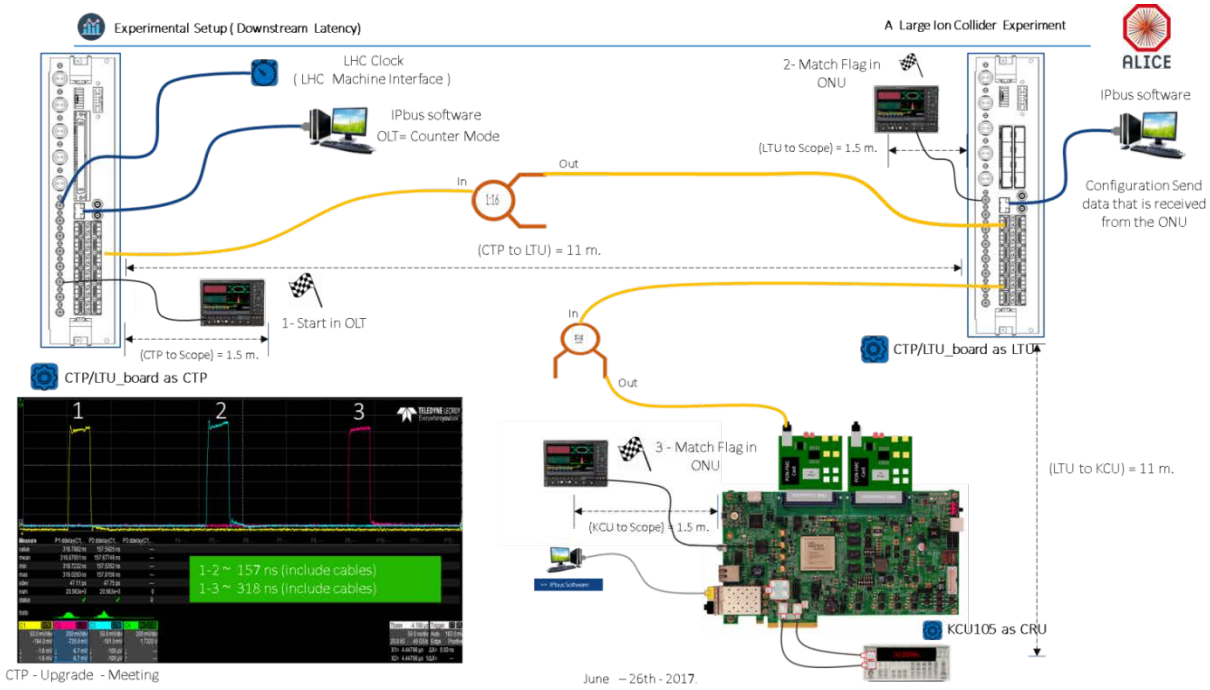

Figure 5.9 Latency with trigger board in CTP LAB setup

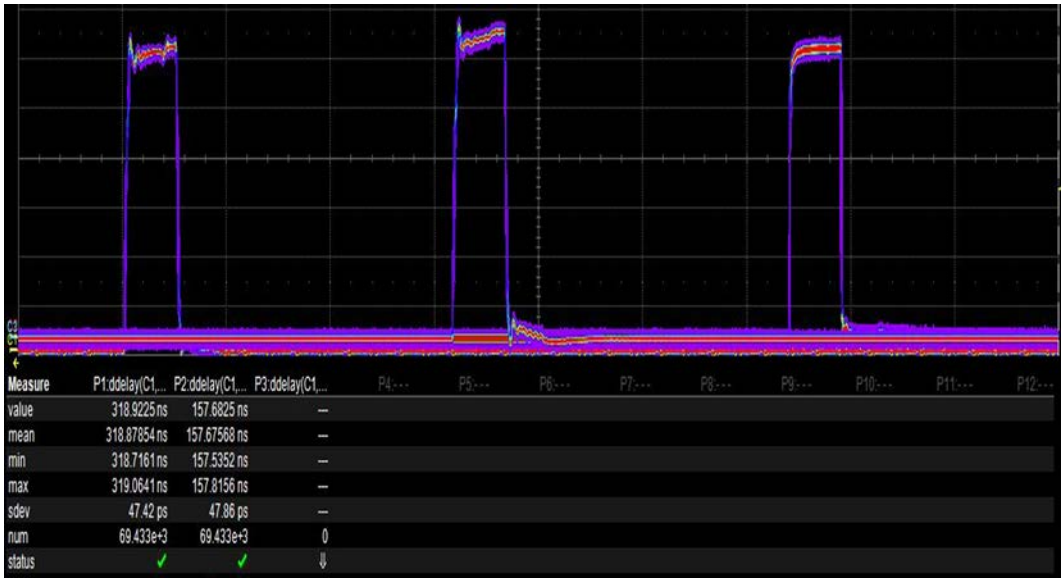

Figure 5.10 Latency after resets

The latency between the OLT TX match flag in the CTP board and the ONU RX match flag in the LTU is measured with the same setup (see Figure 5.9) leading to a latency of 157 ns. Latency of 102 ns is estimated after subtracting 55 ns for the cable length, consistent with the evaluation board measurements. The latency between the OLT TX match flag in the CTP board and the ONU RX match flag in the KCU105 board is 318 ns. Subtracting 2 x 55 ns it gives a latency of 208 ns, estimating the LTU processing time to be 106 ns. The stability of the latency after an OLT reset is demonstrated in Figure 5.10. It shows the superposition of about one hundred latency measurements, i.e. scope in persistent mode, with no indication of latency change.

5.3 Tests with ALICE CTP/LTU and CRU boards

The full chain of CTP-LTU- CRU was tested and the setup is shown in Figure 5.11. The latency measurement defined as the time between TX match flag at CTP and RX match flag at GBTX on Versatile Link Demo Board (VLDB) was performed. Measured latency was 590ns including cables, see Figure 5.12. Subtracting cables (2×5+11*5 ns×2) and CTP/LTU processing 105 ns leaves 365 ns for CRU and VLDB processing. The latency does not change after resetting OLT at CTP board (~10 times).

Jitter measurements were performed with WaveMaster816Zi-B oscilloscope [11]. The results are shown in Figure 5.13. Line 1 corresponds to LTU clock and Line 2 corresponds to GBT clock of VLDB. The random jitter (Ri in Figure 5.13) of 9.5 ps was measured at GBT, consistent with the TTC-PON measurement of 9 ns in [12]. More jitter measurements and discussion with TTC-PON team is planned.

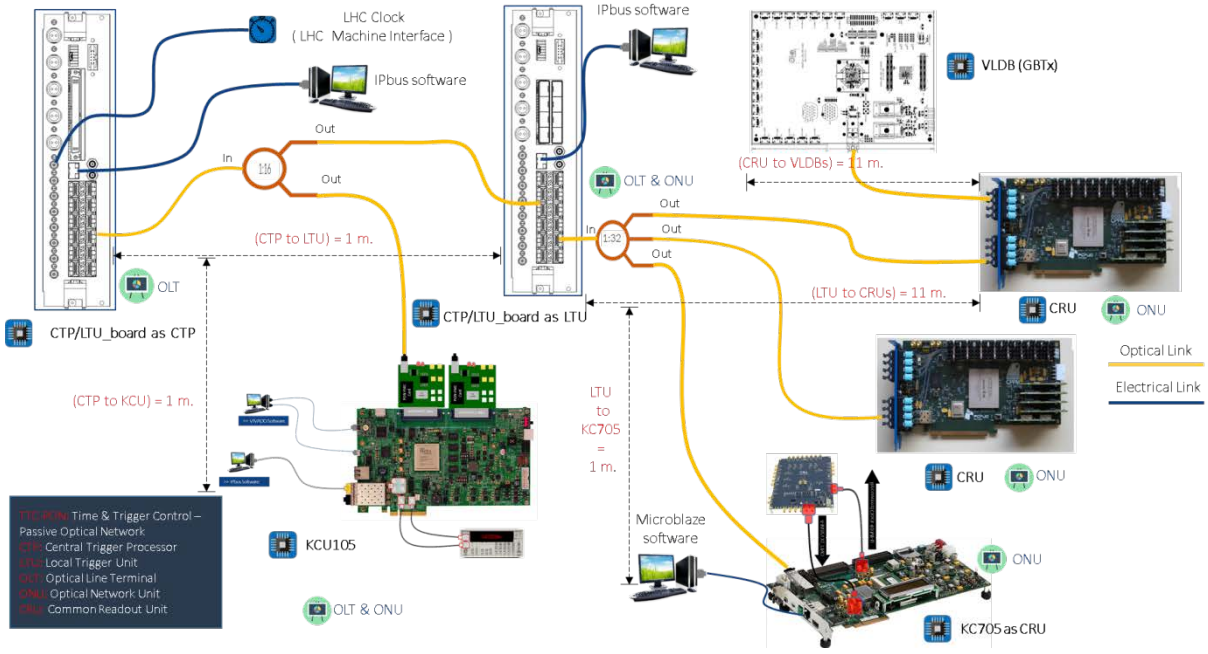

Figure 5.11 CTP-LTU-CRU setup

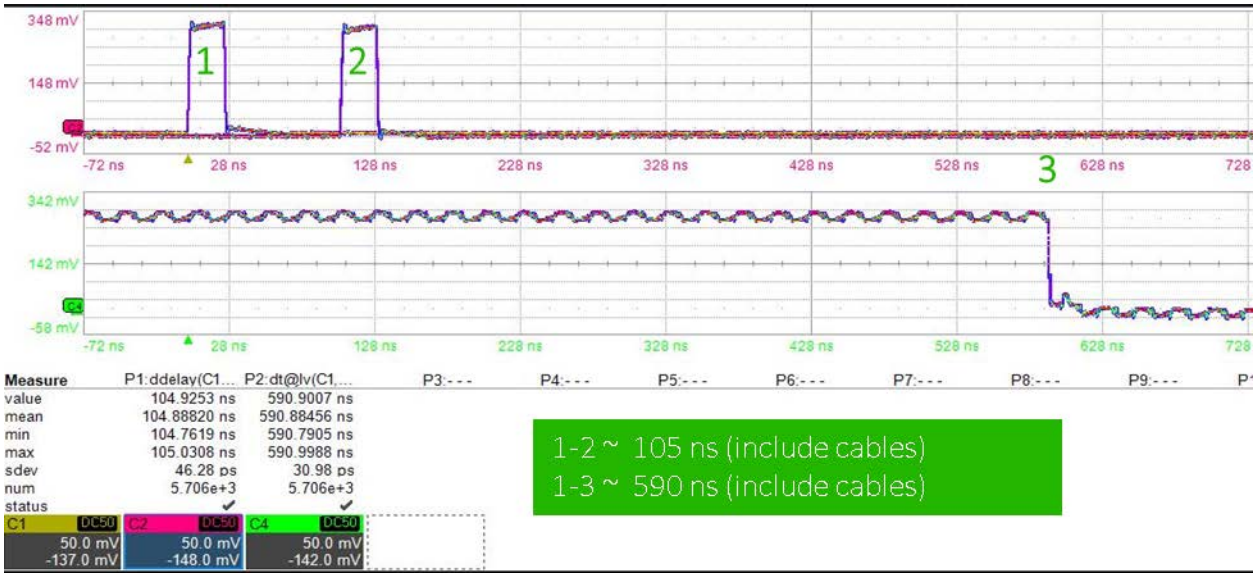

Figure 5.12 Downstream latency measurement CTP-LTU-CRU-VLDB

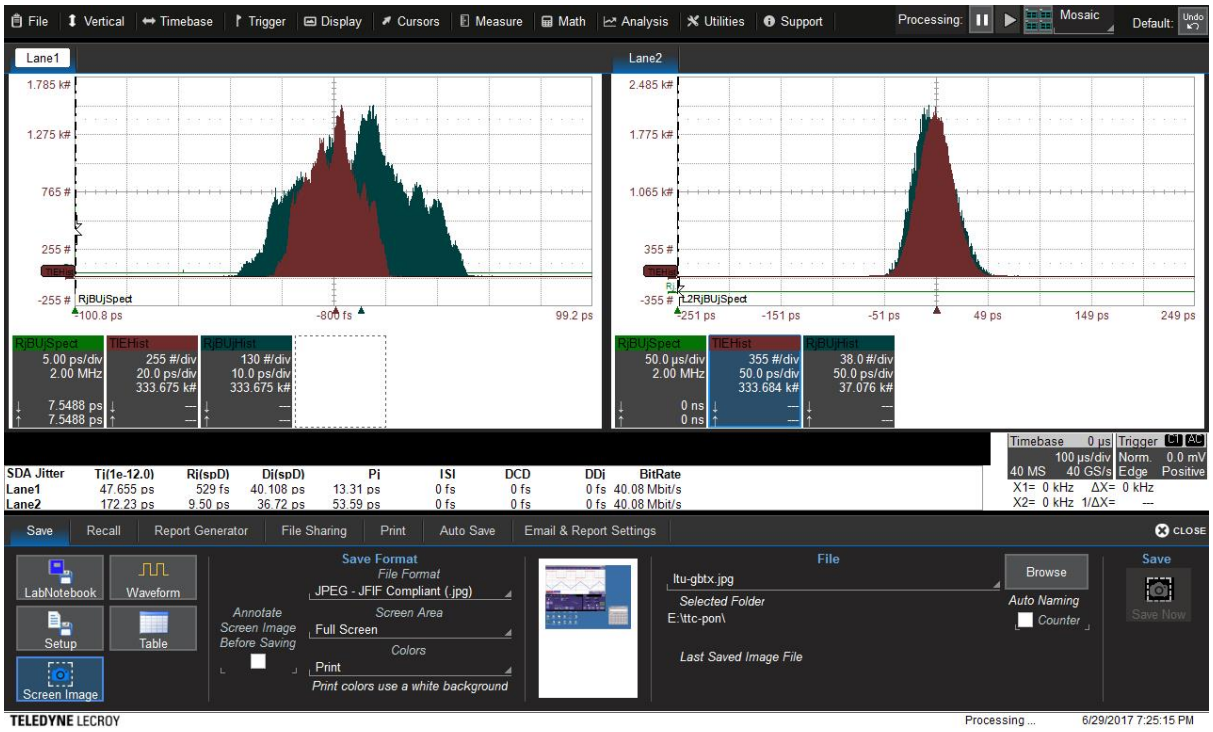

Figure 5.13 Jitter measurement

6. LVDS FMC card

The special FMC card with 70 LVDS inputs/outputs (see Figure 6.1) was designed by Jozef Špalek in Kosice. Generally, it can serve as an LVDS FANIN/FANOUT. It uses SAMTEC connector, see Figure 6.2. Specifically it will accommodate the CTP trigger inputs (and LVDS outputs). The PCB design of the card, using 8 layers, is now complete.

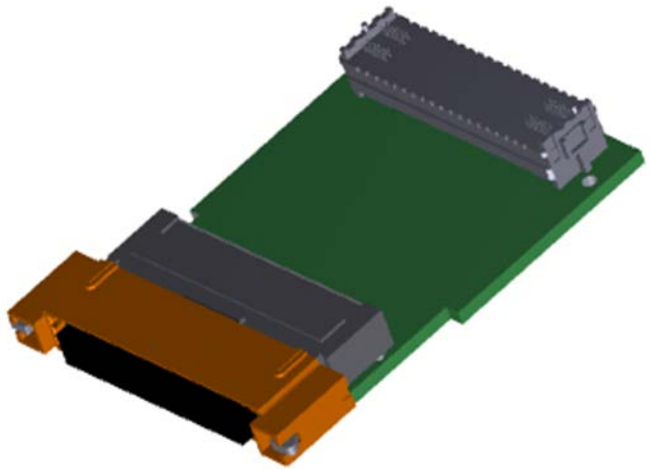

Figure 6.1 FMC LVDS card

The SEAC connector used on this card is from SAMTEC and is shown on Figure 9.2.

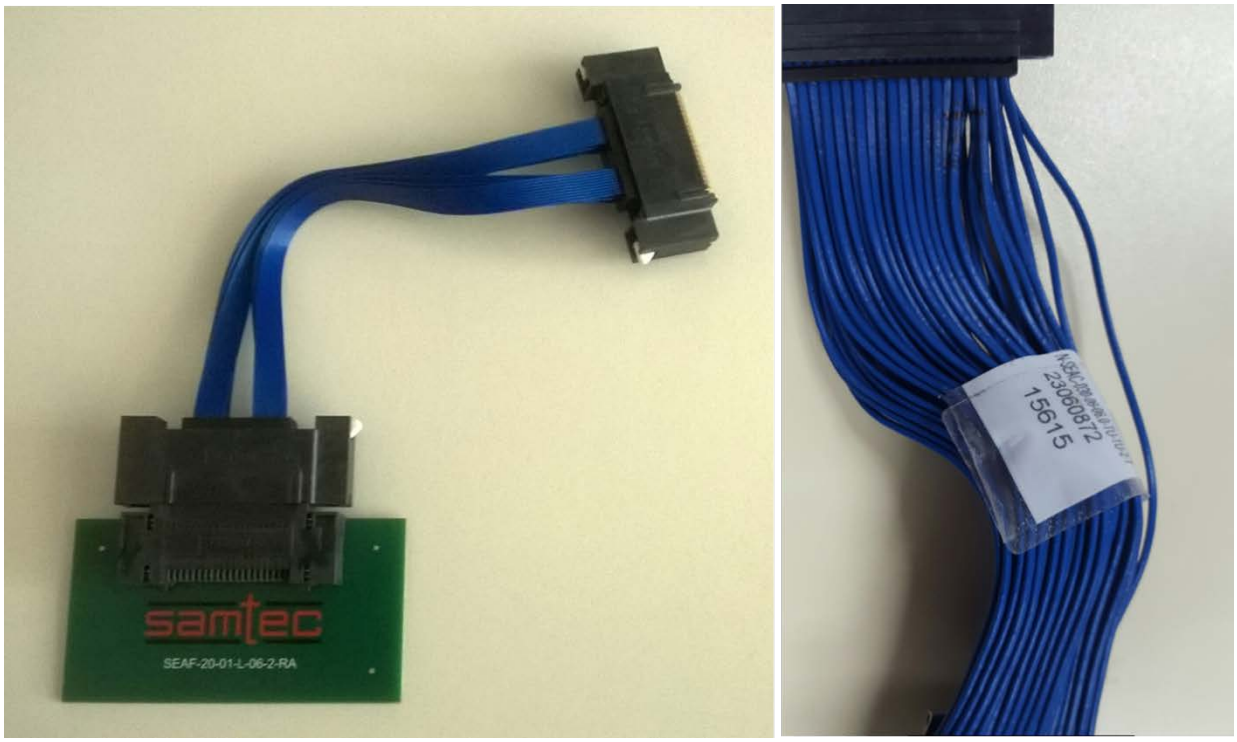

Figure 6.2 SAMTEC LVDS connector

7. LTU in box

There is an option to install the LTU in an ELMA box (see Figure 7.1 and 7.2) with internal power supplies and cooling. This will enable the LTU to be used without the need for a VME crate in the lab.

Figure 7.1 Elma box

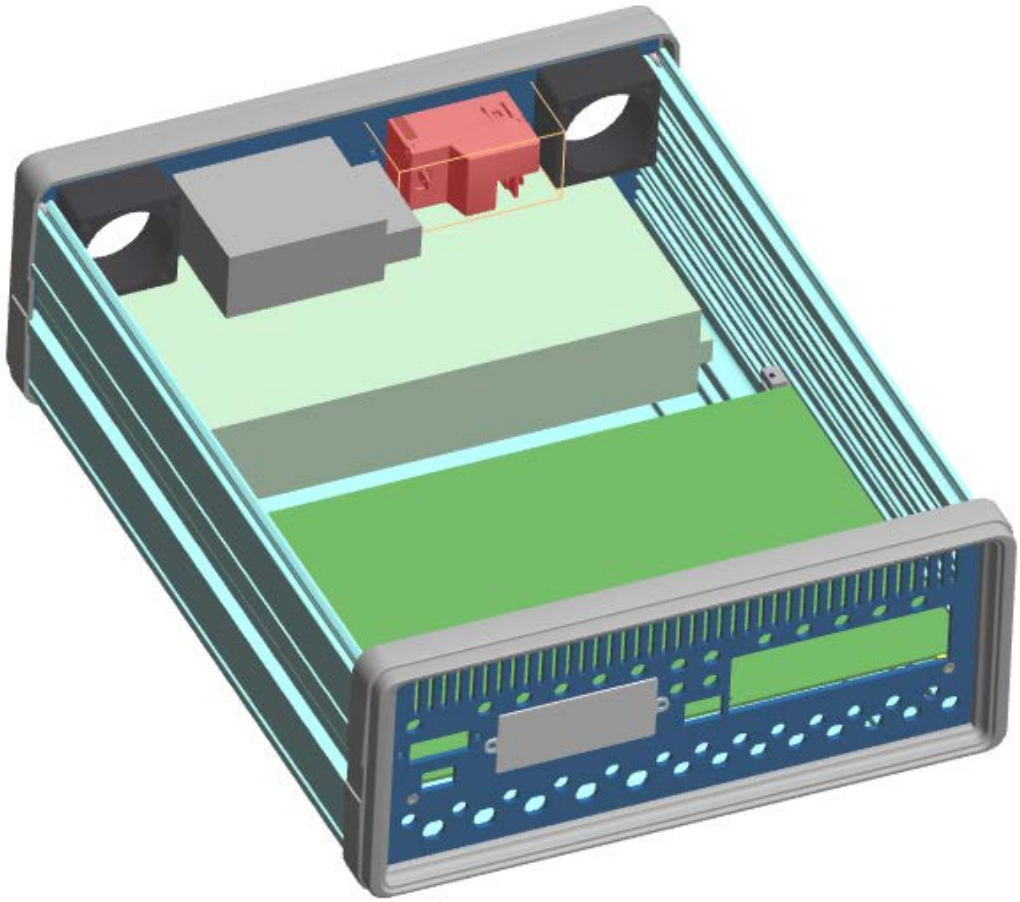

Figure 7.2 ELMA box design

8. Software for Control and Monitoring

Monitoring and control of the CTP and LTU boards will be via the IP Bus protocol. A LTU GUI will be written using the IPbus library allowing its interactive control in standalone mode. The LTU GUI will be written for the Linux operating system in C++ and python.

The main functionality provided by the CTP software will be:

- CTP configuration and control,
- CTP monitoring.

The main functionality provided by the LTU GUI will be:

- the LTU configuration and control,
- CTP emulator programming and control (setting the trigger types and rate),
- BUSY monitoring and trigger signal counting

8.1 IP bus Software Suite

The ALICE trigger system uses IP bus for control and monitoring. The CMS Level-1 Trigger team's firmware and software is used [10]. It provides the Hardware Access Library (uHAL)

for IPbus, the so called IPbus Software Suite. It is based on C++ and also includes Python-bindings.

8.2 Test software

The test software consists of two parts, one focused on CTP/LTU components and the other one on the TTC-PON protocol/connection tests.

The CTP/LTU software allows the control and testing of components on the CTP/LTU board. The components are connected to several SPI or I2C buses driven from the onboard FPGA, which allows for the communication with them over an IPbus interface. CTP/LTU software communicates with the components on the CTP/LTU over two APIs (SPI and I2C) built on top of the IPbus software suite.

The TTC-PON software is based on python code, written by the TTC-PON team, for basic tests with a MicroBlaze setup in the CERN-TTC-PON lab. This software was extended, using IPbus connections for control of TTC-PON firmware on boards hosting KC/KCU FPGAs.

Three different boards, interconnected by TTC-PON fibres and splitters,
can be controlled:

- KC705 controlled over MicroBlaze (ONU only),
- KCU105 with TTC-PON FMC controlled over IPbus,
- CTP/LTU controlled over IPbus.

Two command line interfaces allow the control of these mixed setups:

- `ublaze` -interactive control,
- `erates` -for long time measurements, writing TTC-PON counts/errors into .csv file.

8.2.1 SPI API

This API is written as a python class SPIcore. The constructor requires a pointer to an IPbus board class instance and SPI IPbus slave name. SPIcore provides two basic methods:

- `addDevice(device)` - has to be called for a connected device (current implementation allows only 1 device/SPI bus)
- `stran(bytes)` - max. 16 bytes can be sent/received in 1 transition

8.2.2 I2C API

This API is written as a python class I2Ccore. The constructor requires a pointer to a IPbus board class instance and I2C IPBUS slave name. Basic methods provided by I2Ccore:

- `addDevice(device)` - has to be called for each connected device,
- `i2cw(addr, byte)` - writing 1 byte to I2C address addr,
- `i2cwm(addr, memloc, bytes)` - writing bytes to a memory location memloc in I2C-connected memory at I2C address addr,

- `i2cr(self, addr, length)` - read length bytes from I2C address addr,
- `i2crm(self,addr,memloc, length)` - read length bytes from I2C-connected memory from memory location memloc

The software for I2C devices is working well. The following devices use I2C:

- EEPROM on FMC S-18,
- PLL Si5345 (W/R all registers),
- All types of SFP (AFBR 709DMZ, OLT, ONU),
- TC74 – temperature sensor,
- SYS_MON (internal Xilinx monitoring of temperature and voltages).

All devices (except SYS_MON) were accessed successfully as needed. SYS_MON was tested via JTAG and IPbus will be developed later.

8.2.3 TTC-PON API

The TTC-PON API is created by two classes: OltCore and OnuCore.
When the classes are instantiated, the corresponding connection (MicroBlaze or IPbus) is opened. Both classes provide basic methods allowing read/write to core/user registers of the corresponding TTC-PON firmware in the FPGA. Advanced methods allow full/light TTC-PON calibration and downstream/upstream tests of TTC-PON connections. They are used for ONU control and multi OLT control.

8.3 Board control (aboard/qtboard)

Two general board browsers are used. The first one, so called *aboard*, is written in python and the interface is in command line. Other one, called *qtboard*, is C++ based using qt graphic tools for the user interface.

Table 9.1 Summary of trigger milestones

Date	LTU Milestone	Comments
Sept 2015	LTU pre-prototype delivered to test concepts and enable FW & SW development.	Delivered end of March 2015
Dec 2015	LTU specifications finished	Finished subject to Design Review
Jan 2016	CTP and LTU Design Review	Finished but modified design required.
March 2016	CTP revised specifications completed	Finished subject to 2nd Design Review
May 2016	**Second CTP design Review**	Finished with minor modifications May 2016
July 2016	Schematic capture of Trigger board	Completed July 2016 (after minor mods from EDR)
July 2016	CTP electronics design review (EDR)	Completed June 2016
Nov 2016	PCB layout complete (RAL)	Completed Nov 2016
March 2016	Board prototypes complete	Delivered to CERN early March 2017
July 2017	Testing of prototype boards, including full CTP-LTU-CRU chain complete	Complete subject to PPR
July 2017	**Trigger board production readiness review (PPR)**	
Aug 2017	Minor modifications to PCB layout complete ready for manufacture	
Nov 2017	**Phase I trigger boards production completed (22 boards)**	
Dec 2017	Initial tests of Phase I trigger boards complete	Basic powering and I/O tests etc.
March 2018	Basic LTU firmware complete	
March 2018	First batch of LTUs ready for sub-detectors	
July 2018	Extensive testing, including full system CTP + 14 LTUs, completed	
July 2018	**Phase II** trigger boards production starting (28 boards)	
Oct 2018	**Phase II trigger boards production completed (28 boards)**	
May 2019	**CTP and LTU firmware complete**	
June 2019	**Integration tests of trigger system with DAQ (in CERN lab) completed**	
Sept 2019	Installation and testing of trigger system in ALICE cavern completed	
Oct 2019	Commissioning of trigger system with all ALICE sub-detectors and systems starts	

9. CTP and LTU Milestones

The milestones for the trigger project are summarised in Table 9.1 below with the key milestones written in bold type. It is planned to produce the trigger boards in two phases, with 22 boards being manufactured in phase I and the remaining 28 boards in phase II. Phase I will provide enough boards to satisfy the needs of sub-detector groups, who need a LTU urgently, and allow us to carry out full CTP system tests consisting of one CTP plus fourteen LTUs.

9.1 Trigger Project Gantt Chart

The Gantt Chart of the trigger project is shown in Figure 9.1 below. The critical path is shown in red and is governed by firmware development.

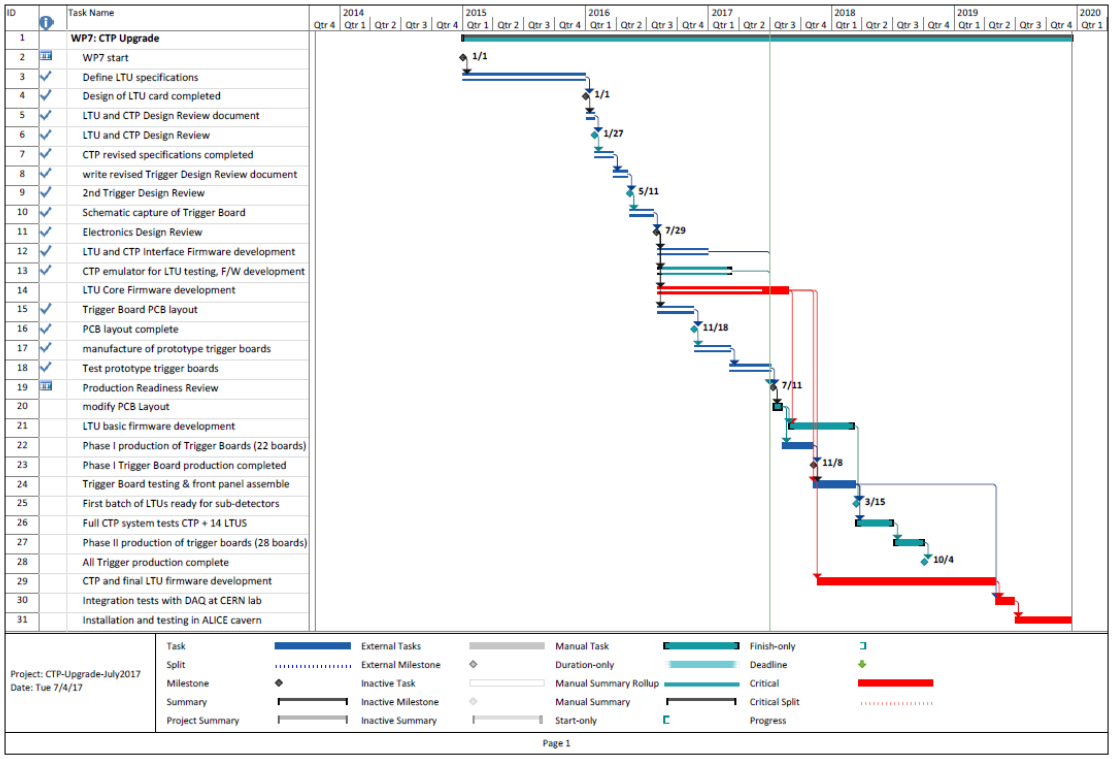

Figure 9.1 Gantt chart

10. References

[1] D. Evans, A. Jusko, M. Krivda, R. Lietava, L.A. Perez Moreno, O. Villalobos Baillie: Trigger System Design Review May 2016, https://twiki.cern.ch/twiki/bin/viewfile/ALICE/EngineeringDesignReview(June2016)?filename=CTPLTU17.pdf;rev=10

[2] B. G. Taylor, Timing distribution at the LHC, Proceedings of the 8thWorkshop on Electronics for LHC Experiments, Colmar France (2002), CERN-2002-003, http://cdsweb.cern.ch/record/592719

[3] S. Baron and A. Monera Martínez, Status of the TTC upgrade, Proceedings of the 12th workshop on electronics for LHC and future experiments, Valencia Spain (2006), CERN-2007-001, http://cdsweb.cern.ch/record/1027471

[4] S. Baron et al, TTC PON, https://indico.cern.ch/event/465344/attachments/1281633/1904473/TTC-PON_ESE_seminar_31_05_16_.pdf

[5] GBTX project: GBTX manual, https://espace.cern.ch/GBT-Project/GBTX/Manuals/gbtxManual.pdf

[6] Vivado software: https://www.xilinx.com/products/design-tools/vivado.html

[7] Digilent: JTAG-SMT Programming Module for Xikinxs FPGAs, https://reference.digilentinc.com/_media/jtag_smt2:jtag-smt2_rm.pdf

[8] **VERSATILE LINK BACK END COMPONENTS SFP+ TRANSCEIVERS,** https://espace.cern.ch/project-versatile-link/public/default.aspx

[9] MicroBlaze Processor Reference Guide, https://www.xilinx.com/support/documentation/sw_manuals/xilinx2016_3/ug984-vivado-microblaze-ref.pdf

[10] Code Archive for the Trigger Upgrades (CACTUS), https://svnweb.cern.ch/trac/cactus/wiki

[11] Teledyn Lecroy scope: http://teledynelecroy.com/oscilloscope/oscilloscopemodel.aspx?modelid=9151

[12] TTC_PON team: TTC-PON jitter, https://indico.cern.ch/event/614031/contributions/2475629/attachments/1422134/2179861/ALICE_ESE_PON_meeting_March_2017_Jitter.pdf