ALICE-EDR-XXX

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Production Readiness Review of the CTP/LTU

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Edited by A. Kluge

Table of contents

1. Review panel

External Reviewers: S. Haas, C. Soos
Internal Reviewers present in person: G. Aglieri, G. Cataldo, F. Costa, J. Imrek, A. Kluge
Internal Reviewers present via video: T. Alt, P. Dupieux, T. Kiss, A. Tello, R. Tieulent, W. Trzaska

2. Introduction

The aim of the review is to evaluate the progress on the design and performance of the CTP/LTU prototypes and their behavior in the ALICE system with respect to the ALICE read-out specifications and whether the design is appropriate for launching the pre-series and production.

Review material

https://indico.cern.ch/event/646273/

3. Review summary and preconditions before design implementation

Introduction

The review panel would like to thank the CTP team for their efficient and clear presentations and the timely provision of the review material. The reviewers would like to congratulate the CTP team to the progress made so far.
The new common trigger board will be used as Central Trigger Processor (CTP) or Local Trigger Unit (LTU), depending on the hardware and firmware configuration. The board has been designed to support higher trigger rates, different trigger distribution schemes (PON or GBT) as well as the handling of throttle/busy signals coming from the CRUs/detectors.

Technical summary

The first two prototypes of this large and complex board are available since March and the tests carried out so far have shown no major problems. The high-speed links of the on-board SPF+ cages show good performance, however, some of the high-speed links on the FMC interface suffer from eye closure at 10 Gb/s. The CTP team used a commercial FMC breakout board, and they claim that the issue could be related to the performance of this board. This must be investigated. So far, only simple loop-back tests have been carried out with the optical transceivers. It would be useful to run bit error rate tests (BERT) using the SFPs on the trigger board as receivers to measure receiver sensitivity and compare it with the expected values (i.e. datasheet specs). This would allow them to calculate the optical link budget. On the transmitter side, they should make a similar test using the high-power optical transmitter and the receiver which is going to be used in the final system. The performance of the power delivery network (PDN) should be checked before the final modifications are made on the board layout. They should check the power plane impedance and verify if there is enough decoupling. They should measure the voltage ripple on critical planes using an oscilloscope (rather than relying on values obtained from XADC). The measurements should be carried out with a functional firmware, possibly including and operating with the DDR4 interface. The temperature of the transceivers when more than one PON OLT are installed in the stacked SFP cages should be checked, since the power consumption of the PON transmitters is quite high and the cooling is likely to be not very good in the chosen configuration. In addition, it is recommended to cross-check the interfaces (e.g. number and type of transceivers, number of boards, data formats, etc.) with each of the sub-detectors again to make sure nothing has changed. A table summarizing this data should be prepared.

Schedule and manpower

The presented production plan seems to be rather tight but it is safe to produce the boards in two batches as eventual problems could be still fixed after the first batch. Additional manpower should be identified to ensure smooth firmware development and support during commissioning.

Decision

The CTP team is encouraged to go ahead with the pre-production after the technical details as described in the sections “technical summary” and “detailed review comments” have been positively verified and documented. The results should be presented in a follow-up meeting in autumn 2017.

The review panel appreciates the approach of producing first a pre-series before the final series is launched, as this allows a further verification step.

4. Detailed review comments

1. Were there Power Design Rules formally included at design time for the Power Distribution Network? Additional dedicated tests, including stress tests on PDN with dedicated firmware are recommended.

2. Suggestion to measure the distribution of optical power at the outputs of the transmitter modules and the sensitivity of the input optical channels (putting an attenuator in the optical link and find minimum power for operation with acceptable BER).

3. What does it mean DDR4 tests ongoing? The communication should be tested before production.

4. What are the specifications of the LVDS inputs in the CTP configuration (FMC LVDS card)? Verify the common signal level and the uncontrolled connections between racks located far away (unwanted 'ground' currents).

5. Define and test the return paths for LVDS inputs of the FMC mezzanine for the CTP (trigger inputs)?

6. The LVDS repeater chip on the Mezzanine does not seem to be supporting wide common level ranges, at first glance. Should be checked and analysed.

7. Is it possibly to validate the constant latency correctly working (e.g. skewing clocks)?

8. Clear agreements with the design office (layout) need to be made in order to avoid again long delays during layout and production.

9. The complexity of the boards might result in a potential long duration of boards testing and commissioning. Is there a specific firmware and test procedure for all the interfaces and features?

10. What are the updated estimates of resource utilisation in the FPGA for the CTP and LTU?

11. What are the plans for integration tests with the detectors, and in particular for those that have special requirements (GBT links)?

12. Galvanic insulation between LTU and detectors using LVDS signals: What is the value of the common mode the LVDS drivers can operate? What is the grounding scheme between CTP racks and ALICE? Were measurements of parasitic currents between main frame and trigger racks

done? It was discussed that the L0 fan-out can operate in a floating ground configuration (replacement of input resistors with capacitors towards ground.) Will these modules still be maintained or does the HMPID have to add the feature of the floating ground on their LM/Busy modules?