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Production Readiness Review of the CTP/LTU

CTP response

September , 2017

Edited by R. Lietava

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1. Review panel

External Reviewers: S. Haas, C. Soos
Internal Reviewers present in person: G. Aglieri, G. Cataldo, F. Costa, J. Imrek, A. Kluge
Internal Reviewers present via video: T. Alt, P. Dupieux, T. Kiss, A. Tello, R. Tieulent, W. Trzaska

2. Introduction

The aim of the review is to evaluate the progress on the design and performance of the CTP/LTU prototypes and their behavior in the ALICE system with respect to the ALICE read-out specifications and whether the design is appropriate for launching the pre-series and production.

Review material

https://indico.cern.ch/event/646273/

3. Review summary and preconditions before design implementation

Introduction

The review panel would like to thank the CTP team for their efficient and clear presentations and the timely provision of the review material. The reviewers would like to congratulate the CTP team to the progress made so far.
The new common trigger board will be used as Central Trigger Processor (CTP) or Local Trigger Unit (LTU), depending on the hardware and firmware configuration. The board has been designed to support higher trigger rates, different trigger distribution schemes (PON or GBT) as well as the handling of throttle/busy signals coming from the CRUs/detectors.

Technical summary

The first two prototypes of this large and complex board are available since March and the tests carried out so far have shown no major problems.

The high-speed links of the on-board SPF+ cages show good performance, however, some of the high-speed links on the FMC interface suffer from eye closure at 10 Gb/s. The CTP team used a commercial FMC breakout board, and they claim that the issue could be related to the performance of this board**.**

CTP comment: The problem is being discussed with company. So far it was identified that some of high speed links on FMC card does not have 100 ohm characteristic impedance.

So far, only simple loop-back tests have been carried out with the optical transceivers. It would be useful to run bit error rate tests (BERT) using the SFPs on the trigger board as receivers to measure receiver sensitivity and compare it with the expected values (i.e. datasheet specs). This would allow them to calculate the optical link budget. On the transmitter side, they should make a similar test using the high-power optical transmitter and the receiver which is going to be used in the final system.

CTP comment: See answer to questions 2.

The performance of the power delivery network (PDN) should be checked before the final modifications are made on the board layout. They should check the power plane impedance and verify if there is enough decoupling.

CTP comment: it would be done in coming weeks, certainly before final series production.

They should measure the voltage ripple on critical planes using an oscilloscope (rather than relying on values obtained from XADC). The

measurements should be carried out with a functional firmware, possibly including and operating with the DDR4 interface.

CTP comment: This will be done in coming weeks, certainly before final series production.

The temperature of the transceivers when more than one PON OLT are installed in the stacked SFP cages should be checked, since the power consumption of the PON transmitters is quite high and the cooling is likely to be not very good in the chosen configuration.

CTP comment: It will be done when the modules are available, certainly before final production.

In addition, it is recommended to cross-check the interfaces (e.g. number and type of transceivers, number of boards, data formats, etc.) with each of the sub-detectors again to make sure nothing has changed. A table summarizing this data should be prepared.

CTP comment: It will be checked again between pre-production and final production time.

Schedule and manpower

The presented production plan seems to be rather tight but it is safe to produce the boards in two batches as eventual problems could be still fixed after the first batch. Additional manpower should be identified to ensure smooth firmware development and support during commissioning.

Decision

The CTP team is encouraged to go ahead with the pre-production after the technical details as described in the sections “technical summary” and “detailed review comments” have been positively verified and documented. The results should be presented in a follow-up meeting in autumn 2017.
The review panel appreciates the approach of producing first a pre-series before the final series is launched, as this allows a further verification step.

4. Detailed review comments

1. Were there Power Design Rules formally included at design time for the Power Distribution Network? Additional dedicated tests, including stress tests on PDN with dedicated firmware are recommended.

The design relies on the best practice and specific guidelines from design engineers, e.g. notes on schematics or reference in datasheets.

In particular:

- Schematic references to datasheets followed, e.g. FPGA, DDR4, LMZ power modules – covering decoupling placement, mini-planes and vias.
- Short, wide tracks with larger vias were used on most power and ground nets where space permits, to reduce inductance. Multiple vias were used at high current junctions.
- Decoupling capacitors were placed close to POL, e.g. small value under FPGA, bulk capacitance on top side periphery. Guidelines followed wherever possible e.g.one capacitor per pin.
- Dedicated plane areas were used for all multi-pin power and ground nets.
- Local planes – e.g. LMZ parts were kept small around physical parts.
- Power supply circuits kept to the right and right lower quadrant of the board, away from sensitive signals.
- Multiple GND planes were used to reduce impedance and increase clean signal return-path options for sensitive signals. 10G signals were all referenced to these planes. Plane splits avoided where possible for sensitive signals.
- Some planes were extended to provide contiguous return path areas for routing. e.g. GND plane under DDR4 tracks.
- Wide planes were used where possible to points of load, reducing the effects of plane perforation.
- 45 degree corners were used on shapes to improve current flow.

The ripple on power rails to be checked with oscilloscope with DDR memories active and 'full' firmware loaded.

PDN simulation is to be done before phase II. The use of HyperLynx and Sigrity tools is being investigated.

2. Suggestion to measure the distribution of optical power at the outputs of the transmitter modules and the sensitivity of the input optical channels (putting an attenuator in the optical link and find minimum power for operation with acceptable BER).

There are 3 types of optical connections:

a) TTC-PON (CTP-LTU, LTU-CRU)

b) GBT (LTU-CRU for CTP readout)

c) GBT (LTU-FE with 1:16 optical splitting for ITS/MFT)

The optical power budget for TTC-PON connections was measured by TTC-PON CERN team:

https://indico.cern.ch/event/608587/contributions/2614195/attachments/1522347/2378845/TTC-PON_TWEPP2017_EMendes_13_09_17.pptx

To be published by the end of the year.

The GBT connection (b) was measured by C. Soos (see slide 61 in Marian's presentation at CTP PRR). The GBT connection to FE (c) will be measured by ITS/MFT teams – plan to test in November.

3. What does it mean DDR4 tests ongoing? The communication should be tested before production.

The electrical connection and timing verification with VIVADO hardware manager was successful.

The basic communication with DDR4 - write/read – was tested:

- write : 3Mbyte/sec
- read: 0.8 Mbyte/sec

The speeds were measured using the python IPbus interface. The test will be repeated with c++ interface.

Test of write-read-check with random data and address for full memory were done for both board memories. No problem is found.

4. What are the specifications of the LVDS inputs in the CTP configuration (FMC LVDS card)? Verify the common signal level and the uncontrolled connections between racks located far away (unwanted 'ground' currents).

- magnitude of input diff. voltage range 100 mV – 3.3V
- common mode input voltage range 50 mV - 3.25 V
- max. input current +-20 micro A
- capacitance 2.0 pF
- Max. diff. input threshold for HIGH - 100 mV
- Min. diff. input threshold for LOW – (-100 mV)

FMC CTP card expects common mode at 1.25 V (typical LVDS driver), so a ground difference should not be bigger than 1.15 V.

During LHC Run1 and Run2 we didn`t have a problem with grounding differences, but with an installation of new detectors during LS2 this can change. We will verify a

ground difference between CTP racks and detectors at next possible occasion. We will ask for help from Technical coordination of ALICE experiment.

5. Define and test the return paths for LVDS inputs of the FMC mezzanine for the CTP (trigger inputs)?

By default all return paths for LVDS inputs are going through LVDS cables i.e. all LVDS chips on FMC CTP card are connected to the same ground (shielding of LVDS cables). In case we need to disconnect the ground coming from a detector, we will do it at a patch panel located at top of rack C25 (CTP rack). Another option would be to isolate patch panel connectors optically or digitally from detector ground.

6. The LVDS repeater chip on the Mezzanine does not seem to be supporting wide common level ranges, at first glance. Should be checked and analysed.

The LVDS common mode specification as defined in point 4 supports range from 50 mV to 3.25 V.

7. Is it possibly to validate the constant latency correctly working (e.g. skewing clocks)?

The fixed latency was validated by regularly resetting the OLT and ONU modules in TTC-PON system. The relative phases of the clock at the CTP and the LTU boards are fixed by the optimal ONU-OLT timing requirement and cannot be changed independently, e.g. to satisfy FE timing requirements.

8. Clear agreements with the design office (layout) need to be made in order to avoid again long delays during layout and production.

During PCB layout, we kept in constant contact with Dan Becket from RAL in order to minimize delays. PCB layout was completed by the end of August. After this date tenders were send to four companies and JALTEK has been awarded the tender. A clear line of contact has been set-up with JALTEK in order to avoid any delays in production. University administration is now completed and the purchase order should have been sent out on September 22.

9. The complexity of the boards might result in a potential long duration of boards testing and commissioning. Is there a specific firmware and test procedure for all the interfaces and features?

The specific firmware – testlogic – was developed. It is accompanied by specific software which allows semi-automatic tests of all interfaces.

10. What are the updated estimates of resource utilisation in the FPGA for the CTP and LTU?

Below are estimates of resources for three board configurations – Standard LTU, LTU for ITS/MFT and CTP. The estimates are based on available firmware. In particular we have

a) The work in progress version of LTU software consisting of IPBus,CTP emulator, 1 ONU and 8 OLTs. The FPGA resources used are:
   - LUT 52195 (21.53% of LUTs)
   - LUT RAM 1312 (1.16 % of LUTs)
   - FlipFlop (FF) 83461 (17.2 %)
   - Block RAM 72 (12 %)
   - Global Buffer (BUFG) 26 (5.42 %)
   - Mixed Mode Clock Manager (MMCM) 5 (50 %)
   - PLL 2 (10 %)

b) The GBT firmware. The FPGA resources are:
   - LUT 1784 (0.7 %)
   - LUT RAM 2 (0.002 %)
   - FF 323 (0.07 %)
   - BRAM 5 (0.8%)

c) The run2 CTP LM board firmware consisting of DDL interface, VME interface, DDR3 interface and CTP logic. The FPGA resources used are:
   - LUT 92810 (38.3 %)
   - LUT 13735 RAM (12.2 %)
   - FF 127044 (26.2%)
   - BRAM 117 (19.5 %)
   - BUFG 13 (2.7 %)
   - MMCM 2 (20%)
   - PLL 3 (15%)

These numbers indicates that there is enough resources for the final run3 boards.
Firmware for standard LTU board would consists of IPbus, CTP emulator , ONU, 8xOLT and 1xGBT which would require (a+b) resources.
Firmware for ITS/FMT LTU LTU board would consist of IPbus, CTP emulator, 1xONU, 1xOLT and 12xGBT which would require less then (a+12xb) resources.
Firmware for CTP board would consist of IPbus, CTP Logic, 6xOLTand 5xGBT which would require less than (a+c+4xb) resources.

To be on the safe side, extra PCB, are to be produced which can be populated with more powerful FPGA allowing XCKU060 (default is XCKU040) , see EDR.

11. What are the plans for integration tests with the detectors, and in particular for those that have special requirements (GBT links)?

The integration tests have the following steps:

- Tests in detector labs with LTU.
- Tests at CERN (at P2 or in CTP/O2 lab). Detector has to pass a specified set of precisely defined tests to be allowed to join the full system.
- Tests of full system at P2 with detectors which pass above tests.

The special requirement detectors would follow the general scheme with support from CTP team.

12. Galvanic insulation between LTU and detectors using LVDS signals: What is the value of the common mode the LVDS drivers can operate? What is the grounding scheme between CTP racks and ALICE? Were measurements of parasitic currents between main frame and trigger racks done? It was discussed that the L0 fan-out can operate in a floating ground configuration (replacement of input resistors with capacitors towards ground.) Will these modules still be maintained or does the HMPID have to add the feature of the floating ground on their LM/Busy modules?

FMC CTP card has 70 LVDS drivers and 70 LVDS receivers (FIN1101, each chip has 2 x 3.1 mm). There is no space on the PCB for bigger chips (optical or digital isolators).

A common mode for the LVDS driver (located at detector FEE) can be in range of 50 mV - 3.25 V.

The grounding scheme was mentioned at Point 4 and 5.

Current Faninout modules will not be supported in LHC Run3. Instead them we offer FMC CTP card for their LTU.

13. The optical version of IPbus was tested.

IPbus was tested with the smart layer 2 optical switch S3800-244S equipped with optical transceivers SFP1G-SX-85.

14. Temperature and cooling of SFPs.

A test in lab with full optical power and monitoring the temperature of each SFP provided by SFP module is planned.