



HL-LHC Circuits and Protection Options

Samer Yammine on behalf of the Magnet Circuit Forum

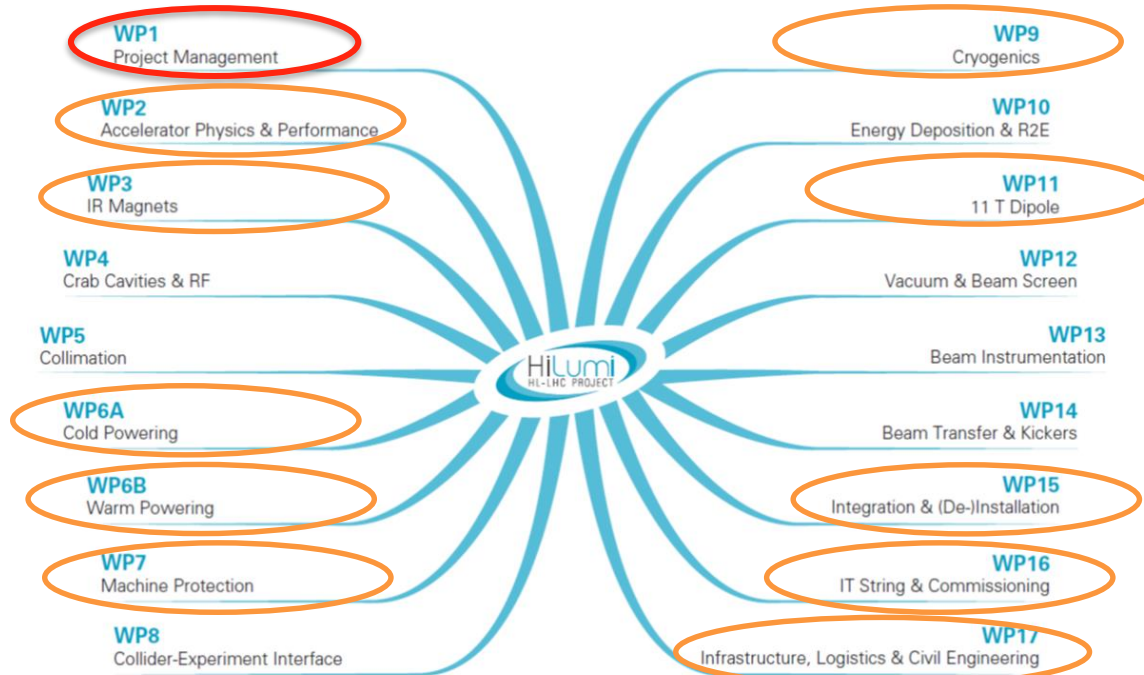
7th HL-LHC Collaboration Meeting – 14th November 2017



Content

- 1) Background and Current Global Status
- 2) Progress on the Inner Triplet Circuits
- 3) Progress on the Matching Section Circuits
- 4) Progress on the 11T Dipole Circuit
- 5) Conclusions

HL-LHC Magnet Circuit Forum



MCF Contributors

Mandate

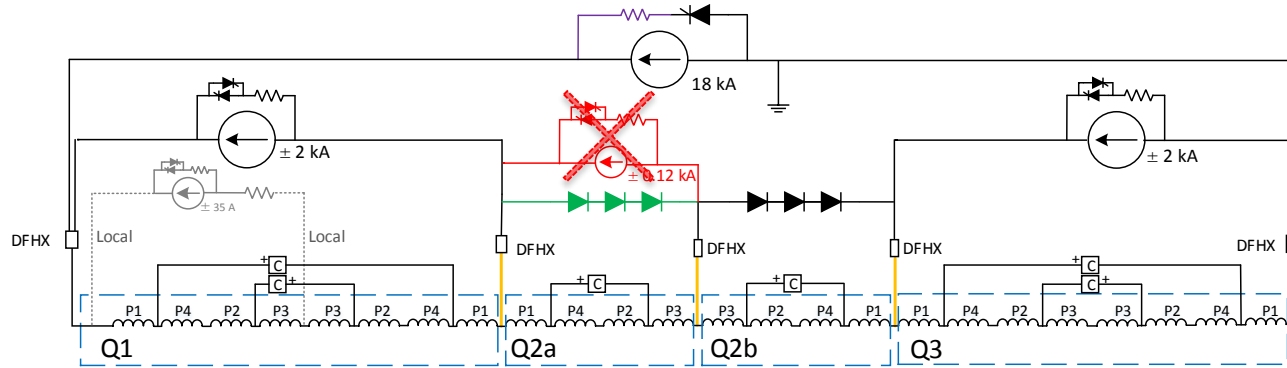
- The Magnet Circuit Forum (MCF) is the meeting where all aspects related to powering and protection of the HL-LHC circuits are discussed, in particular the ones pertaining to the optimization of circuit layouts and definition of protection means.
- Subjects in the agenda are defined in close collaboration with the relevant WPs.
- Interface aspects between systems are clarified through meetings at the forum. To this end, a documentation plan has to be developed and completed.
- The aim is to prepare a set of functional interface specifications that can be used as input for the design (technical specifications) of the different systems.
- Assessment on realistic failure scenarios and required mitigation strategies on a global basis is part of the activities of the MCF.
- The MCF is the meeting where aspects related to high voltage withstand levels are discussed and harmonized.
- The MCF reports regularly to TCC and takes up any relevant discussion within the domain of cold/warm powering and protection of the HL-LHC circuits in collaboration with the relevant WPs.

Background

Since the 6th Hilumi Collaboration Meeting:

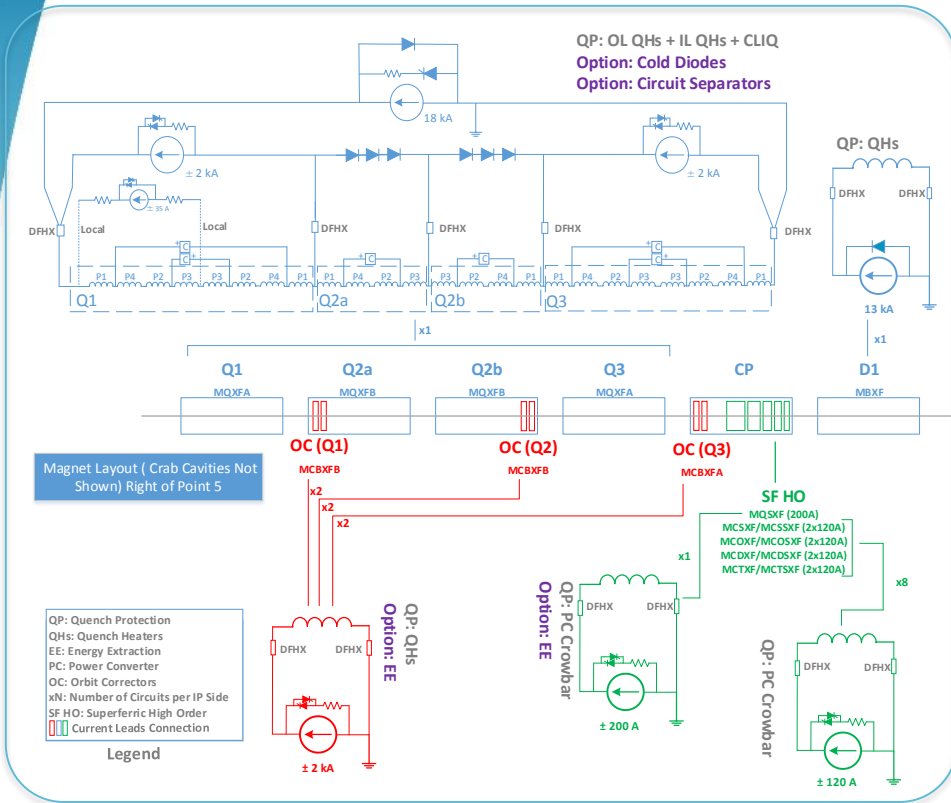
- Common work with relevant WPs within **Magnet Circuit Forum (MCF)**
 - **Sixteen** regular meetings and **eight** topical meetings ([link](#))
- CERN internal review on HL-LHC magnet circuits (17th March 2017 - [link](#))
 - Very useful exercise that provided many recommendations and statements
 - Important work to follow-up the recommendations with concerned work packages
- Following the review, several changes have been applied to the baseline of the circuits (ECR to the HL-LHC baseline in TDR is in draft)
- This presentation shows the consolidated changes to the baseline
- The several options will be shown as well

Inner Triplet Main Circuit : Changes to Baseline of TDR V0.1 after the Internal Circuits Review



- Removal of Q2a trim power converter (sorting of Q2a and Q2b magnets will be applied before installation to mitigate transfer function differences)
- Addition of warm diodes over Q2a to limit the voltage to ground during quench
- Addition of a Q1a K-modulation circuit to meet the HL-LHC optics requirements
- Upgrade the s.c. link trim cables capability to 7 kA and 5 MIITs
- Addition of crowbar resistance to the RQX power converter to discharge the circuit faster (in case of cryogenic failure, water failure, powering failure, etc.)

Current Status of the Inner Triplet Circuits



Cold Powering Status:

- Document by WP6a and MCF – EDMS [1821907](#)
- Talk by A. Ballarino on Thursday ([link](#))

Warm Powering Status:

- Talk by M. Martino on Thursday ([link](#))

Quench Detection and Protection:

- Talk by R. Denz on Thursday ([link](#))

Cold Diodes Option:

- Later in talk

Circuit Separators Option:

- Later in talk

EE Option for MCBXF & MQSXF:

- Talk by E. Todesco on Thursday ([link](#))

Open Issues & Class of Uncertainty

Circuits	Powering Scheme	Open issue	Class
Inner Triplet	Baseline	Q1a k-modulation circuit design	2
		IT main circuit bus-bars design	3
		Design and integration of the cables and feedthroughs for CLIQ	3
		Polarities of the connection of quench heaters and CLIQ	3
		Design and implementation of interconnects and splices	4
		Design and integration of protection instrumentation	4
	Options	Study on the IT alternative configurations	1
		Circuit separators	3
		Local integration of leads for the superferric correctors	4
		Cold diodes qualification and integration studies	4
Matching Section	Baseline	Follow-up on the DSL dismantling decision	4
11T	Baseline	Define the global 11T interlock strategy within the RB circuit	1
		Flux Jumps: Prototype test to elaborate a suitable QD strategy	3
		Current leads and protection scheme for 11T trim	3
		Decision on test the impact of the trim PC on the QDS in case of power abort on the 11T and neighbouring MB magnets in SM18	4

Estimate Class	% of complete definition
Class 1	50 – 100
Class 2	30 – 70
Class 3	10 – 40
Class 4	1 – 15
Class 5	0 – 2



2) Progress on the Inner Triplet Circuits

- a) Circuit Consolidation: Simulations and Cross-check Simulations
- b) Option: Cold Diodes and Quench Protection
- c) Option: Circuit Separators



2.a) Baseline Consolidation: Simulations and Cross-check Simulations on the Inner Triplet

Conclusions from Simulations & Analysis in a Nutshell

- For **standard** cases of quench, currents in the 2kA trim leads can go up to 4.3 kA and 2.2 MIITs (up to ultimate currents) => **5 kA** current capability in s.c. state would suffice for not quenching the conductors within the s.c. link
- For the **very conservative scenario**, those values could go up to **6.1 kA** (nominal) and **6.8 kA** (ultimate), and **5 MIITs** (nominal and ultimate), these numbers are obtained considering a full magnet suddenly quenching in its whole volume
- **the analysis covers the whole spectrum of operating conditions, from low to ultimate current**

TALES Simulations by E. Ravaioli (LBNL)

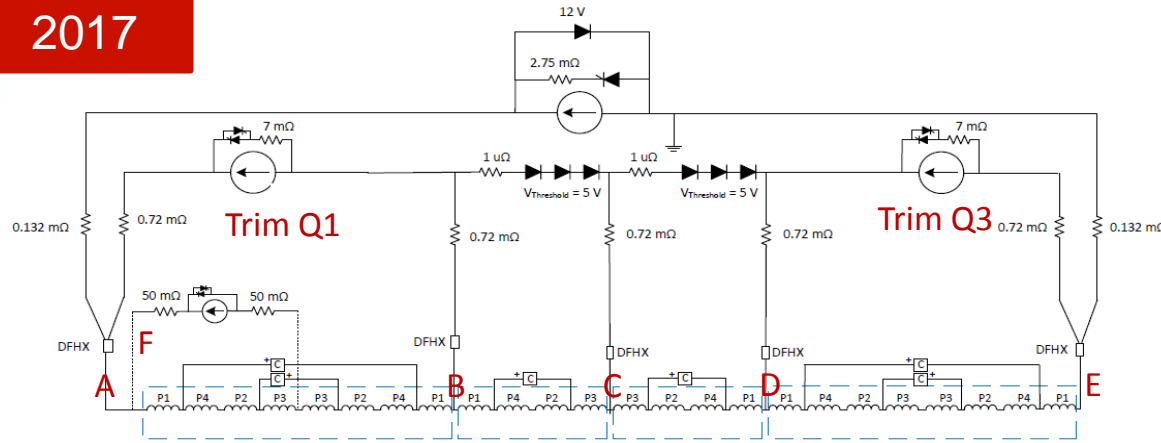
May
2017

Extract from Panel Report of the 2017 HL-LHC circuits internal review ([link](#)):

- *The panel considers that the presented powering circuit is a robust solution, provided the 2 kA and 120 A SC trim cables in the superconducting link can be upgraded to a rating of about 5-6 kA (to avoid quenching of the SC link in almost all cases of a magnet quench, an event considered rare and estimated in once a year) and 5 MIITS (to provide safety against any event of quench).*

Cross-check Simulations

October
2017



Assumptions

- **Maximum current, ramp rate, and MIITs evaluated under different scenarios**
(Reference cases provided by E Ravaoli)
- Regular quench: **Detection + validation time = 15 ms**
- Global magnet quench: **Detection + validation time = 10 ms**

Highest values	Leads A / E	Leads B / D	Lead C	Lead F	Trim Q1	Trim Q3
Current [kA]	17.8	6.1	4.3	4.1	5.1	4.2
Ramp rate kA/s	250	170	100	70	160	160
MIITs	32.6	3.8	1.9	1.5	2.9	1.9

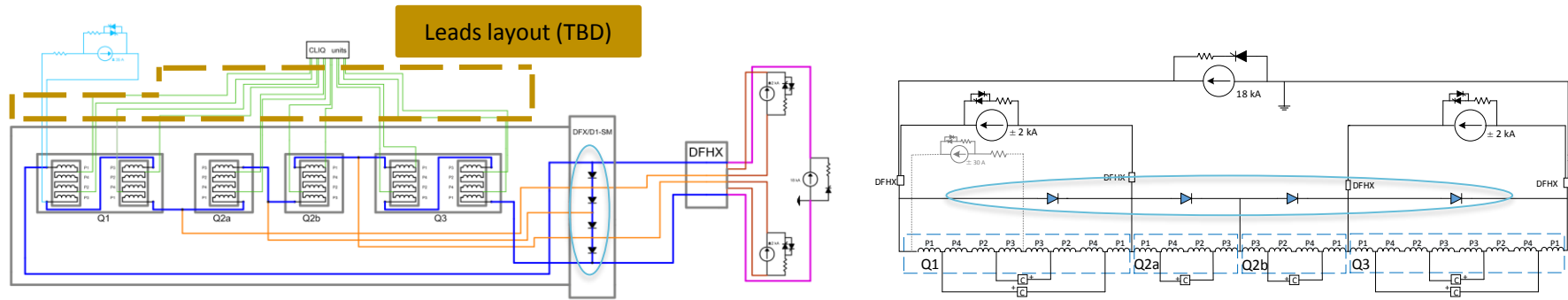
STEAM-LEDET simulation results consistent with previous TALEs simulations

M. Mentink on Thursday ([Link](#))



2.b) Option: Cold Diodes and Quench Protection

Inner Triplet Main Circuit with Cold Diodes



Advantage of cold diodes as considered by the Panel of the Internal Circuit Review :

- Diodes will protect the cold powering components from high over currents in case of quench unbalance in between magnets.
- Diodes will also provide more margin and flexibility in case of unforeseen larger over-currents, decoupling the warm and cold part of the circuit.

Options to Protect MQXF Magnets and Bus-bars

Protection baseline: Any quench in any element → Fire all the QHs/CLIQ systems

R. Denz on Thursday ([Link](#))

When introducing the cold diodes, two possible strategies:

1. One element quenches → All QHs/CLIQ systems will be fired. Diodes carry only the over-currents (capability of more than 13 kA peak if LHC diodes are re-qualified) for an equivalent time = 100 ms
2. One element quenches → Selective QHs/CLIQ fired. Diodes should carry 18 kA, time constant = 100 s

Possible additional advantage for option 2:

- If a quench of the other magnets following the first cannot be completely avoided, it would happen at lower current.
- Reduction of the stress on the magnet and the heat dissipated into the cryogenic system, which will allow a faster recovery.

Conclusion on Cold Diodes Options

Option 1: One element quenches → All QPS systems will be fired

Advantages to WP3:

- Bus-bar integration in the cryostat is less complex
- No need to size the trim bus bars to 18 kA (s.c. state and quenching state)
- No need to integrate heat sinks for diodes

Advantages to WP7:

- Keeps the QDS reliability like in the LHC's IT circuit
- The triplet circuit in itself is the most complex HL-LHC circuit. Option 1 does not add further complexity from the QDS point of view.
- The use of the LHC diodes if qualified for radiation levels.

Disadvantages:

- When quench, no quick distinction between quench in coil and bus-bars in terms of detection

Option 2: Selective quench strategy

Possible advantages of the selective quench protection:

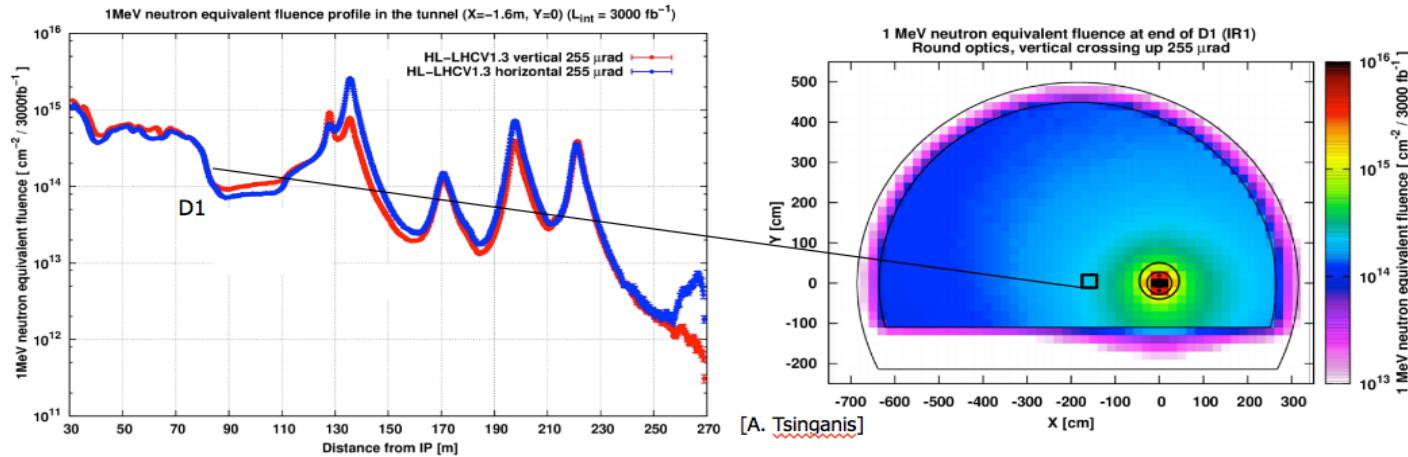
- Triggering of the QHs/CLIQ of the other (not initially-quenching) magnets at a lower current (expected ca. 10% less from one magnet to the adjacent one)
- It will allow more energy to be dissipated in the crowbar of the RQX PC

Disadvantages:

- It includes complexity in the implementation of the QDS which leads to a less reliable system.
- Due to the quench propagation, all the magnets could eventually be fired (in the order of ten seconds between the quench of the different magnets)
- Diodes (+heat sinks) and bus-bars will be significantly bigger
- Imposes new (non-LHC) diodes to support the current of 18 kA

After discussions, MCF considers option 1 as more adequate and proposes to discontinue efforts in the direction of option 2. TCC endorsed this consideration.

Radiation Doses and Qualification of Cold Diodes



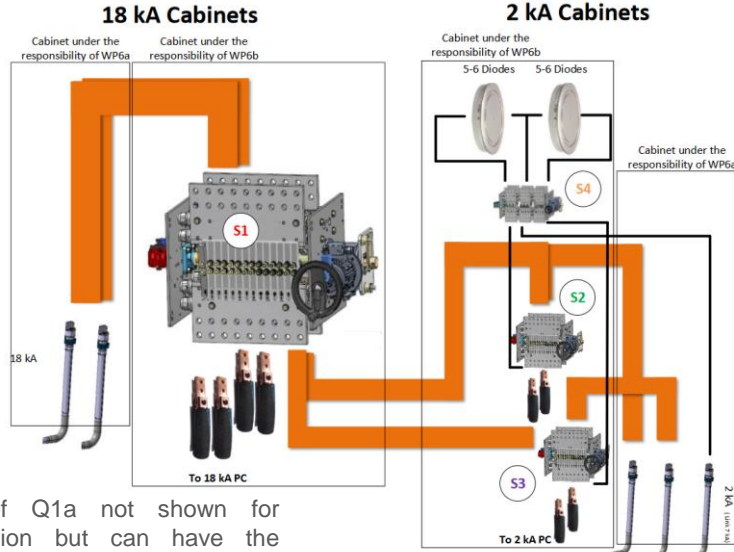
Courtesy F. Cerutti, R2E Cost and Schedule Review, 12.10.2017

- LHC type diffusion diodes tested (15 years ago) up to $\sim 2\text{ kGy}$ and $3 \times 10^{13}\text{ n cm}^{-2}$ (LHC project Report 688)
- Qualification is required up to 30 kGy and $10^{15}\text{ n}_{\text{eq}}\text{cm}^{-2}$



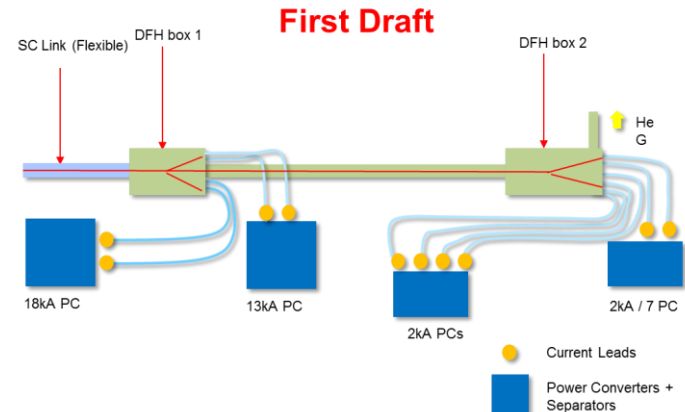
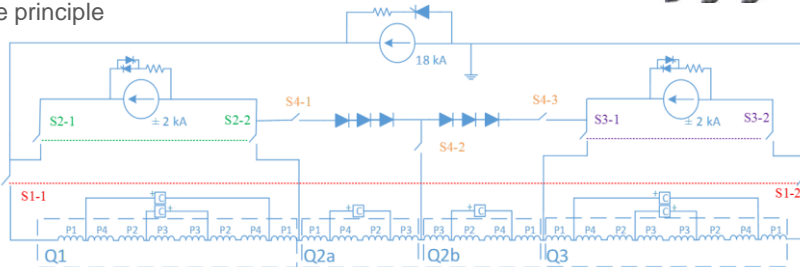
2.c) Option: Circuit Separators

Circuit Separators in a Nutshell



- Separators in IP2x cabinets provide a viable solution for personnel and equipment protection (Commissioning, Operation, ELQA, etc.)
- Disconnect, connect, short circuit and to ground connections

Circuit of Q1a not shown for simplification but can have the same principle





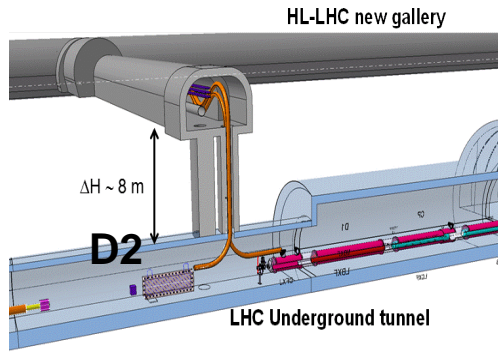
3) Progress on the Matching Section Circuits

Status on the Powering of the MCBYs

- Q4 and Q5 correctors will be powered individually
- Upon a request by WP6b (transmitted to the MCF), WP6a has accepted to provide enough leads to feed **individually the corrector MCBY magnets of Q4 and Q5**. This means that 1 assembly of four leads will be integrated in the Q4 cold mass and 3 assemblies in the cold mass of Q5.
- This will mitigate the development of a new family of power converters to deal with the high energy and the inductance of two MCBYs in series.
- The decision on the necessity of **dismantling the DSL during LS3 should be taken by the end of 2017 or beginning of 2018**. By then, a roadmap on the strategy will be proposed to MCF and TCC.

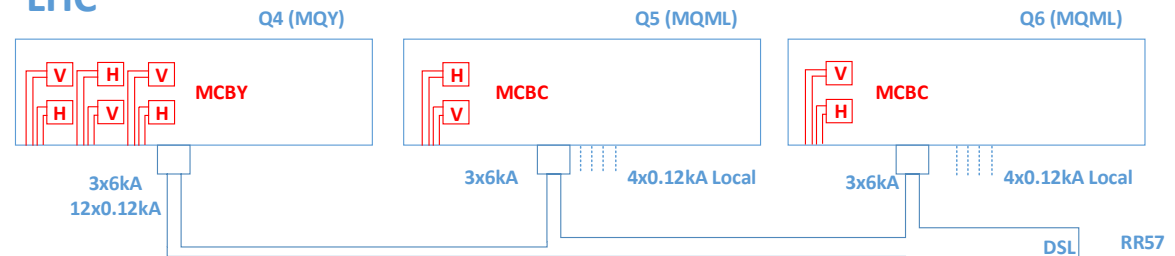
Matching Section Overall Powering Scheme

Layout Right of Point 5

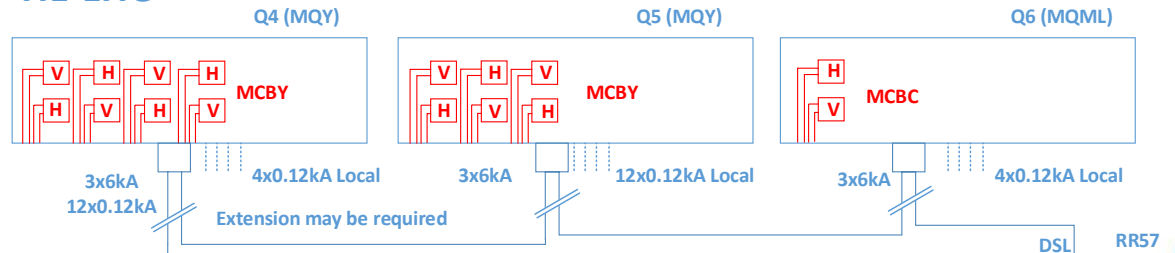


- Powering of D2 from UR (DFHM):
 - 2x13 kA + 8x0.6 kA

LHC



HL-LHC



- DFBL + DSL for Q4 + 6xQ4 correctors , Q5 and Q6
- Local powering for supplementary 2xQ4 correctors
- Local powering of Q5 correctors
- Q6 as LHC configuration



4) Progress on the 11T Dipole Circuit

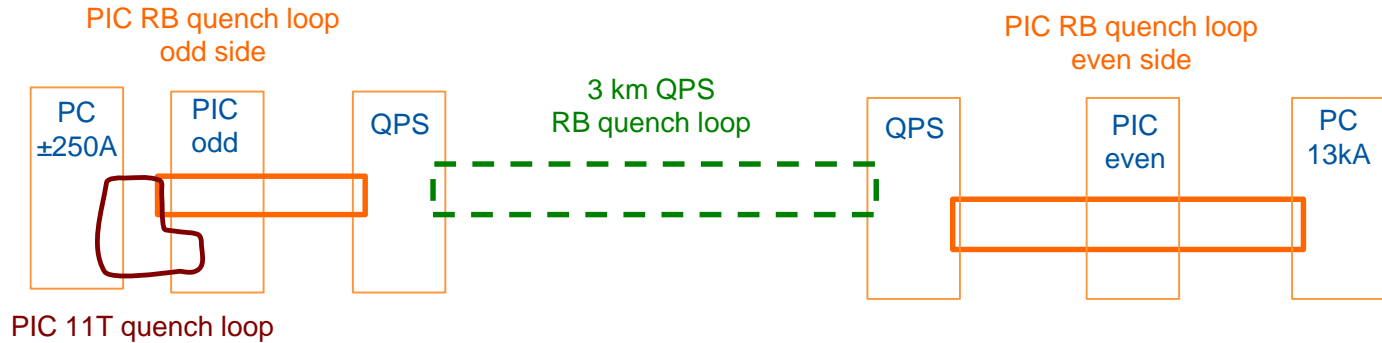
- a) 11T Powering Interlock Controller
- b) 11T Trim Powering with Conduction-Cooled Leads
- c) 11T Dipole – Powering and Protection Document



4.a) 11T Dipole and RB Circuit Interlock System

Proposed Implementation of 11T Trim Circuit Interlock

11 T trim PIC proposal

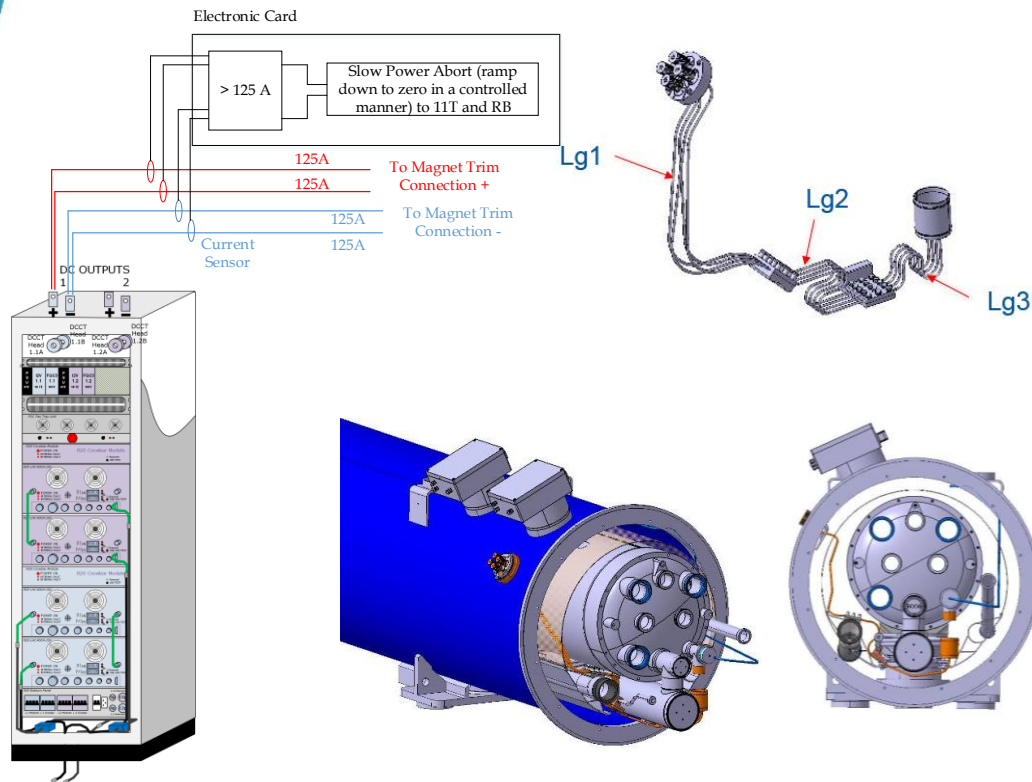


- Hardware connection to the Power Interlock Controller (PIC) of the main dipole quench loop at the odd side
- Separate the 11T trim and the RB (dipoles) circuit → easier diagnostics in case of trip
- Slow power abort requests of both power converters would be implemented in the PIC as a function of the status of the systems.



4.b) 11T Trim Powering with Conduction-Cooled Leads

11T Trim Powering with Conduction-Cooled Leads



- Electrical insulation tests on LHC conduction-cooled leads ($V_{ins} > 5$ kV in He gas, RT, atmospheric pressure)
- Two CLs per polarity
- Requirements:
 - Protection of leads when voltage across lead ≈ 100 mV
 - Protection of leads when $I_{CL} > 125$ A
 - Protection by slow power abort (≈ 10 s)



4.c) 11T Dipole Powering and Protection Document

11T Dipole Powering and Protection

This report describes the powering and protection of the 11T dipole circuit. The **different elements of the circuit** are described and **simulations** for currents and quench behaviour are shown. **Measurements** done on the 11T magnet are also reported. The magnet protection aspects are discussed, as well as, hints to the hardware requirements. **Case study of normal and failure scenarios** related to the magnet circuit are analysed.

EDMS no: **1764166** ([Link](#))

Authors: **S. Izquierdo, G. Willering, S. Yammine, R. Denz, F. Menendez, A. Antoine, I. Romera, D Wollman and Jens Steckert**



EDMS NO. 1764166	REV. 0.1	VALIDITY DRAFT
REFERENCE :		

REPORT		
11 TESLA DIPOLE		
11T DIPOLE CIRCUIT - POWERING AND PROTECTION		
Abstract		
This report describes the powering and protection of the 11T dipole circuit. The different elements of the circuit are described and simulations for currents and quench behaviour are shown. Measurements done on the 11T magnet are also reported. The magnet protection aspects are discussed, as well as, hints to the hardware requirements. Case studies of normal and failure scenarios linked to the magnet circuit are analysed.		
<div style="border: 2px solid blue; padding: 10px; font-size: 24px; font-weight: bold; color: blue;">Under verification process</div>		
TRACEABILITY		
<i>Prepared by:</i> S. Izquierdo Bermudez, G. Willering, S. Yammine, R. Denz, F. Menendez Camara, A. Antoine, I. Romera Ramirez, D. Wollman and J. Steckert		<i>Date:</i> 2017-03-16
<i>Verified by:</i> H. Bajas, R. Garcia Alia, H. Prin, F. Rodriguez Mateos, H. Thiesen, Jan Uythoven, A. Verweij and G. Willering.		<i>Date:</i> 20YY-MM-DD
<i>Approved by:</i> M. Bajko, I. Bejar Alonso, J-P Burnet, P. Fessia, M. Pojer, F. Savary and D. Wollman		<i>Date:</i> 20YY-MM-DD
<i>Distribution:</i> N. Surname (DEP/GRP) (in alphabetical order) can also include reference to committees		
Rev. No.	Date	Description of Changes (major changes only, minor changes in EDMS)
X.0	20YY-MM-DD	[Description of changes]





5) Conclusions

Conclusions

- ✓ Great effort carried out with the different work packages
- ✓ Significant advancements to optimize the circuits
- ✓ Follow-up activity on recommendations from the review
- ✓ Good status with respect to the open issues
- ✓ ECR on the modifications to the baseline (in TDR) under preparation



Thanks for your attention



Spare slides

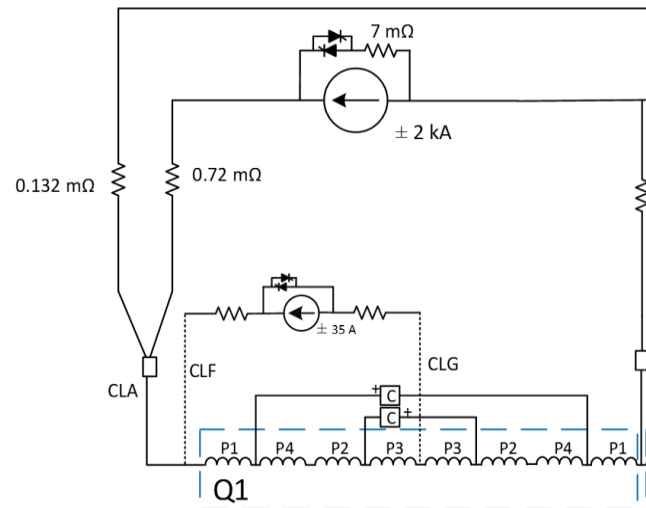
Q1a k-modulation circuit simulations

Developed simulations on

- Current profile during magnet quench
- Current profile during power aborts (without quench)
- Required PC voltage
- Control performance during operation
- Copper cable section for cold powering

Summary of the simulations

- DC cable resistance (resistance during operation) value of less than 265 mOhm is optimal from a powering point of view (PC voltage and design)
- DC cable resistance + Crowbar resistance should be at least 230 mOhm to limit current looping above the DC design value of the circuit
- Overcurrent due to quench for the 'most conservative scenario' generate a hot spot temperature of 314 K.
- If integration accepted, it is fairly straightforward to define the parameters of the circuit (2x20mm²).
- Standard HL-LHC-60A-10V can be therefore used.



Current proposal

Circuit resistance: 230-240 mOhms

- Max current: 4.2 kA
- Max MIITs: 1.66
- Copper cable section: 20 mm²
- Hot-spot temperature: 314 K

Document co-authored by WP6a and MCF - MS

Magnet	Circuit type	Current (A)	Feedbox Type	Lead Type	N _{TOT} leads	SC Link Type	N _{TOT} cables in the SC link
MQY	Q4 Quadrupole	6000	*DFBL	HTS*	3	*DSL	3*
MCBY	Q4 Correctors	120	*DFBL	Resistive*	12	DSL	12*
		120	-	Local**	4	-	-
MQY	Q5 Quadrupole	6000	*DFBL	HTS*	3	*DSL	3*
MCBY	Q5 Correctors	120	-	Local**	12	-	-
MQML	Q6 Quadrupole	6000	*DFBL	HTS*	3	*DSL	3*
MCBC	Q6 Correctors	120	-	Local**	4	-	-
MCBRD	D2 Correctors	600	DFHM	HTS***	8	DSH	8***
MBRD	D2 Recombination Dipole	13000	DFHM	HTS***	2	DSH	2***

Circuit	Rating (A)	Worst case V to Gnd (V)	Acceptance		Installation		Current (μA)	Time (s)
			RT	NOC	RT	NOC		
D2	13000	110	1440	720	335	705	10	30
D2 Corr.	600	660	3640	1820	364	792	10	30
Q4	6000	110	1440	720	150	150	15	30
Q4 Corr.*	120	160	1640	820	300	600	3	30
Q4 Corr.**	120	60	1240	620	300	600	3	30
Q5	6000	110	1440	720	150	150	15	30
Q5 Corr.	120	60	1240	620	300	600	3	30
Q6	6000	110	1440	720	260	480	15	30
Q6 Corr.	120	60	1240	620	300	600	3	30