



Electrical design criteria for HL-LHC

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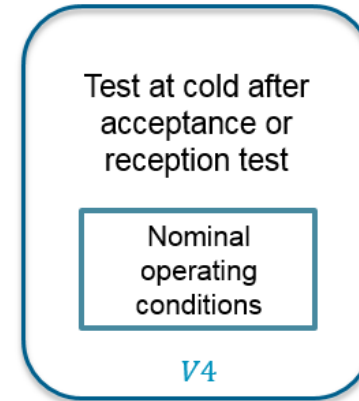
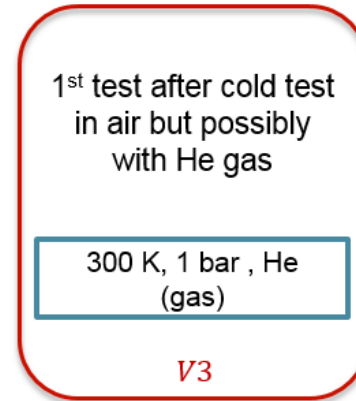
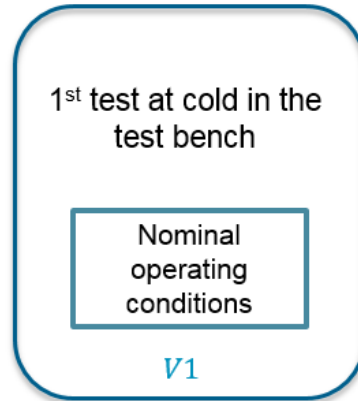
Introduction and some rules

- Electrical tests are performed to verify that the integrity of the insulations of the elements of a circuit are within the pre-defined nominal limits.
- Electrical tests are required to certify acceptance before cooling down components at cryogenic temperatures, before installation of components in the tunnel and further during commissioning and operation
- Components (magnets, bus bars, link, current leads, instrumentation, including also the warm DC distribution elements) must be designed according to voltages that they should withstand during operation. Defining test levels (according to worst conditions) is something intrinsically linked to the design of components. Defining realistic testing conditions requires the understanding of both design of components and the operational aspects.
- For HL-LHC, it has been decided to apply worst case conditions including one (in some cases two) levels of failure – e.g. one or two heater circuit failing
- The values taken as reference are given at nominal currents; ultimate current values are intrinsically included within the established, engineering margins.
- No margins with respect to worst case calculated values are taken for inter-turn voltages.

Hi-Pot Test procedure

Acceptance /Reception

Installation



$$V2 = 2 * V1$$

$$V1 = 2 * U_{Coil\ to\ gnd} + 500$$

$$V3 = \frac{V1}{5}$$

$$V4 = 1.2 * U_{Coil\ to\ gnd}$$

Simulations

If $V_1 = a * U_{coil-to-ground} + b$, IEEE Standard 95-177 suggests $a=2$, and b from 1000 to 2000 V
We took $b=500$ V for LHC, and now also for HL-LHC

Reference conditions

	Circuits	Worst case conditions
Inner triplet	<i>MQXF</i>	<ul style="list-style-type: none"> • 1 (2) Quench heater circuit failing • Nominal current
	<i>Orbit correctors</i>	<i>TBD</i>
	<i>Superferric correctors</i>	<ul style="list-style-type: none"> • 1 Quench heater circuit failing • Nominal current • #<i>Superferric order 2</i> – <i>EE system</i>
D1	<i>Separation dipole D1</i>	<i>TBD</i>
D2	<i>Recombination dipole D2</i>	<ul style="list-style-type: none"> • 1 Quench heater circuit failing • Nominal current
	<i>Orbit correctors D2</i>	<ul style="list-style-type: none"> • Nominal current • EE system
Matching section	<i>Q4, Q5, Q6 and correctors</i>	<i>Same as LHC</i>
11T	<i>11T dipole</i>	<ul style="list-style-type: none"> • 2 Quench heater circuits failing (worst possible case) • Nominal current

Electrical test levels – Magnets– Part I

Magnet	Max discharge V to GND	Max V coil to GND	Max V coil to heater	Minimum design withstand voltage {Acceptance/ Reception}				Test Voltage to GND {Installation}		V Inter-turn
				Gnd	QH	Gnd	QH	Ground		
MQXF	-	670	900	1800	2300	3700	3000	810	360	70
MCBXF	#	#	#	#	#	#	#	#	#	#
MQSXF *	450	300	NA	1100	NA	2200	NA	360	220	-
MCSXF/MCSSXF	-	135	NA	770	NA	1540	NA	162	154	-
MCOXF/MCOSXF	-	70	NA	640	NA	1280	NA	84	128	-
MCDXF/MCDSXF	-	36	NA	572	NA	1144	NA	43	115	-
MCTXF/MCTSXF	-	251	NA	1002	NA	2008	NA	302	201	-

Blue: Nominal operating conditions

Red: Room temperature

*EE system

#Not enough inputs

Felix Rodriguez Mateos

Electrical test levels – Magnets– Part II

Magnet	Max discharge V to GND	Max V coil to GND	Max V coil to heater	Minimum design withstand voltage {Acceptance/ Reception}				Test Voltage to GND {Installation}		V Inter-turn
				Gnd	QH	Gnd	QH	Ground		
MBXF	-	#	#	#	#	#	#	#	#	#
MBRD	-	587	900	1674	2300	3348	4600	705	335	43
MCBRD *	#	450	NA	1400	NA	2800	NA	540	280	150
11 Tesla	450	1450	1400	3400	3300	5000	3300	1740	680	85

Blue: Nominal operating conditions

Red: Room temperature

*EE system

#Not enough inputs

Electrical test levels – Magnets– Part III

Magnet	Max discharge V to GND	Max V coil to GND	Max V coil to heater	Minimum design withstand voltage {Acceptance/ Reception}				Test Voltage to GND {Installation}		V Inter-turn
				Gnd	QH	Gnd	QH	Ground		
MQY (Q4)	-	125	-	750	1500	1500	3000	150	150	-
MCBY	-	500	NA	1500	NA	3000	NA	600	300	-
MQY (Q5)	-	125	-	750	1500	1500	3000	150	150	-
MCBY	-	500	NA	1500	NA	3000	NA	600	300	-
MQML	-	400	-	1300	1500	2600	3000	480	260	-
MCBC	-	500	NA	1500	NA	3000	NA	600	300	-

Blue: Nominal operating conditions

Red: Room temperature

Test levels for cold powering– Inner triplet and D1

Rating (kA)	Worst case voltage to ground during operation (V)	Acceptance tests of components to ground (V)		Insulation test voltage of system to ground (V)		Leakage current per component (μ A)	Test duration (s)
		RT	NOC	RT	NOC		
18	210	1840	920	360	810	≤ 10	30
7	210	1840	920	360	810	≤ 10	30
2	560	3240	1620	324	672	≤ 10	30
0.2	527	3108	1554	311	633	≤ 10	30
0.12	60	1240	620	220	360	≤ 10	30
0.035	210	1860	920	360	810	≤ 10	30

Worst case voltage to ground during operation

18 and 7 kA: 10V (Q1a k-modulation circuit – crowbar and cabling) + 100V (RQX – Crowbar and cabling resistances) + 100V (sc. Link)

2 kA: 500V (EE system) + 50V (crowbar resistance) + 10V (cabling resistance)

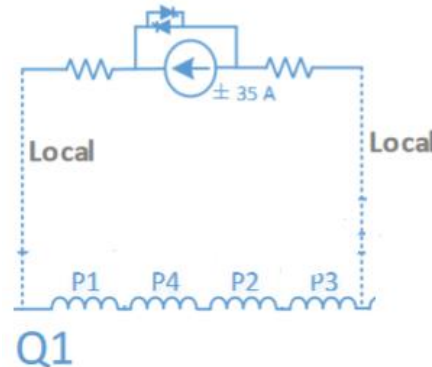
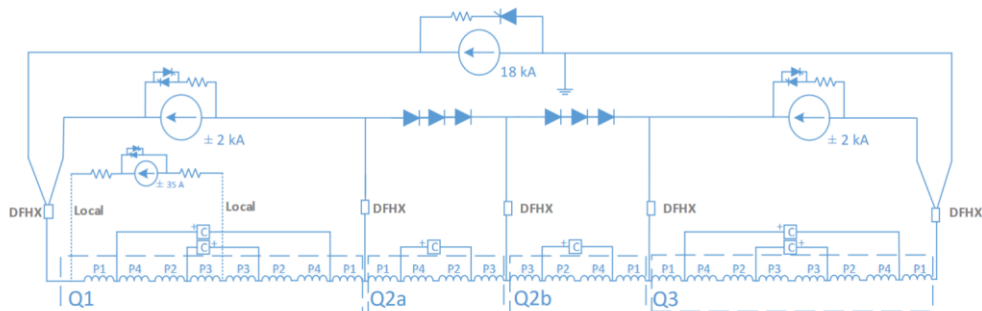
0.2 kA: 500V (EE system) + 17V (crowbar resistance) + 10V (cabling resistance)

0.12 kA: 50V (crowbar resistance) + 10V (cabling resistance)

0.035 kA: 10V (Q1a k-modulation circuit – crowbar and cabling) + 100V (RQX – Crowbar and cabling resistances) + 100V (sc. Link)

Q1a k-modulation - HVWL

~ 230 mOhms



Resistance assumption:

- First approach/idea was a high impedance circuit (with around 20-30 Ohms) → HVWL issues : ~ 1kV to ground in case of power abort → higher value than the magnet itself develops
- After an analysis of the circuit, in the following [presentation given on the 17th of October 2017 at the Magnet Circuit Forum \(MCF\)](#), it was stated that the Q1a k-modulation circuit will be a low impedance circuit. The low impedance value will be ~230 mOhms (still to be endorsed by TCC).
- Over-currents in the Q1a k-mod leads (4 kA, 1.5 MIITs) may create back overvoltage in the case of the conservative scenario presented by S. Yammine at the plenary talk. To be followed up.

Test levels for cold powering – Matching section

Rating (kA)	Worst case voltage to ground during operation (V)	Acceptance tests of components to ground (V)		Insulation test voltage of system to ground (V)		Leakage current per component (μ A)	Test duration (s)
		RT	NOC	RT	NOC		
13	110	1440	720	335	705	≤ 10	30
6	110	1440	720	260	480	≤ 15	30
0.6	660	3640	1820	364	792	≤ 10	30
0.12	60	1240	620	300	600	≤ 3	30
0.12*	160	1640	820	300	600	≤ 3	30

*Rating corresponding to the leads for Q4 correctors through the s.c. Link.

Worst case voltage to ground during operation

13 and 6 kA: 100V (sc link) + 10V (cabling resistance)

0.6 kA: 500V (EE system) + 60V (crowbar and cabling resistance) + 100V (sc link)

0.12 kA: 50V (crowbar resistance) + 10V (cabling resistance)

0.12 kA*: 100V (sc link) + 50V (crowbar resistance) + 10V (cabling resistance)

Test levels for 11T dipole

Magnet

Rating (kA)	Worst case voltage to ground during operation (V)	Acceptance tests of components to ground (V)		Insulation test voltage of system to ground (V)		Leakage current per component (μ A)	Test duration (s)
		RT	NOC	RT	NOC		
		13	1450	5000	3400		

Cold Powering

Rating (kA)	Worst case voltage to ground during operation (V)	Acceptance tests of components to ground (V)		Insulation test voltage of system to ground (V)		Leakage current per component (μ A)	Test duration (s)
		RT	NOC	RT	NOC		
		13	1000 **	5000	2500		

* Special pressure conditions ($p > 5$ bar) in LHC

** Earth fault at PC considered

WP6b stated that the trim PC will be designed to withstand **1.2kV** (full energy extraction voltage at ultimate + 20% margin).



Documentation

Engineering specification HVWL

Contents



EDMS NO. 0000000	REV. 0.0	VALIDITY DRAFT
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REFERENCE : LHC-EQCOD-ES-XXXXX

ENGINEERING SPECIFICATION

HIGH VOLTAGE WITHSTAND LEVELS FOR ELECTRICAL TESTS ON MAGNETS, BUS-BARS, SUPERCONDUCTING LINKS AND CURRENT LEADS FOR THE DIFFERENT HL-LHC MACHINE CIRCUITS

Abstract

This document describes the voltage withstand levels for the different components of the HL-LHC electrical circuits working at cryogenic temperatures. The values presented here will be used during tests prior to installation and during commissioning as systems in the tunnel.

The definition of electrical test levels is derived from the voltage for the operation of components in the machine, and includes an engineering security factor.

DRAFT

TRACEABILITY

Prepared by: Fernando Menendez Camara, Felix Rodriguez Mateos, Samer Yammine **Date:** 20YY-MM-DD

Verified by: N. Surname [Persons with relevant experience in the field] **Date:** 20YY-MM-DD

Approved by: N. Surname [Project hierarchy Ex. WP Leader, PL, ...] **Date:** 20YY-MM-DD

Distribution: N. Surname (DEP/GRP) (in alphabetical order) can also include reference to committees

Rev. No.	Date	Description of Changes (major changes only, minor changes in EDMS)
X.0	20YY-MM-DD	[Description of changes]

Conclusions

- ❖ Well-advanced status for the definitions of HVWL levels, but still optimization required for the influence of the Q1a k-mod circuit
- ❖ Also missing are IT orbit correctors and D1; after obtaining these values, document to be launched to verification process
- ❖ Structured feedback on experience from models and prototypes must be organized
- ❖ Test stations should be prepared with margins to cope with the proposed test values
- ❖ The Project is providing in 2018 one EIQA engineer who will work on homogenizing procedures, calibrations, hardware at the manufacturers premises. To be discussed with involved WPs.



Thanks for your attention