Level 1 Tracker Trigger for the CMS Phase-2 Upgrade

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Context: LHC and the CMS Experiment

Large Hadron Collider: Phase I

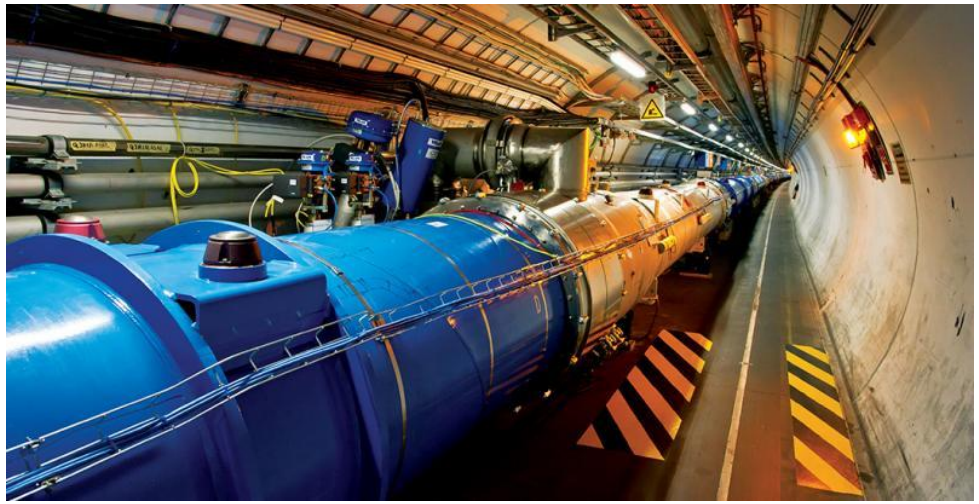
- CERN (Switzerland/France)
- 27 km length
- Proton-Proton Bunch Crossings (BX)
  - @ 40 MHz
  - 20-40 interactions per BX

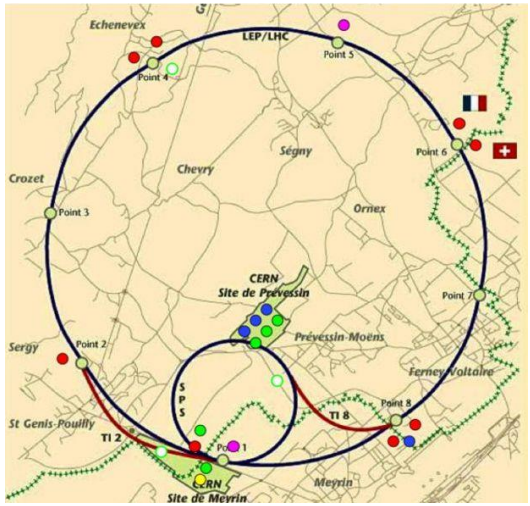
LHC Upgrade – Phase II (2023)

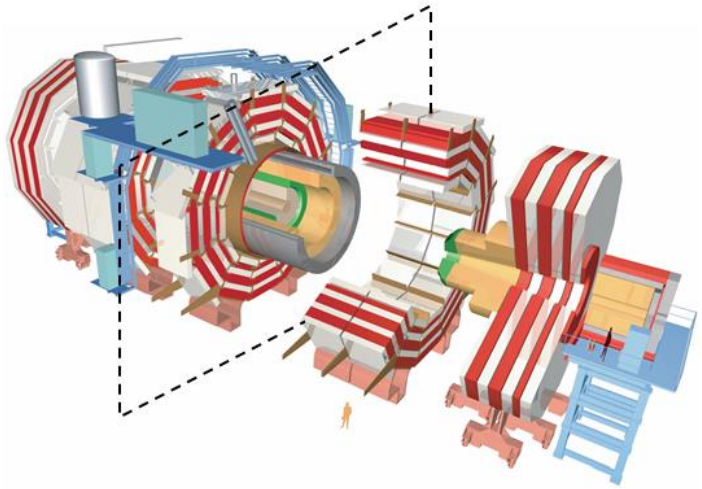
- Increase interactions per BX
  - 140-200 interactions

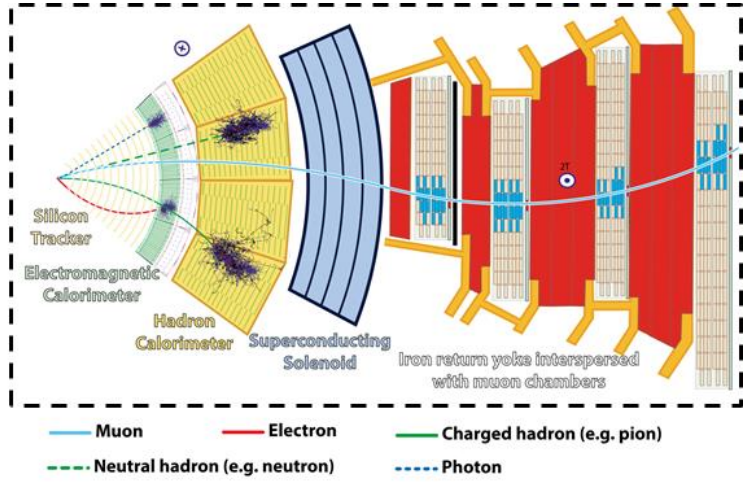
CMS Detector

- Silicon Tracker, ECAL, HCAL, Muon Chamber
- 40 TB/s raw data
- Upgrade of L1 trigger system









CMS Trigger

Phase I (up to 2023)

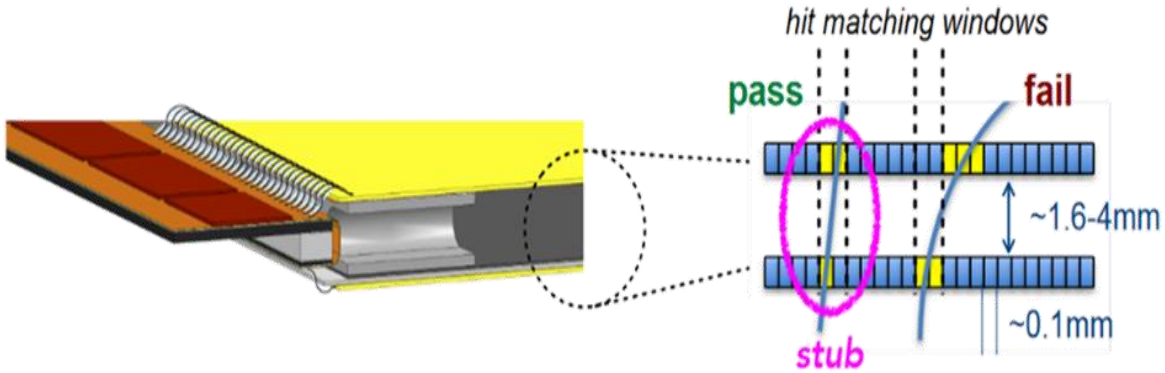
- L1 trigger from Calorimeters and Muon System

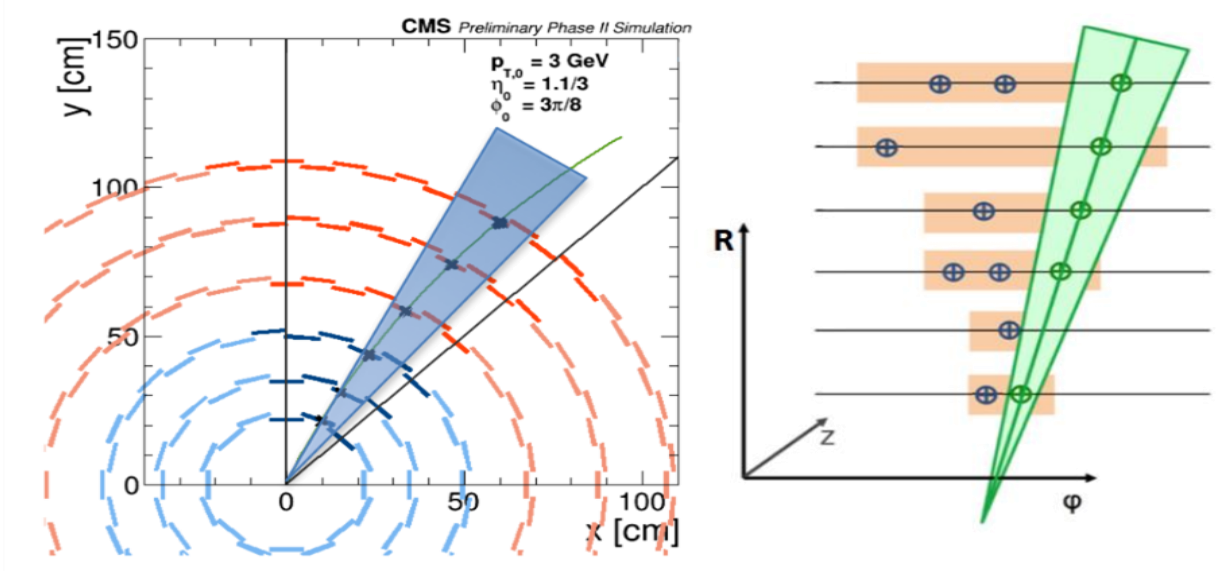
Phase II CMS (from 2023 on)

- Include Silicon Outer Tracker on L1 Trigger

L1 Tracking Trigger

- Interesting track: high pT
- Process pre-trigger data (“stubs”)
- Improve analysis of events candidates
- Filter and reduce the data to be transferred and recorded
  - From 40 TB/s to 100 MB/s
  - Latency < 4 µs





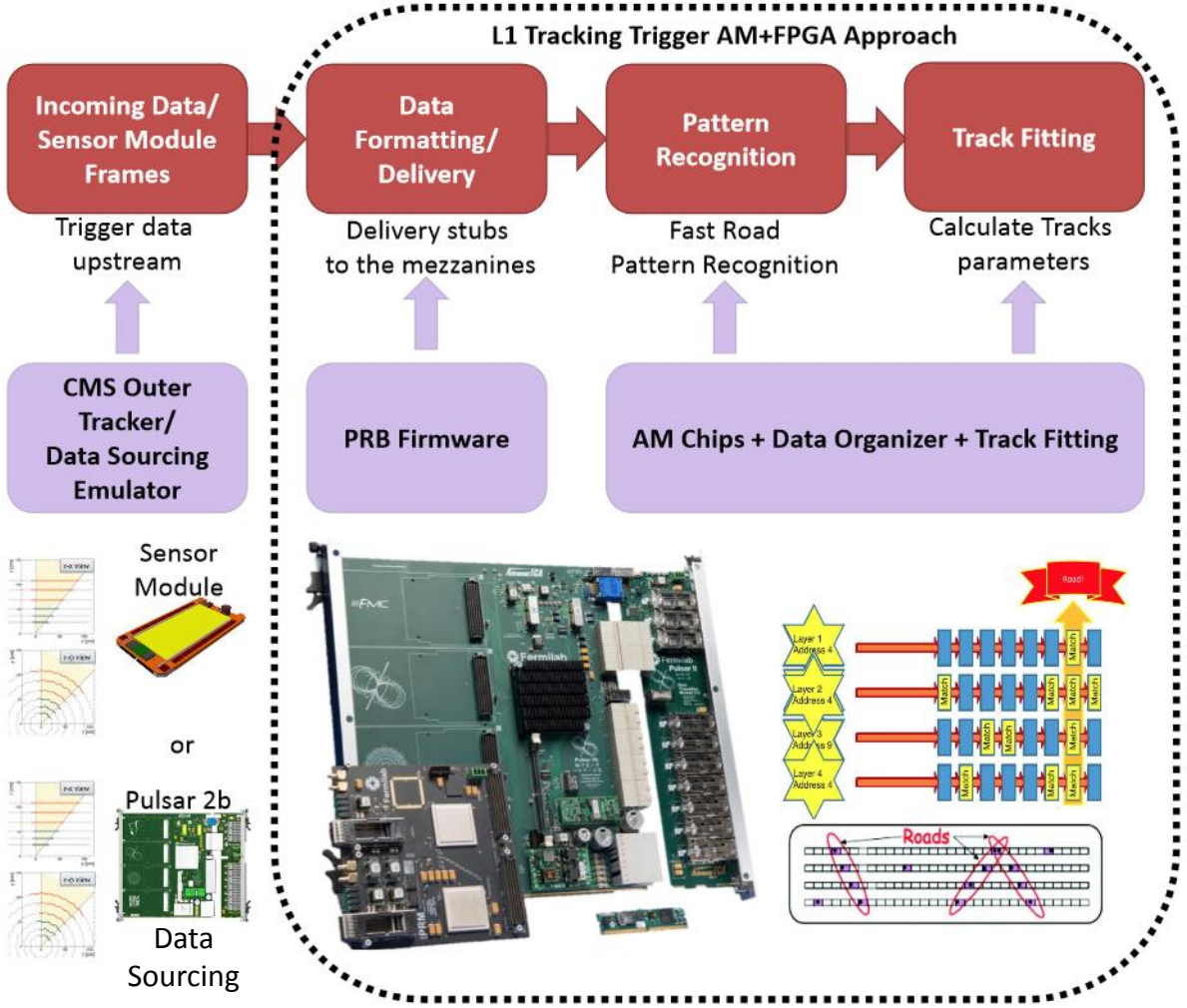
CMS Phase II: L1TT Approaches HW Demo 2016

Tracklet Approach

Time Multiplexed Trigger - TMT Approach

Associative Memory plus FPGA - AM+FPGA Approach

- FPGA hardware provides data formatting and sharing
- AM ASIC is a Content-addressable memories (CAMs) that provides Pattern Recognition
- Hardware demonstration based on Pulsar 2b ATCA Board
  - Custom Pattern Recognition Mezzanine for Pulsar 2b
- SPRACE team contribution are related to
  - ATCA infrastructure
  - CMS Outer Tracker Data Sourcing Emulator

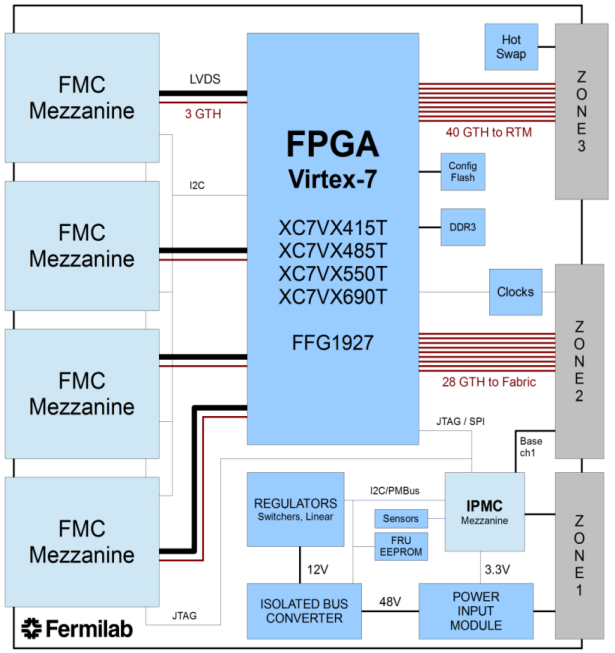


Pulsar 2b ATCA Carrier Board

General purpose ATCA board developed by Fermilab
- Designed to support L1 track trigger R&D

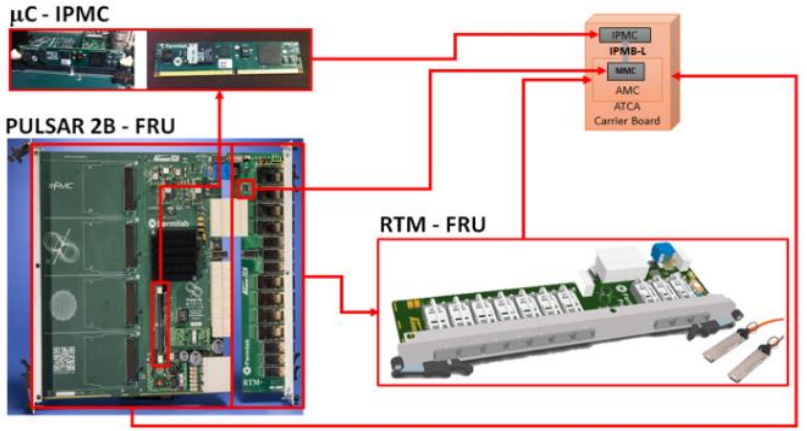
Xilinx Virtex 7 FPGA
- XC7VX690T-FFG1927-2

Up to 80 GTH transceivers
- 40 for RTM
- 28 for Backplane
- 12 for Mezzanines



Four FMC Slots
- Up to 35W each
- LVDS up to 34 Gbps unidirectional
- 3 X GTH up to 30 Gbps bidirectional

Board Management
- IPMC Microcontroller – IPMI protocol
  - ATCA Standard communication w/ Shelf Manager
- TCP/IP Services
  - XVC - FPGA remote programming/debugging



SPRACE Instrumentation Contributions

SPRACE Implementation – FNAL ATCA Infrastructure*

IPMI

- Management & Control of the ATCA boards
- Cooling Control
- Energy Management
- Hot Swap Operations

DONE

XVC

- Service for FPGA remote access
- Development/debugging from distance

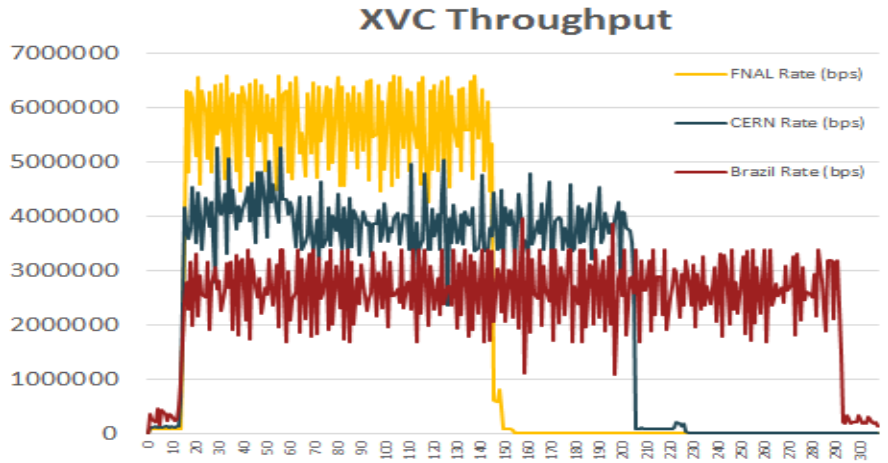
Rear cabling

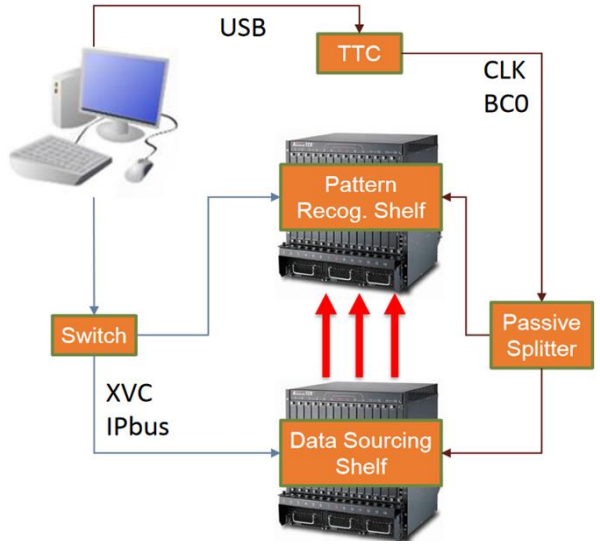
- 120 optical cables
- 480 channels @ 10 Gbps capability

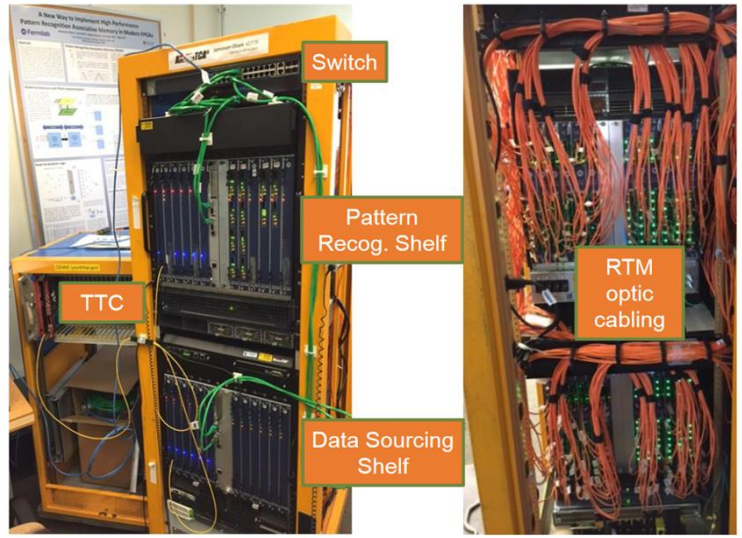
TTC synchronization

- Clock and Control Signals to all boards

*A similar, despite smaller, ATCA infrastructure is about to be implemented at SPRACE São Paulo







SPRACE Implementation – Data Sourcing System FPGA Designs

User Interface

- IPbus protocols compatible
- Control/Debugging operations
- W/R operations at DSM BRAM

Data Sourcing Modules (DSM)

- Emulates 40 detector sensor module
- 16 kB memory per module

Serial Link Bandwidth

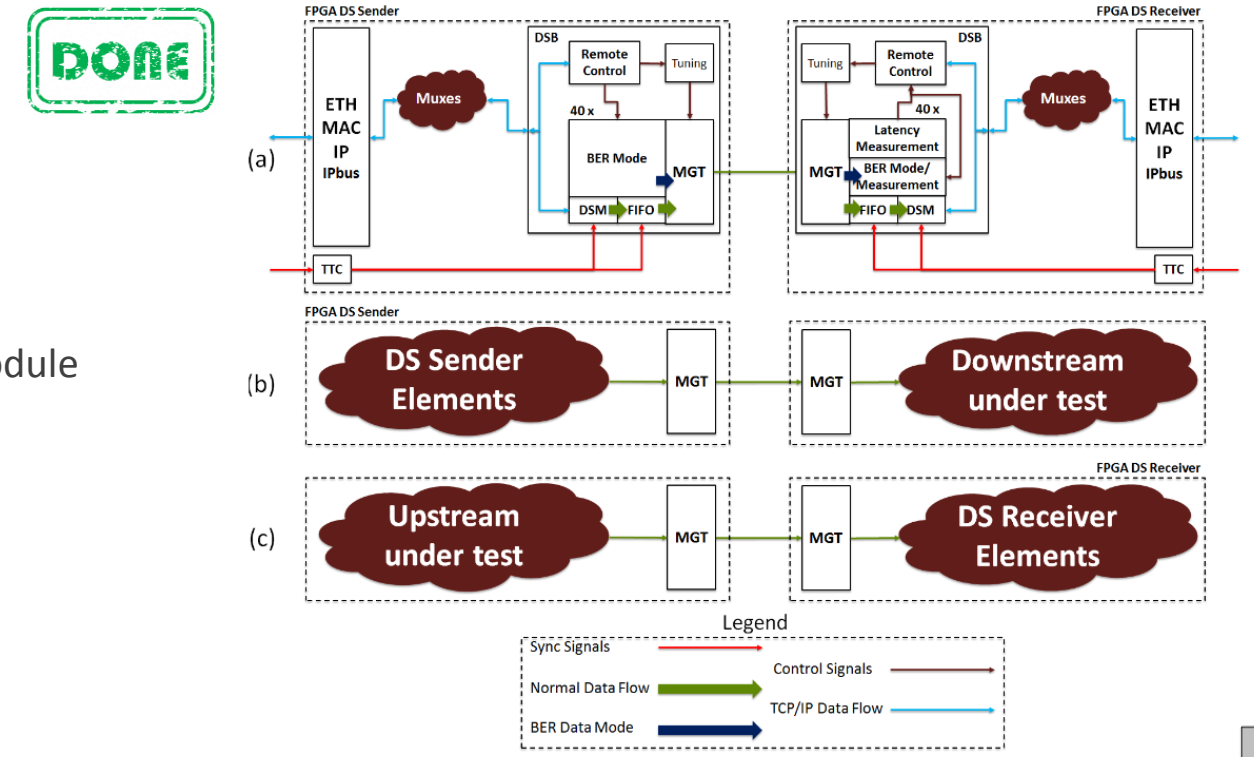
- 8 Gbps per module
- 320 Gbps per board
- 3.84 Tbps per ATCA Shelf

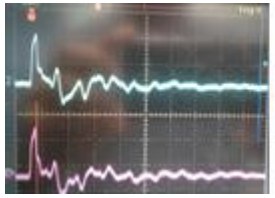
Synchronization

- TTC signals synchronize both Shelves

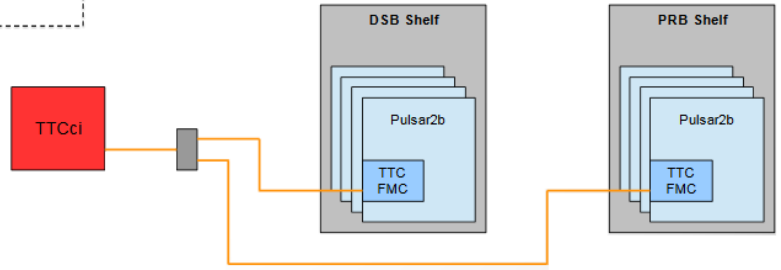
DSS: General purpose testing system

- ATCA BER, Latency, Synchronism measured





BC0 In both Shelves



SPRACE Implementation – High Speed Link Integrity

Auto Tuning System

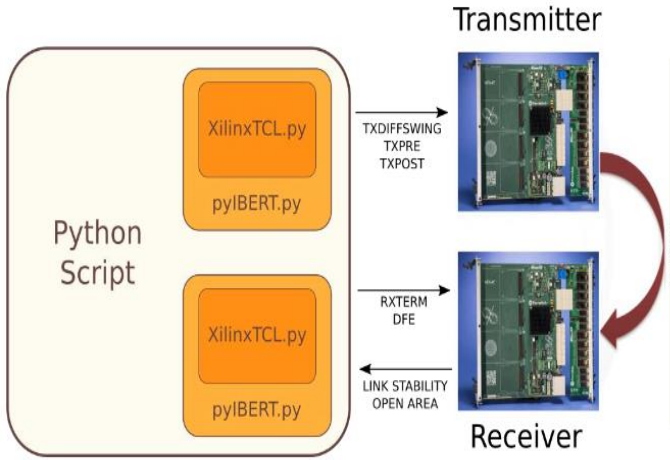
- Based on Python
- Handles with two Vivado Instances
- Debugs IBERT automatically

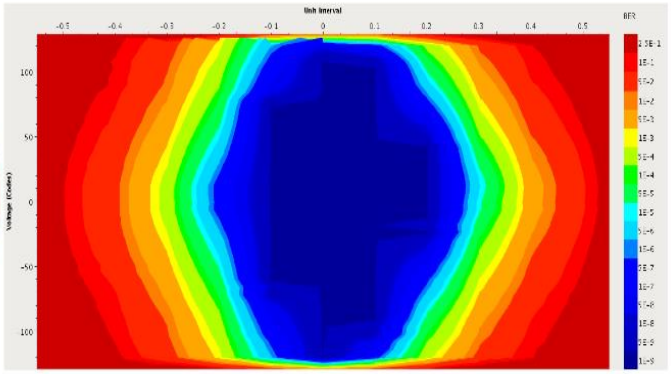
Auto Tuning Steps

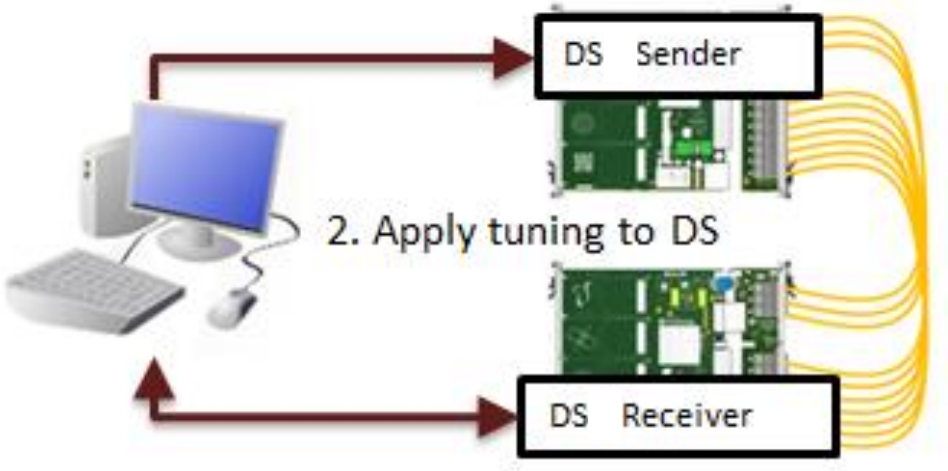
- Stress the channel with PRBS 31 (PRBS 7)
- Tests several tuning combinations
- The system checks the result at receiver side

After best settings for RTM Links

- 8 Gbps presents good reliability
- BER in the order of 1E-11 or less





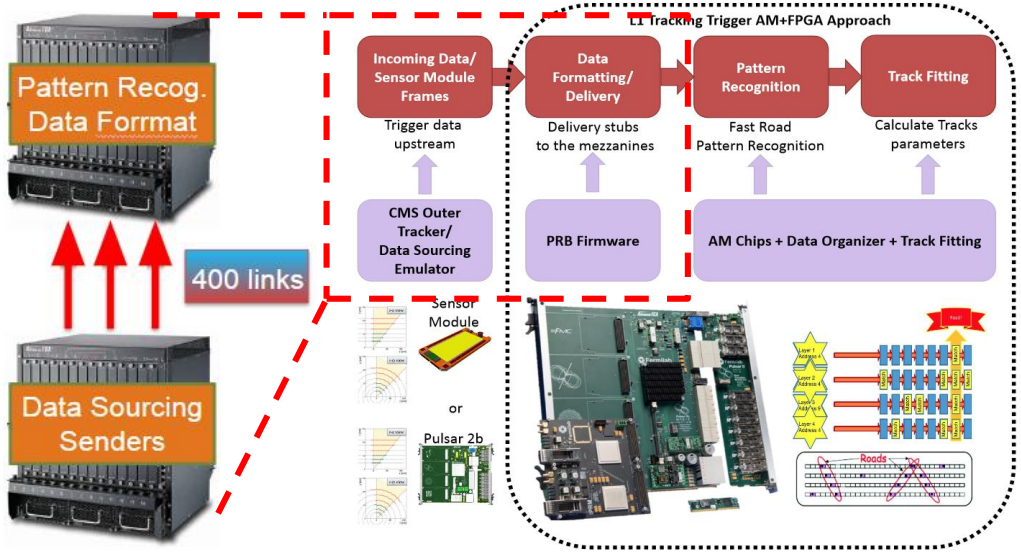


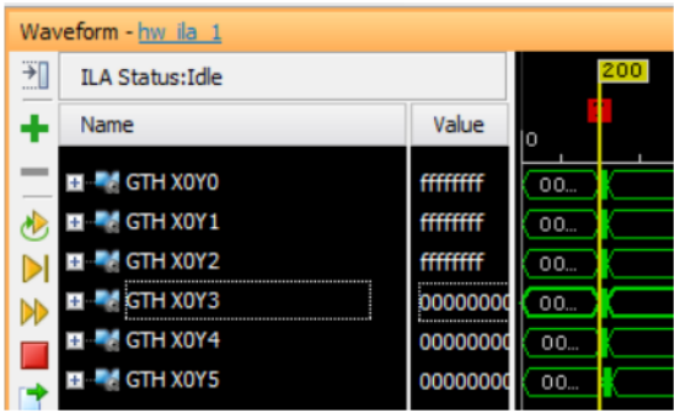
SPRACE Implementation – L1TT Integration

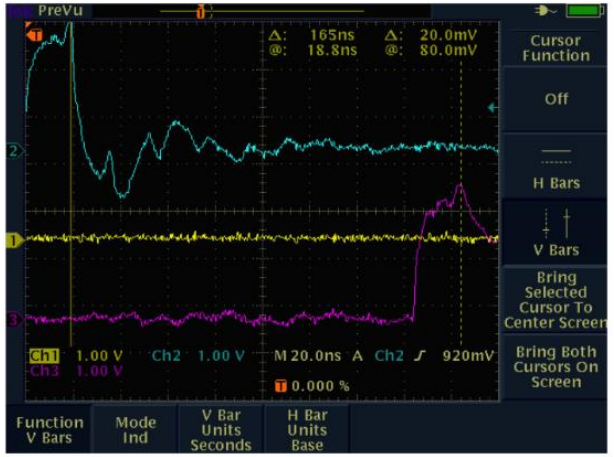
Integration Succeeded in Shelf Level

- Data Sourcing to Pattern Recognizer
- Measurement of the transmission latency
  - 170 ±8 ns @ 250 MHz and 8 Gbps
- Sent and received data perfectly match

AM+FPGA Collaboration used the Data Sourcing System as input data for L1TT system development







Summary

SPRACE instrumentation Milestones

- L1TT AM+FPGA demonstration requirements were reached!
  - AM+FPGA collaboration had used the ATCA infrastructure and the DSS for development and debugging purpose
  - Shelf Level Demonstration @ 8 Gbps was succeeded
  - DSS is user friendly to rearm and shoot again
  - Auto tuning system improved links performance

Ongoing Projects

- MGT Links
  - Increase reliability of the links in higher speed
  - Investigate clock schemes
  - Evaluate Clock Jitter
  - Tune Parameters
  - Power Supply
- SPRACE ATCA infrastructure is being implemented at São Paulo

Possible Future Improvements

- IPMI
  - New functionalities (IPMC)
  - Configurations for Shelf Manager
  - System Manager for IPMI sensors
- XVC
  - Multi-Node XVC – Multi-board per JTAG chain
- Implement/Test New Serial Links Protocols
  - Codification, Clock Correction, Synchronism
- IPbus
  - GUI and Burst Mode
- DSS
  - Usage in order up/downstream scenarios
- ATCA
  - Design of a carrier board and/or mezzanine cards
- Machine Learning
  - Study of ML algorithms implementation in FPGAs

Thanks!

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SEE BACKUP SLIDES FOR MORE DETAILS.

Backup Slides

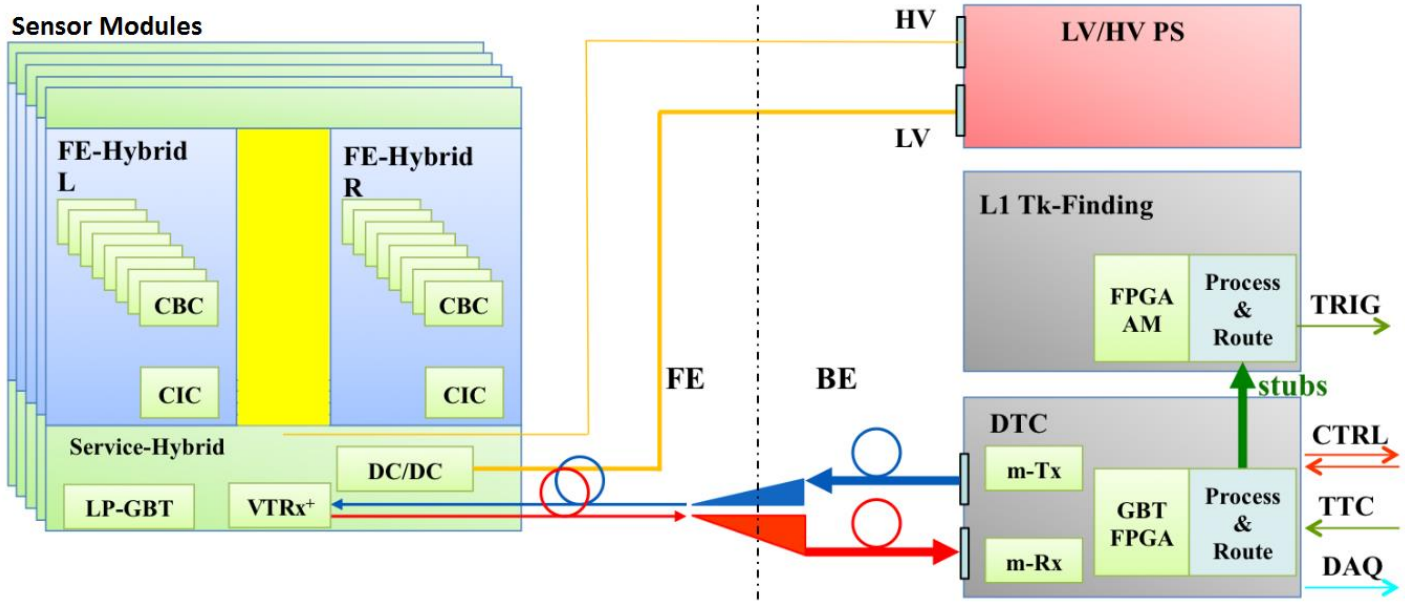
L1 Tracking Trigger Data flow

Front End (FE) Electronics

- CMS Binary Chips (CBC)
  - Converts hits to stub data
- Concentrator IC (CIC)
  - Provides a frame with 8 BX stubs
- Service Hybrid
  - Provides power payload and serial optical communication

Back End (BE) Electronics

- Data, Trigger and Control (DTC)
- L1 Track finding system
  - Receives data from the DTC
  - Processes with pattern recognition algorithms
  - Selects tracks of interest
  - Sends signal to Global Trigger Decision

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For CMS L1
Track Trigger
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Les deux infinis
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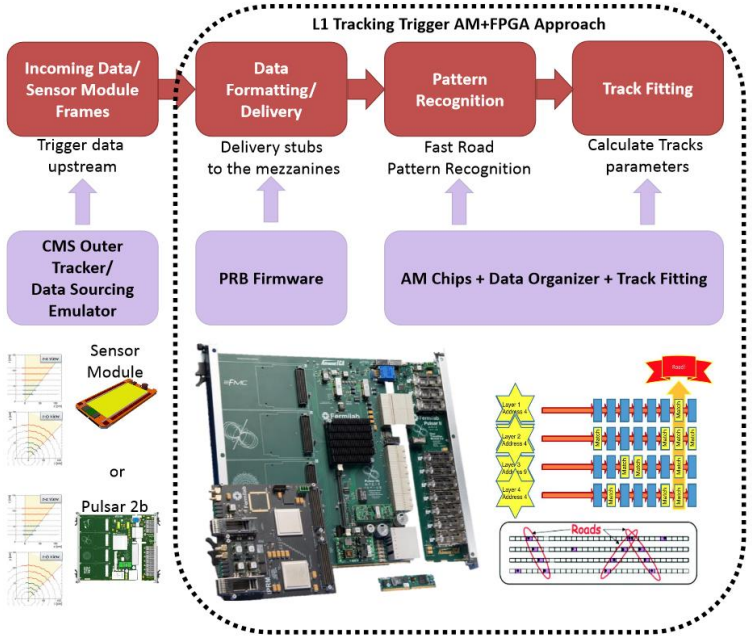
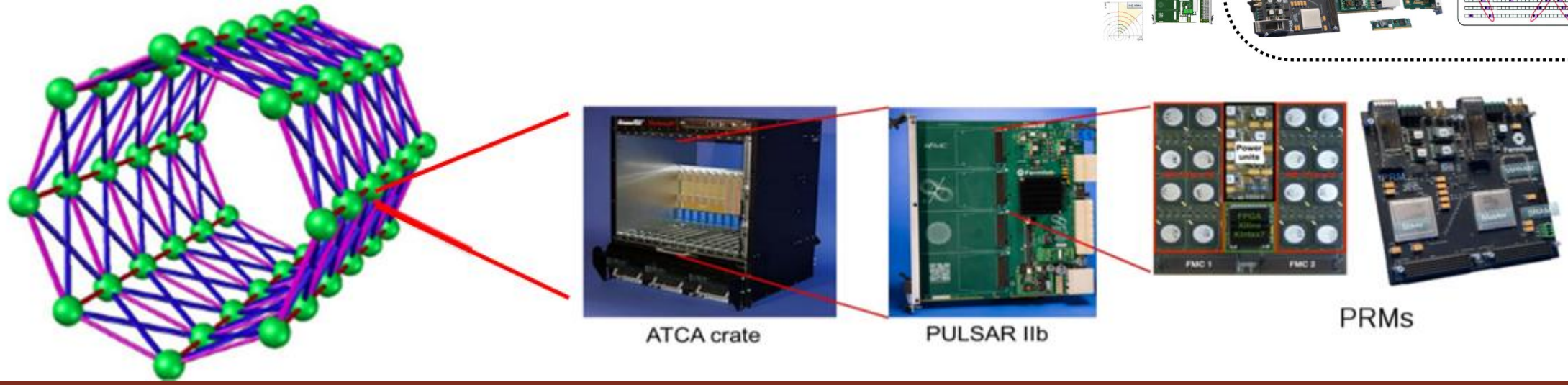
AM+FPGA Approach

- Divides the detector in 48 Vertical Slices – Trigger Towers
- Receives data from Trigger Tower in an ATCA Shelf
  - Pulsar 2b: a general purpose ATCA Board
  - Developed by FNAL R&D project
- Formats/shares data via high speed links in the backplane
- Associative Memory (AM) ASICs for pattern recognition

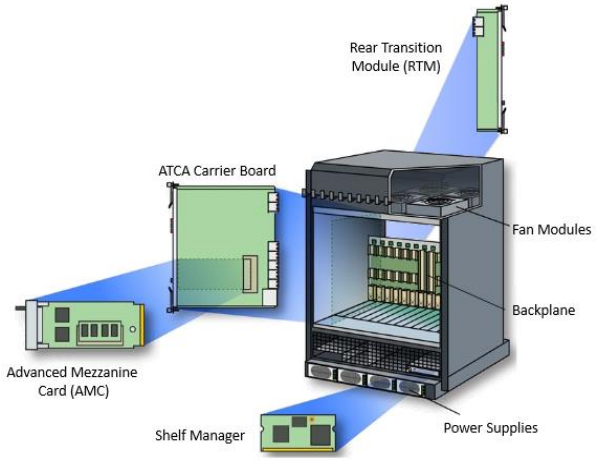




ATCA Backplane

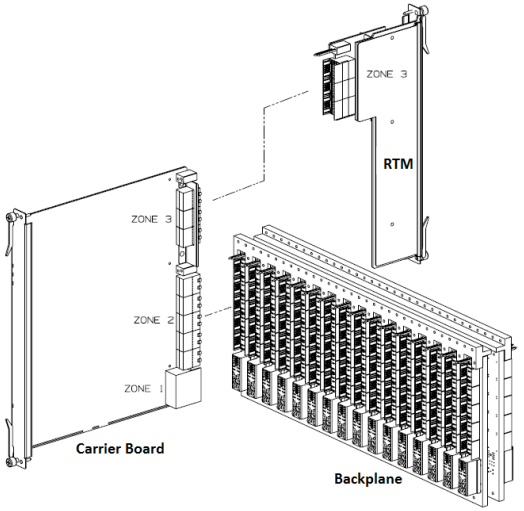
Advanced Telecommunication Computing Architecture (ATCA)

- Modular architecture
- Redundancy
- Hot-swap
- Self-controlling system
- Backplane distribution for high speed communication



Zone Connectors

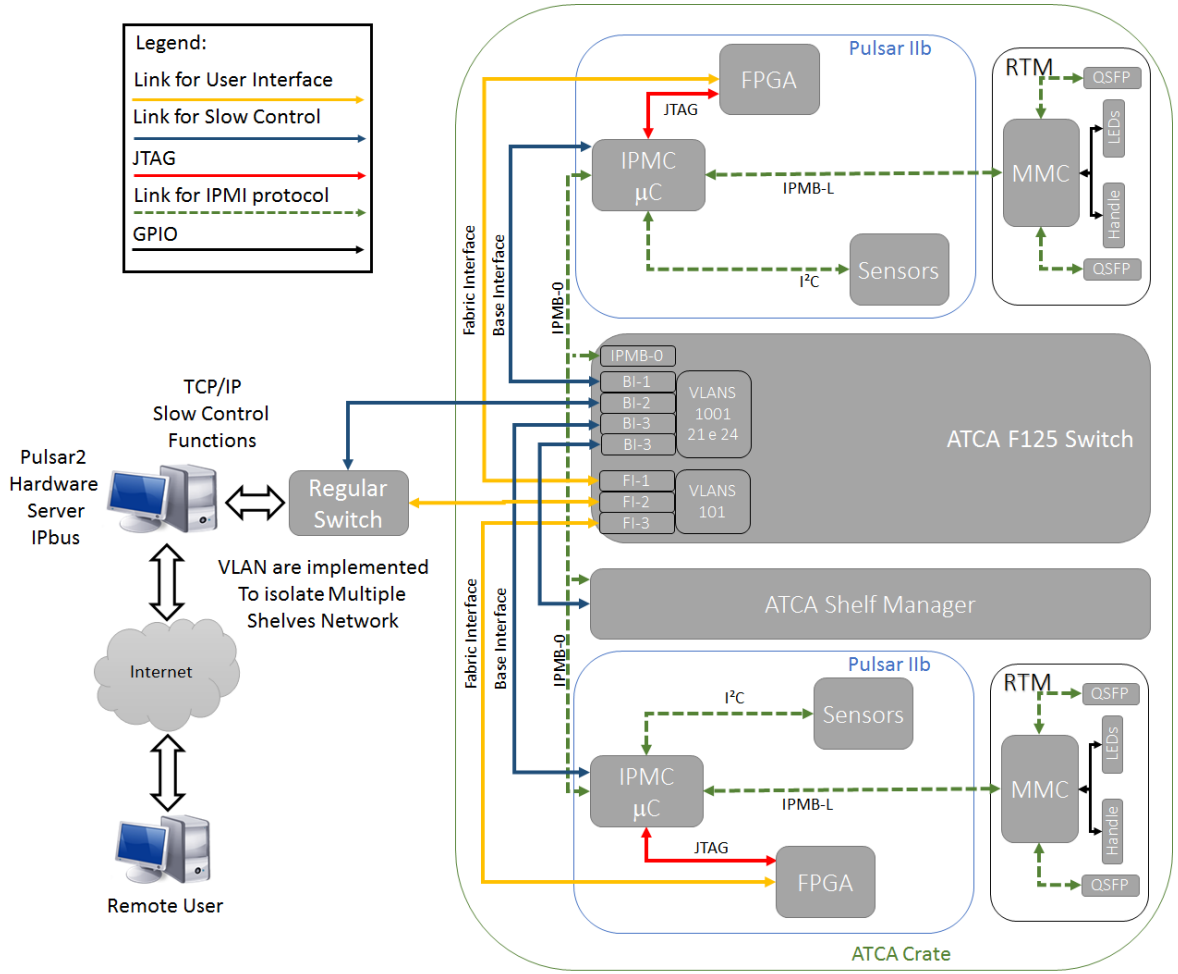
- Zone 1 - power supply and boards management through IPMI protocol. It contains the metallic test bus, the ringing generator bus, and low-level HPM signals
- Zone 2 - base interface, fabric interface and synchronization clock interface signals
  - Base interface – Dual star topology with the Switch physical slot and compatible with 0/100/1000BASE-T signaling
  - Fabric interface – Dual star or Full Mesh topology
- Zone 3 – Non-Standarized access to the Rear Transition Modules



ATCA Backplane@FNAL Implementation

ATCA Switch is the ATCA gateway for

- Fabric Interface Full Mesh
  - Communication between Pulsar 2b FPGAs
  - Serial Link protocols 10 Gbps
- Fabric Interface Dual Start
  - Communication between Switch and Pulsar 2b FPGA
  - Up to 10 Gbps TCP/IP communication
  - Main usage: User Interface protocols
  - Other TCP/IP protocols can also be used
- Base Interface
  - Communication between Switch and Pulsar 2b IPMC
  - TCP/IP 100 Mbps
  - Main usage: XVC for FPGA remote program/debug
  - Telnet, SSPI, FTP and other TCP/IP protocols
- Zone 1 IPMB-0 link
  - IPMI control signals between Pulsar 2b IPMCs and Shelf Manager
- Other links: JTAG, IPMB-L, GPIO, I²C
  - Board Standalone usage usage



XVC

XVC is an internet-based protocol that acts like a JTAG cable

- Debug and programming via Vivado hardware manager

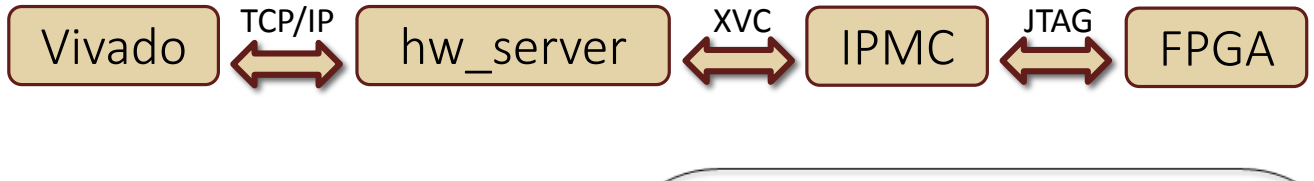
The implemented XVC Service has

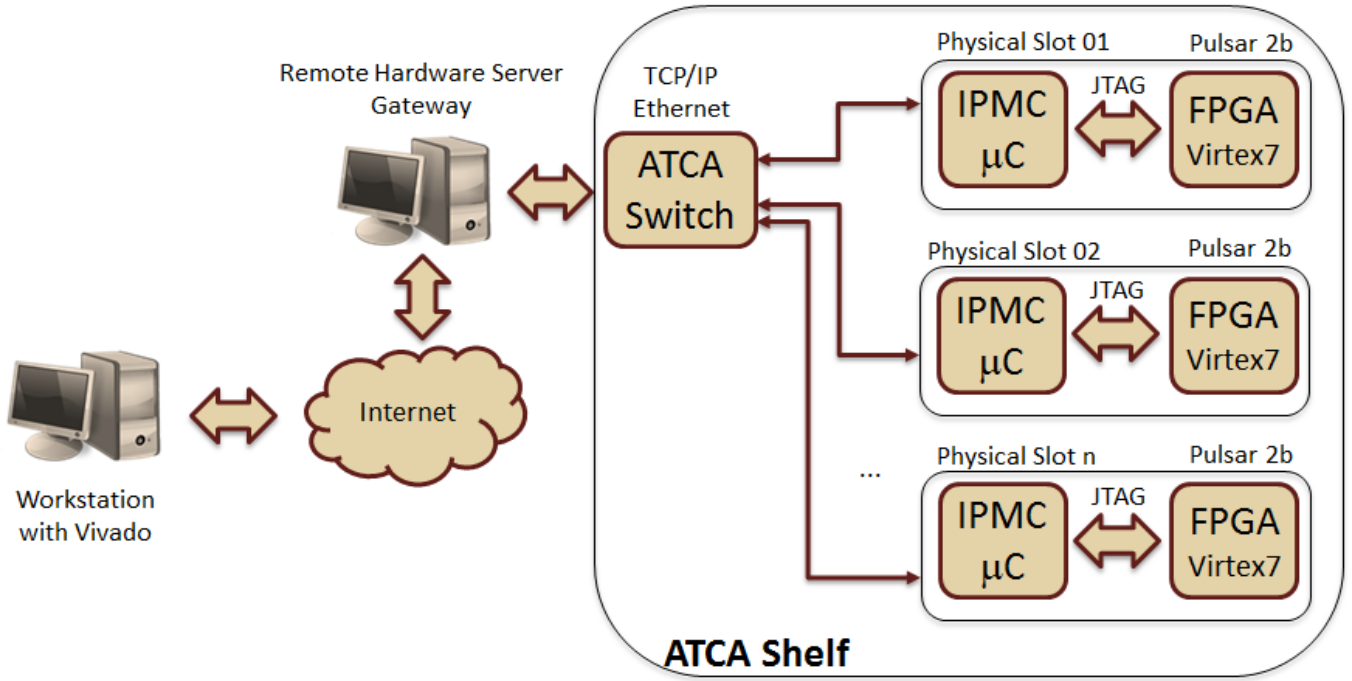
- Reliability - It has the same result as conventional JTAG program cable
- Mobility
  - The User can remotely connect the FPGAs in ATCA Shelf
  - No USB JTAG programming cable is needed anymore
- Scalability
  - The simultaneous FPGA program do not interfere each other
- Speed
  - Performance depends on

    XVC User computer performance

    XVC User internet connection

    FPGA image size





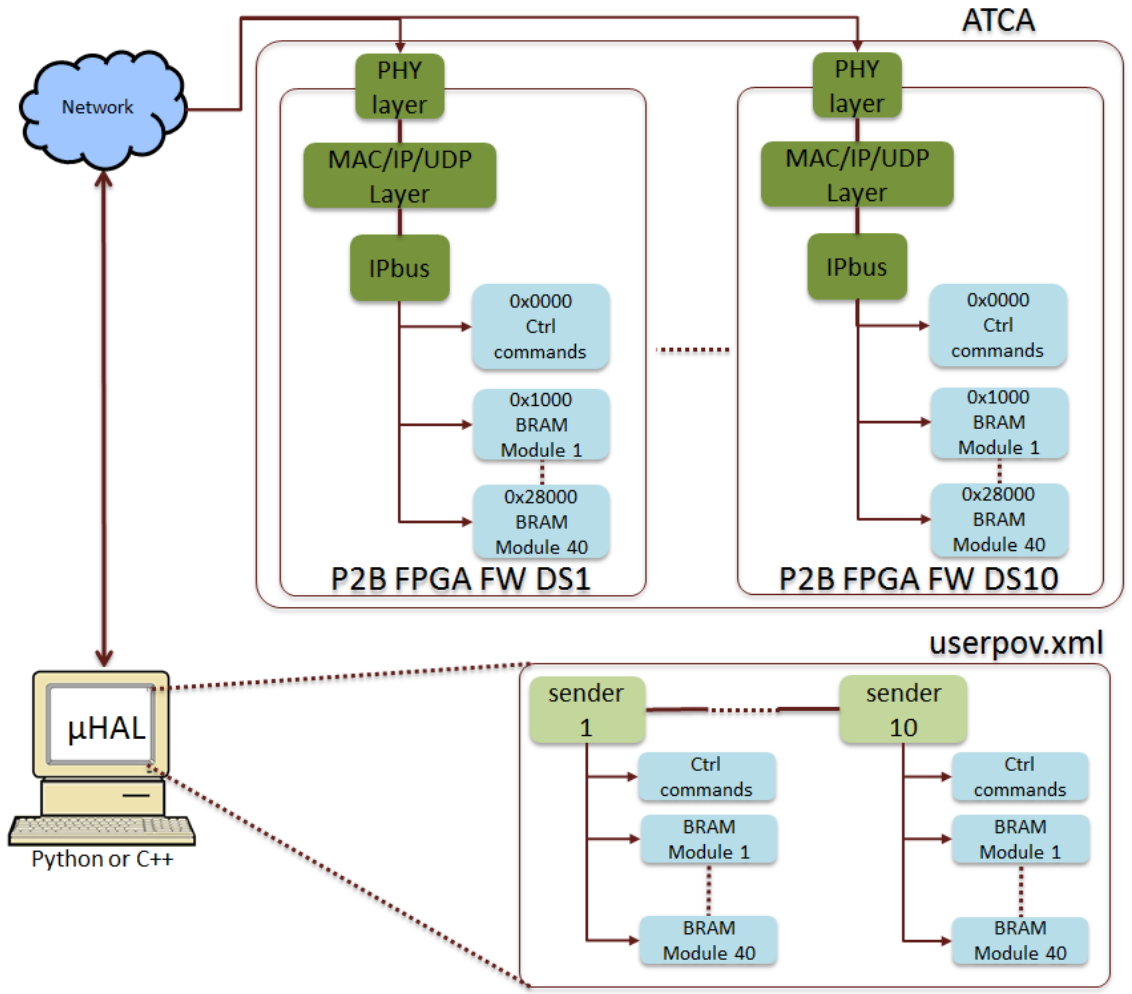
IPbus

µHal (Hardware Access Library) Library with connections.xml

- µHal provides a Python/C++ API to control the interface bus implemented in the FPGA
  - Allows W/R operations in the hardware through a PC via standard network links
- The XML file makes the addressing be transparent to the user point of view
  - It can scale to several FPGAs control in several different boards in the ATCA Shelf

Data Sourcing FW with IPbus

- Offers a generic interface bus flexible enough to be used according to the project requirements
- Implements a UDP server and translates its messages, providing data transactions to user-defined modules attached to that bus
- In case of DS the system provides
  - An VHDL entity logic for control commands management – up to 4096 addresses available
  - 4096 x 32 bits BRAM for each Sensor Module emulated and each GTH Channel



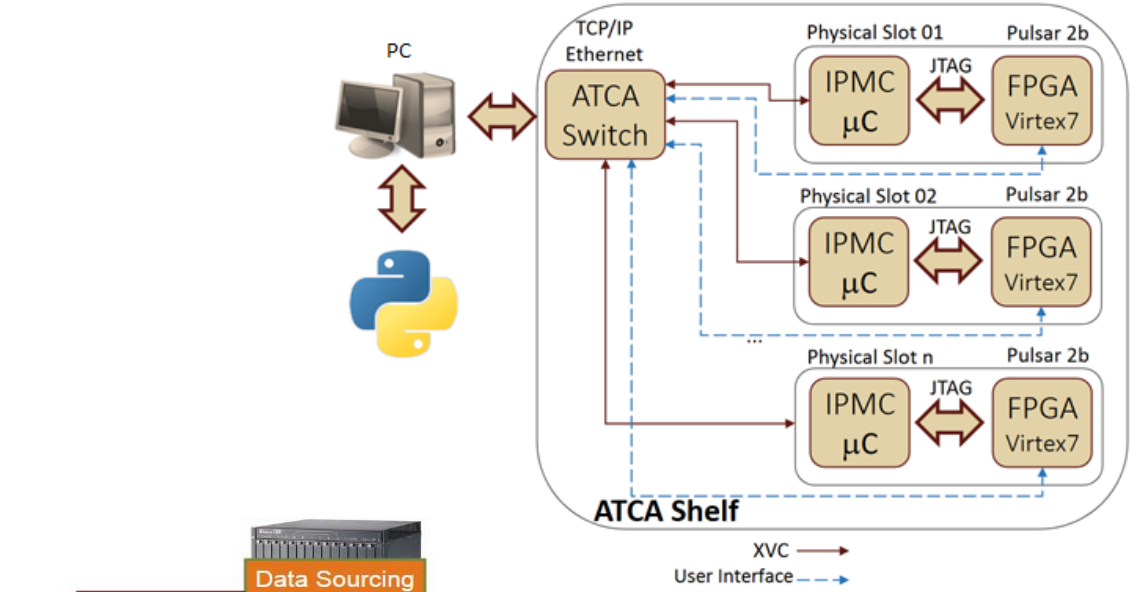
User Interface Commands

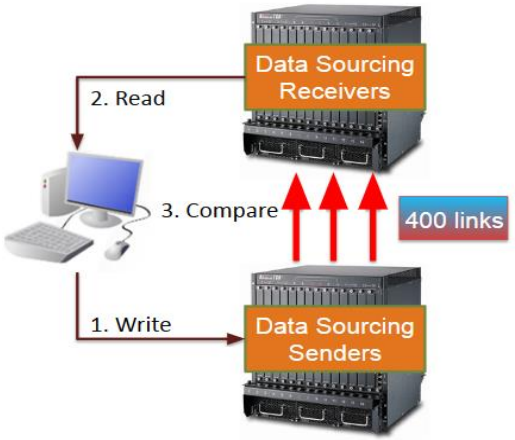
Basic Functions

- Compatible with OEI and IPBus
  - Protocols that provide PC access to FPGA Memory Blocks
- Python interface
  - Can write Real Data Sample at Sender in the IP chosen
  - Can Read and Compare Real Data Samples in the IP chosen

Advanced Functions

- Python Interface
  - Can change IP/MAC Address
  - Reset/Rearm Signals
  - Serial Link Latency Measurements
  - BER measurements
  - Remote online tuning

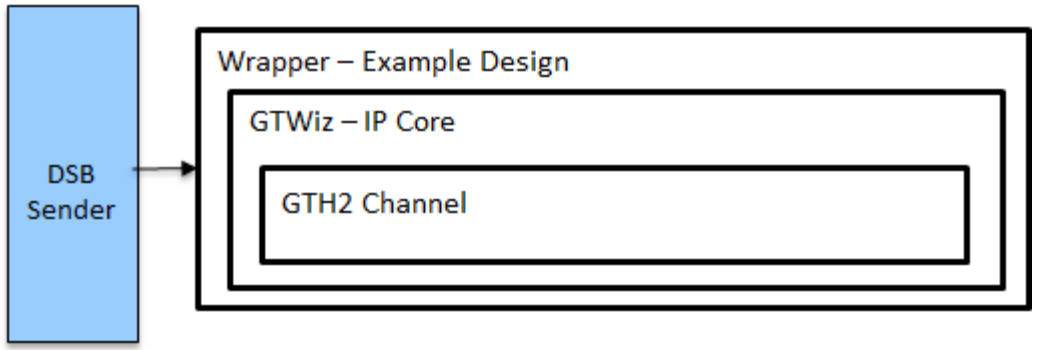


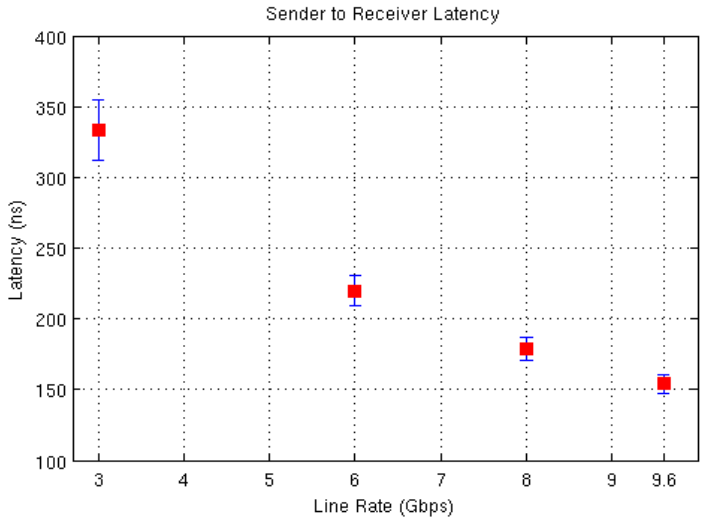


Serial Link Protocol – GT Wizard Aurora 64b66b

64b66b encoding

- 3.125% overhead between data rate and line rate
  - i.e 7.75 Gbps data rate => 8 Gbps line rate
- Data input/output is controlled by the Gearbox
  - Considering 64 bits per clock cycle
  - 32 clock cycles with valid data I/O
  - 1 clock cycle with a pause
  - Pauses are different between GT in the same FPGA
- Clock frequency depends of speed rate, oscillator available and PLL capabilities
- Latency is linear related to the speed rate
  - Jitter depends on the GearBox pauses





SPRACE Implementation – High Speed Link Integrity

Links @ 10 Gbps using PRBS31

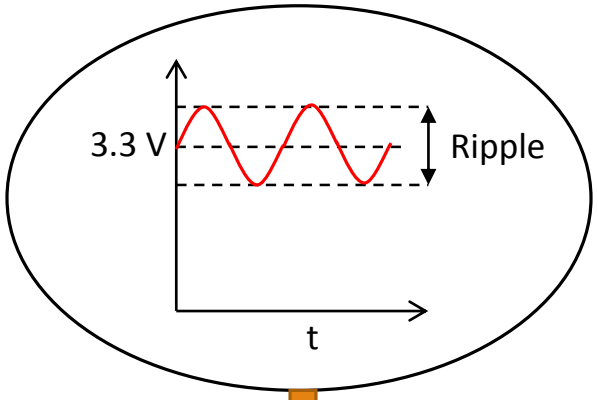
- KC705 board, GTX transceivers
- Links performance (BER ≈ 10^{-8})
- Similar performance found at Pulsar 2b

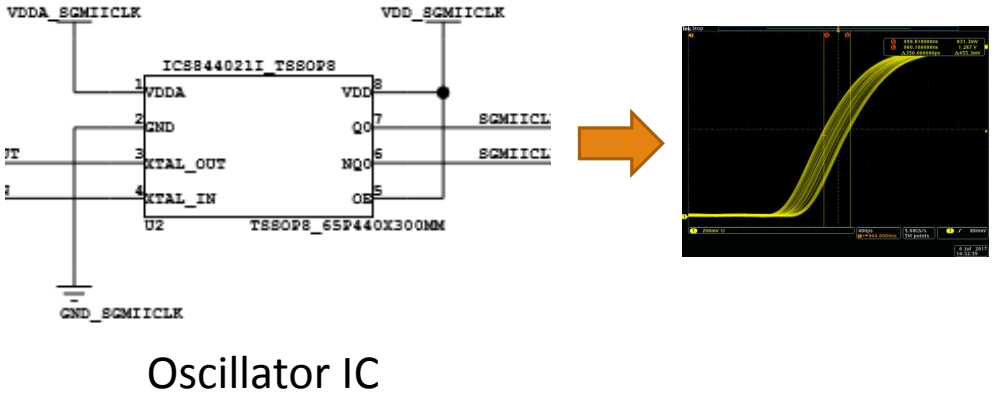
Clock Jitter on MGTREFCLK

- The transceiver clock had unexpected jitter
  - Causes link performance decrease

Studies performed find out that

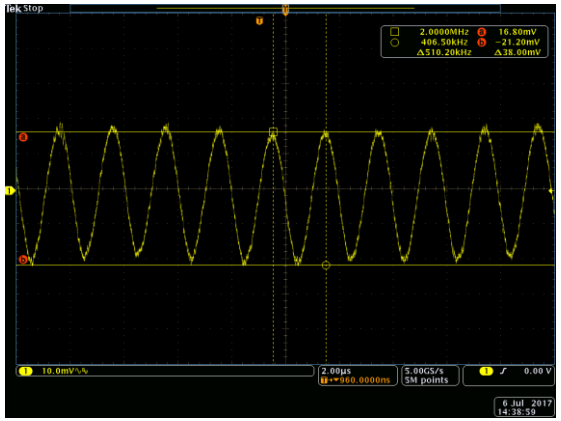
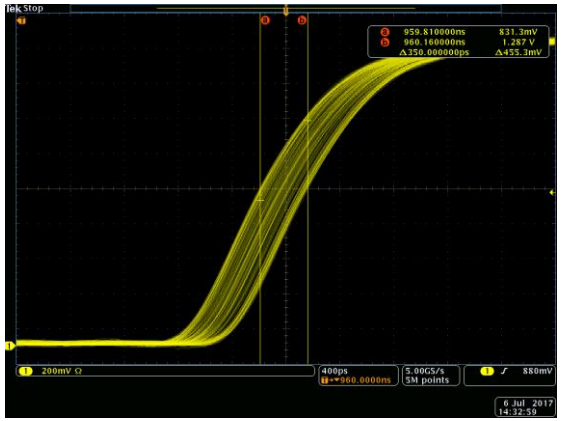
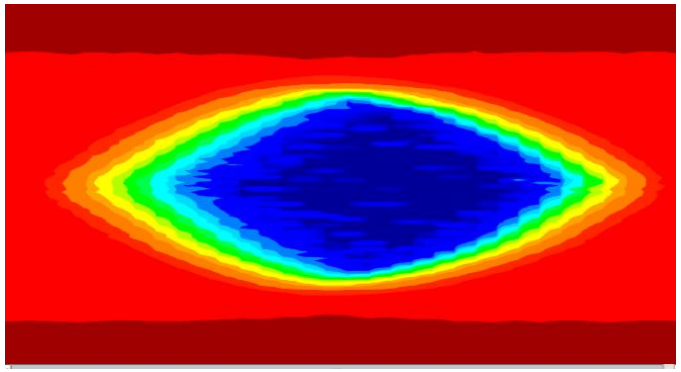
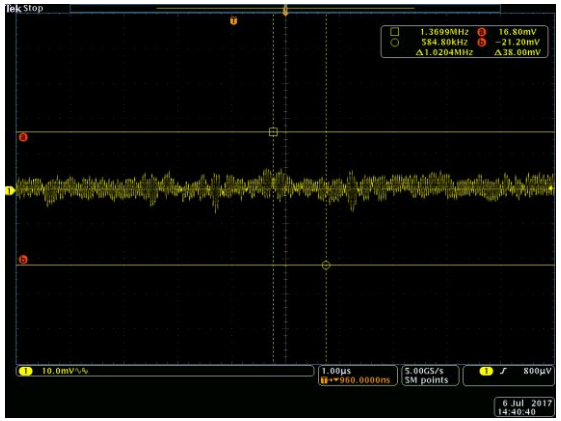
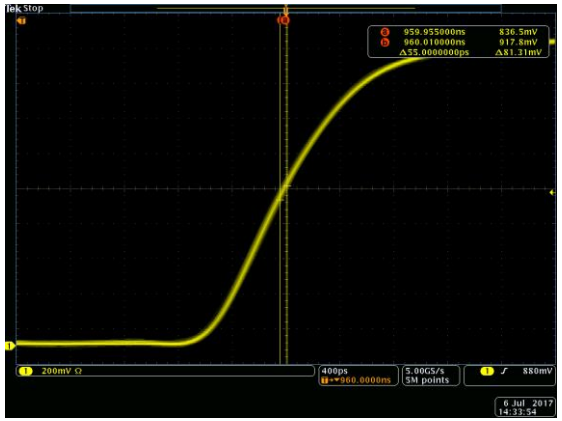
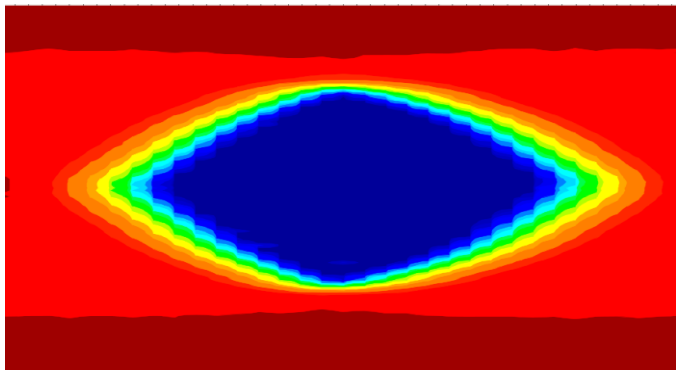
- The clock jitter have great influence of the power supplies



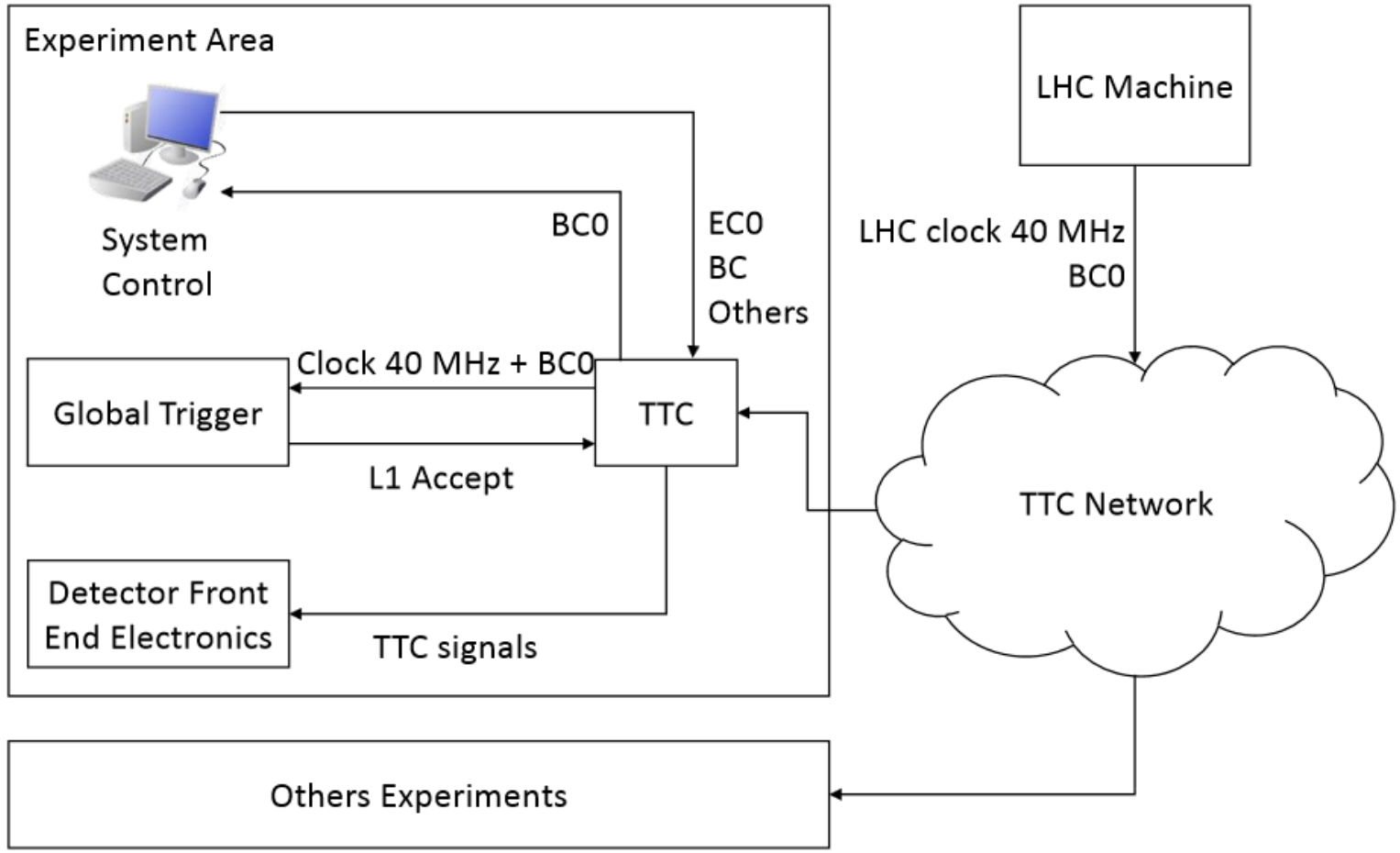


Oscillator IC

SPRACE Implementation – High Speed Link Integrity

	Supply Noise	Jitter	Eye Scan
"Dirty" Supply			 **BER ≈ 10^{-8}**
"Clean" Supply			 **BER < 10^{-14}**

LHC CMS TTC network



Synchronization by CERN TTCci system

TTC USB to VME Board

- Translates communication between TTC VME Board and PC

TTC VME Board

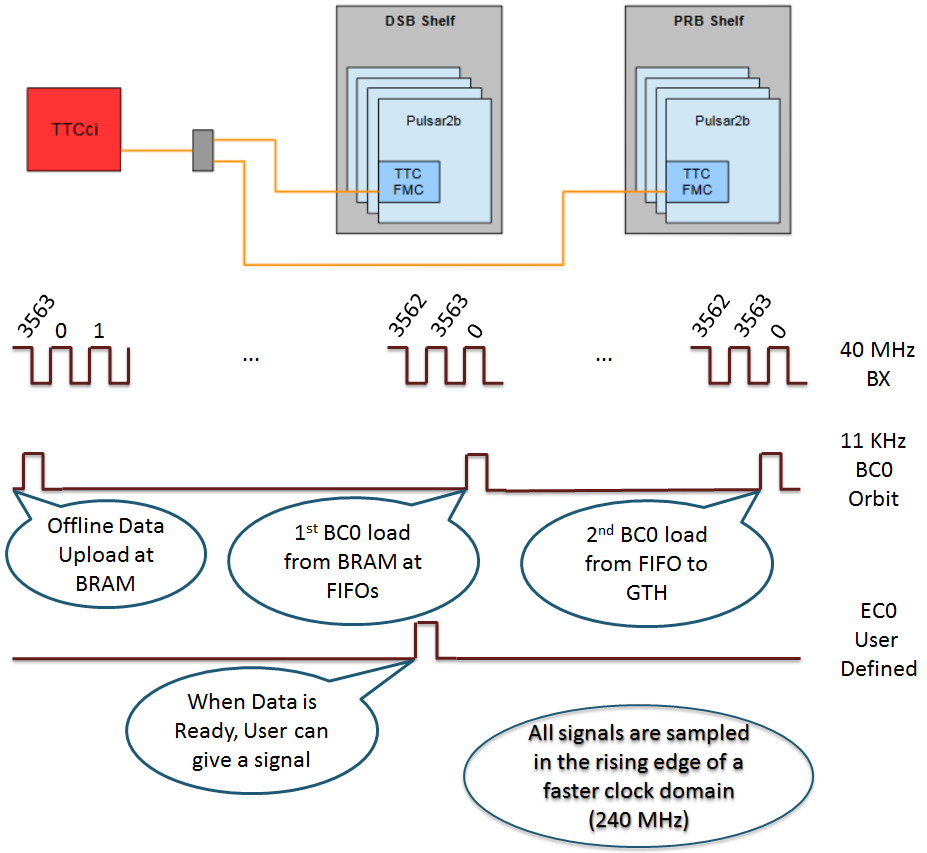
- Can generate internal signal or use external signals as reference
  - LHC Sync system i.e
- An optical cable sends the signals needed
  - Common Clock Reference for the FPGA logic
  - Bunch Crossing Zero Flag (11 KHz)
  - Event Counter Zero Flag (User Defined)

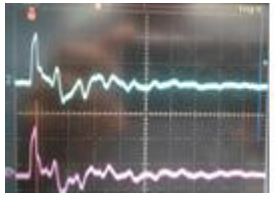
TTC FMC Card

- Receives optical signals and sends via LVDS in FMC to Pulsar 2b Virtex 7

Pulsar 2b with the TTC FMC is the sync master

- Replicate the signals through the backplane to the other slave Pulsar 2b boards



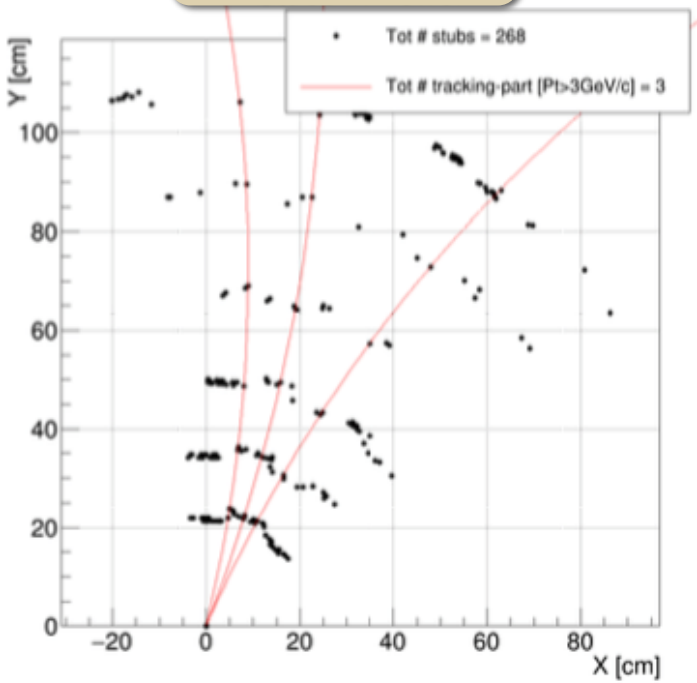


BC0 In both Shelves

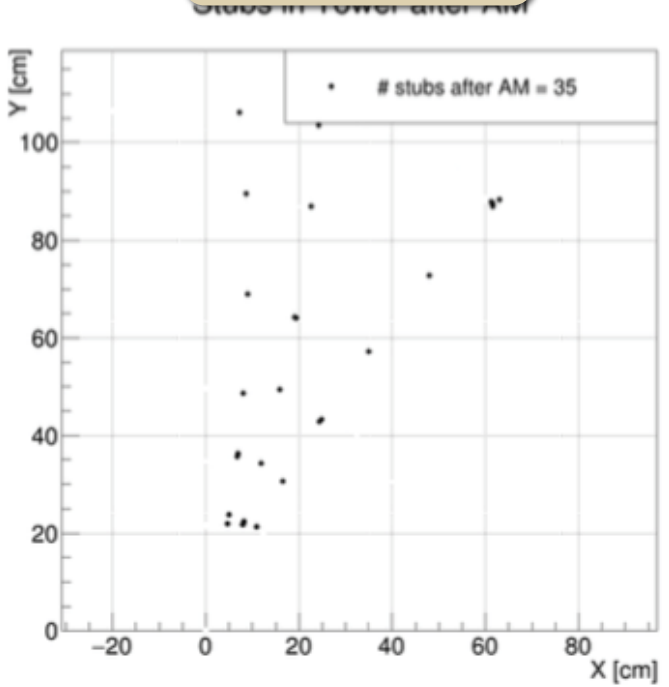
Simulation Contributions

AM+FPGA Simulation

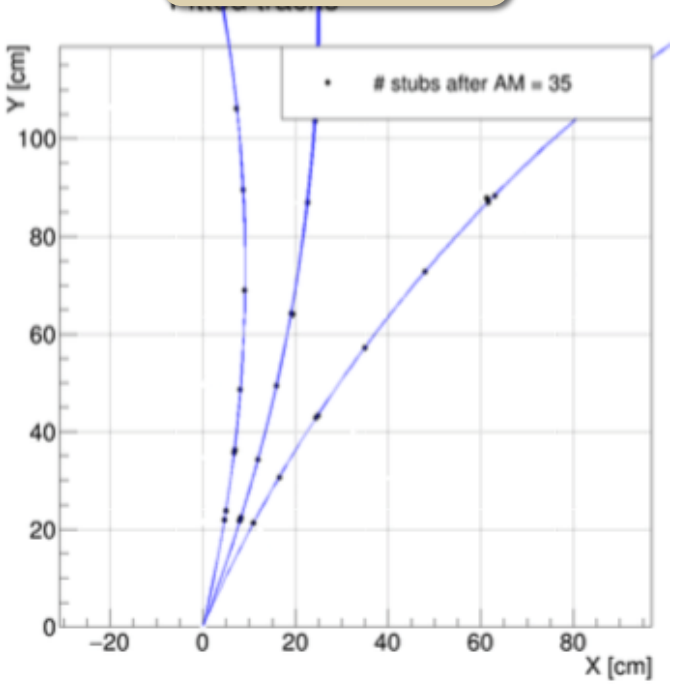
Hits → Roads → Tracks



- 1 event with ~140 interactions
- 3 ”true” tracks (high-energy)
- 268 hits in this region



- After Pattern Recognition (AM)
- 35 hits in this region



- Hits @ FPGA
- 3 tracks found
- Same tracks as the generated

Simulation Studies: High-Energy Jets

Jets = sets of collimated high-energy tracks

High-energy jets (E_T > 100 GeV) very frequently produced in LHC

- One order of magnitude more hits combinations for track fitting
  - 95% CI → 5% bigger values
- What is the impact of these events in terms of trigger latency?