CMS Experiment at the LHC, CERN Data recorded: 2016-Sep-08 08:30:28.497920 GMT Run / Event / LS: 280327 / 55711771 / 67

 $\begin{array}{c|c} \mbox{Anti-}k_{\rm T} \ {\rm R=}0.8 \ {\rm jet} \\ \hline p_{\rm T} & 1374 \ {\rm GeV} \\ \eta & 0.79 \\ \phi & 0.43 \\ M_{\rm SD} & 94.8 \\ \hline \tau_{21} & 0.29 \end{array}$

CMS Experiment at LHC, CERN Data recorded: Mon Jul 18 19:59:10 2016 CEST Run/Event: 276950 / 1080730125 Lumi section: 573

CMS

CMS Experiment at LHC, CERN Data recorded: Mon Jul 18 19:59:10 2016 CEST Run/Event: 276950 / 1080730125 Lumi section: 573

Particle flow and PUPPI @ L1 for CMS at HL-LHC

Can we trigger on boosted jets at 25ns?

Jennifer Ngadiuba (CERN)

on behalf of the CMS Collaboration

BOOST 2018 July 16 - 20 Campus de Jussieu, Paris



The challenge: triggering at (HL-)LHC

Squeeze the beams to increase data rates → multiple pp collisions per bunch crossing (pileup)

2016: <PU> ~ 20-50 2017 + Run 3: <PU> ~ 50-80 HL-LHC: 140-200

CHALLENGE: maintain physics in increasingly complex collision environment

→ <u>untriggered events lost forever!</u>

Sophisticated techniques needed to preserve the physics!

Particle flow and PUPPI THIS TALK!

Machine learning (see talk on Thursday)

ennifer Ngadiuba - Particle flow and PUPPI @ L1 for HL-LHC

Particle flow

Efficient combination of complementary detector subsystems Reconstruct and identify individually all particles Improves any single system energy/spatial resolution

JINST 12 (2017) P10003

Key ingredients: efficient track reconstruction for charged particles and fine granularity calorimeter



muons, electrons, photons, neutral hadrons, charged hadrons

Particle flow

Widely used in offline and HLT event reconstruction since LHC Run 1

Particle flow physics performance impact

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Improved jet p_T resolution

Improved missing p_T resolution

PUPPI

Particle flow: reconstructs all particles, also from PU interactions

PileUp Per Particle Identification (PUPPI):

an algorithm that determines, per particle, a weight for **how likely** a particle is from PU **key insight:** using QCD ansatz to infer neutral pileup contribution

- Define a local discriminant, α, between PU and LV (leading vertex)
- 2. Get data driven α distribution for PU using charged PU tracks

$$\alpha_i^C = \log \left[\sum_{j \in Ch, LV} \frac{p_{T,j}}{\Delta R_{ij}} \Theta(R_0 - \Delta R_{ij}) \right]$$



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- Define a local discriminant, α, between PU and LV (leading vertex)
- Get data driven α distribution for PU using charged PU tracks
- For the neutrals, ask "how un-PU-like is α for this particle?", compute a weight
- Reweight the 4-vector of the particle by this weight, then proceed to interpret the event as usual

$$\alpha_i^C = \log\left[\sum_{j \in Ch, LV} \frac{p_{T,j}}{\Delta R_{ij}} \Theta(R_0 - \Delta R_{ij})\right]$$



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PUPPI

Large gain with PUPPI, especially at high pile-up

Jet p_T and missing p_T resolution Fake jet rate Jet substructure Lepton isolation

Efficiency 1.4 1.2

0.8

0.6

0.4

0.2

0

0

arxiv.1407.6013 (original), LHCC-P-008 (CMS Phase-2 upgrade), JME-14-001, JME-16-003, JME-16-004 many CMS physics analyses...



Results from BOOST17, see new results in A. Benecke's talk on Tuesday

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The CMS trigger system

Triggering typically performed in multiple stages



Trigger decision to be made in O(µs) Latencies require all-FPGA design

Computing farm for detailed analysis of the full event Latency O(100 ms)

For HL-LHC upgrade: latency and output rates will increase by ~ 3 (from 3.8 \rightarrow 12.5 µs @ L1)

Upgraded CMS trigger for HL-LHC



Upgraded CMS trigger for HL-LHC

Addition of **tracks** to L1 trigger is a game-changer Re-think algorithms: how to best combine *tracking, calorimeter, and muon information* The big challenge: mitigation of **pileup**



PF algorithm @ L1



PF algorithm @ L1



- Clusters with no associated tracks \rightarrow photon
- If $p_T^{cluster} \ge \sum p_T^{track}$ within uncertainties \rightarrow electron
- If $p_T^{cluster} >> \sum p_T^{track} \rightarrow electron+photon$

PF algorithm @ L1



PF+PUPPI algorithm @ L1



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Performance for MET and jets

Gains in rate reduction, H_T and p_T^{miss} resolution, signal efficiency, lower threshold



For a fixed L1 accept rate of 20 kHz: lower threshold and sharper turn-on

Missing p_⊤: better trade-off between L1 rate and signal efficiency

LHCC-2017-009

What are FPGAs?

Latencies at L1 trigger require all-FPGA design

Field Programmable Gate Arrays are reprogrammable integrated circuits

Contain array of **logic cells** embedded with **DSPs**, **BRAMs**, etc.

High speed input/output to handle the large bandwith

Support highly parallel algorithm implementations

Low power (relative to CPU/GPU)



FPGA diagram



Digital Signal Processors (DSPs): logic units used for multiplications

Random-access memories (RAMs): embedded memory elements

Flip-flops (FF) and look up tables (LUTs) for additions

How are FPGAs programmed?

Latencies at L1 trigger require all-FPGA design

High Level Synthesis is used to compile the algorithms into a firmware block (IP core)

generate standard register-transfer level (RTL) code for FPGA from more common C/C++ code

pre-processor directives and constraints used to optimize the timing

firmware for PF developed in 2-3 months, only physicists

We use Xilinx Vivado HLS

Main reference: https:// www.xilinx.com/support/ documentation/sw_manuals/ xilinx2014_1/ug902-vivado-highlevel-synthesis.pdf





FPGA diagram



Digital Signal Processors (DSPs): logic units used for multiplications

Random-access memories (RAMs): embedded memory elements

Flip-flops (FF) and look up tables (LUTs) for additions

Firmware implementation

- To best profit from FPGA capabilities:
 - use integers instead of floating-point
 - keep the mathematics simple
- Expolit parallelism to guarantee latency
 - the algo is **pipelined** to accept new inputs every 1 or 2 clock cycles
 - combinatorical **loops**, e.g. on object pairs in the linking, are **unrolled** to compute all values in parallel



3 cycles

WR

CMP

Firmware implementation

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 - keep the mathematics simple
- Expolit parallelism to guarantee latency
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 - combinatorical **loops**, e.g. on object pairs in the linking, are **unrolled** to compute all values in parallel

Preliminary estimate from HLS

1 Xilinx Virtex Ultrascale+ (VUP9) 4 $\Delta \eta \times \Delta \phi = 0.6 \times 0.6$ regions 25 tracks + 20 clusters every BX ~ 40% resource usage 0.7 µs latency: 550 ns for PF, 150 ns for PUPPI

- The PF+PUPPI is inherently a regional algorithm → different detector regions can be processed independently and in parallel
 - complexity and FPGA resource use depend on the maximum allowed number of input objects, determined by the size of the detector region

Hardware demonstration

A proof-of-concept implementation running on current and early prototype trigger boards

based on Xilinx Virtex-7 FPGAs, VU9P with development kit and on Amazon AWS

Interface the core with the board infrastructure using IPbus or AXI-PCIe to **inject input patterns** from CMS detector simulation into the core, and **the output is checked for bitwise identity** with the expections from HLS.





Summary and outlook

Bringing advanced physics algorithms to the hardware trigger!

Proof-of-concept for **PF+PUPPI running at L1** Large physics gain: H_T , missing p_T , jet, lepton isolation



How about machine learning?

Many new ML algorithms developed for offline boosted-jet tagging using only kinematics of **particle candidates as input**, few examples:

Lola (G. Kasieczka et al. JHEP05(2017)006) \rightarrow fully connected layers DeepAK8 and double b-tagger (<u>CMS-DP-2017-049</u>) \rightarrow one-dimensional convolutional layers





NN inference of such models possible on FPGA in L1 latency (see talk on Thursday)

DeepJet for boosted resonances



See L. Gouskos's talk on Wednesday

Towards FPGA-friendly jet algos

Energy flow polynomials: complete set of jet substructure observables forming a discrete linear basis for any common jet observables



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Towards FPGA-friendly jet algos

Anti-kT jet clustering algo preferred by theorists and good for offline reconstruction

sequential clustering not suitable for low latency on FPGA

Explore more FPGA friendly algos for L1 applications with use of PF/PUPPI candidates

Jets without jets: use local computation to characterize jet-like and subjet-like structures w/o jet clustering algo

$$\begin{split} \widetilde{N}_{j\text{et}}(p_{T\text{cut}},R) &= \sum_{i \in \text{event}} \frac{p_{Ti}}{p_{Ti,R}} \Theta(p_{Ti,R} - p_{T\text{cut}}), \\ \widetilde{H}_{T}(p_{T\text{cut}},R) &= \sum_{i \in \text{event}} p_{Ti} \Theta(p_{Ti,R} - p_{T\text{cut}}), \\ \widetilde{p}_{T}(p_{T\text{cut}},R) &= \left| \sum_{i \in \text{event}} \vec{p}_{Ti} \Theta(p_{Ti,R} - p_{T\text{cut}}) \right|, \end{split}$$

$$\widetilde{N}_{ ext{subjet}}(p_{T ext{subcut}}, R_{ ext{sub}}) = \sum_{i \in ext{jet}} rac{p_{Ti}}{p_{Ti, R_{ ext{sub}}}} \Theta(p_{Ti, R_{ ext{sub}}} - p_{T ext{subcut}}).$$

D. Bertolini et al., JHEP04(2014)013



Fast PUPPI

Proof-of-principle studies indicate the feasibility of performing Particle Flow reconstruction and PUPPI pileup mitigation in the CMS HL-LHC Level-1 Trigger

Significant physics performance improvements over traditional trigger algorithms

For the first time, possibility to trigger on boosted jets at 25 ns with large gain for physics!



Fast PUPPI

Backup

Implementation of Puppi proof-of-concept using High level synthesis (HLS) as well

COMPUTE FOR EACH NEUTRAL

Θ

[1] define a local discriminant, a, between pileup (PU) and leading vertex (LV)

$$\alpha_i^C = \log$$

 $i \in Ch.L$

$$(R_0-\Delta R_{ij})$$

[2] get data-driven a distribution for PU using charged PU tracks

[3] for the neutrals, ask "how un-PU-like is α for this particle?", compute a weight

[4] reweight the four-vector of the particle by this weight, then proceed to interpret the event as usual PRECOMPUTE STEP 2 OFFLINE WITH CONSTANTS (FOR GIVEN PILEUP LEVEL)

DO STEP 3/4 WITH A LOOK-UP TABLE

RESOURCE USAGE ONLY FEW % OF FPGA AND 100S OF NS LATENCY WITH LITTLE DEGRADATION IN PERFORMANCE

Input data size to the correlator

Input	Object	N bits/object	N objects	N bits/BX	Total BW (Gb/s)
Tracker	Track	100	900	90 000	3 600
Barrel Calo	Cluster	16	2 4 4 8	39 168	1 567
Barrel Calo	Tower	32	612	19 584	783
HF	Tower	10	1 4 4 0	14 440	553
Endcap Calo	Cluster	128	400	51 200	1 600
Endcap Calo	Tower	16	2 400	38 400	1 536
Barrel Muon	Track	64	36	2 3 0 4	92
Endcap Muon	Track	64	36	2 304	92
Total					8 547

Table 5.1: Summary of prototype logical input data to the CT.