Pixel readout chip for the HL-LHC

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on behalf of the RD53 Collaboration

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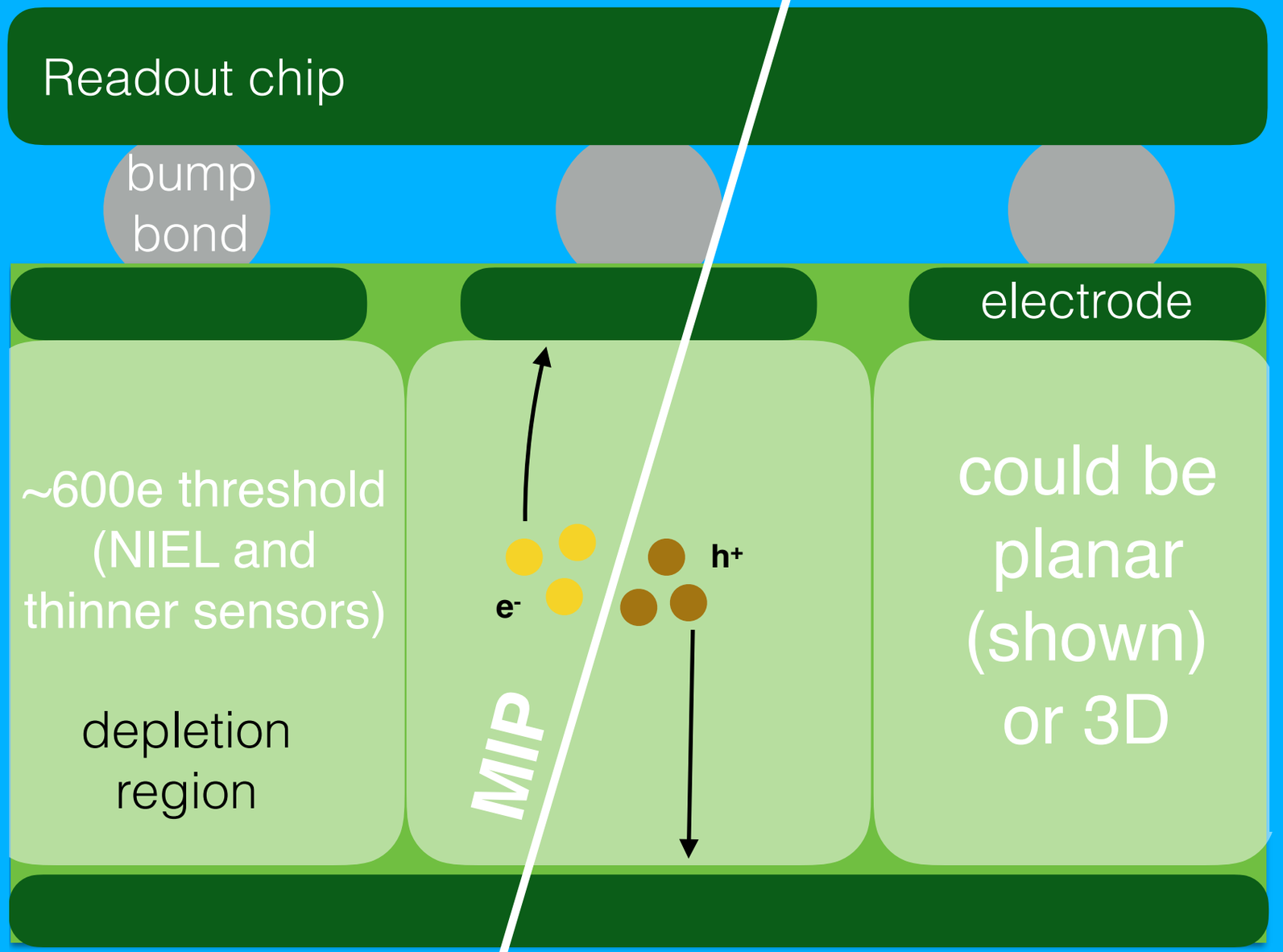
Outline: Introduction ⇢ Challenges of the HL-LHC
⇢ FE65P2 chip ⇢ Optimization studies

Pixel Module Specs for the HL-LHC

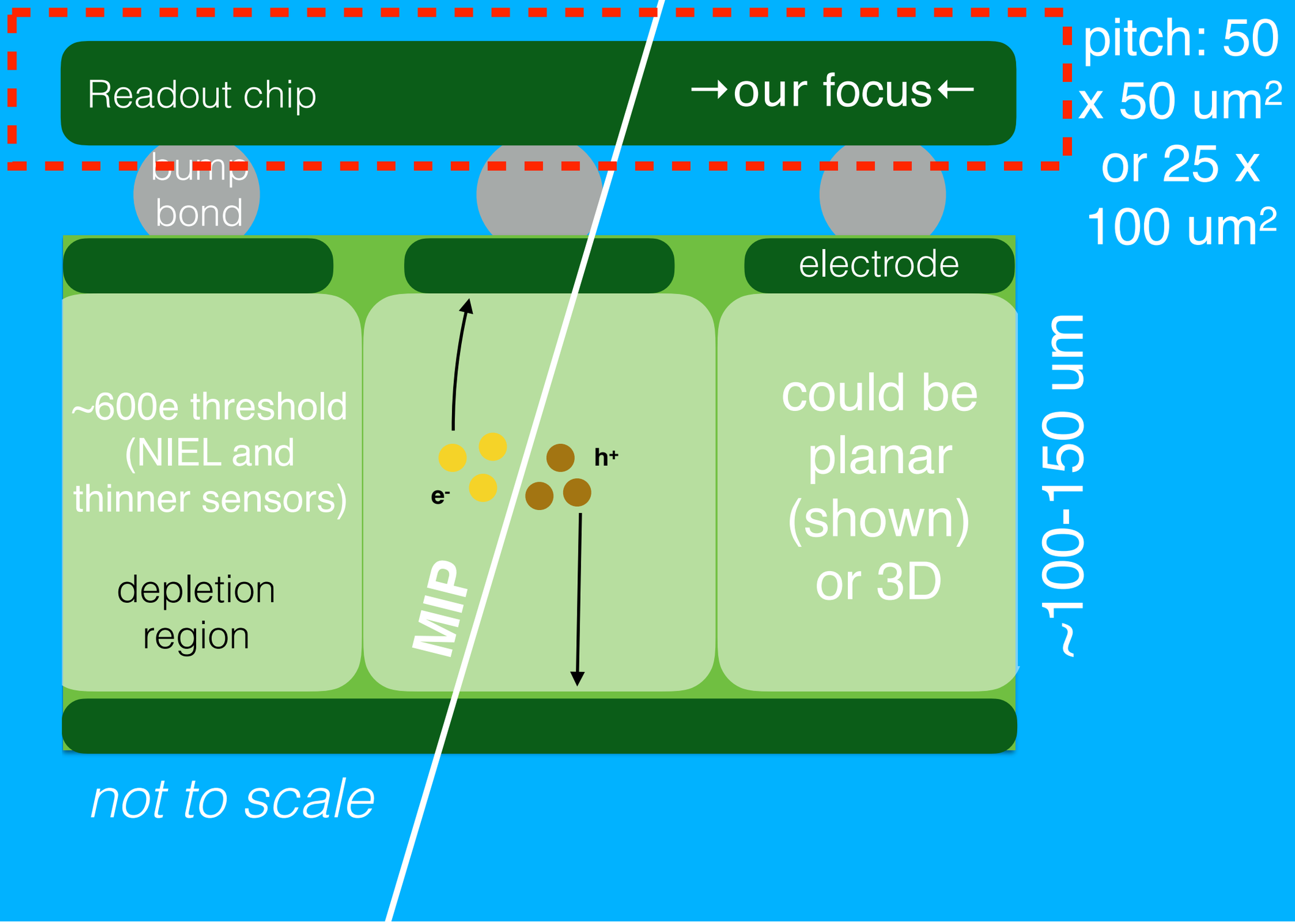


pitch: 50 x 50 um² or 25 x 100 um²

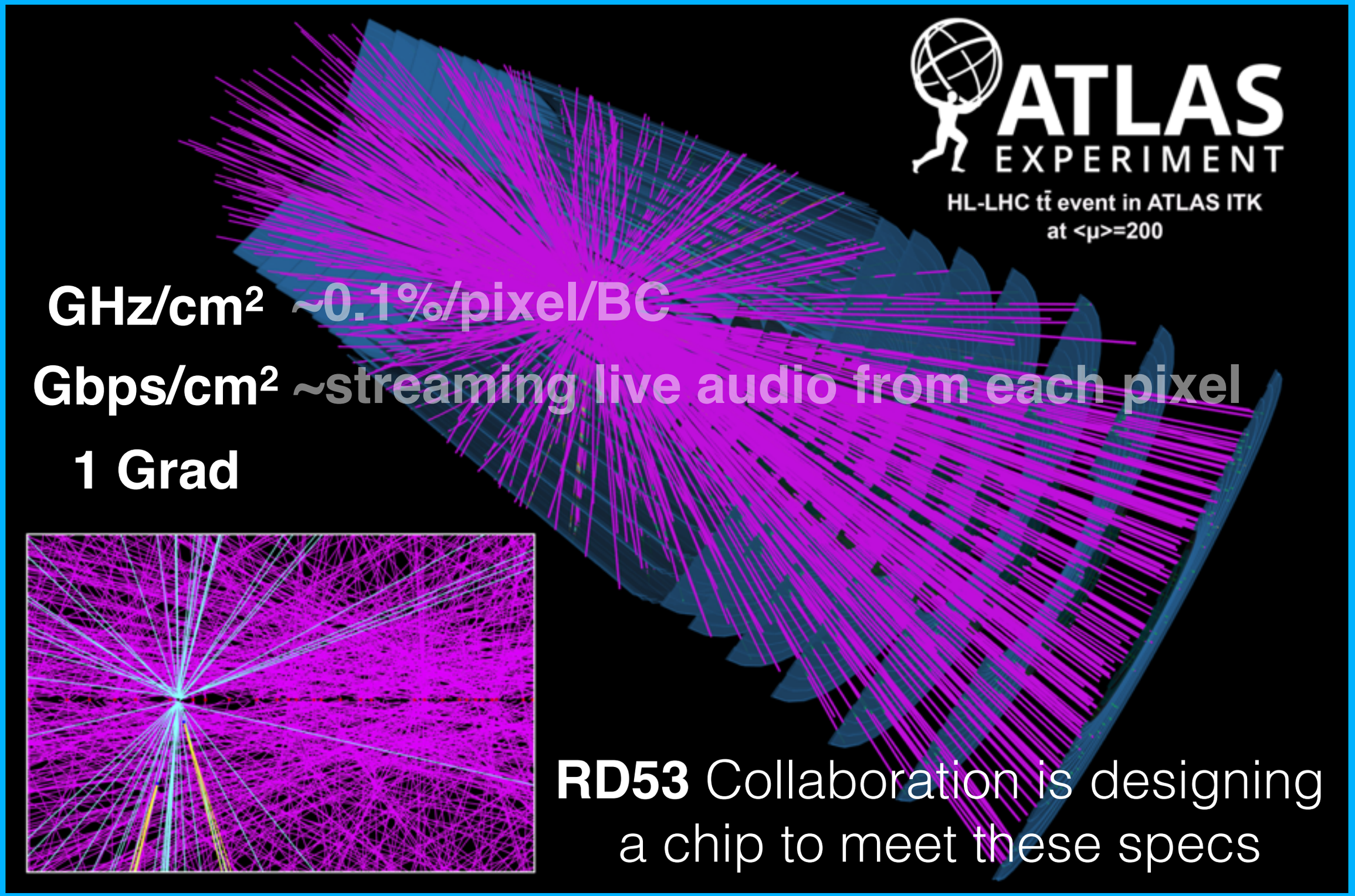
not to scale

Design set by the innermost layer (~30 mm from interaction)

Our goal: push the hybrid detector to the extreme



The future: Higher bandwidth, hit rate, radiation damage



GHz/cm² ~0.1%/pixel/BC

Gbps/cm² ~streaming live audio from each pixel

1 Grad

RD53 Collaboration is designing a chip to meet these specs

The Challenge of the HL-LHC

Generation	Run 1 (FEI3, PSI46)	Runs 2+3 (FEI4, PSI46DIG)	Runs 4+5
Chip Size	7.5 x 10.5 mm^2 8 x 10 mm^2	20 x 20 mm^2 8 x 10 mm^2	> 20 x 20 mm^2
Transistors	3.5 M 1.3 M	87 M	~1 G
Hit Rate	100 MHz/cm^2	400 MHz/cm^2	~2 GHz/cm^2
Hit Memory / Chip	0.1 Mb	1 Mb	~16 Mb
Trigger Rate	100 kHz	100 kHz	200 kHz - 1MHz
Trigger Latency	2.5 us 3.2 us	2.5 us 3.2 us	6 - 20 us
Readout rate	40 Mb/s	320 Mb/s	1-4 Gb/s
Radiation	100 Mrad	200 Mrad	1 Grad
Technology	250 nm	130 nm 250 nm	65 nm
Power	~1/4 W/cm^2	~1/4 W/cm^2	1/2 - 1 W/cm^2

Working toward an HL-LHC chip (sociology first)

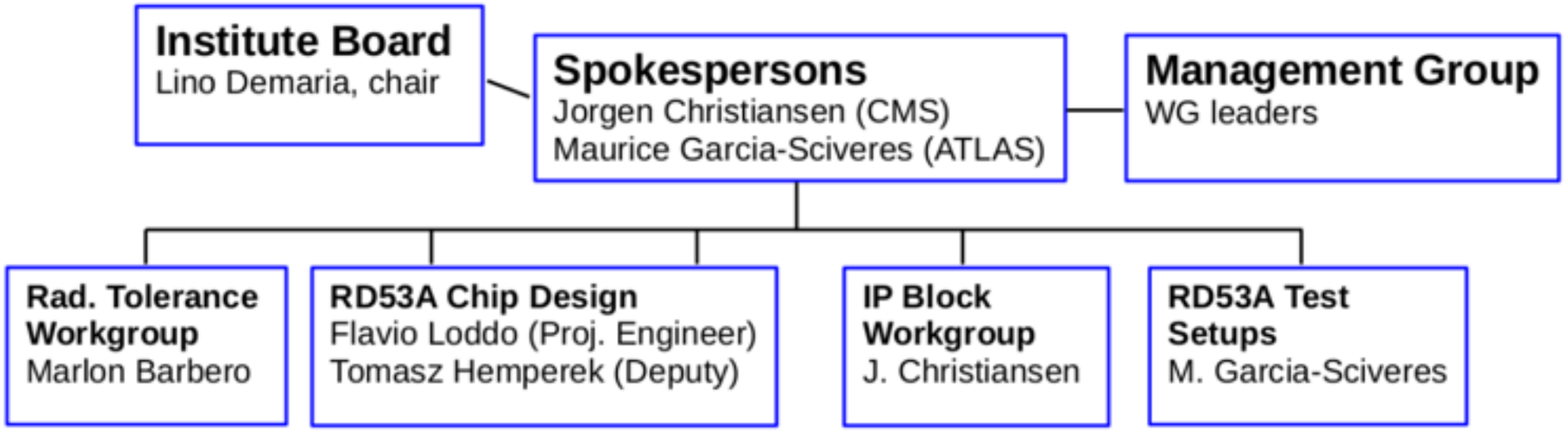
ATLAS and CMS (and CLIC) have come together to design a state-of-the art 65 nm readout chip(s)

RD-53 Collaboration Home

RD-53 will develop the tools and designs needed to produce the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC. There is also interest and participation by CLIC. More details can be found in the collaboration proposal.

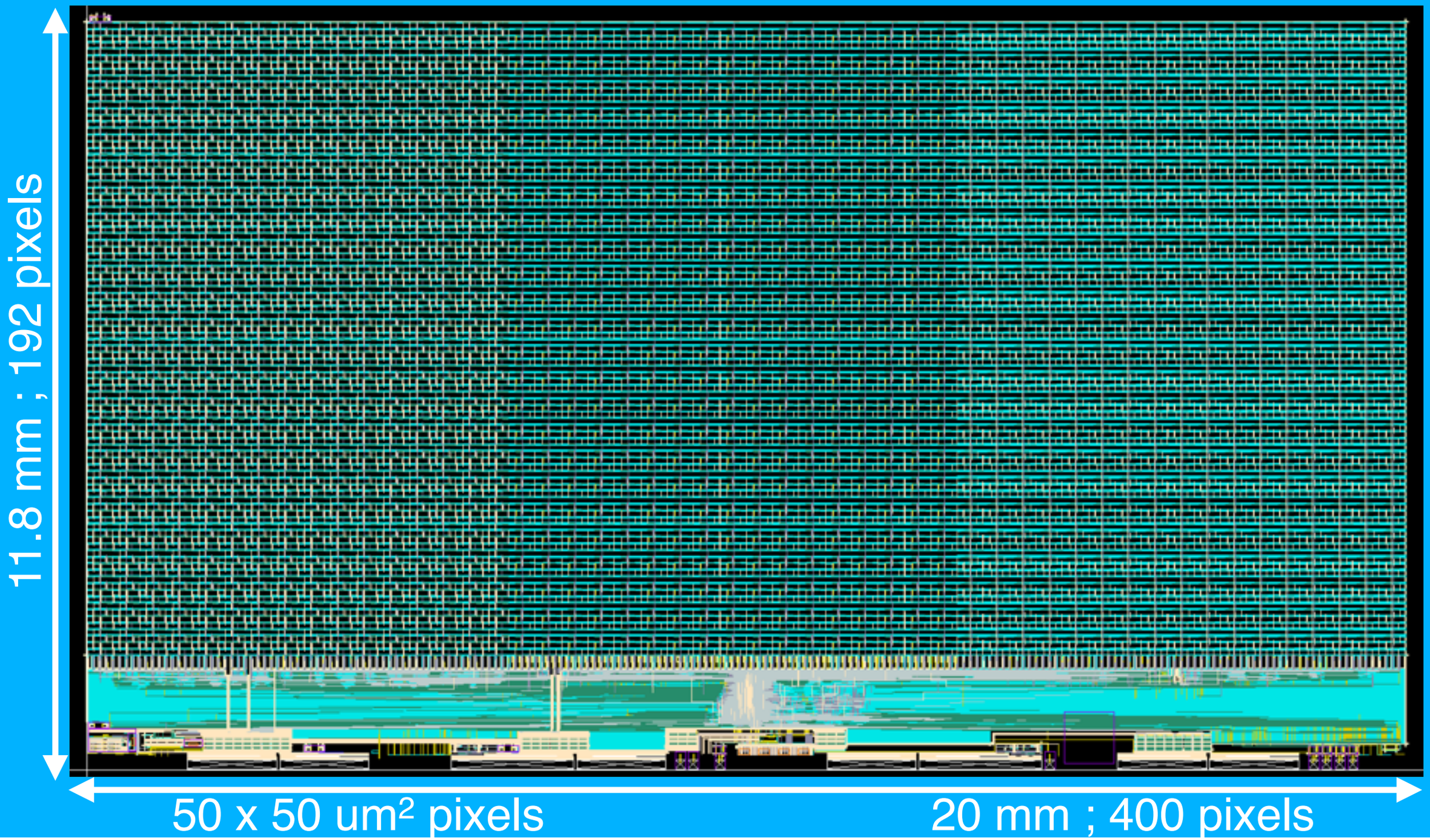
* **News** * **Meetings** * **Documents** (including papers) * **Press** * **Conferences** *

RD-53 Organization



Working toward an HL-LHC chip: RD53A

The RD53A prototype chip will demonstrate the needed performance. We will soon submit the design for fabrication.



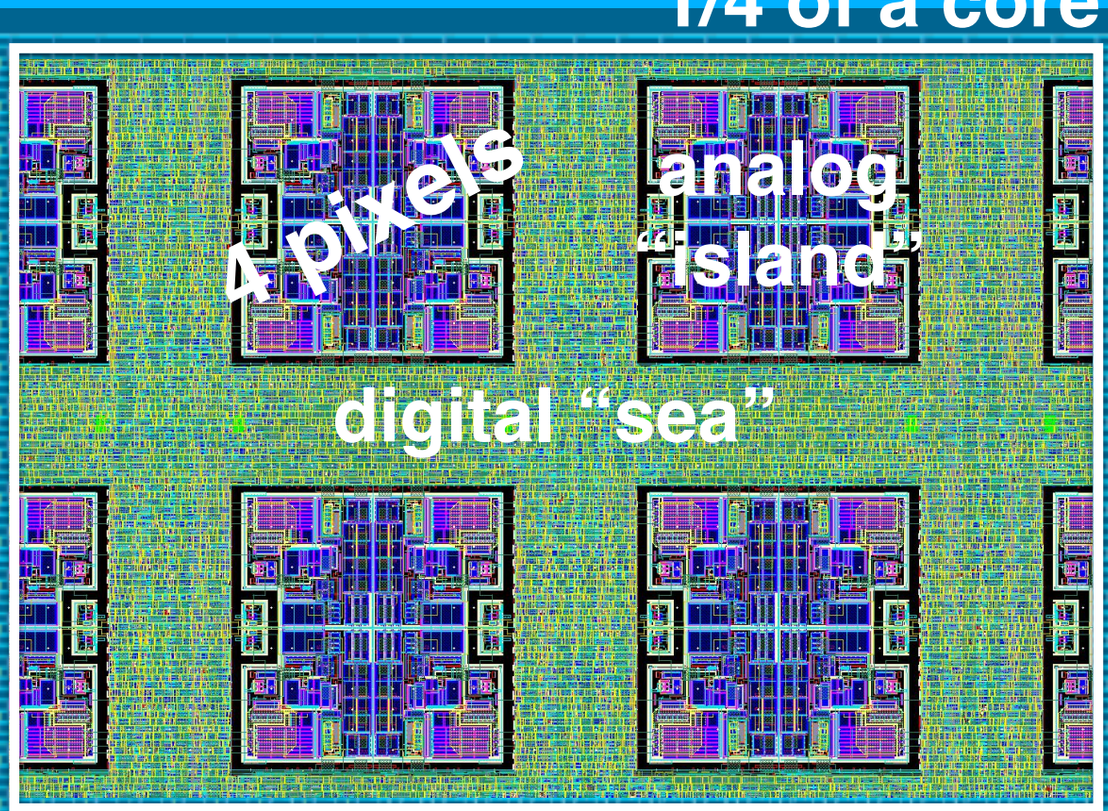
Analog Islands in a Digital Sea

The pixel matrix is organized into 8 x 8 pixel cores

Circuitry around islands not identical (globally optimized)

Core is small enough for transistor-level simulations

Memory shared between 4 x 1 or 4 x 4 pixels (more on next slide)



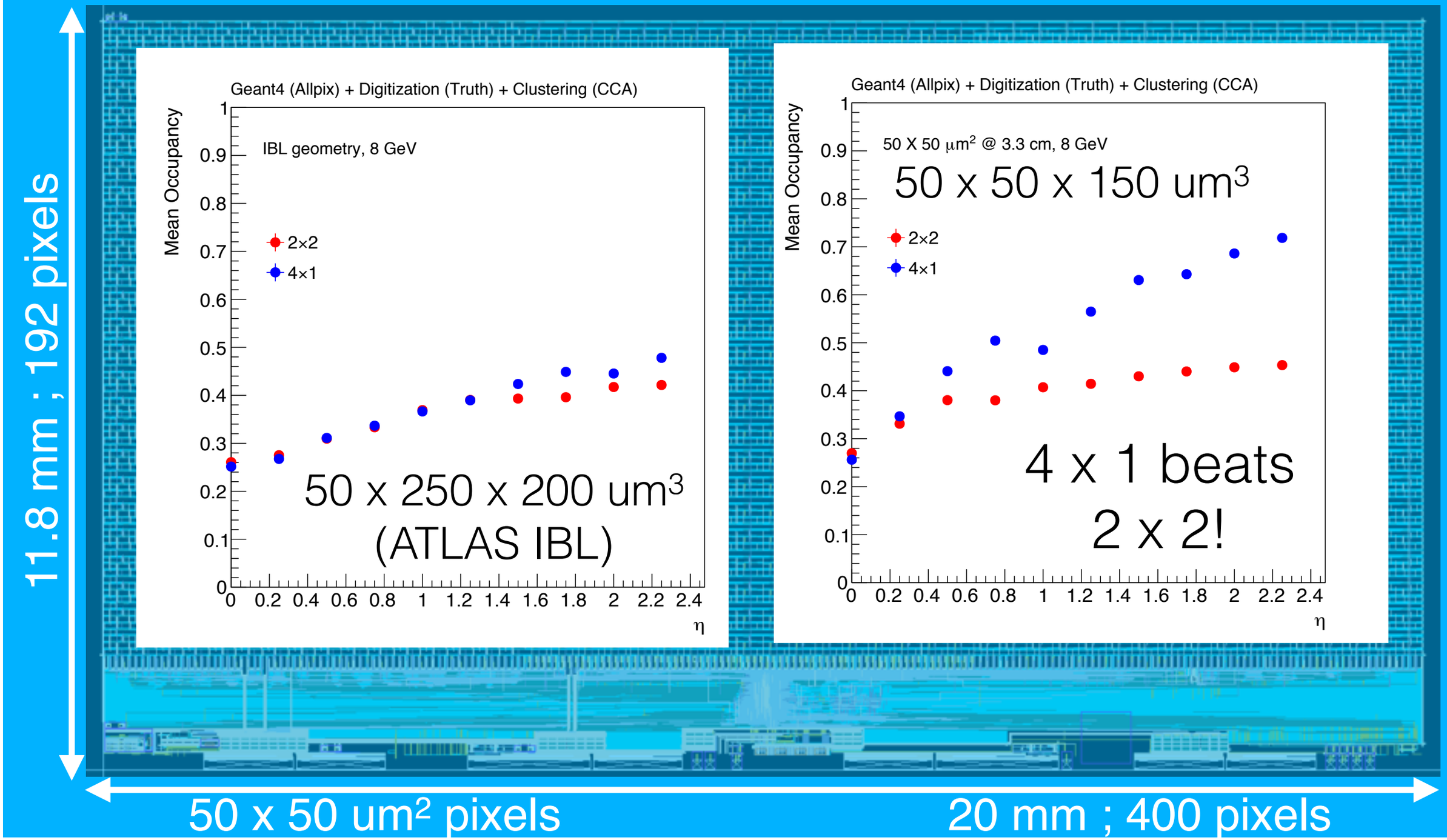
11.8 mm ; 192 pixels

50 x 50 um² pixels

20 mm ; 400 pixels

Readout Windows

Readout regions N x M pixel regions; helps to recover small hits. ATLAS uses 2 x 2 - will that be optimal for the HL-LHC?

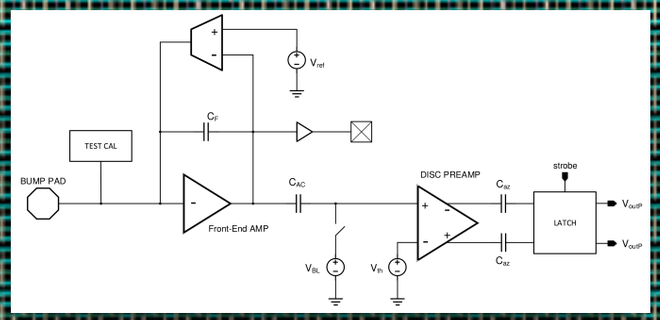


Working toward an HL-LHC chip: RD53A

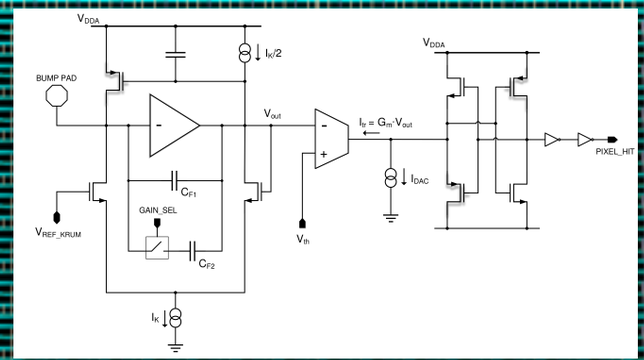
RD53A is a chip-of-chips with 3 analog front-ends (output of the cores is the same for each)

11.8 mm ; 192 pixels

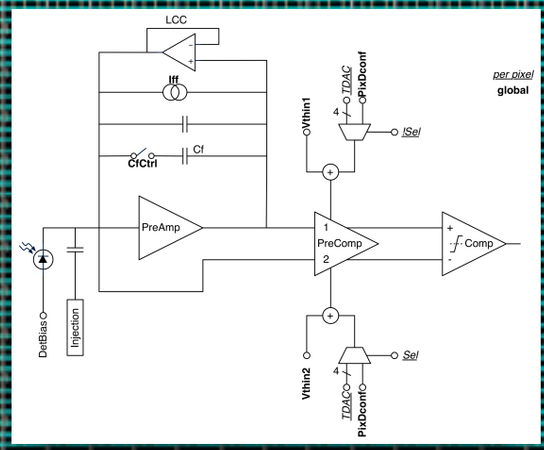
Synchronous



Linear



Differential



synchronous discriminator can be used for a fast ToT counter

~Chipix65 demonstrator~

single amplification stage for minimal power consumption

differential threshold reduces coherent noise

~FE65P2 demonstrator~

50 x 50 um² pixels

20 mm ; 400 pixels

Working toward an HL-LHC chip: RD53A

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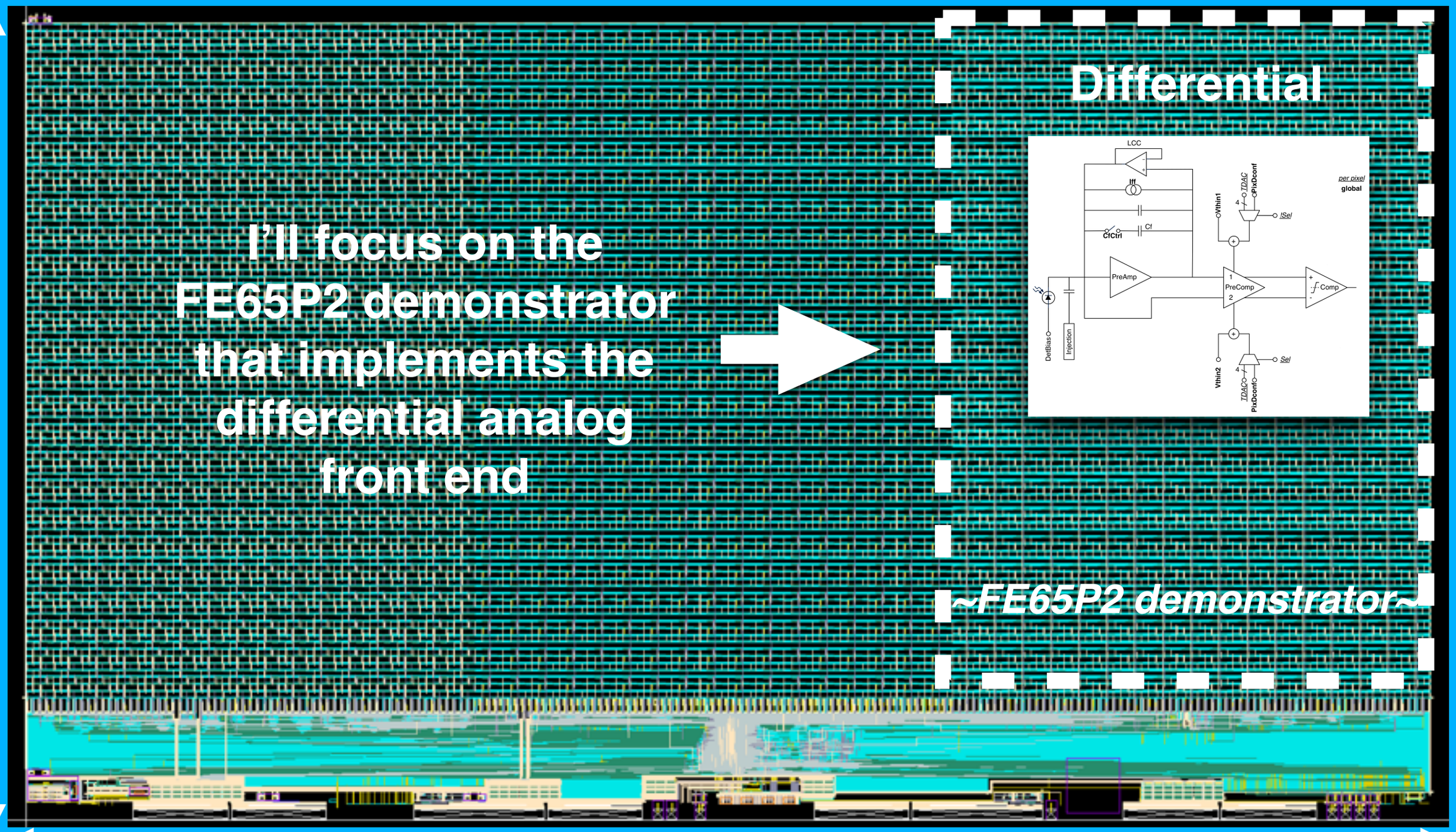
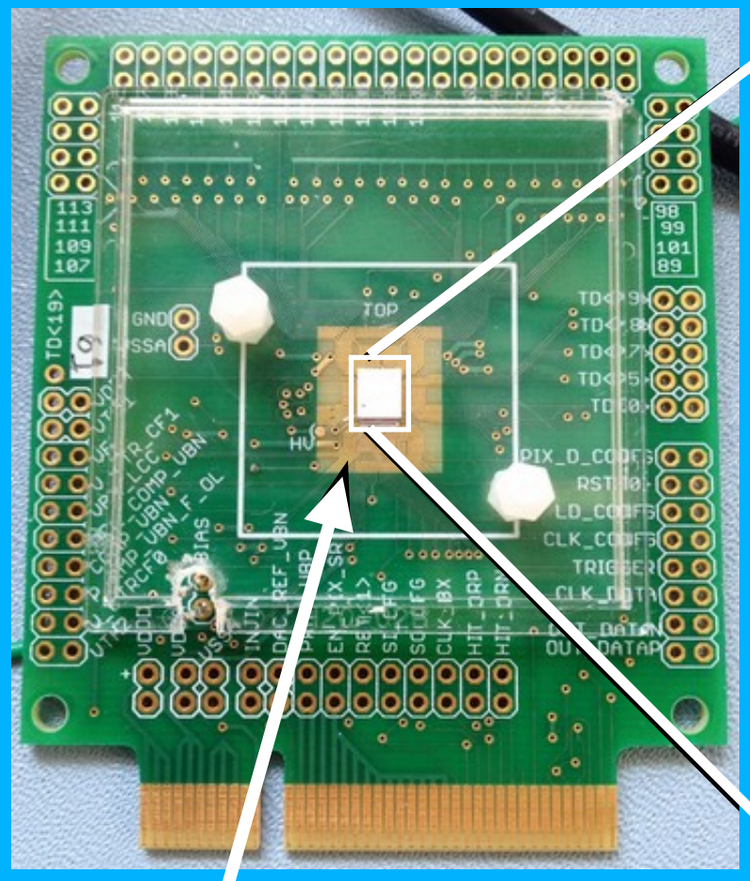
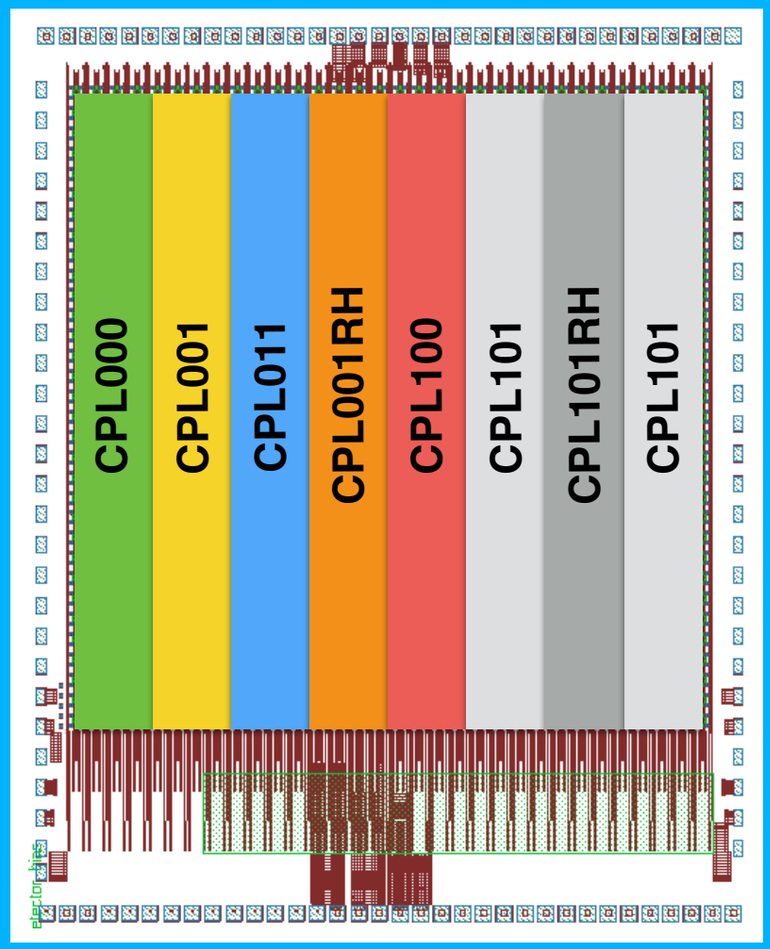


A proto-RD53A chip: FE65P2

FE65P2 is a demonstrator chip for the RD53A differential analog front end.



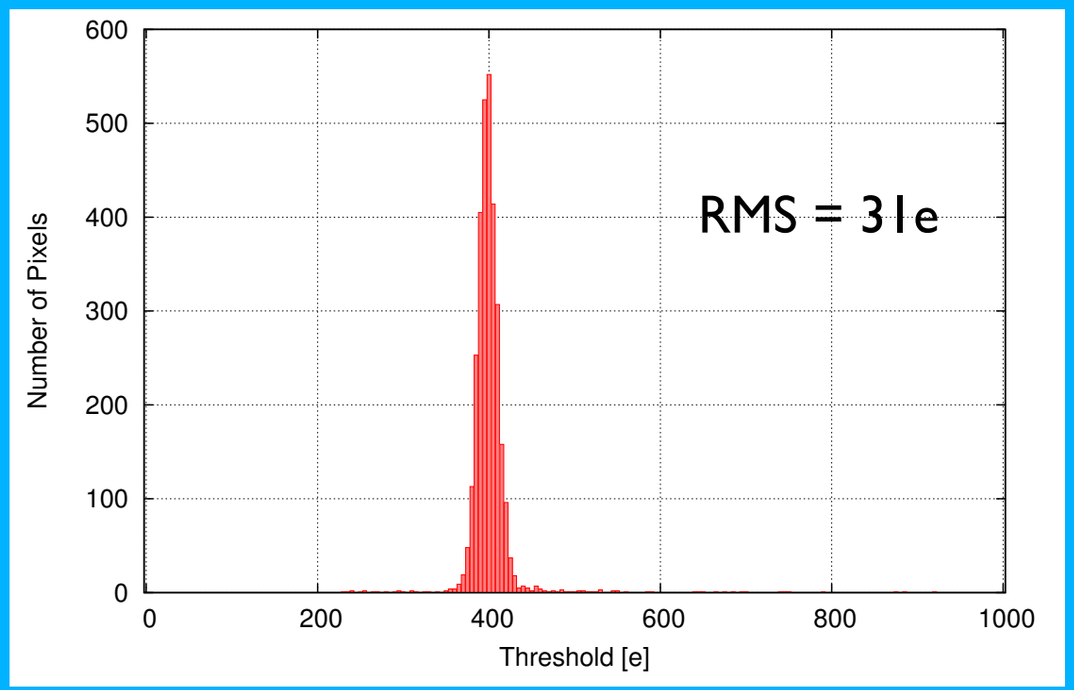


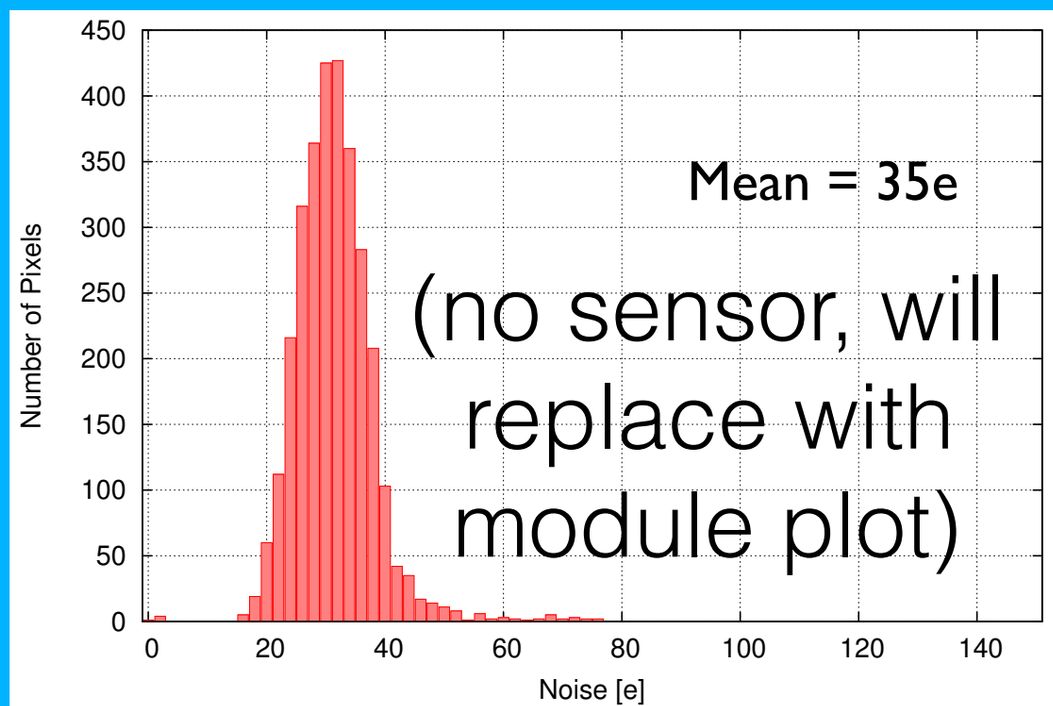
sensor bump-bonded to chip at SLAC

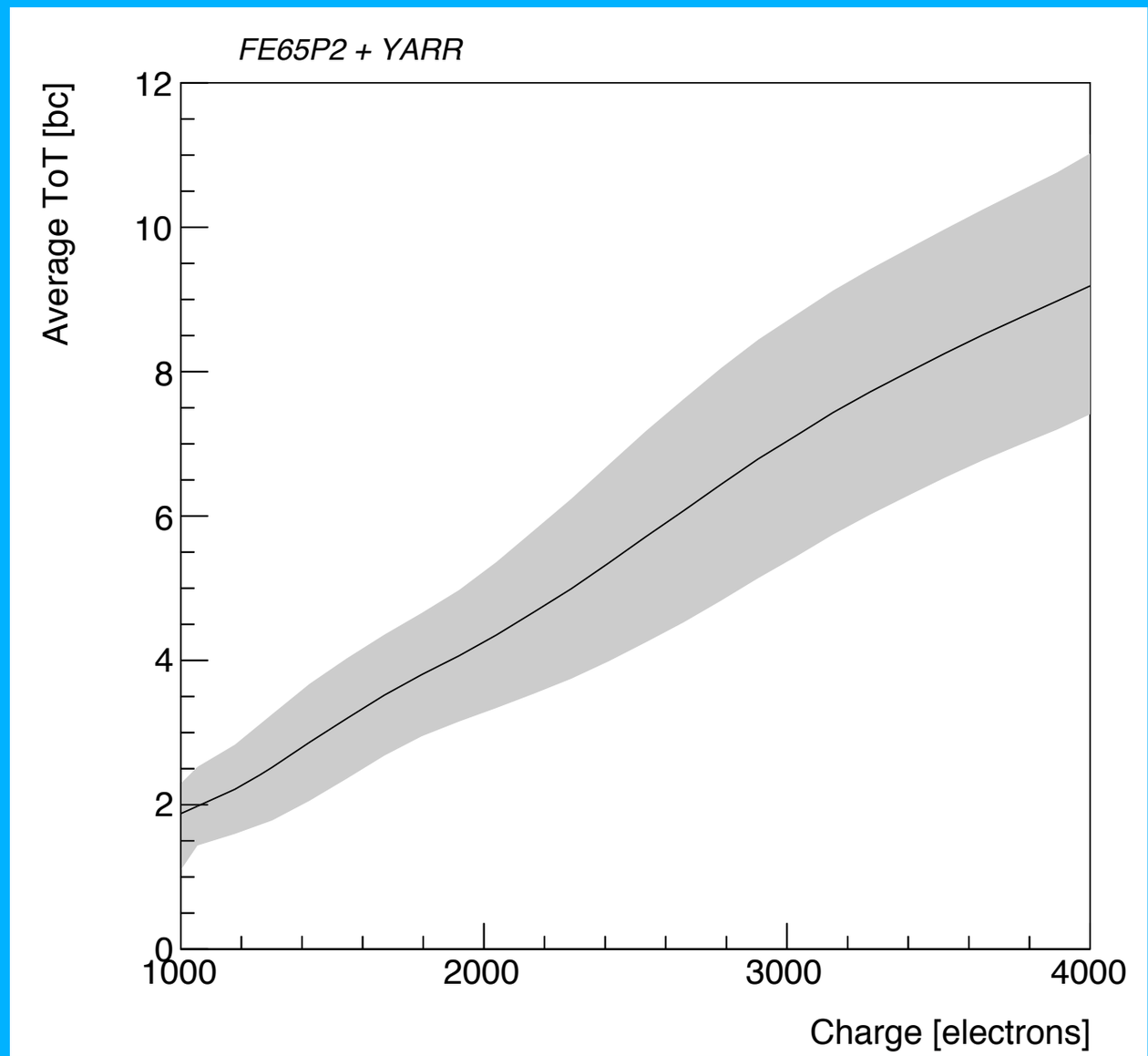
8 columns with different analog ‘flavors’

leakage current compensation, increased amplifier gate width, etc.

FE65P2: Charge Measurement

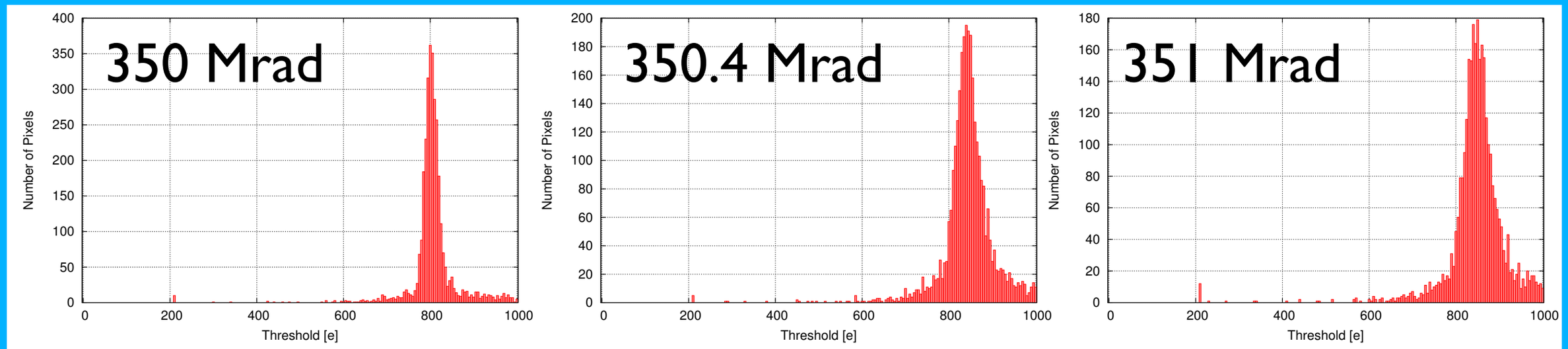


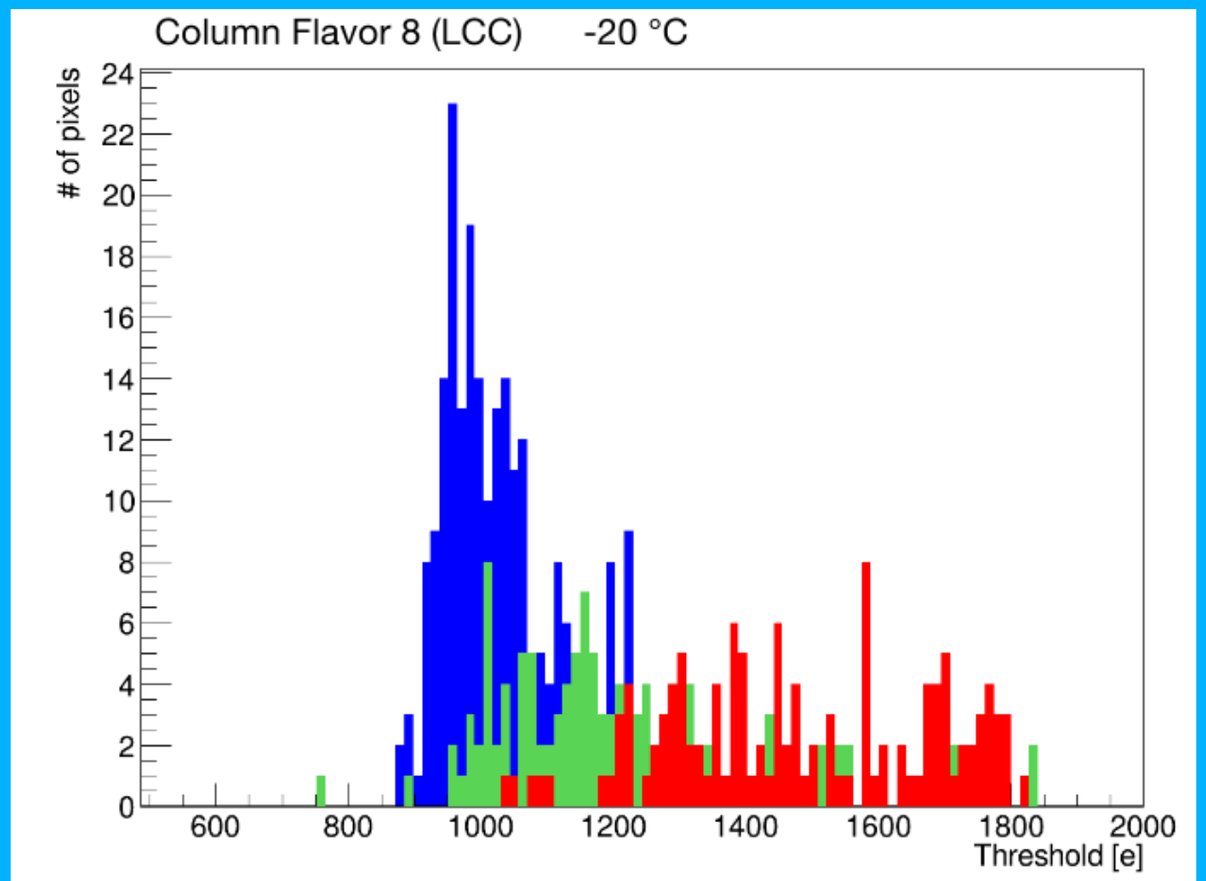


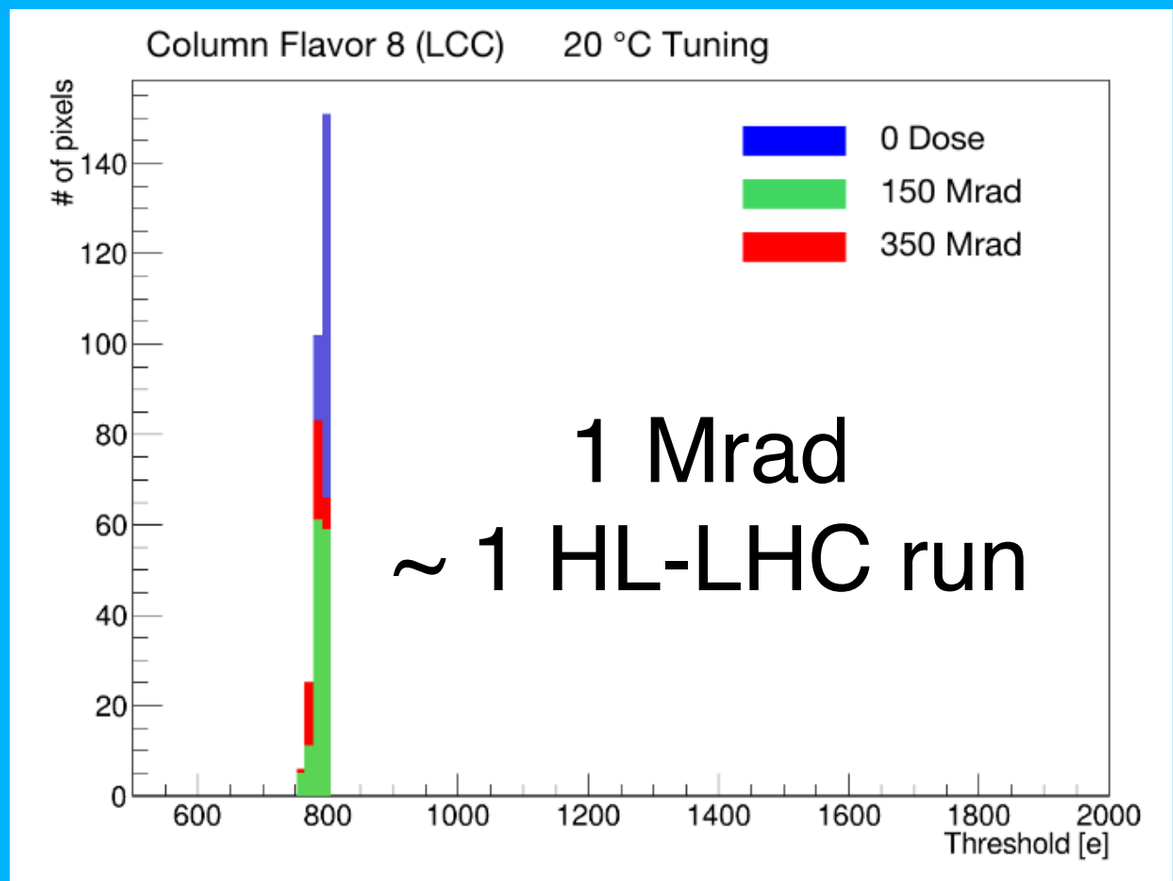


For comparison: 100 um thick sensor ~ 8ke MIP peak prior to irradiation

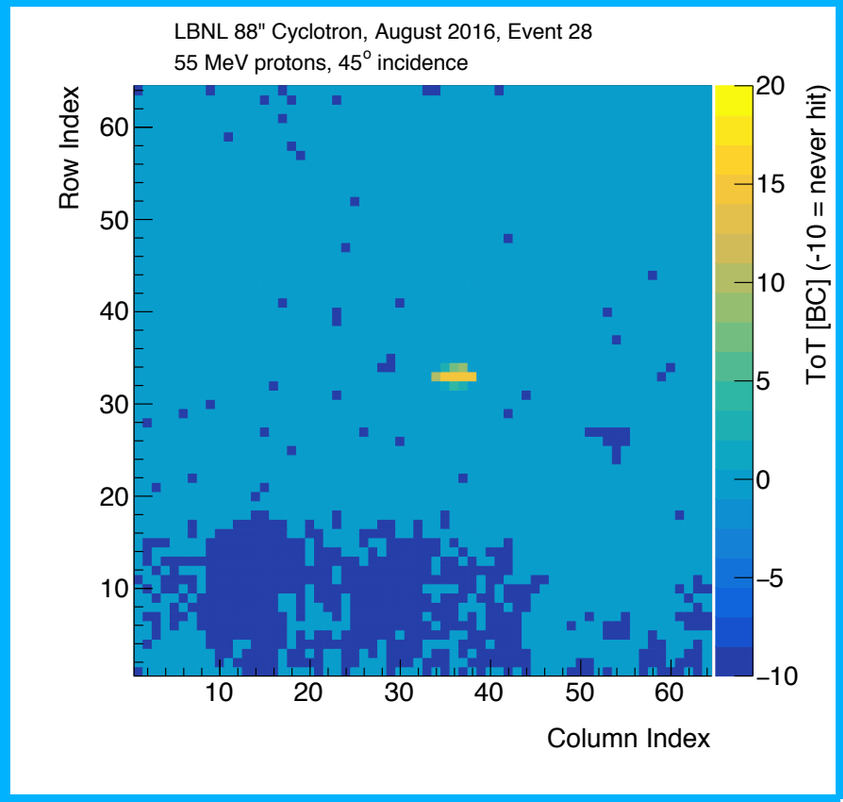
FE65P2: Threshold Stability

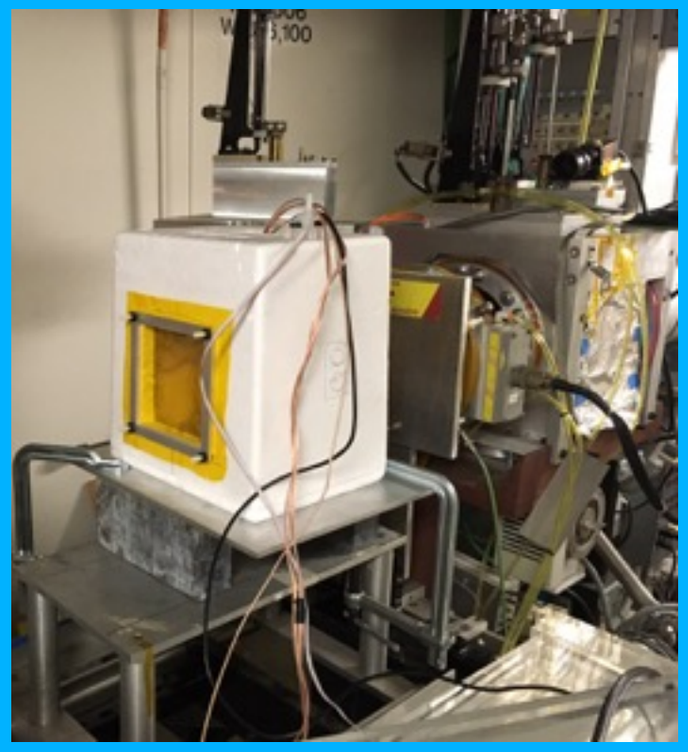






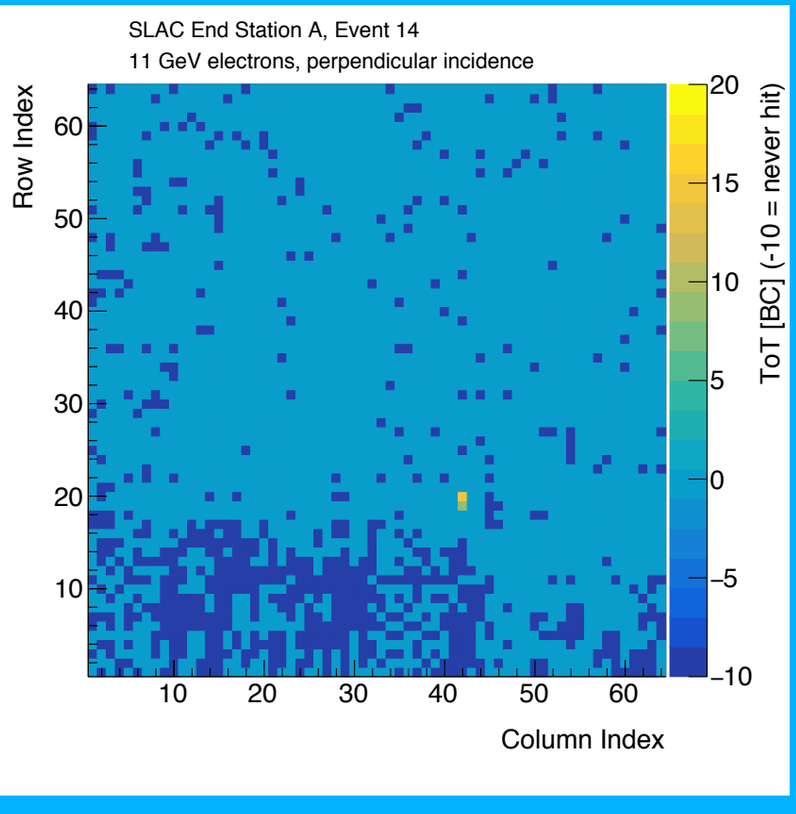
FE65P2 Modules: First Beam Studies





Berkeley Cyclotron

SLAC End Station



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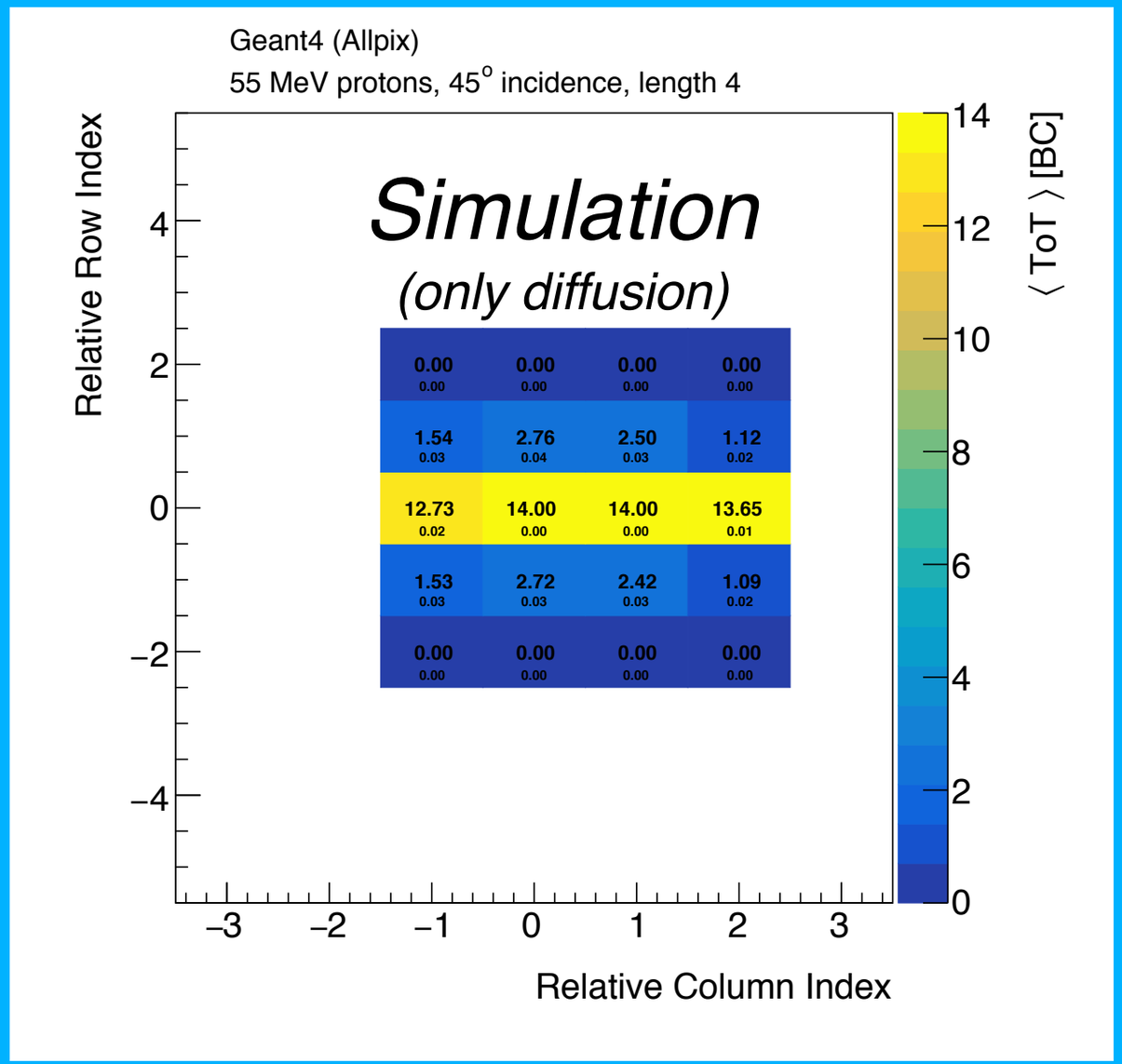
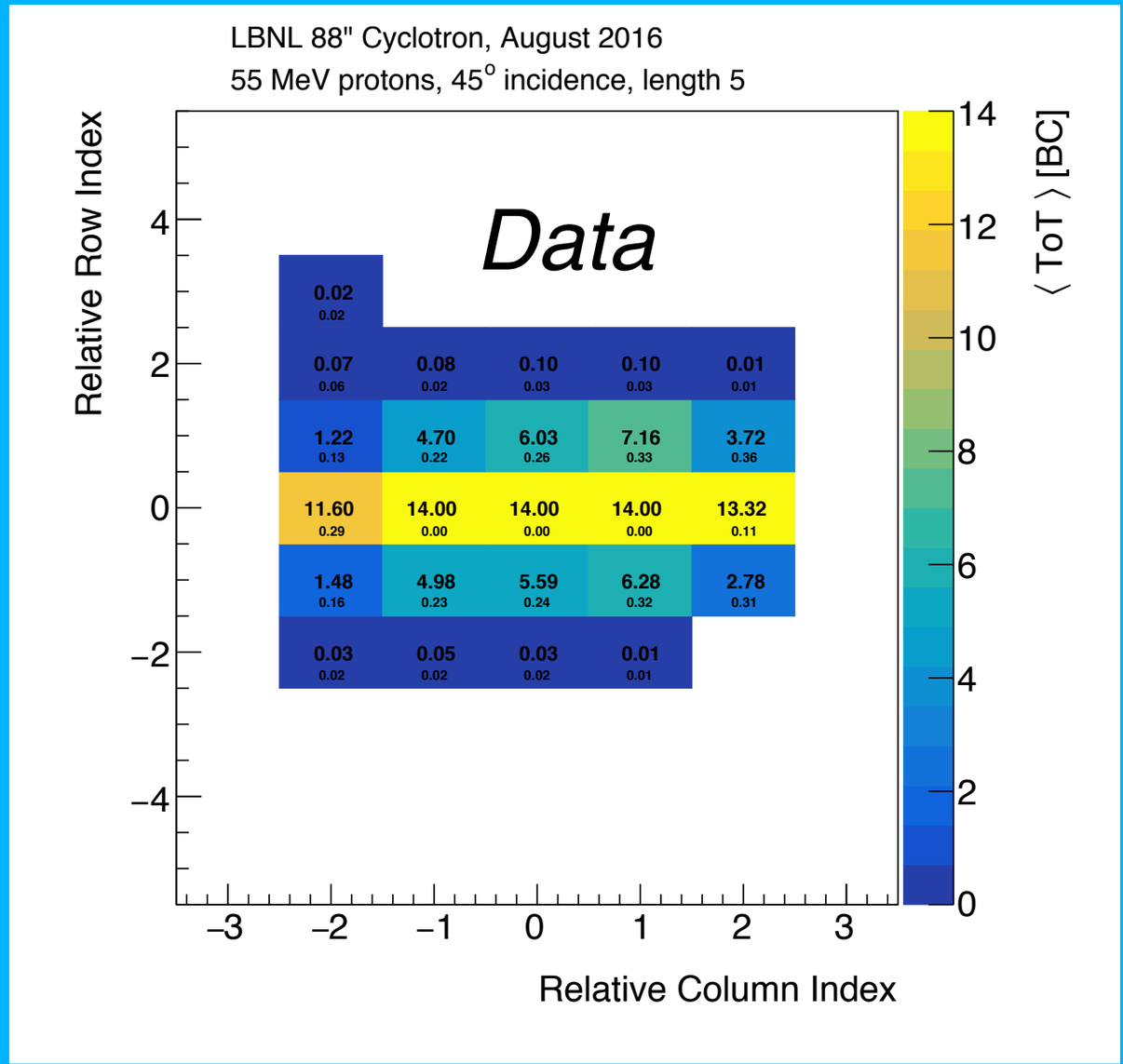




Capacitive coupling-induced charge sharing

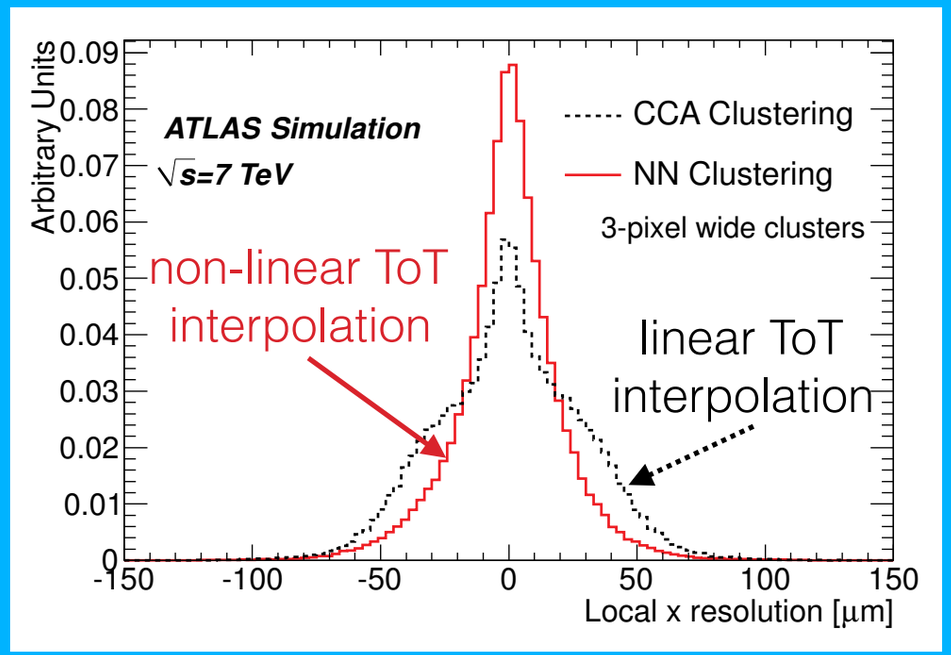
$$\sim \frac{\text{(6-3) ToT x 400e / ToT}}{\text{6 x (80 e/um) x (150 um)}} \sim 2\%$$

diffusion part (left plot)

more than MIP

(typical)

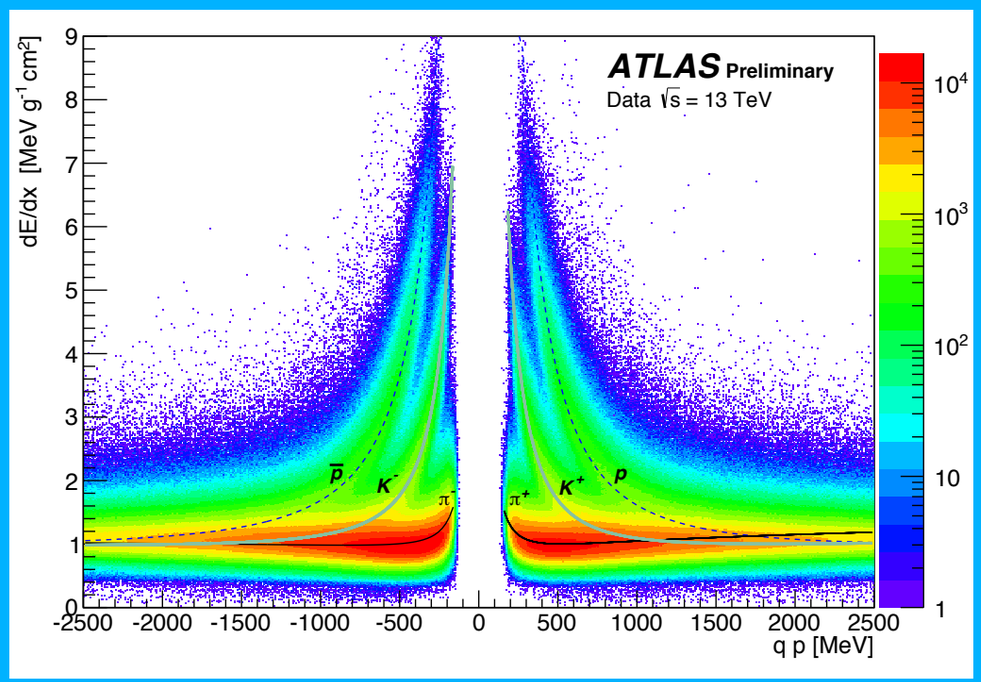
Optimization studies: Use of charge



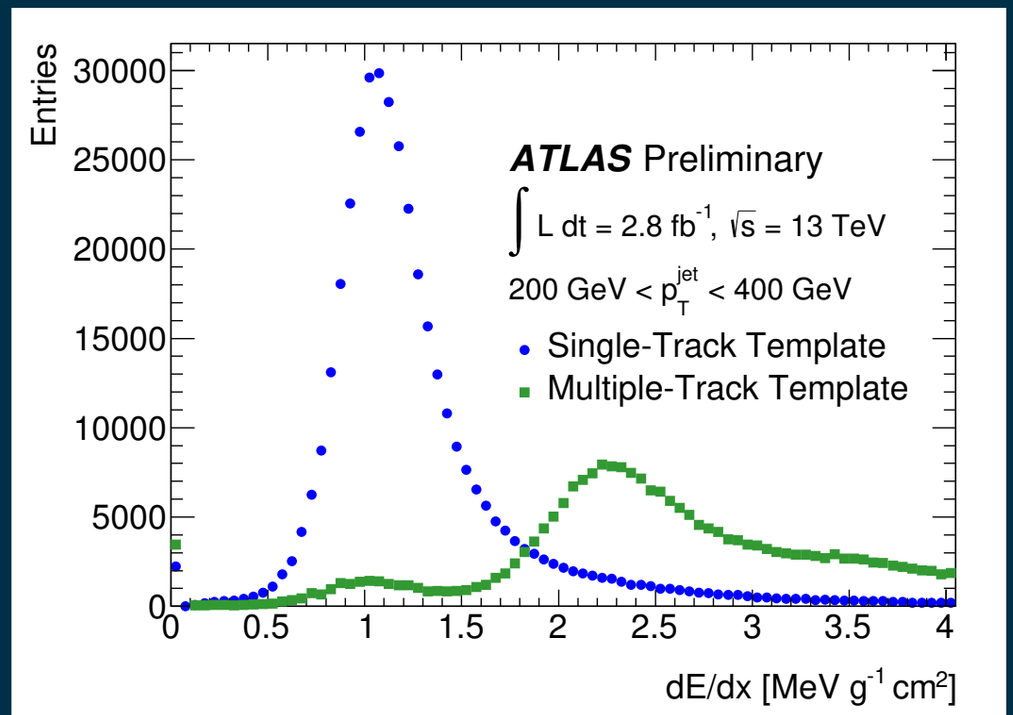
JINST 9 (2014) P09009

As we design the RD53 chip, we have an opportunity to make optimal use of its readout

There is (useful) information contained in the analog signal



ATLAS-PIX-2015-002



ATL-PHYS-PUB-2016-00

The Run 1 CMS detector had a full analog readout while the ATLAS FEI3/4 use 8/4 bits of charge (measured in ToT)

Optimization studies: Use of charge

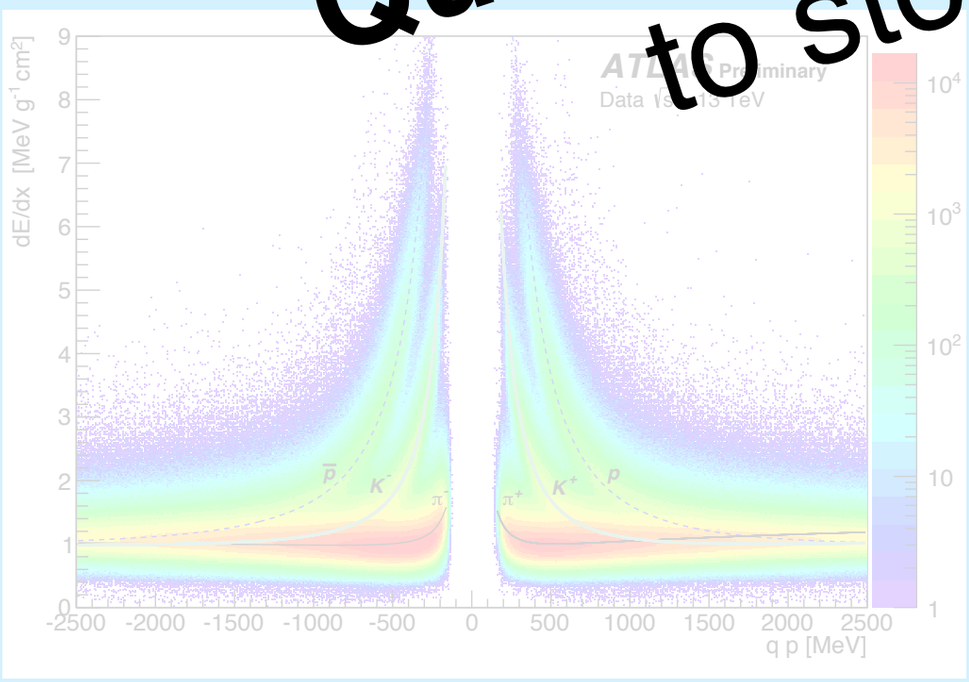
JINST 9 (2014) P09009

As we design the RD53 chip, we have an opportunity to make optimal use of its readout

There is (useful) information contained in the analog signal

Question: what is the "best" way to store/utilize charge?

ATL-PHYS-PUB-2016-007



ATLAS-PIX-2015-002

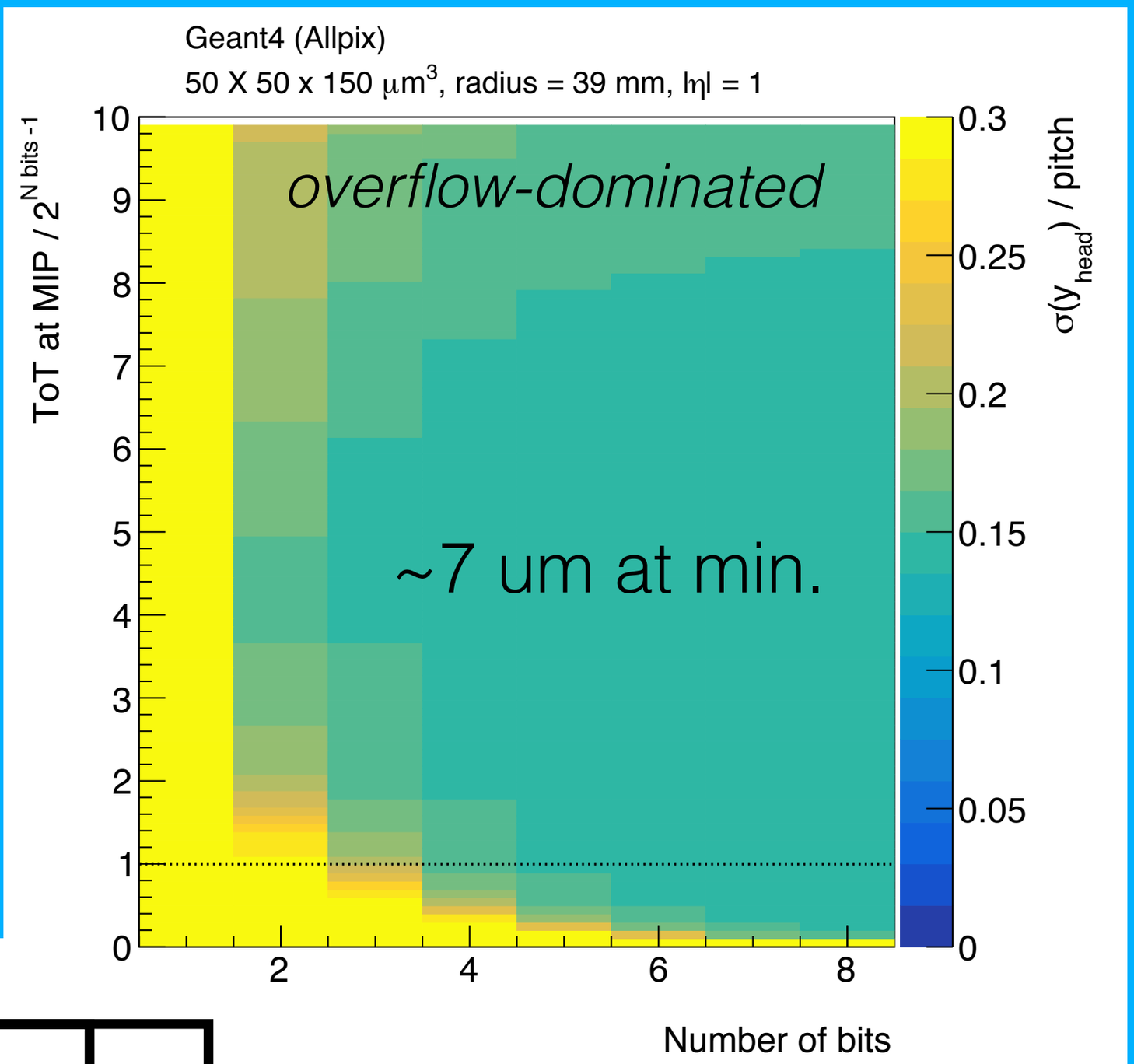
The Run 1 CMS detector had a full analog readout while the ATLAS FEI3/4 use 8/4 bits of charge (measured in ToT)

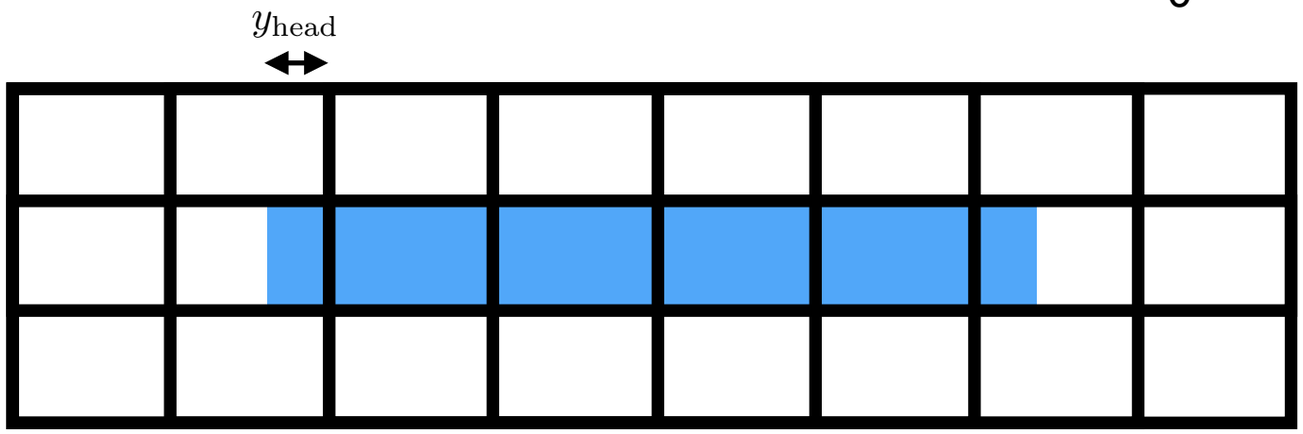
Resolution: one-particle clusters

For a fixed number of bits, prefer higher ToT @ MIP

bits	Resolution
1	0.29
2	0.19
3	0.16
4	0.15
5	0.14
infty	0.13

(for path-length corrected MIP)



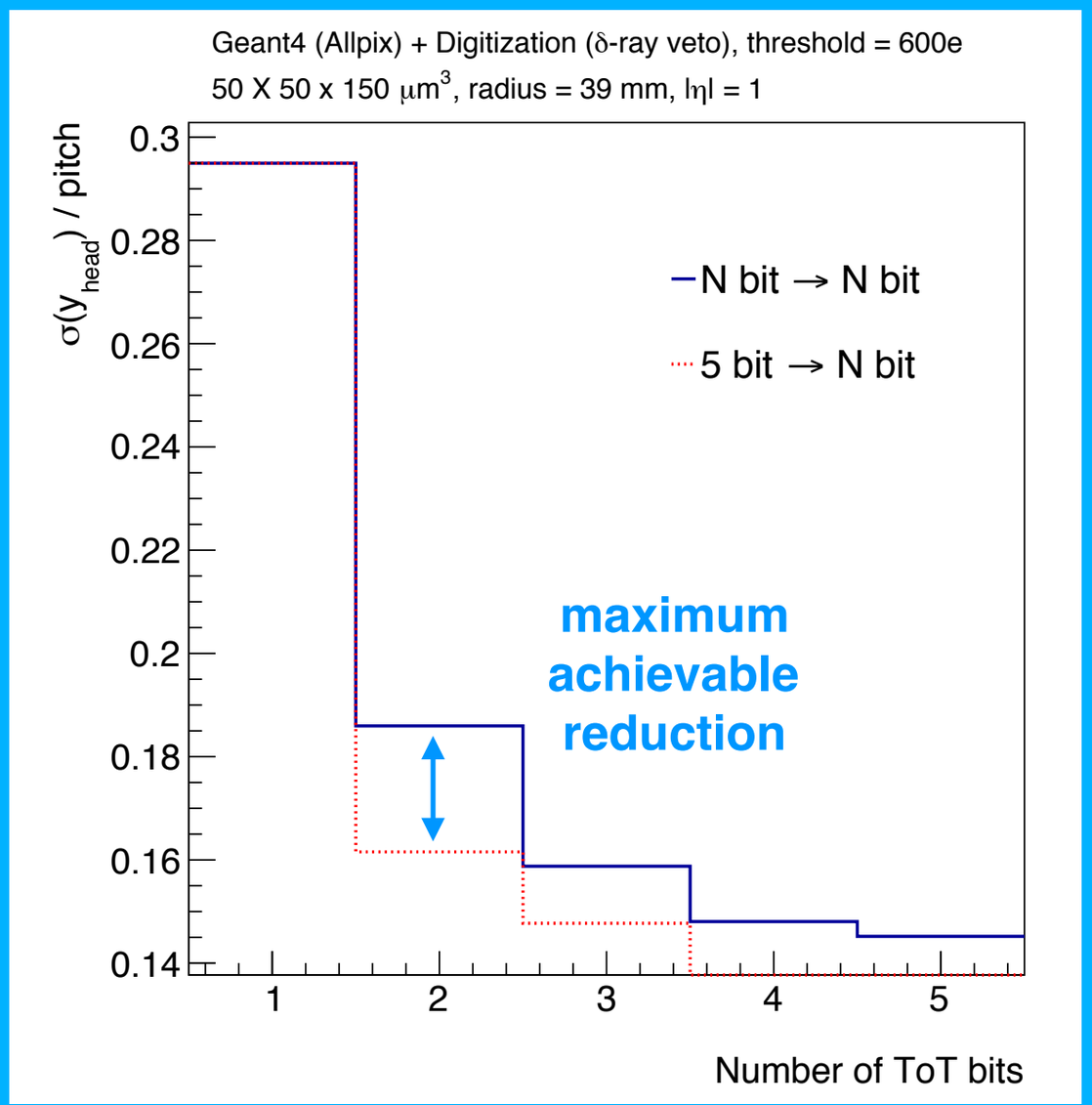


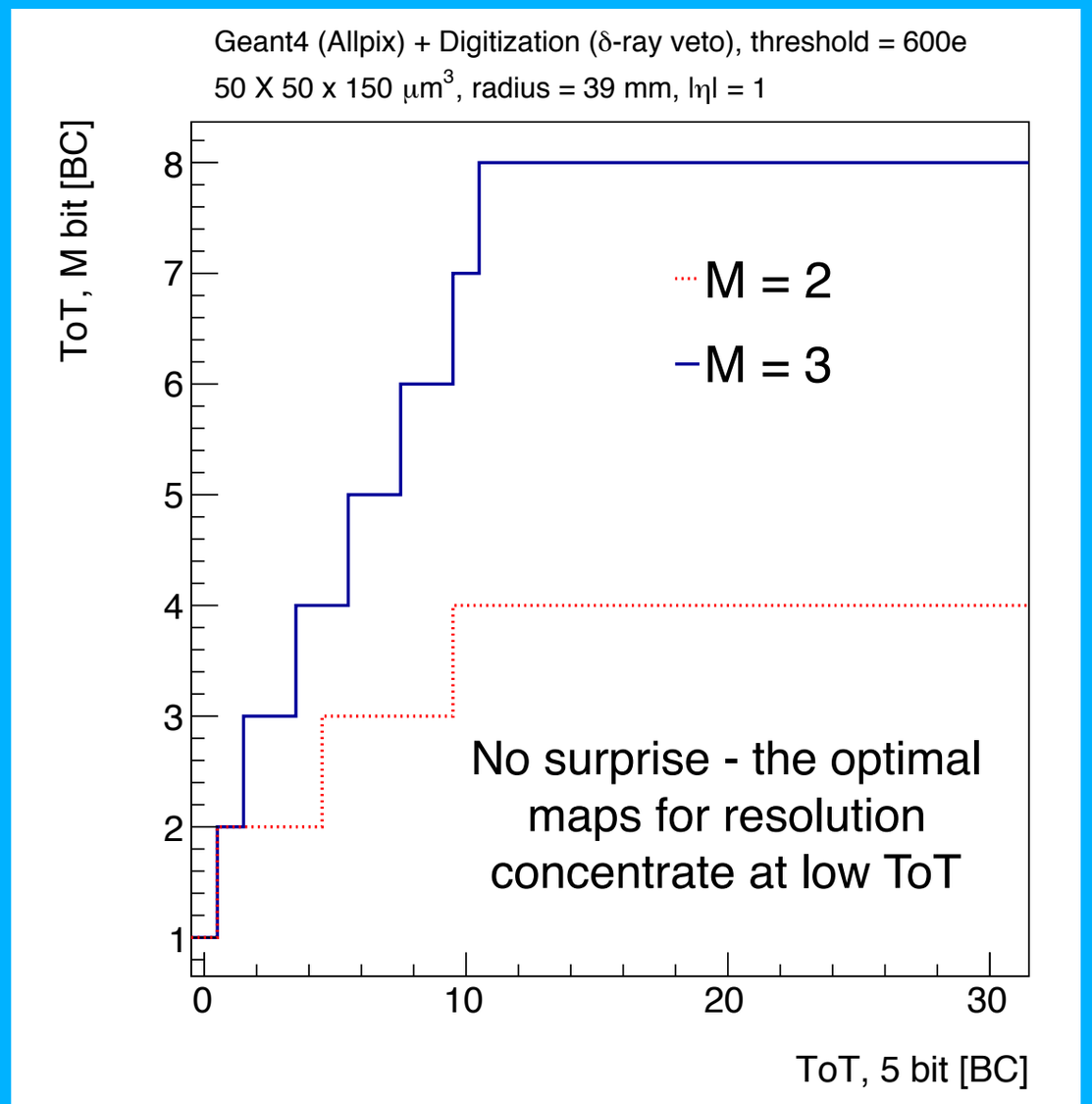
ceiling: $1/\sqrt{12} \sim 0.29$

Down-sampling

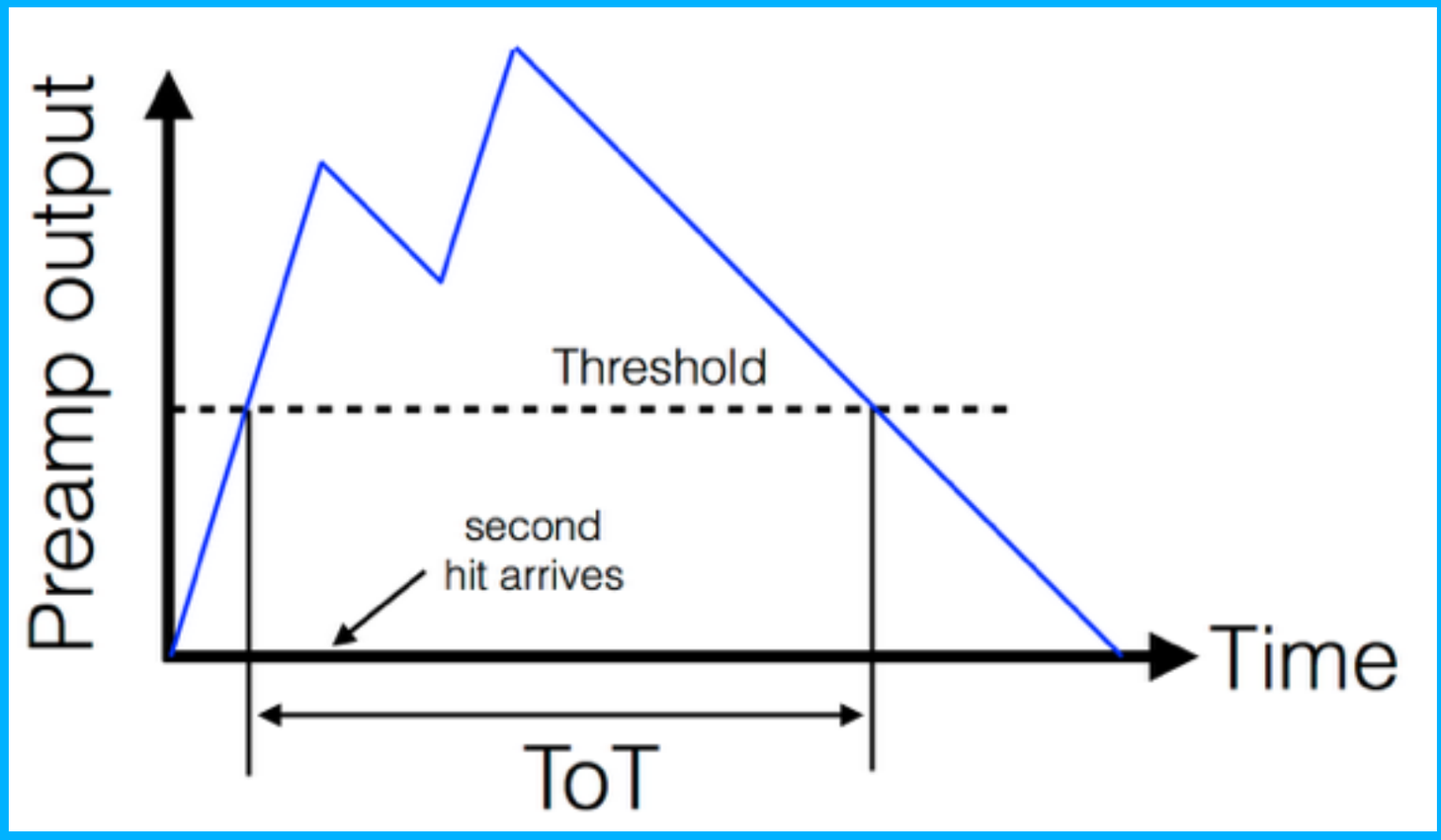
Can add digital logic so that N digitized bits are stored as M ≤ N bits.

There are $\binom{2^N - 2}{2^M - 2}$ possible functions mapping N to M bits.





Efficiency



Counting longer increases precision but also **in-pixel pileup**

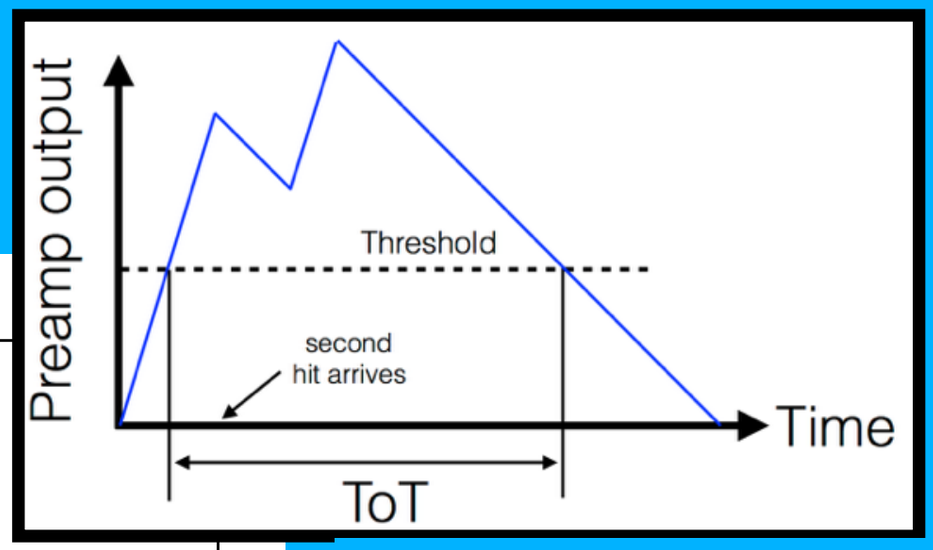
Could mitigate by counting faster than 40 MHz, but if fixed:

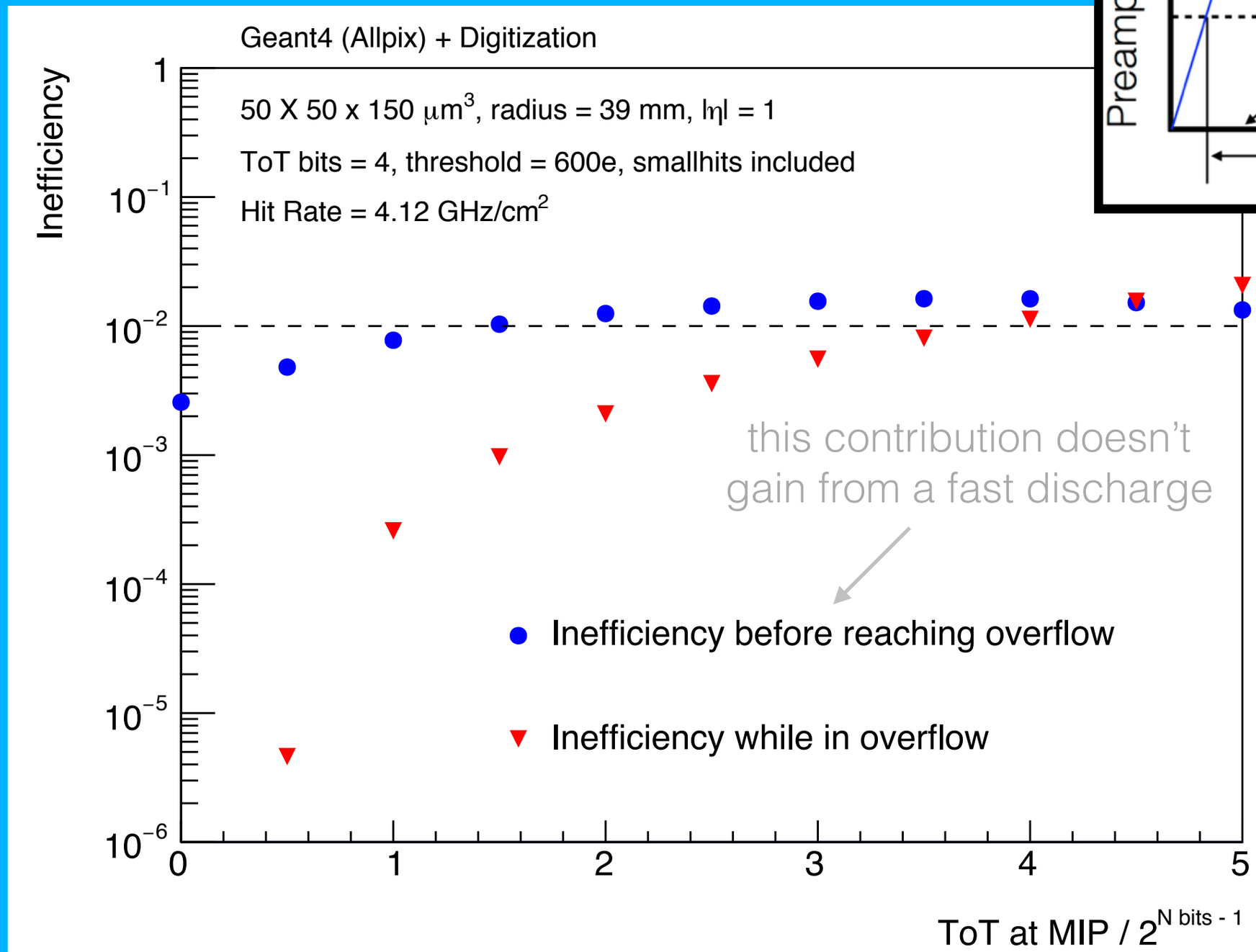
there is a tradeoff between dynamic range
(charge / ToT + N bits) and efficiency

N.B. can't just reduce N bits - still need to discharge overflow!

Fast (analog) discharge

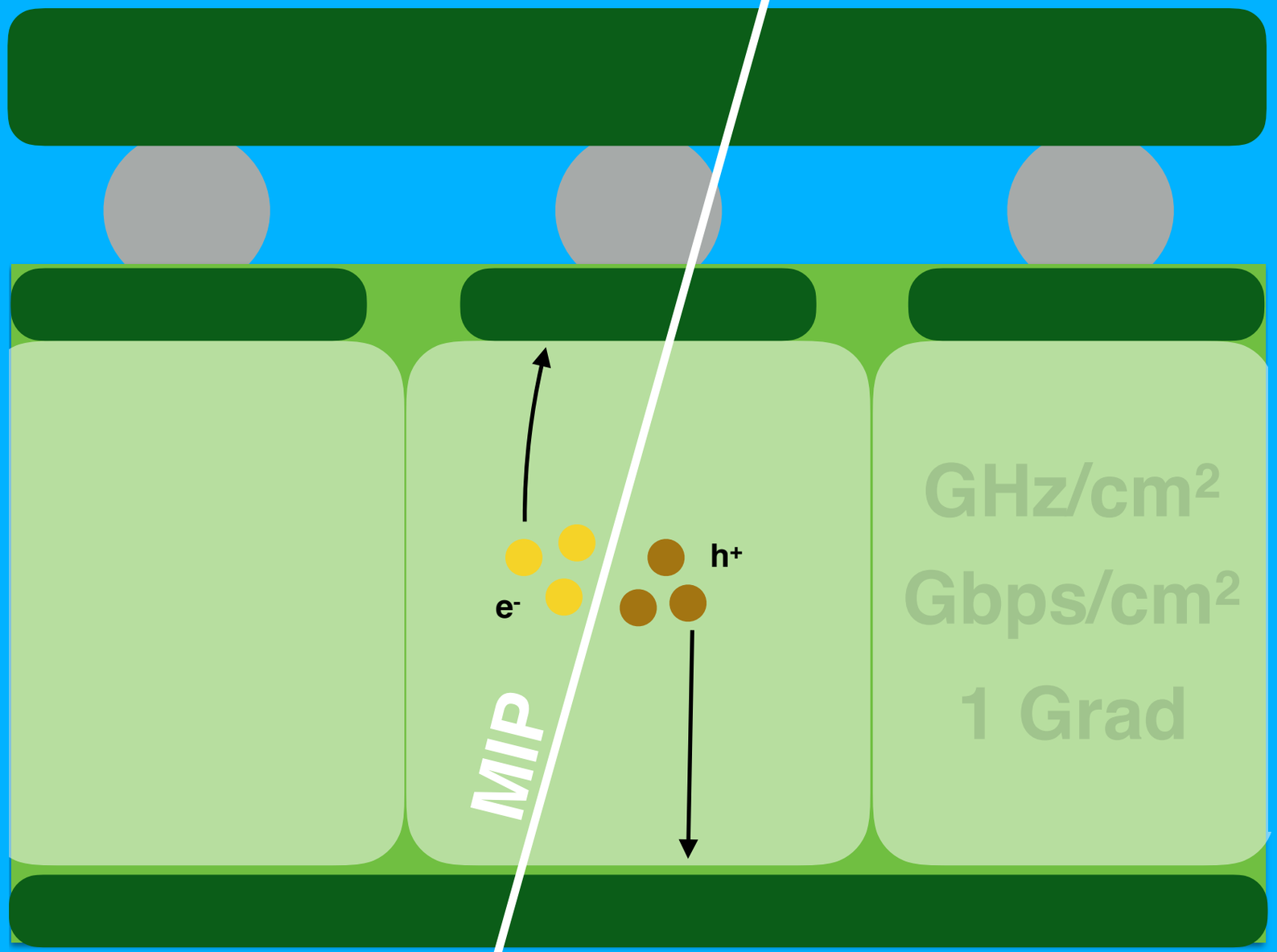
What if you could ~instantly remove charge when the counter reached 2^N - 1?





The HL-LHC will be an extreme environment for tracking.

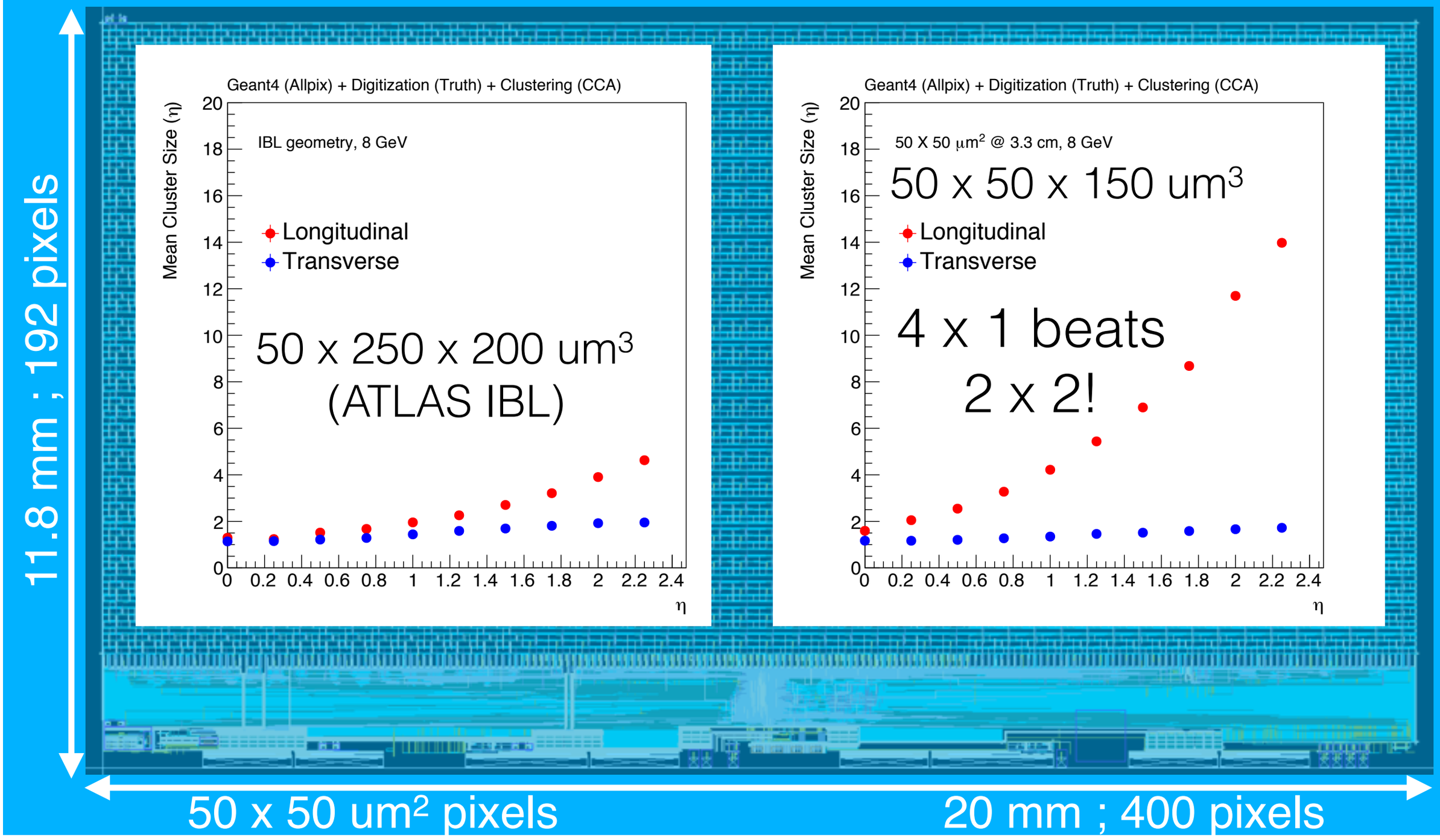
The RD53 collaboration has formed to pool resources in order to be able to maintain and exceed current performance.



Backup

Readout Windows

Readout regions N x M pixel regions; helps to recover small hits. ATLAS uses 2 x 2 - will that be optimal for the HL-LHC?



Time over Threshold Method