RADSAGA Initial Training Event
1-6 October 2017, Geneva

From Radiation Hardening To BRAVE FPGA devices

October 2017

Rad Tolerant vs Rad Hardened

Radiation Hardened material is **immune to the effects of the radiation** and has a higher life cycle. The devices are specifically designed in a control environment and the property is unique.
Moreover, Radiation Hardened material are used on devices which are meant to work in high radiation prone areas such as **space**.

Radiation Tolerant material is a property of the device to be bear radiation till certain limit the material will need replacement afterwards. The devices are designed without compromising other properties of the device.
The radiation property could be find in a lot of devices and does not need a specialized controlled environment to make it.
Most of these materials usually don't see their use in their lifespan as they are meant to work in normal environment, they are generally used in Cell Phones, Computers, Consumer Electronics, Radiation suits and so on.

Source: https://www.quora.com/What-is-the-difference-between-radiation-hardened-and-radiation-tolerant-components-used-in-space-industry

RADSAGA

European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

SEU Tolerance

The SEU tolerance is a combination of several factors

Process Technology

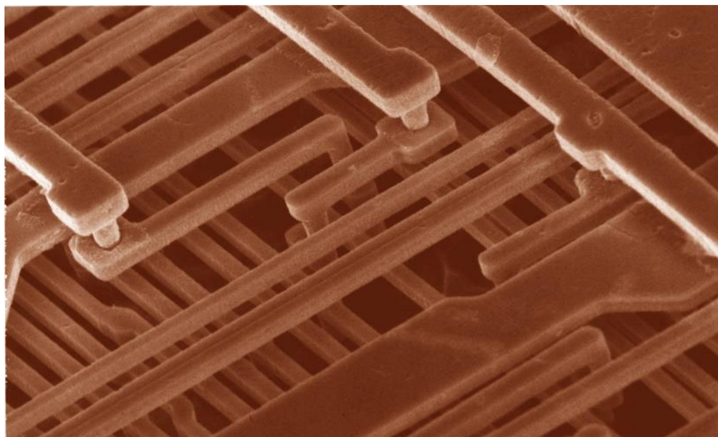
Circuit Design

SEU Tolerance

Device Density

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

Process Technology: STM C65 SPACE



Features

Process

- STMicroelectronics C65SPACE (65nm CMOS)
- 3.3V IO gate oxide GO2 (5nm)
- 1.2V core gate oxide GO1 (1.8nm), triple VT transistors
- 7 copper metallization,5 thin and 2 thick
- Low-K inter-metallic dielectrics for thin metal layers
- High density SRAMs
- Compatible with flip-chip and wire bonding packaging

Radiations

- SEL-free up to LET = 60Mev/mg/cm2 at 125°C Tj and Vdd max
- SEE hardened library
- Tested up to a total dose of 300 krads (Si)

Reliability

- Library cells models with 20 years aging
- Transistor models including aging alteration
- ESD better than:
  - 2kV in HBM (Class 2 / MIL-STD-883H)
  - 150V in MM
  - 250V in CDM

Library offer

- Comprehensive library of standard logic with PVT and aging corners models
- IO pad libraries provide interfaces at 3.3V +/- 0.30V, 2.5V+/-0.25V and 1.8V +/-0.15V
- High speed IO Pad LVDS supplied at 2.5V +/- 0.25V up to 650Mbps
- Cold sparing IOs with single/double row support
- Memories generation: single port SRAM, ROM, Dual port SRAMs, BIST library, EDAC library
- Wide-range PLLs 1.2GHz with multi-phase outputs
- 6.25Gbit/s high speed serial links (HSSL)

Design flow

- An ST customized design flow (RTL to GDS) invoking commercial solutions (Synopsys, Cadence, Mentor…) is available for partners and certified design houses:
  - Front-End kit from RTL to gates based
  - SiPKit for IO ring generation
  - FFKit for place and route
  - SignOffKit for final verification before tape-out
- For customer owned tools (COT) flow, ST provides the C65SPACE design platform along with the DRM and sign-off kit.

Description

The C65SPACE is fabricated on a proprietary 65nm, 7 metal layers CMOS process intended for use with a core voltage of 1.2V ±0.10V.
The ST standard-cells, memories and PLL have been designed and characterized to be compatible with each other.

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

Circuit Design: STM RH65nm Skyrob library

ST 65nm rad hard library

Technology	Std cells libraries	Total Cells-drives	Target
65 nm SPACE	CLOCK65LPSVT	110	Clock Network
	CORE65LPSVT	866	General purpose
	SKYROB65LPSVT	15 (DFF) 58 (Combinatorial)	Radiation Hardened
	SKYROB65LPLVT	15 (DFF) 58 (Combinatorial)	Radiation Hardened (Q2-2012)
	PRHS65	154	Place & route cells

- All cells latchup immune (characterised up 80Mev)
- Rad Hard cells, SEU rate enhanced by a factor ~ 100 compared to commercial cells
- Library cells ageing models extended from 10 years (commercial library) to 20 years (Space library)
- Ageing models sustaining temperature ranges from -40°C to +125°C Tj
  Extreme corners simulations supported:
  - MAX (125°C Tj/Process Slow/Voltage MIN/20 year ageing)
  - MIN (-40°C Tj/Process Fast/Voltage MAX/0 year ageing)
- -55°C characterisations have been carried out under CNES contract LIBEVAL
- Library fully compatible with standards flows based on Synopsys or Cadence

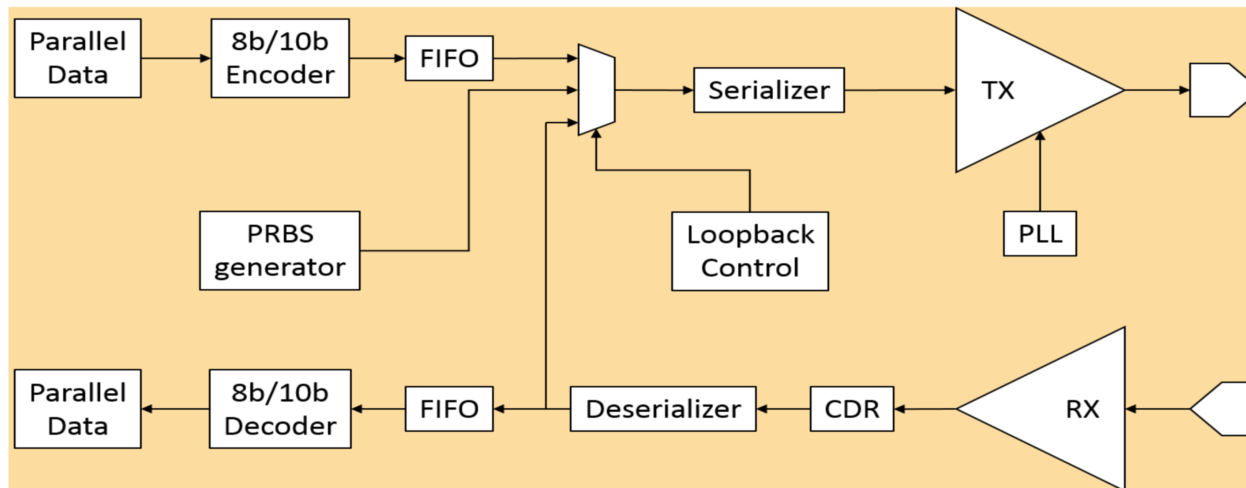
European Space Agency

ESA UNCLASSIFIED – Releasable to the Public

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

Device Density: NX FPGA Design Strategy

- NanoXplore technology is **90% full custom**
  - Technology independent
  - We can target the most advance process node (i.e 7nm end 2016)
- We have a very strong experience in designing digital and analog full custom cells
- For instance, we have launched project VELOCE in October 2015 to design a 6,25Gbs **SerDes in 65nm STM**
  - Tape-out October 2016 – Evaluation ongoing



RADSAGA

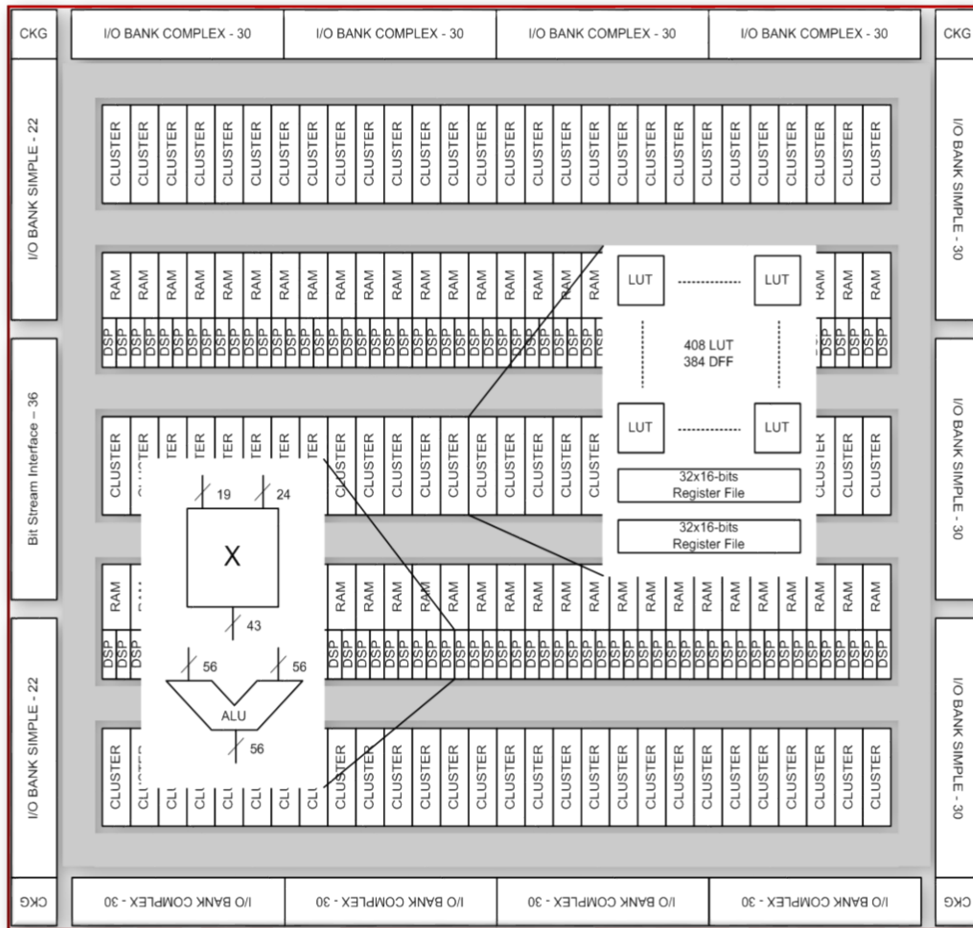
European Commission

RADECS 2017 CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

NG medium FPGA



- STM 65nm process
- Medium complexity
  - *35K LUT4 & DFF*
  - *2,8Mb RAM*
  - *112 DSP blocks*
  - *SpW link interface*
    - *(1 CODEC, 16 PHY)*
  - *16 DDR/2/3 PHY*
  - *Up to 374 User I/Os*
- Radiation Performances
  - *TID > 300krads(Si)*
  - *SEL immune*
  - *SER: § further slides*

RADSAGA

European Commission

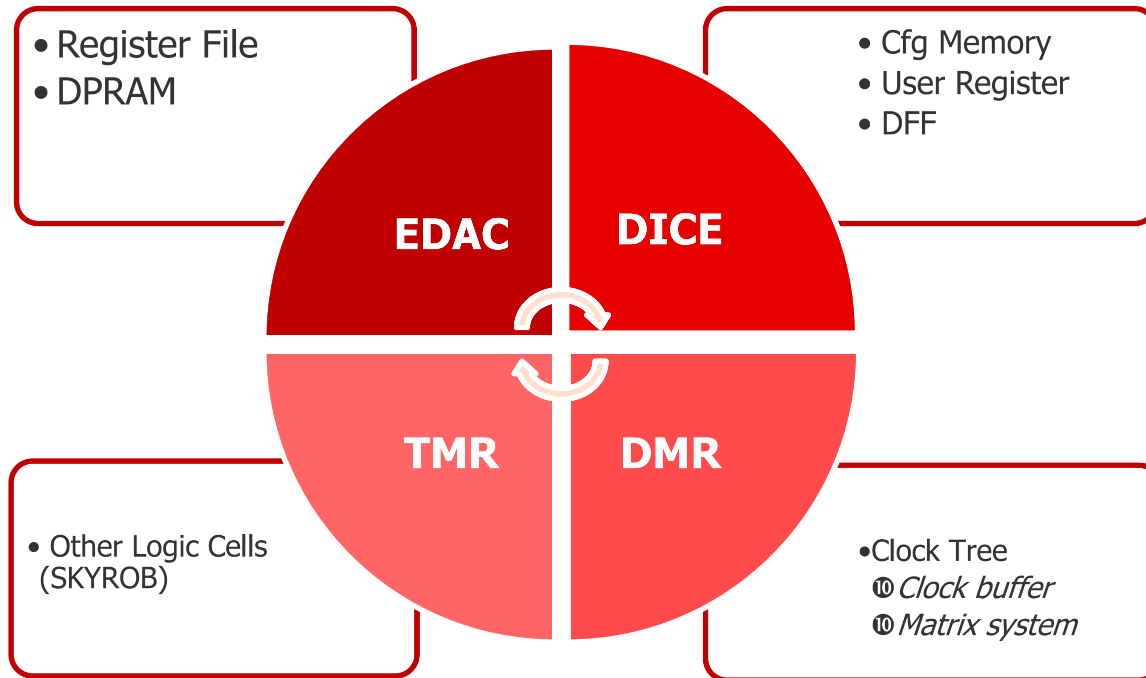
RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

NX FPGAs are Rad Hardened

All logic of NX FPGAs is hardened by design (RHBD) and simulated with TFIT software



On top of it,
Embedded Configuration Memory Integrity Check ("CMIC")

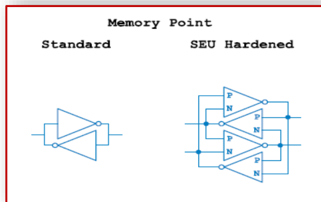
RADSAGA
European Commission
RADECS 2017 CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

DICE cell

- Regarding Radiation Hardened Memory Cells & DFF, all solutions go against the level of integration, since we add transistors.
- 5 well-knowns solutions:
  - *DICE cell (12T)*
  - *HIT cell (12T)*
  - *LIU cell (15T)*
  - *ROCKET cell (16T)*
  - *WHITAKER cell (16T)*
- Choice of DICE *



The SEU Hardened Memory point can only change value if 2 channels switch at the same time ➔ An ion impact on a single channel cannot flip the memory.

SEU hardening of flip-flops and SRAM

standard latch

Resistor memory cell

HIT memory cell

DICE hardened memory cell

esa Microelectronics Section

TWEPP 2010
21 September 2010
(9)

* DICE stands for Dual Interlocked storage CEll

RADSAGA

European Commission

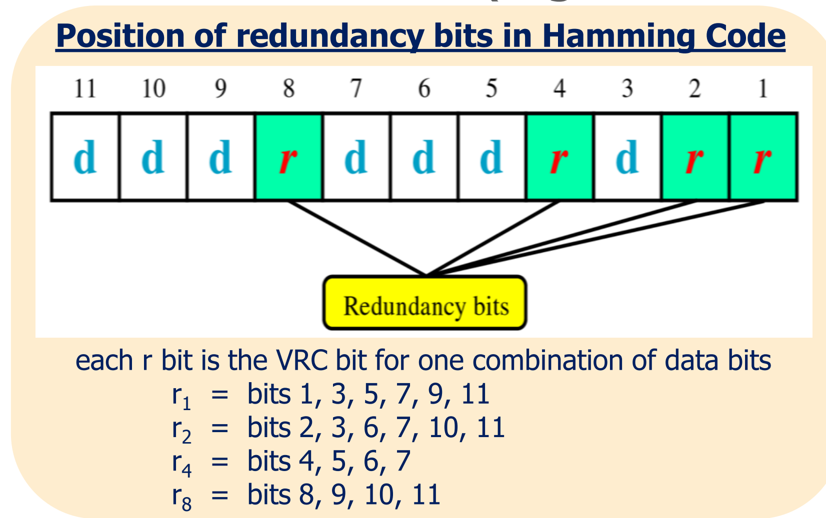
RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

EDAC Overview

Error Detection And Correction:

- **Fundamentals**: Instead of saving the data as they are, they are stored making use of an error correction code (E.g. Hamming Codes)



- **Advantages**:
  - *Easy implementation*
  - *Able to Detect and Correct SEUs*
  - *Able to Detect MBUs*
- **Drawbacks**
  - *DPRAM 48Kb effective size decreases*
    - *2K * 24 without ECC*
    - *2K * (24 bit: 18 data bit with 6 bit ECC)*
  - *Can detect but not correct any sort of MBUs (~1-2% of Soft-Errors)*

RADSAGA

European Commission

RADECS 2017 CERN, Geneva

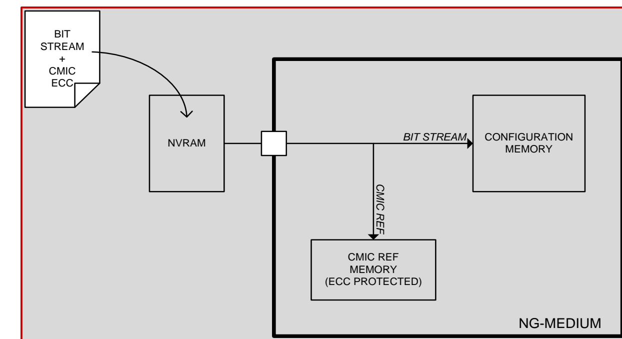
© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

CMIC Overview

CMIC= Configuration Memory Integrity (= Scrubber Ctrl)

- The CMIC is an embedded engine performing automatic verification and repair of the configuration memory.
- A CMIC reference memory is initialized during the bit stream download process with reference data computed by the NanoXmap software.
- Once the initialization is done, the CMIC engine can be periodically activated to perform the following sequence:
  - 1. Read configuration data
  - 2. Calculate signature
  - 3. Compare the signature with CMIC reference
  - 4. If a mismatch is detected:
    - *a. Calculate faulty address (BAD @) and faulty bit location*
    - *b. Read DATA[BAD @]*
    - *c. Repair flipped bit*
    - *d. Write DATA[BAD @]*



- The CMIC period can be set by the user. The minimum period is 5.3 ms and the maximum 65 days. The configuration memory scan takes 4ms.
- The CMIC reference memory is protected by ECC.
- The CMIC does not need to access the external NVRAM when performing checks and repairs at run time.

RADSAGA European Commission RADECS 2017 CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

medium Radiations Results

north
Earth
south
inner belt
outer belt
outer belt

RADSAGA

European Commission

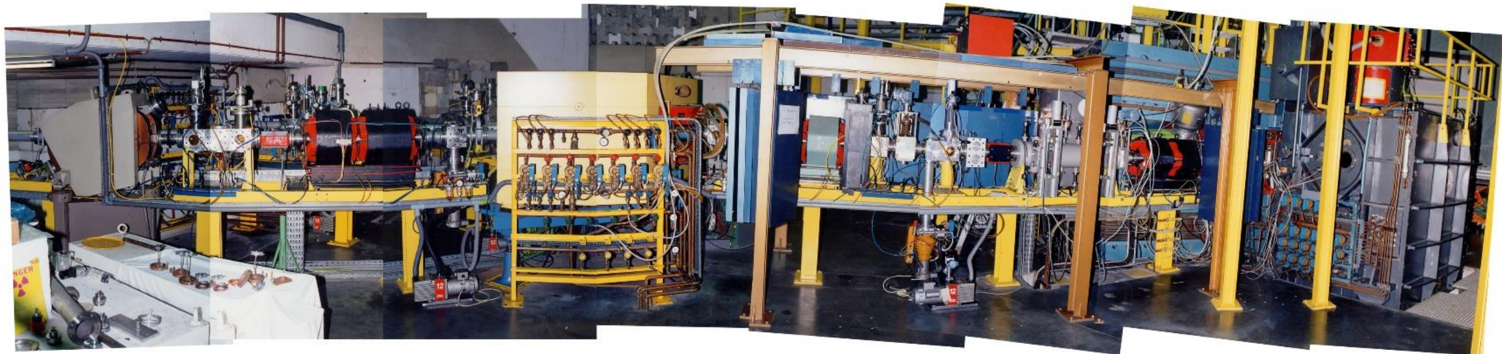
RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

SEE campaign

UCL
Université catholique de Louvain

- 2 SEE campaigns done in Q4CY16
  - 1st silicon used, out of wfab in Summer-16,
  - Packaged in LGA625 tested,
  - First radiative test done in October 2016:
    ➔ *memory configuration test done – SER / day device level 1.96e-4*
  - Second radiative test campaign done end of November 2016:
    ➔ *DFF static and dynamic test, CMIC and DPRAM*



RADSAGA

European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

SEE campaign

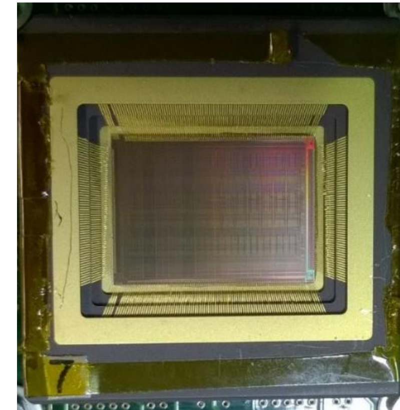
Ion Beam cocktail used (High penetration ions):

Ion	DUT energy [MeV]	Range [µm Si]	LET [MeV/mg/cm²]
$^{13}C^{4+}$	131	269.3	1.3
$^{14}N^{4+}$	122	170.8	1.9
$^{22}Ne^{7+}$	238	202.0	3.3
$^{27}Al^{8+}$	250	131.2	5.7
$^{40}Ar^{12+}$	379	120.5	10.0
$^{53}Ni^{18+}$	513	107.6	16.0
$^{58}Ni^{18+}$	582	100.5	20.4
$^{84}Kr^{25+}$	769	94.2	32.4
$^{124}Ni^{35+}$	995	73.1	62.5

More information: http://www.cyc.ucl.ac.be/HIF/HIF.php

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

Radiations: SEU / SET Tests Overview



- Temperature measured 19->34° C
- Supply at their min value (-10%):
- VDD1V2 Core supply 1.08V
  - **No voltage sensor->1.045V inside the chip.**
- Angular cross-section for config given in chip plan
- Normal incidence for other tests
- Fluence over 10^6 p/cm² for config, static DFF, dynamic DFF

Test	Devices under test
Config SEU	6 138 096 configuration memory
DPRAM SEU	56 DPRAM with EDAC ST_DPHD_2048x24m4_b = 2 752 512 bit
DFF static	32 256 DFF
	1008 matrix system output of the clock tree

RADSAGA

European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

Radiations: SEU / SET Tests Results

- Chess-board pattern
- SER normal incidence

Weilbull parameter chip6+7	
SIGsat (cm2/bit)	5.1852E-09
L0 (MeV/(mg/cm²))	0.11214
W (MeV)	36.4286
s	4.44737

- Orbital Upset Rate calculation (CREME 96 model):
  - GEO
  - solar min
  - shielding = 100mils
  - sensitive volume thickness = 2µm
  - Unhardened SRAM SER /9400

Configuration Memory SEU @ 30°C,1.045V	SER
SEU/config/day	**2.7E-11 SEU/config/day**
SEU/chip/day	1.7E-04 SEU/chip/day
SEU/chip/year	6.1E-02 SEU/chip/year ➔ SER 16,4years

RADSAGA

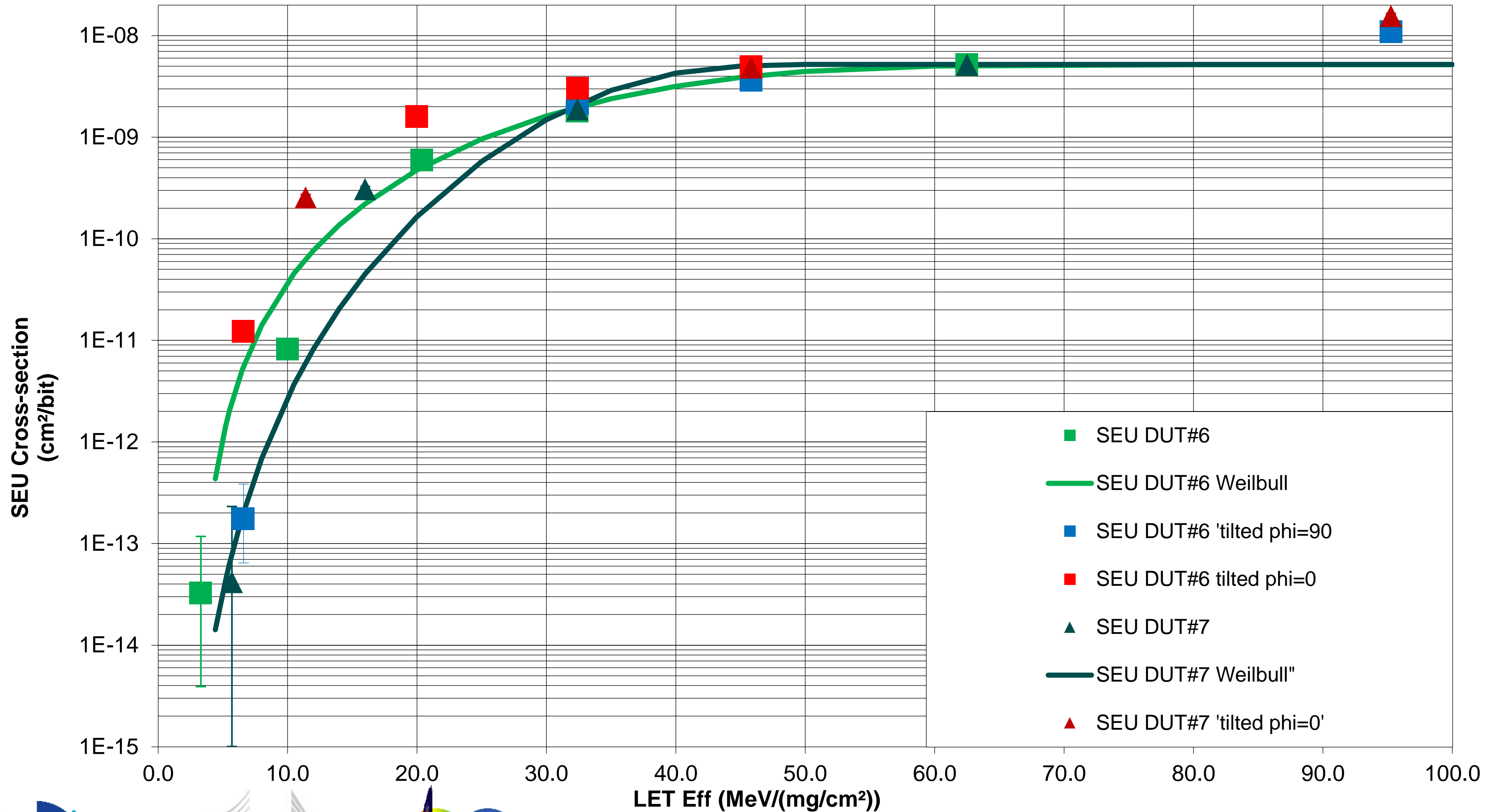
European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

Radiations: Config SEU



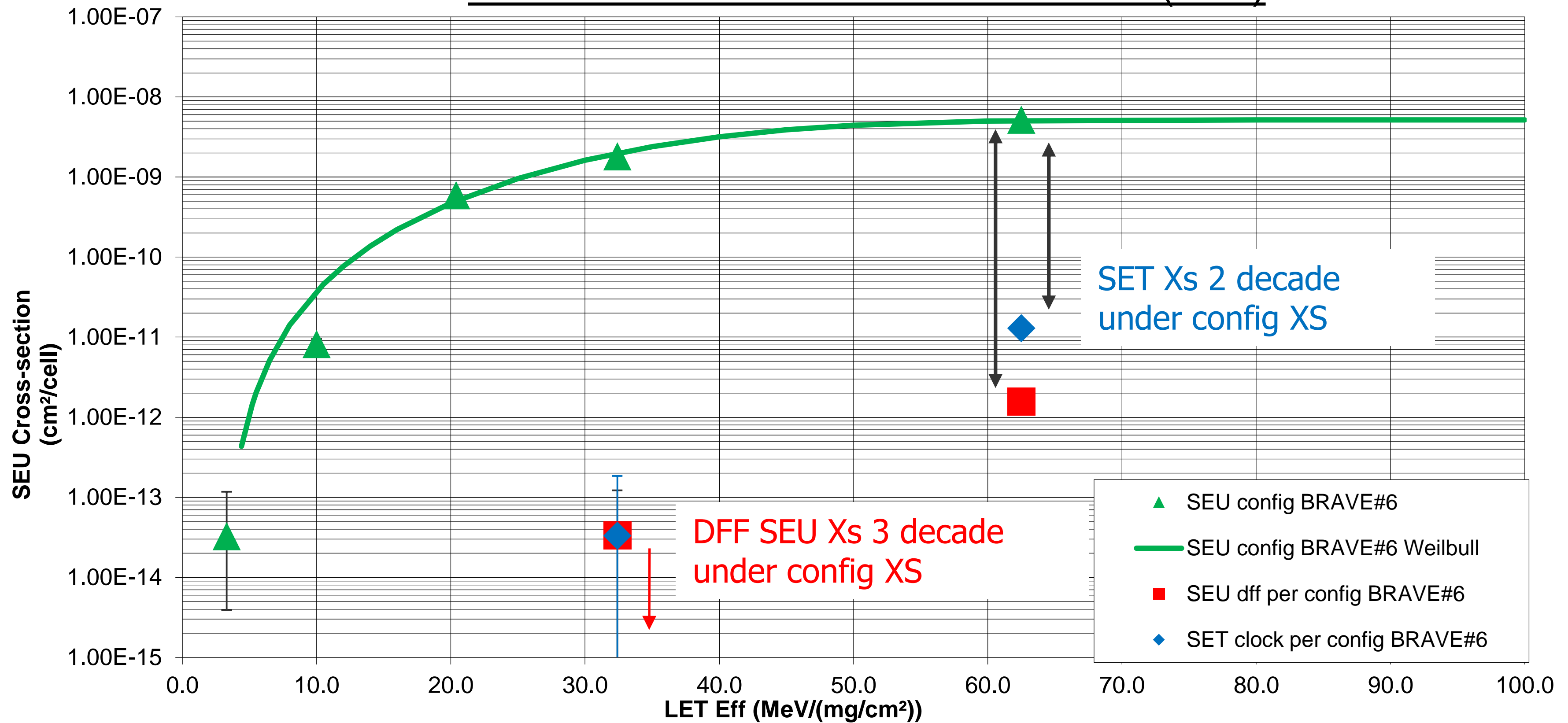
RADSAGA

European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

Radiations: Static DFF SEU, clock SET



RADSAGA

European Commission

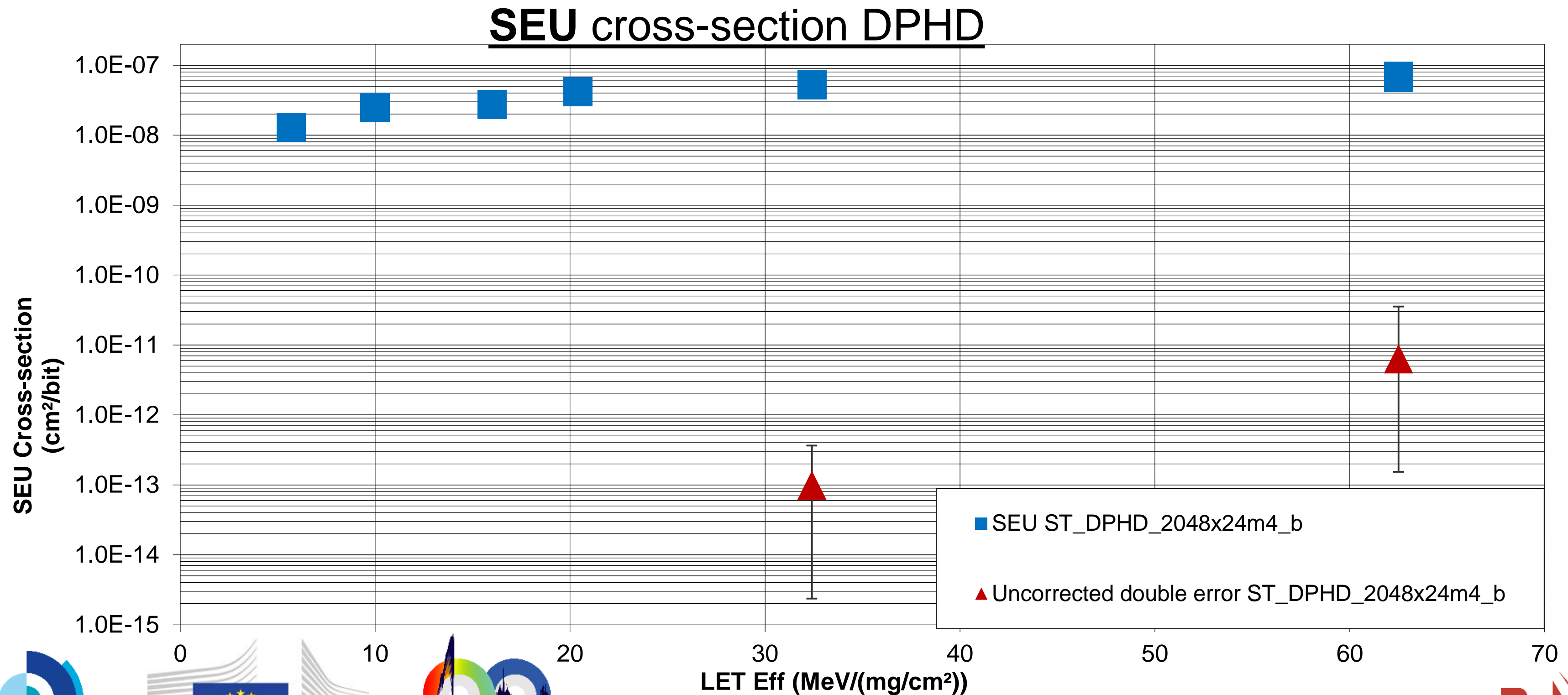
RADECS 2017 CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

Radiations: EDAC Results

- Double error cross section tow decades lower than these of config
- 6 138 096 config > 2 752 512 DPRAM bit

→ Chip level: **DPRAM SER << config SER**



RADSAGA

European Commission

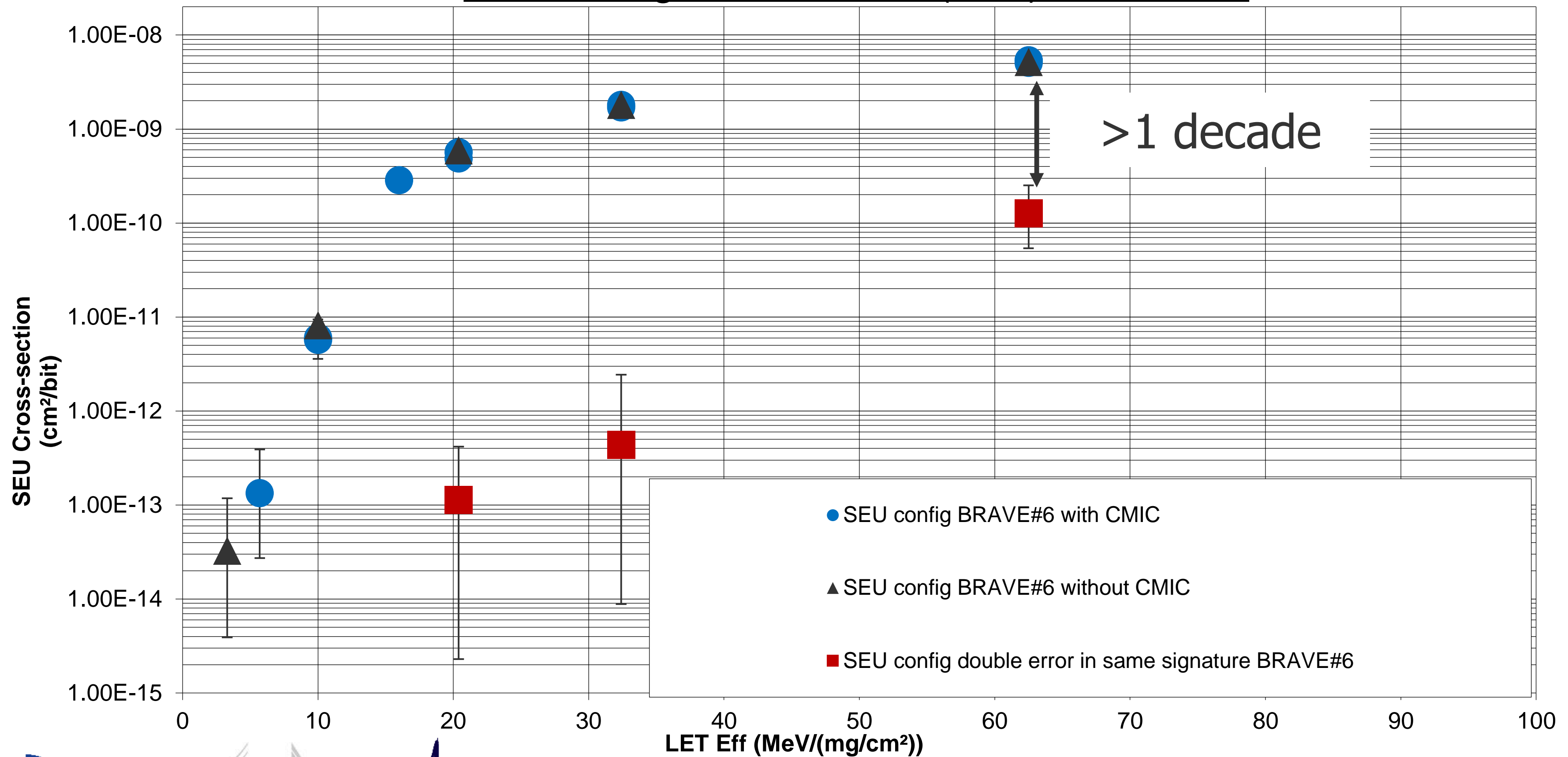
RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

Radiations: CMIC Results

- No double error recorded in the EDAC reference memory ST_SPREG_144x27m4



RADSAGA

European Commission

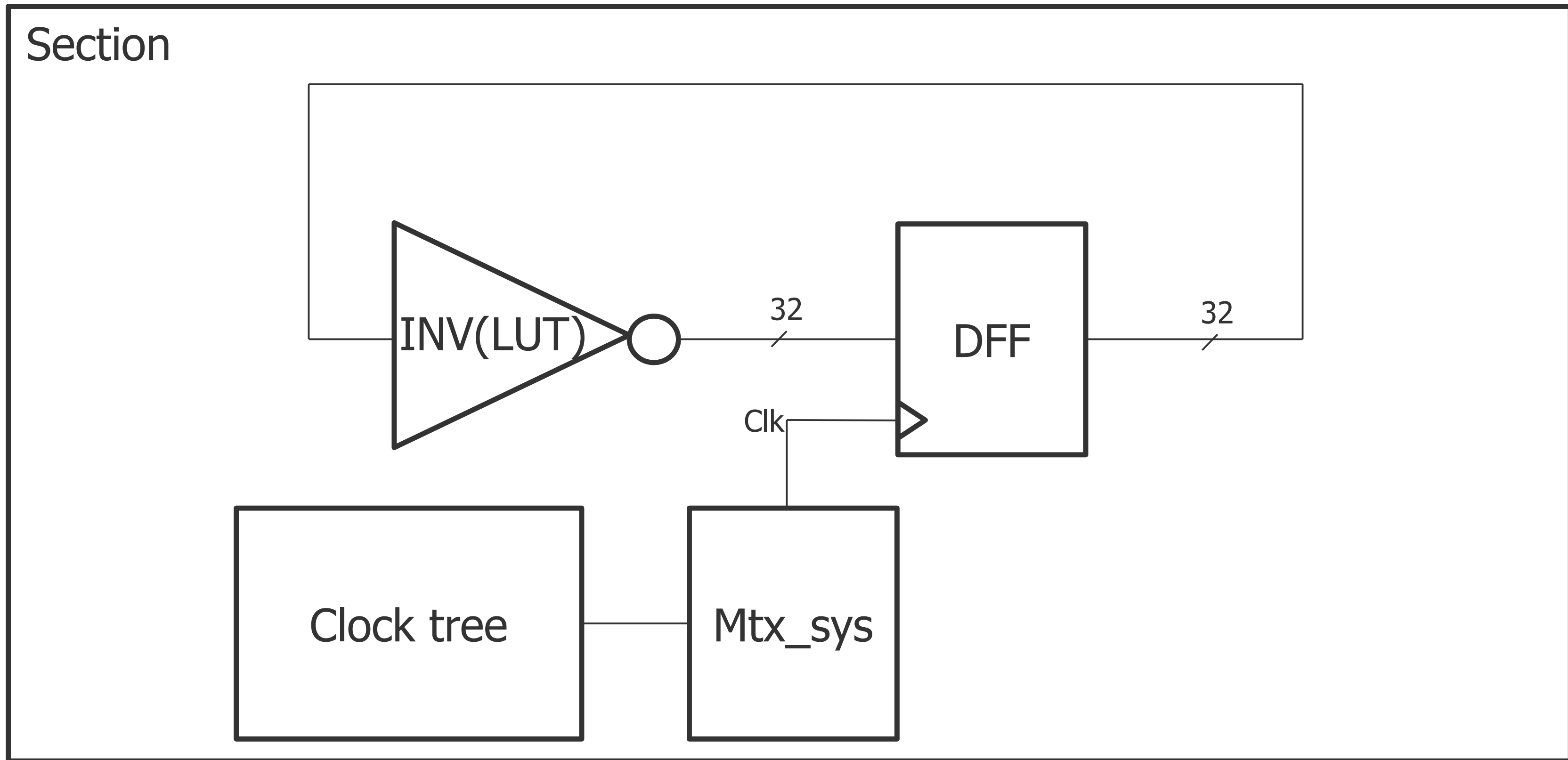
RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

Radiations: Dynamic DFF test

- DFF dynamic with no Reset



RADSAGA

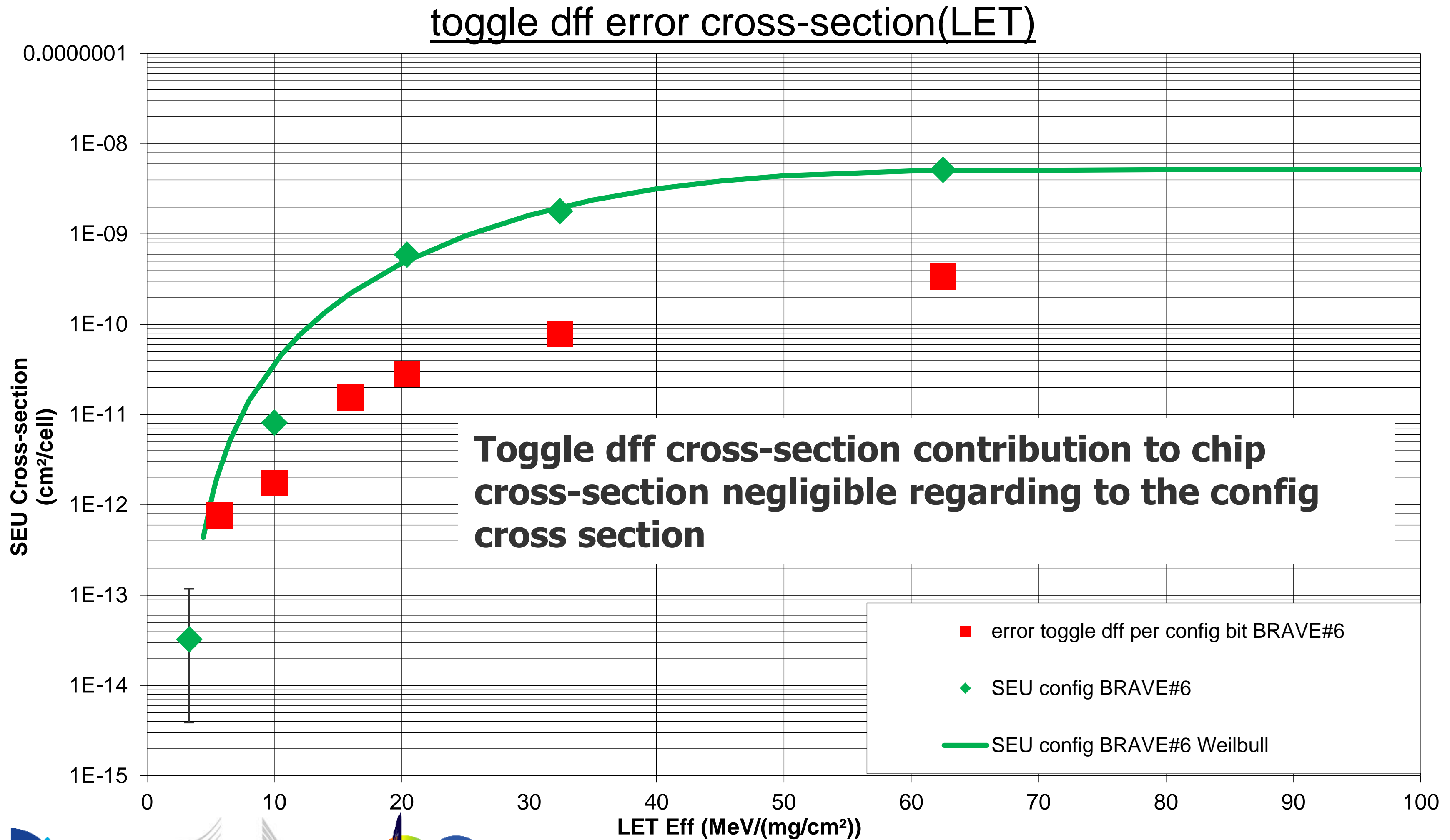
European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

Radiations: Dynamic DFF test



RADSAGA

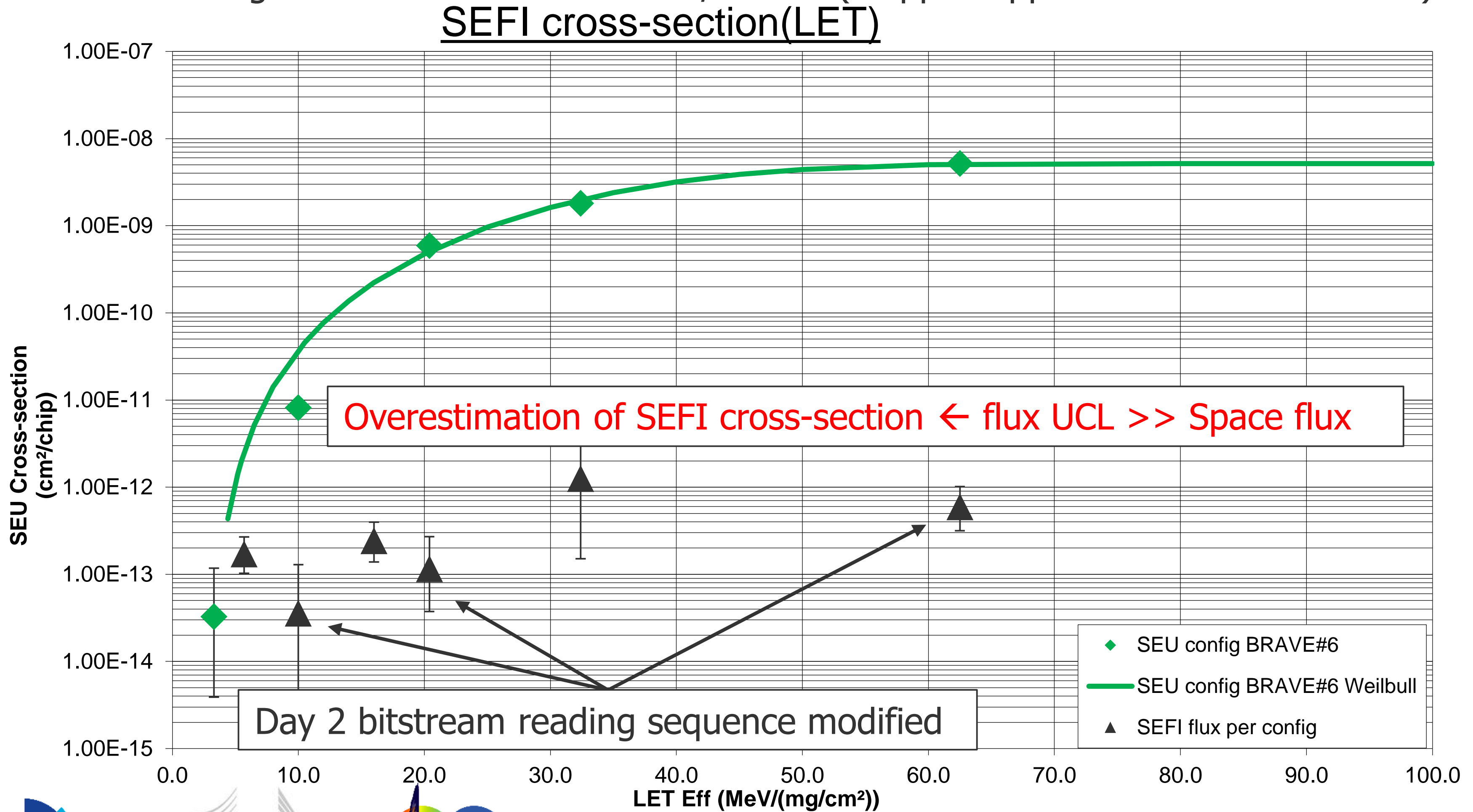
European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

Radiations: SEFI

- SEFI → Config or context can not be read/written (mapped application status unknown)



RADSAGA

European Commission

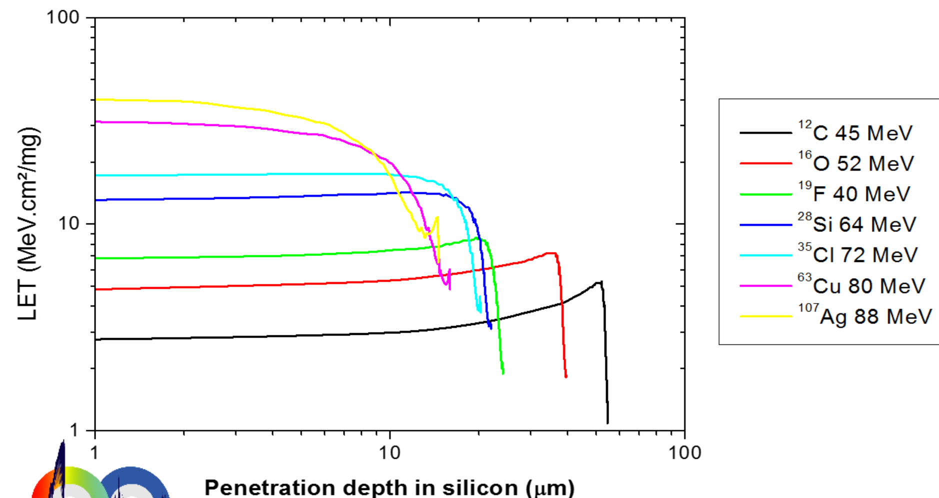
RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

Next SEE Campaigns

- Heavy Ions campaign on 2nd run NG-Medium, on behalf of VEGAS contract, at UCL HIF
- Protons campaign, done by ESA at PSI
- New Radiation campaign, expected from CERN at PSI & CHARM
- New Radiation campaign, expected from Brasilian partner
  - TID (^{60}CO & X-Rays)
  - Heavy Ions
  - Protons
  - Neutrons

- SEP17
- NOV17
- TBD
- T0= SEP17?
  - T0+4mths
  - T0+3mths
  - T0+3mths
  - T0+3mths



RADSAGA

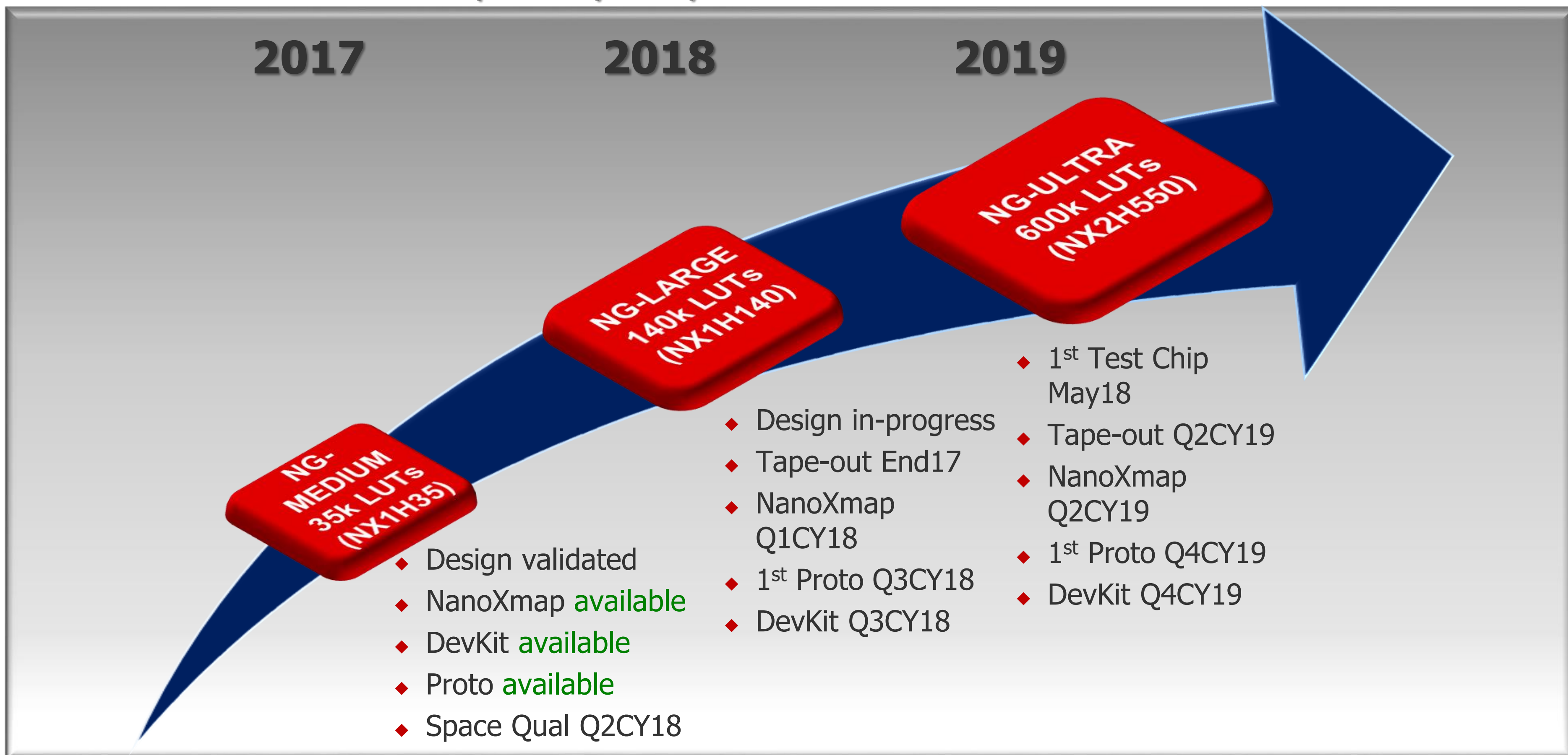
European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NanoXplore Rad-Hard FPGA Roadmap

NX has successfully delivered the NG-MEDIUM on time
and doesn't expect any delay on NG-LARGE and NG-ULTRA schedule



RADSAGA

European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX

NanoXplore

Questions & Answers
Thank you

RADSAGA

European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NanoXplore

www.NanoXplore.com

Questionnaire

Q1. What are 3 factors which have impact of SEU performances?

- Answer: The 3 factors are
  - Process Technology
  - Circuit design
  - Device density.

Q2. Which are NX design solutions used to harden their FPGA devices?

- Answer: NX has used 4 different design approaches to harden FPGA devices:
  - Selection of DICE as a RHBD memory latch
  - Use of ECC for RAM blocks
  - Duplication of Clock tree
  - Extract of IP block from a European 65nm ASIC library.

  Even on top of that, NX has embed a Scrubber Controller which verifies the integrity of the bitstream, 24h a day, 7days a week and 365days a year.

Q3. What is the main interest of Weibull parameters?

- Answer: Weibull parameters allows the user to comput the orbital upset rate for a dedicated Space mission, such as LEO/EOS or GEO/SatCom.

RADSAGA

European Commission

RADECS 2017
CERN, Geneva

© 2017 Nanoxplore SAS Company Confidential
Copy not authorized without written approval

NX