



# MiniDAQ2 clock tree and clock distribution

MiniDAQ workshop  
31 July 2017

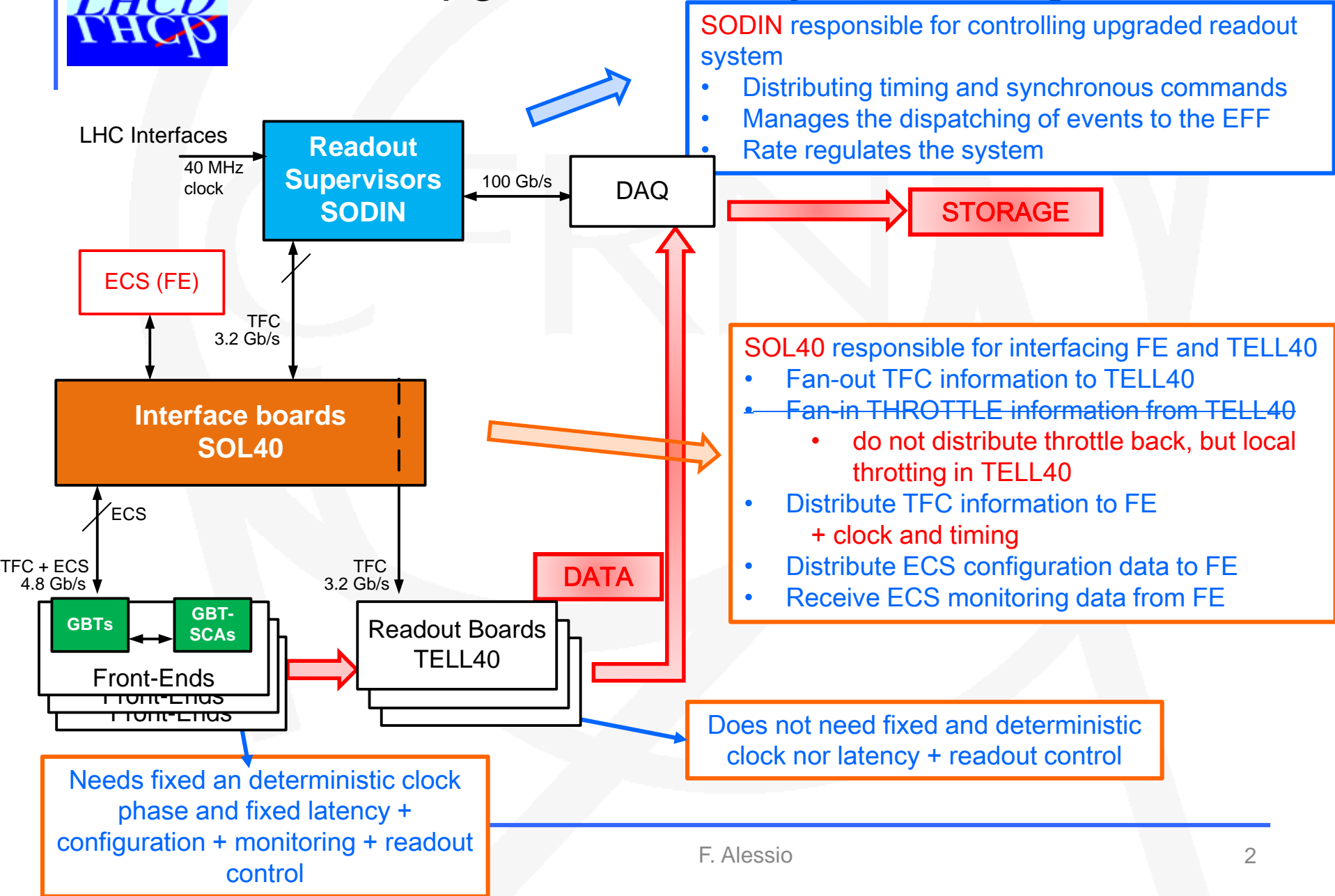
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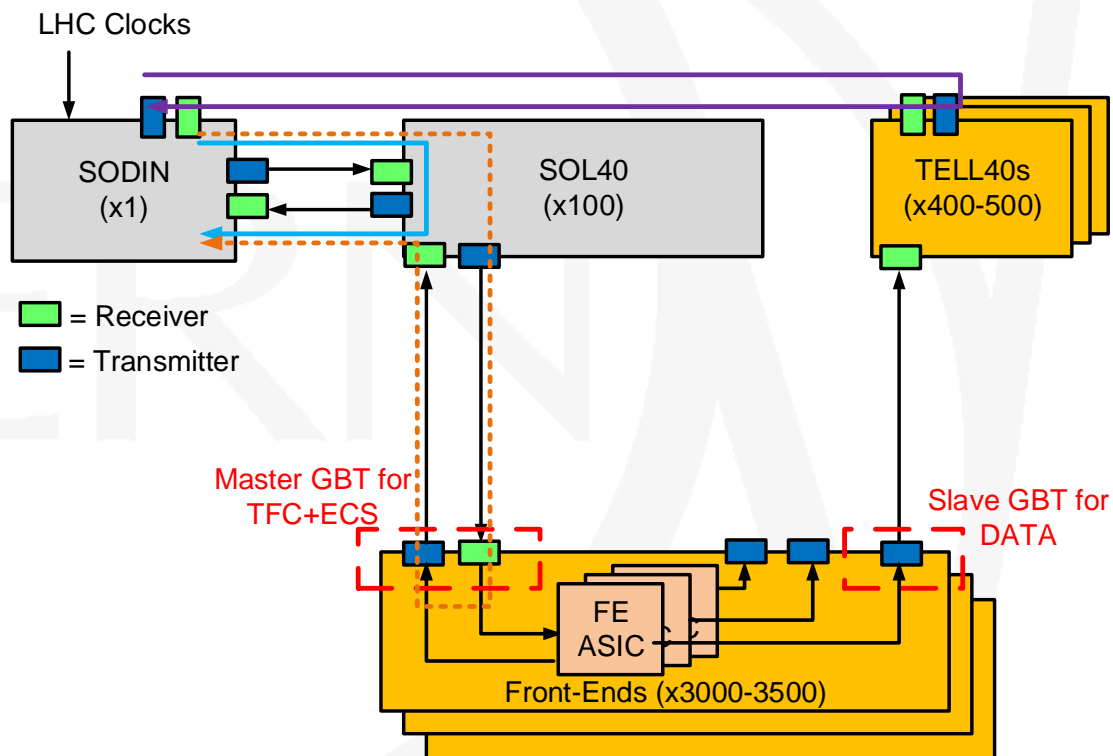
# The upgraded TFC system at a glance



# Timing and command distribution

## Master GBT @ FE controls the FE ASIC + Slave GBTs

- Clock from Master GBT
- TFC commands on e-links
- ECS configuration and monitoring through SCA
- Slave GBTs controlled through SCA from Master GBT

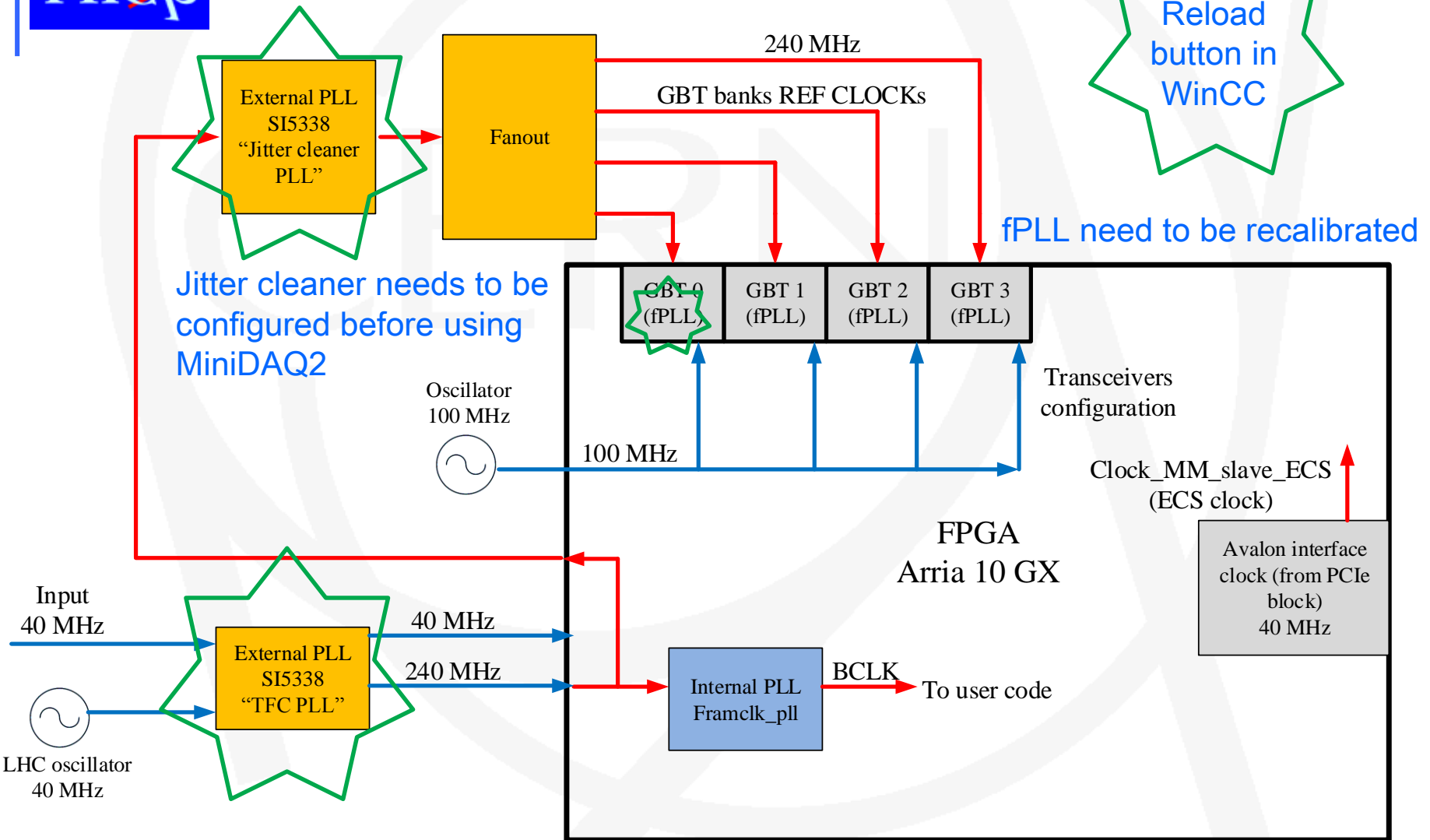


Fixed latency and deterministic phase recovery of TFC commands is ensured by combination of FPGA and GBT features

- Customization is needed to synchronize links and make sure that TELL40s decodes data properly
- Customization is needed to properly decode TFC commands
- ECS to FE through TFC links via SOL40 (Joao)



# Clock tree on MiniDAQ2



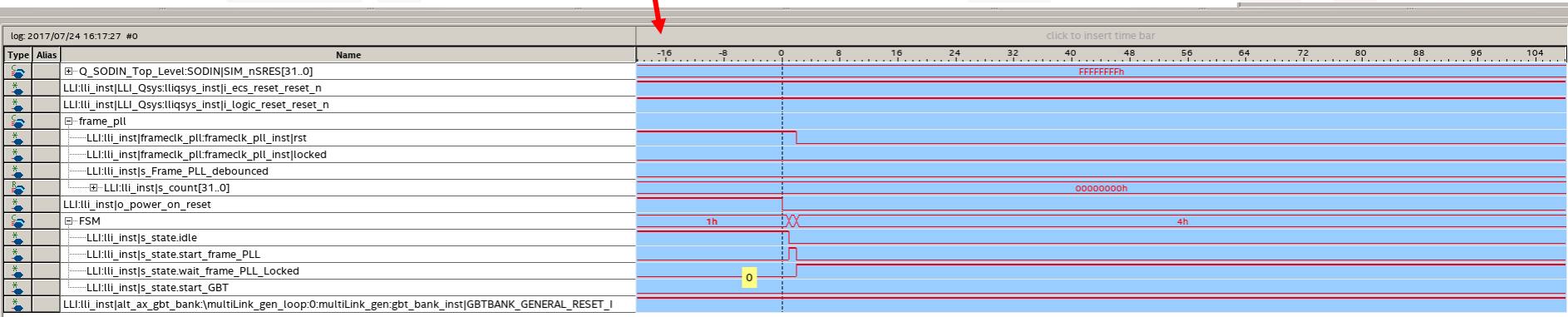
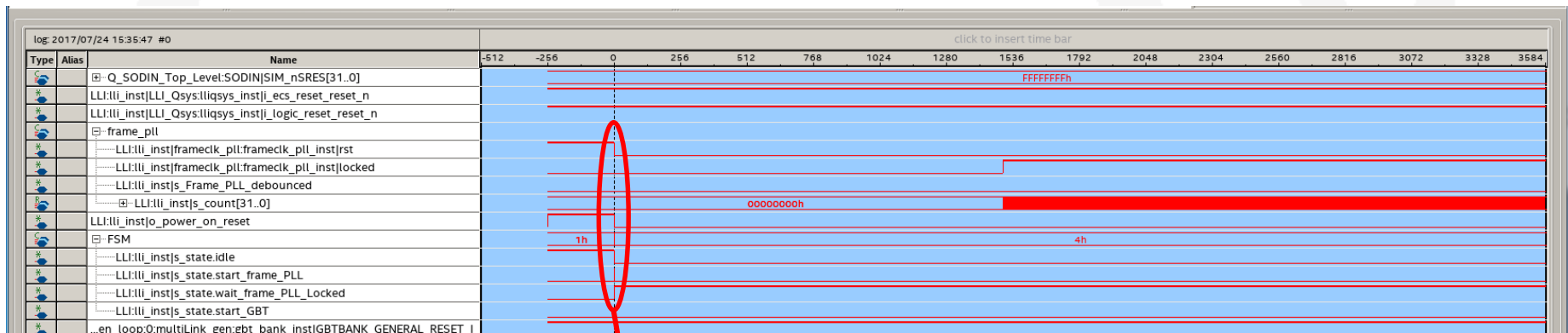
This is already hard configured, no need to do anything





# Power-on procedure

Power-on procedure to make sure that clocks are well generated (Fred Hachon)



At this point the firmware waits for the fPLL to be recalibrated



# Power-on procedure

When done a register is set to 0x1 and the internal state machine starts, release the reset to the GBT banks

log: Trig @ 2017/07/27 20:13:07 (0:0:0.0 elapsed)

Type	Alias	Name	0	512	1024	1536	2048	2560	3072	3584	4096
		Q_SODIN_Top_Level:SODIN SIM_nSRES[31..0]					FFFFFFFFh				
		LLI:lli_inst LLI_Qsys:lliqsys_inst i_ecs_reset_reset_n									
		LLI:lli_inst LLI_Qsys:lliqsys_inst i_logic_reset_reset_n									
		PLLs									
		LLI:lli_inst frameclk_pll:frameclk_pll_inst refclk									
		LLI:lli_inst frameclk_pll:frameclk_pll_inst rst									
		LLI:lli_inst frameclk_pll:frameclk_pll_inst locked									
		LLI:lli_inst s_Frame_PLL_debounced									
		LLI:lli_inst s_count[31..0]					0000000h				
		LLI:lli_inst o_power_on_reset									
		LLI:lli_inst LLI_Qsys:lliqsys_inst o_system_status_export[31..0]					0000001h				
		..._gbt_bank:\multiLink_gen_loop:0:multiLink_gen:gbt_bank_inst GBTBANK_GENERAL_RESET_I									
		FPIL_Locks					FFh				
		FSM					8h				
		LLI:lli_inst s_state.idle									
		LLI:lli_inst s_state.wait_frame_PLL_Locked									
		LLI:lli_inst s_state.check_system									
		LLI:lli_inst s_state.start_GBT									

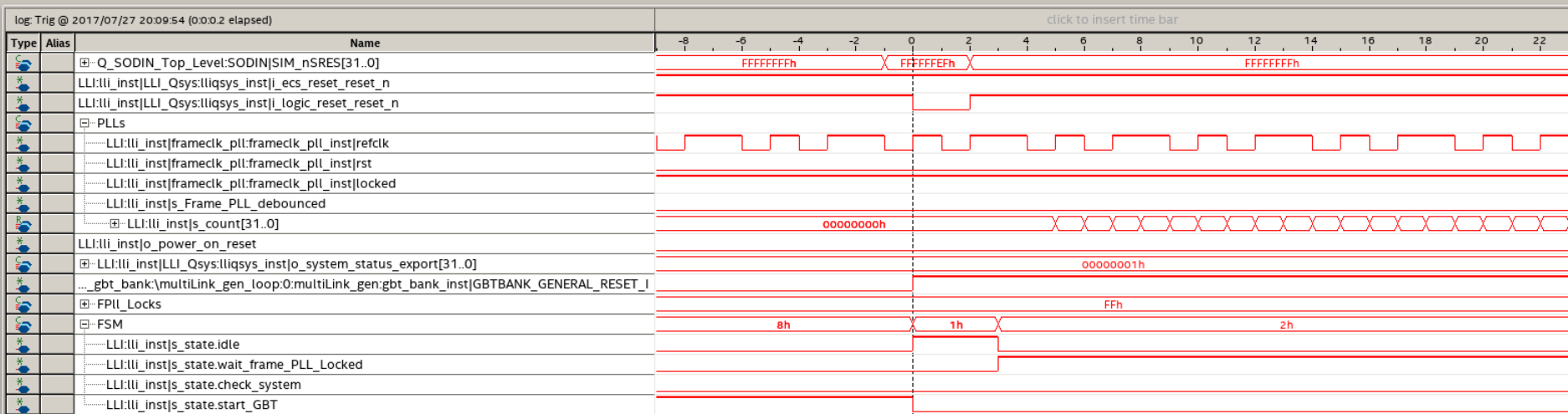
Data Acquisition can start now.





# Power-on procedure

If a «logic reset» is issued to the LLI, the procedure restarts  
Then, the user need to hit the button reload again



Data Acquisition can start again after this procedure.

# Clock tree in a GBT bank

Inside a GBT bank, the clock tree looks like this

