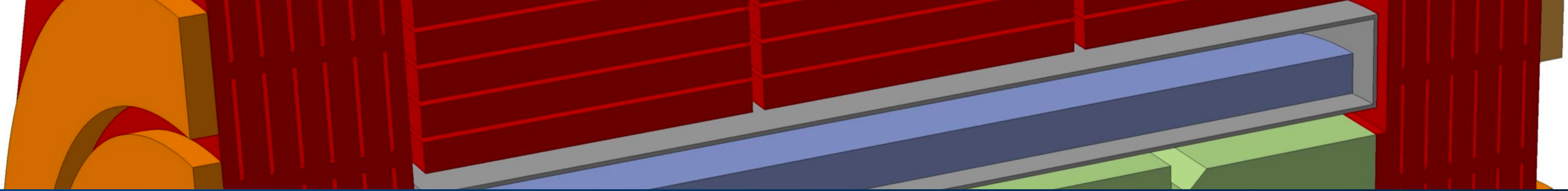
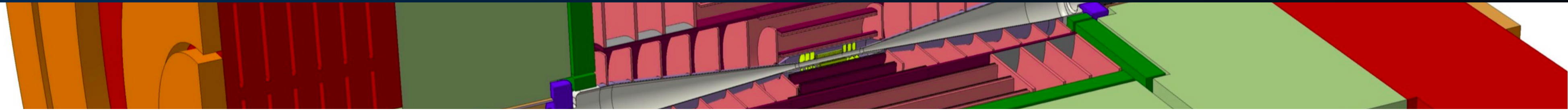


Recent progress on the SiW ECAL technological prototype

A. Irles, LAL

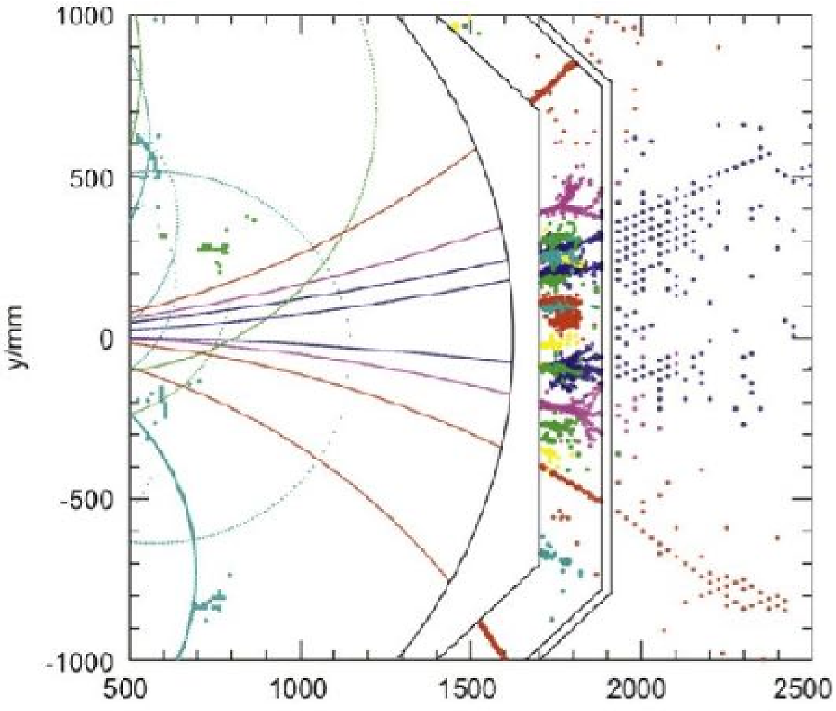
25th January 2018, CLIC Workshop



Outline of the talk

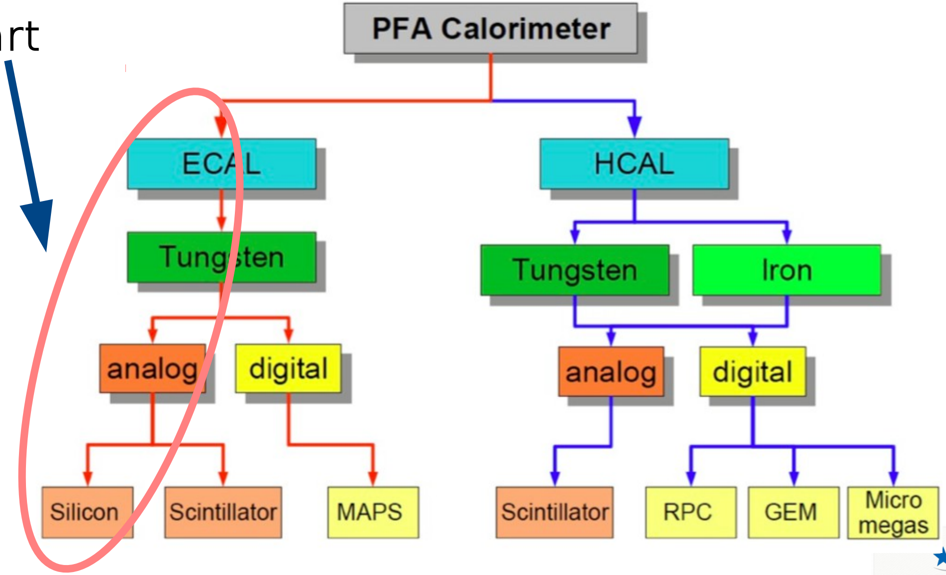
- Calorimetry for linear colliders:
  - Imaging calorimetry for detectors optimized for Particle Flow

    See F. Sefkow talk from yesterday
  - R&D conducted by the CALICE collaboration
- The SiW-ECAL technological prototype
- Beam Test 2017
- Towards a real detector: challenges
  - Long slabs
  - Compactification of the signal units
  - Compactification of the DAQ



- R&D for calorimeters for **future Linear Colliders** optimized for **Particle Flow** (PF) is conducted by the **CALICE** collaboration

- **SiW-ECAL**: one of the **ECAL** proposals for **LC.**
  - This talk will only cover this part



Basic requirements of a **PF calorimeter** for future LC *(see F. Sefkow talk from yesterday)*

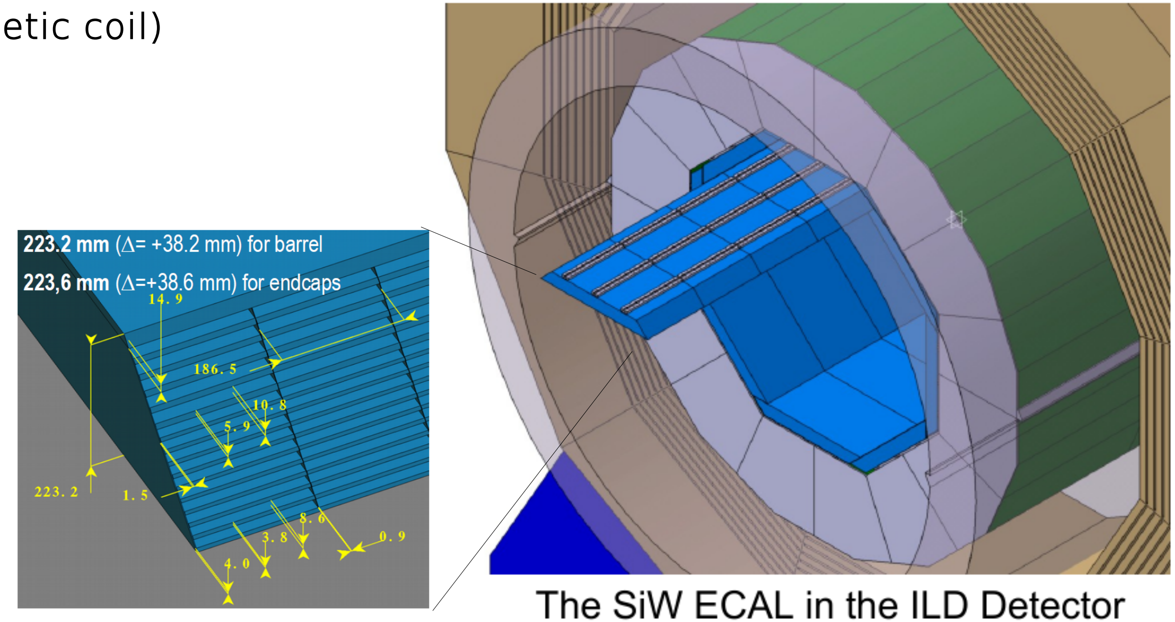
- Extreme high granularity
- Compact and hermetic (inside magnetic coil)

Tungsten as absorber material

- Narrow showers
- Assures compact design
- Low radiation levels forseen at LC
- X_0=3.5 mm, R_M=9mm, I_L=96mm

Silicon as active material

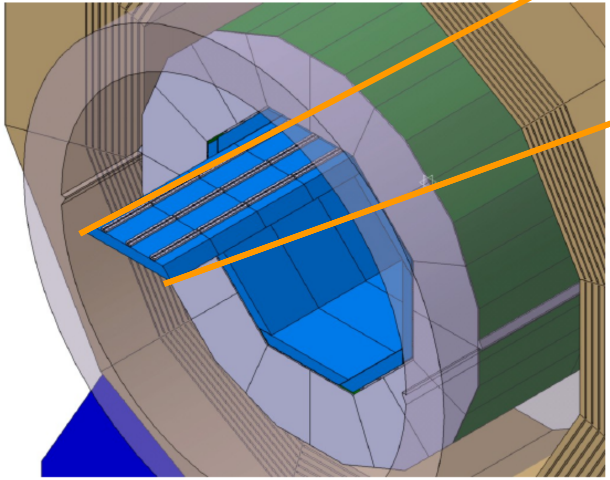
- Support compact designs
- Allows pixelisation
- Robust technology
- Excellent signal/noise ratio



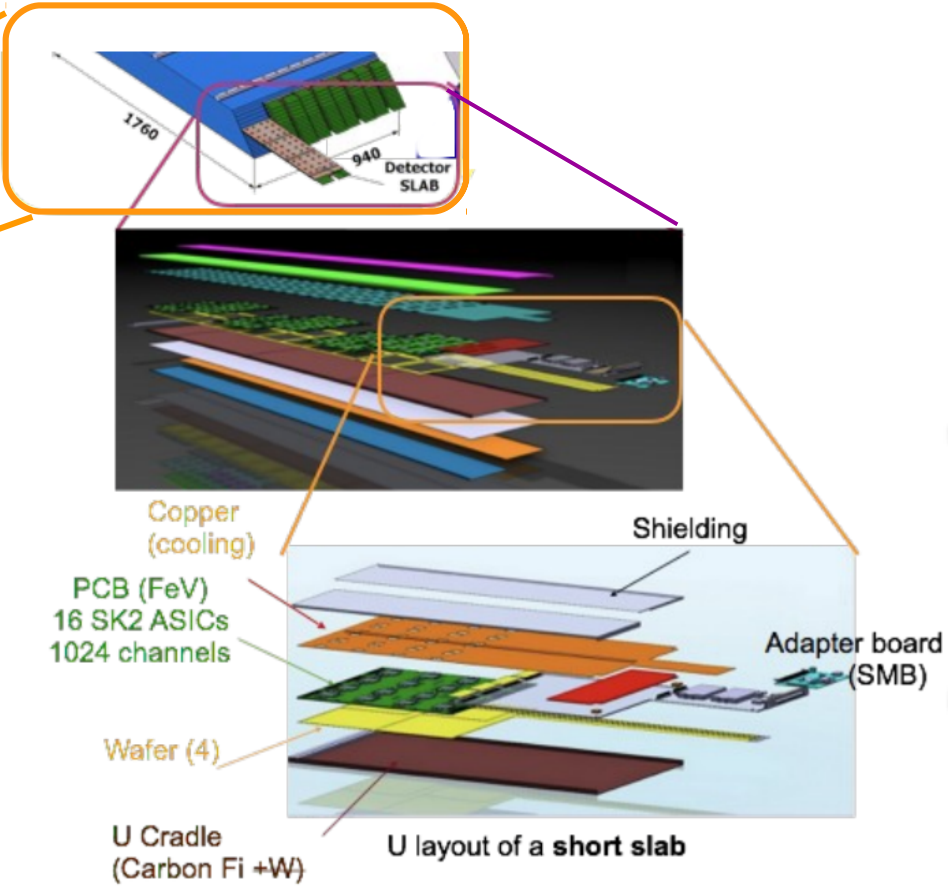
The SiW ECAL in the ILD Detector

The **SiW ECAL R&D** is tailored to meet the specifications for the **ILD** ECAL **baseline** proposal

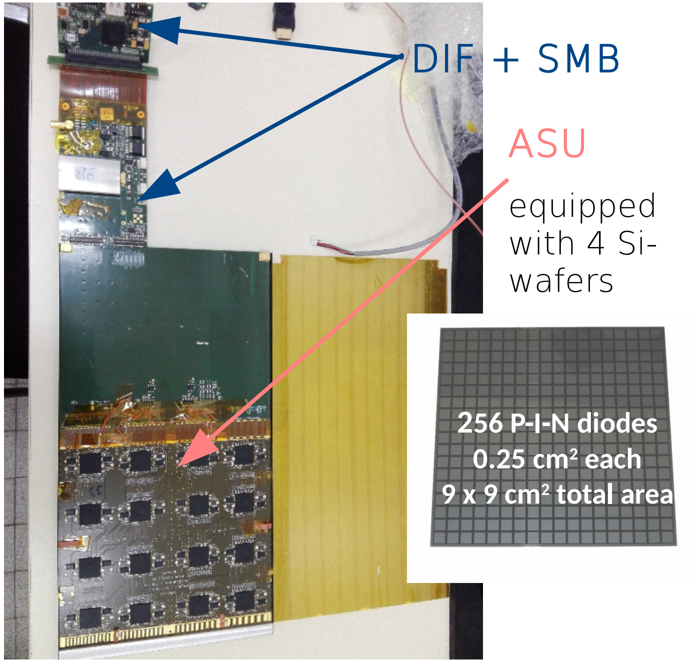
SiW-ECAL for the ILD



The SiW ECAL in the ILD Detector

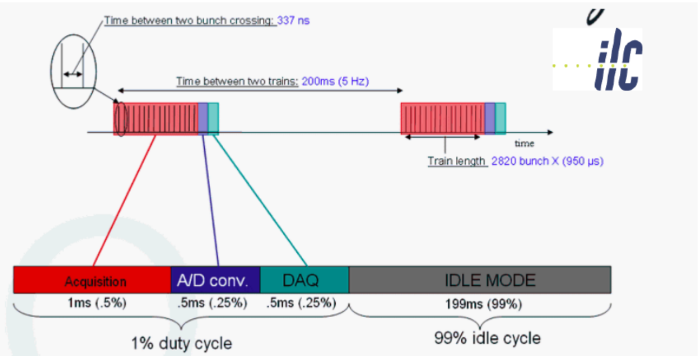


SiW-ECAL technological prototype



Short slab:

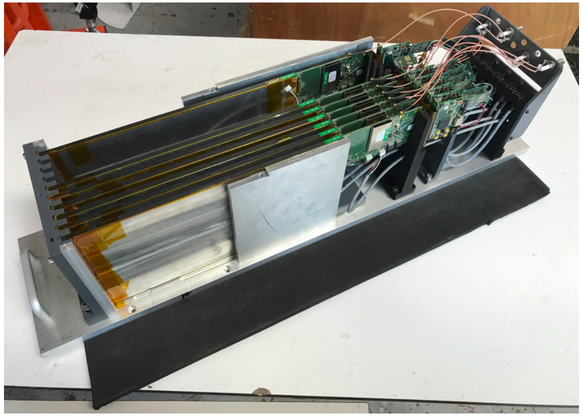
- Adapter board (**SMB**) and Detector Interface (**DIF**)
- **ASU (Active Sensor Unit),**
  - PCBs (FEV10/11) with silicon P-I-N diodes as active material (325um, 4 kΩcm, N-type)
  - 1024 channels per slab
- VFE electronics: 16 **Skiroc ASICS** (in the ASU)
  - Auto trigger, double gain ADC
  - Low power consumption & power pulsing (25µW/ch)

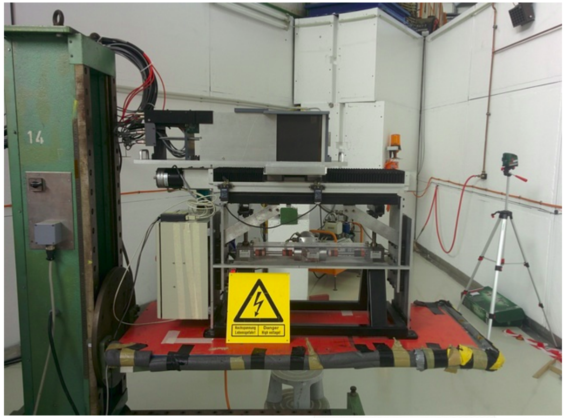


N.B. Final numbers may vary

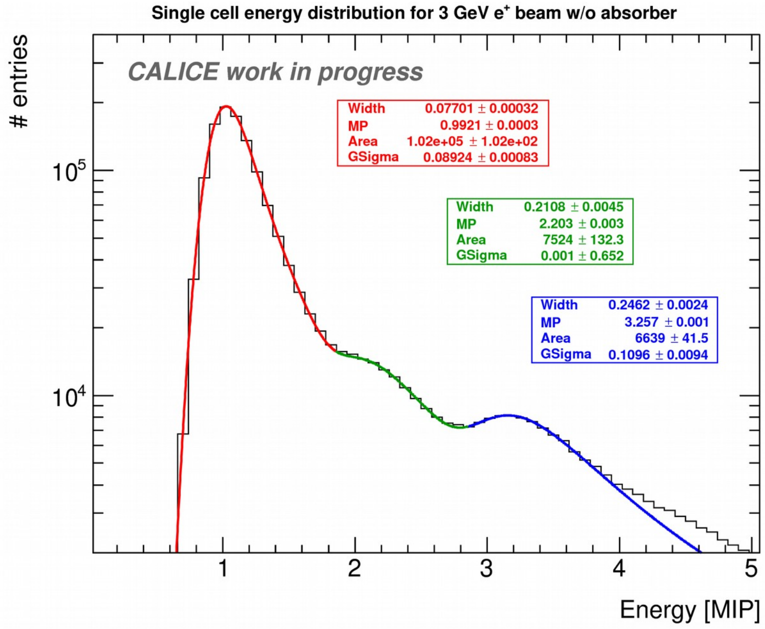
Test Beam at DESY

- **Commissioning** & Passport delivery
  - noisy channels: 7-8%: very conservative approach. It can be reduced by individual threshold settings, (sk2A)
  - 7/10 shorts slabs passed it, the other 3 were rejected for lower performance: under investigation
- **Setup** :
  - 6 FEV11, 1 FeV10 each equipped with 4 325um Si wafers and 16 Skiroc2
  - Power pulsing and ILC mode (emulated ILC spill conditions)
- **Physics program:**
  - Calibration run with 3 GeV positrons perpendicular beam without tungsten absorber plates
  - Electromagnetic showers program.
  - Calibration run with 3 GeV positrons in ~45 degrees (6 slabs)
  - Magnetic field tests with 1 slab (up to 1 T)

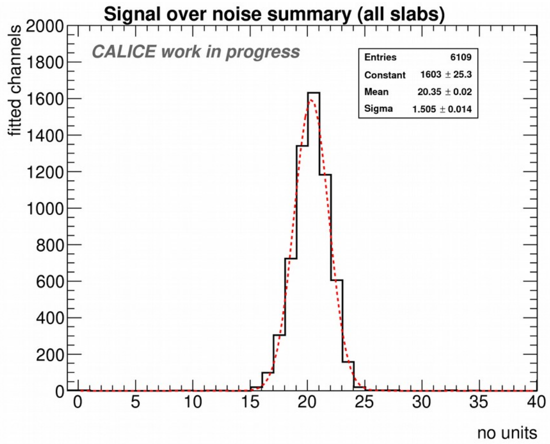




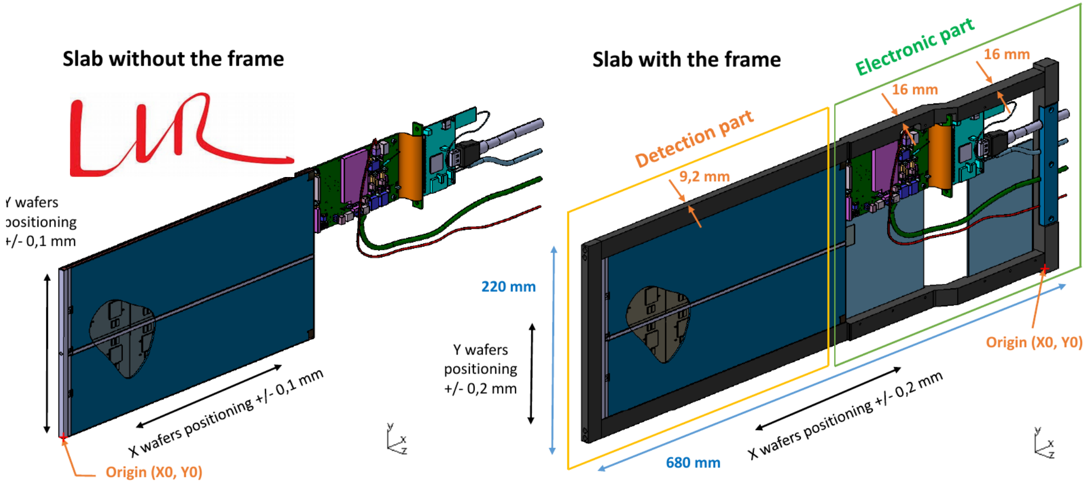
- MIP scan: Si - ECAL **(w/o the W)**
  - Positrons of 3 GeV (~2 kHz rate, beam spot with slightly irregular shape and size <2cm diameter)
  - Data used for **pedestal subtraction** and **energy calibration** for following runs.
  - Pedestal correction done chip/channel/sca wise, Energy calibration done chip/channel wise



- We **fit** the **98%** of available channels
- **MPV** = 62.2 ADC, sigma= 3.2 ADC **(dispersion of 5.1 %)**
- **S/N = 20.3**, sigma = 1.5 (7.4 % dispersion)
  (MIP position – pedestal position) / pedestal width

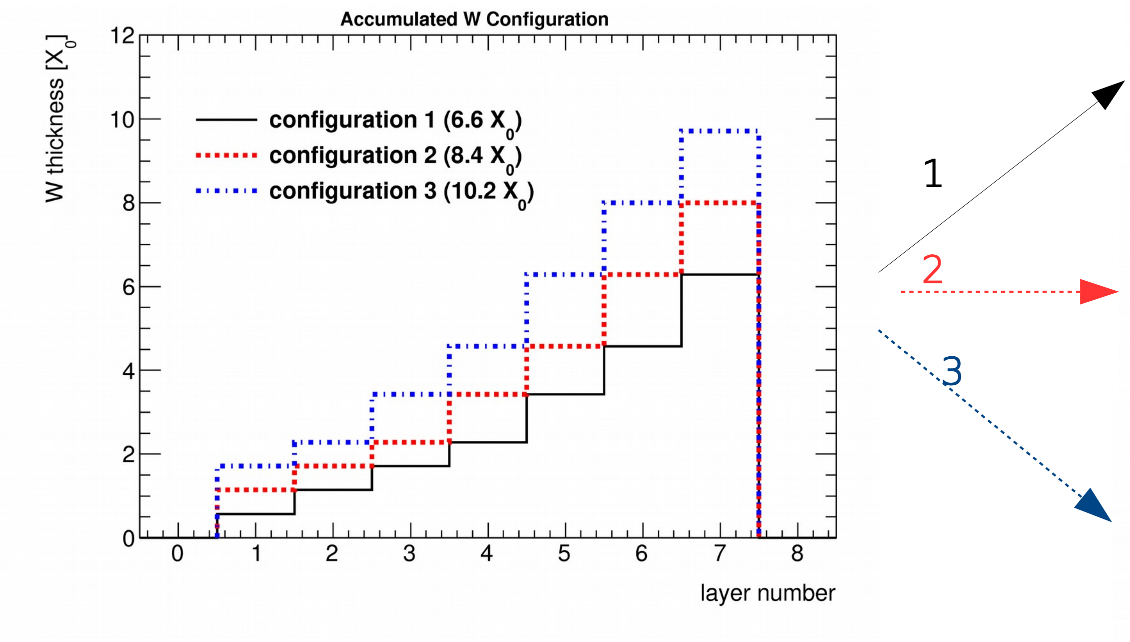


- Magnetic field tests
  - One slab in a special plastic support
  - Magnetic field from 0 to 1 T.
  - With and without beam.
- **No failure/loss of performance observed during the operation and after the first analysis.**
  - ~20 hours of data in total.



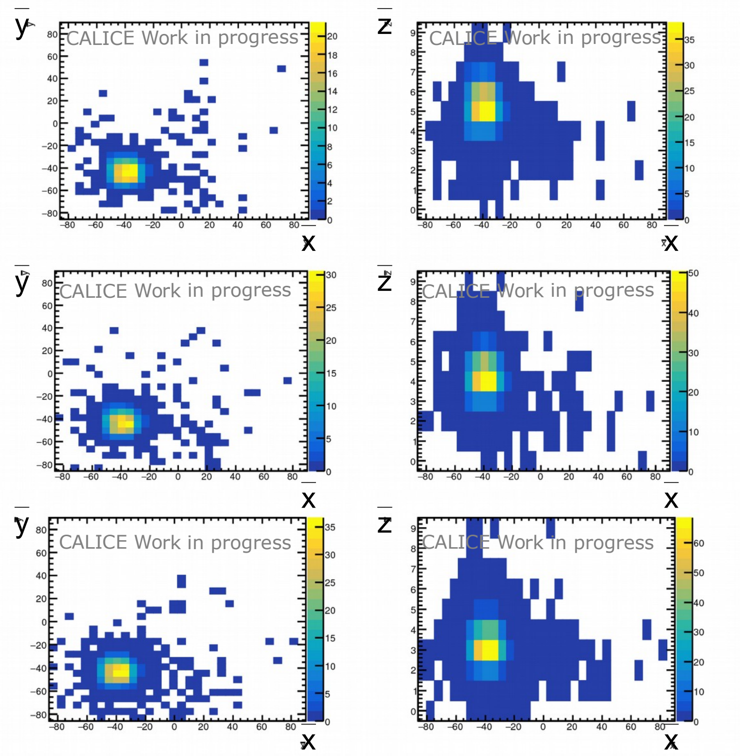
SiW-ECAL performance for electromagnetic showers

- Tungsten program
  - Scans of various energies (from 1-5.8 GeV).
  - Scan using different tungsten configurations



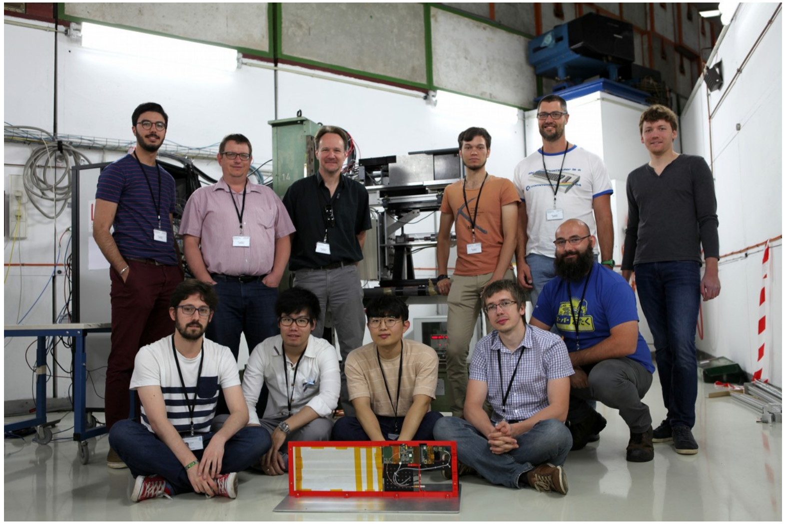
Raw shower barycenter maps

$$\bar{x} = \sum_{i=cells,\, j=layer\ number} x^i w_0^j E_i \Big/ \sum_{i=cells,\, j=layer\ number} w_0^j E_i$$



Test beam performance summary

- Successful beam test of the SiW-ECAL technological prototype.
  - first time with fully assembled detectors elements (first 7 of 10000 needed for ILD)
- **Very good S/N** performances in all the SLABs of (20±1.5)σ on mips
- Raw calibration achieved at the **5% level.**
- First looks at **shower response are very promising**
- **Operating in 1T magnetic field**
  - Also nice and consistent calibration results

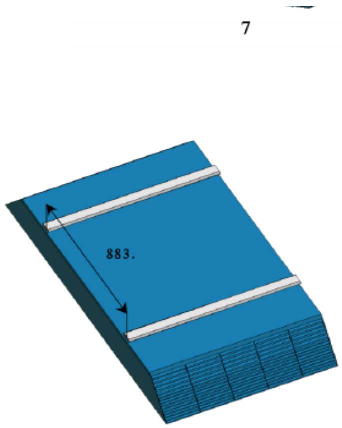


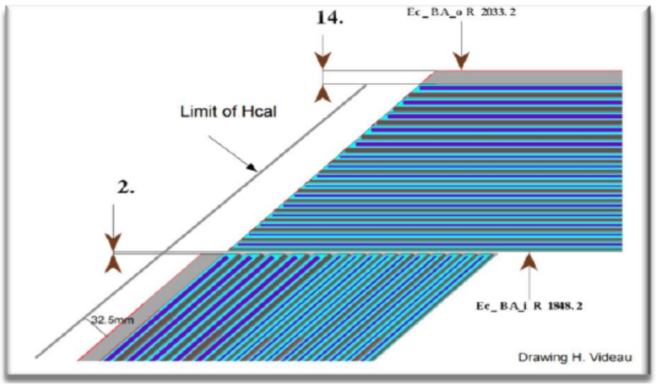
- Presentations + proceedings for **CHEF2017, IEEE2017, LCWS2017**
- Construction & beam test **technical paper ongoing**.

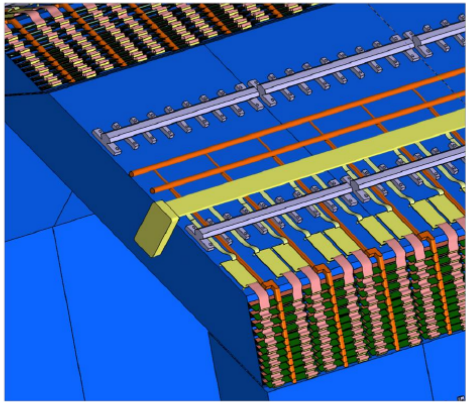
- Excellent prospects for next beam tests !!

Towards a real detector: challenges

- **Long slabs** : up to ~15 ASU (~3m)
  - Complex object: mechanics and electronics
- **Spatial constraints**:
  - limited space between layers and between ECAL and AHCAL
  - Control & Readout electronics at the extremity of the Slab
  - Signal Integrity over the Slab
- Low power consumption.
- Thermal uniformity
- Mechanical Assembly process

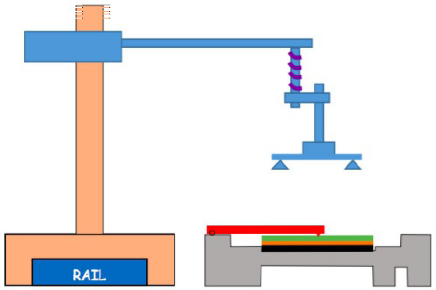


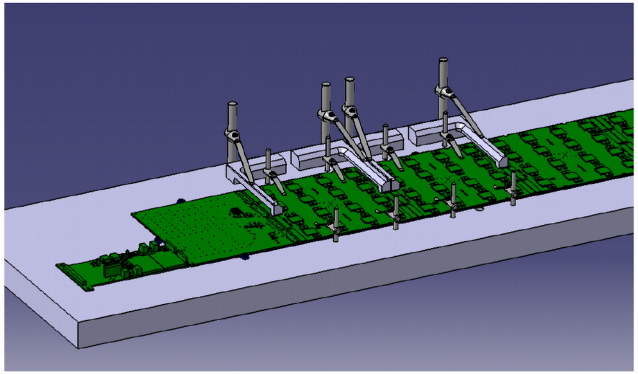




Long slab: assembly bench

- 2nd generation of manipulator:
  - Pick-up by vacuum aspirator, pressure protection by springs
  - Motorization along longitudinal and vertical axes is envisaged.
- Different assembly scenarios under study, all with different possibilities to intervene in case of damaged ASUs.
- Final layout to be defined after decision on assembly scenario.
- Work done by the mechanics department in close collaboration with the electronic department (SERDI)

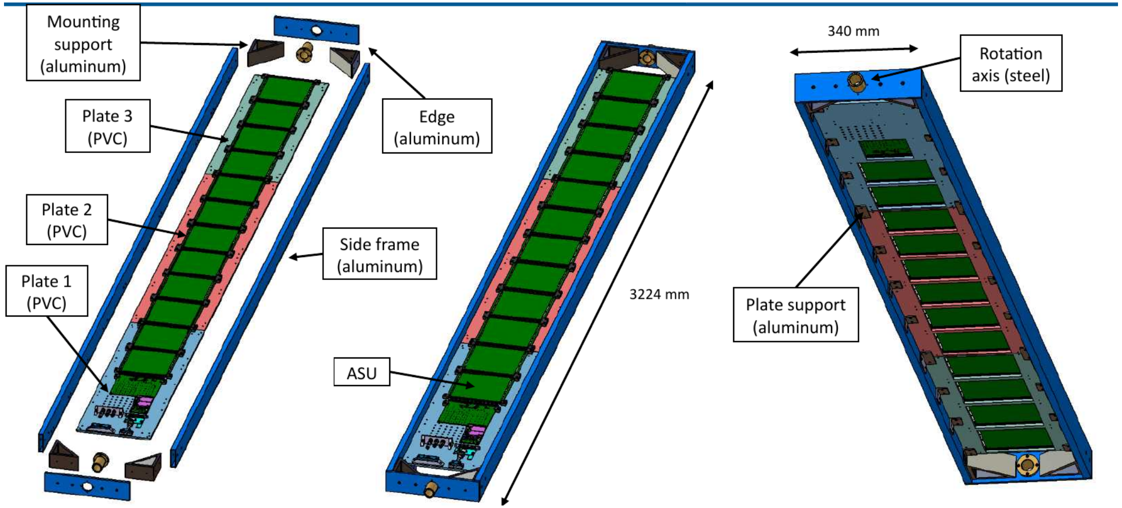


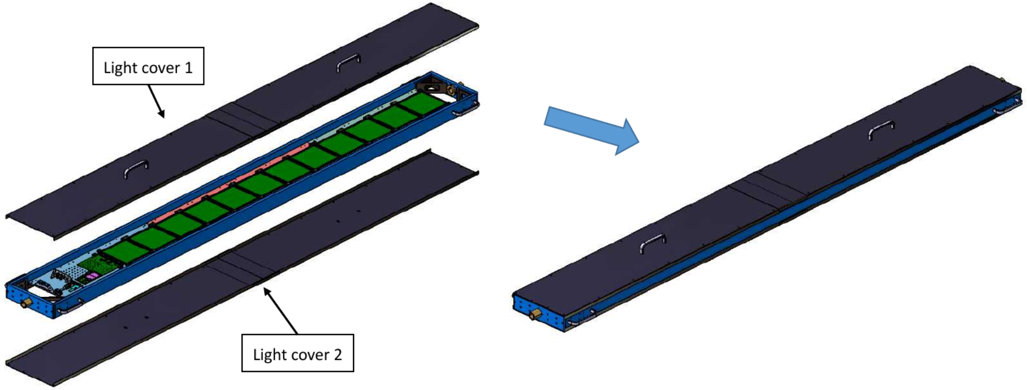


- Preparation of upgraded testbench (In step from drawing to fabrication)

Electric long slab prototype

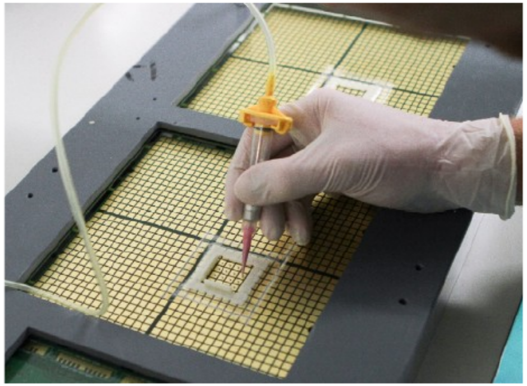
- Scale to support electronics
  - 2+6+4 ASUs = ~3.2 m
  - Support of SMB
  - Total access to upper and lower parts
  - Baby wafers (4×4 pixels) on the bottom
- Mechanical characteristics
  - Movable: table and to beam test
  - Rotatably along long axis (for beam test)
  - Rigidity : ≤ ~1 mm per ASU
  - No electrical contacts scale / cards
- Shielding
  - vs Light and CEM

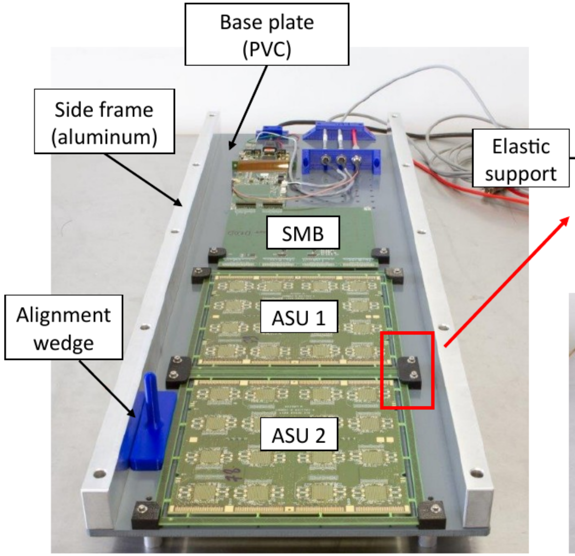




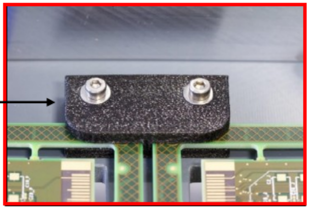
Electric long slab prototype

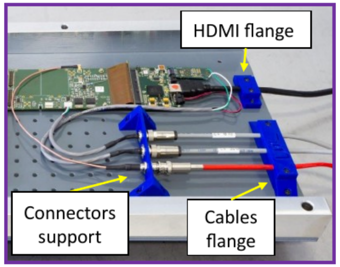
- 2 ASUs prototype.
  - FEV11, sk2.
- Equipped with baby wafers
  - Calibration with RA sources ^{90}Sr, ^{137}Cs.
  - Beam test in summer 2018

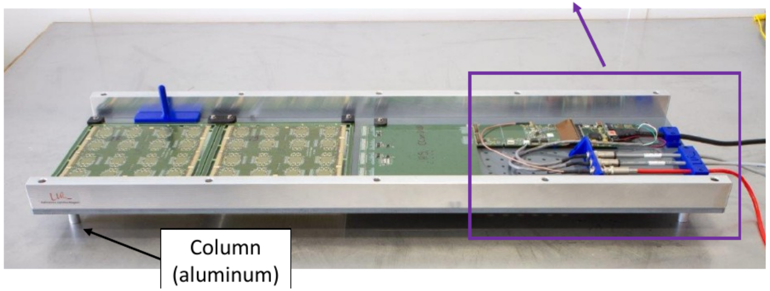


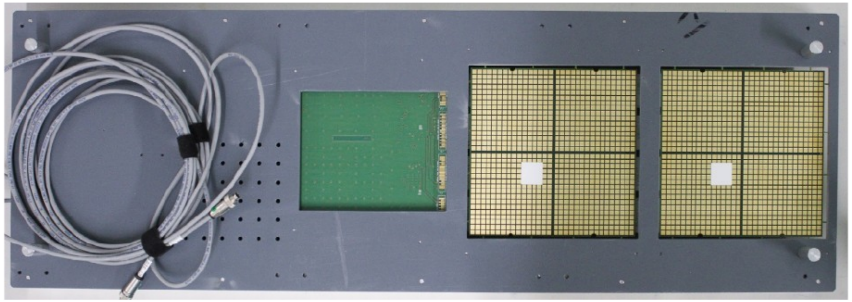


2 ASU



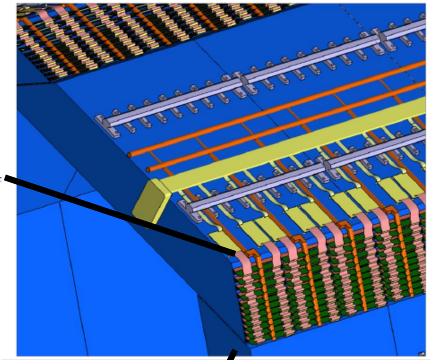


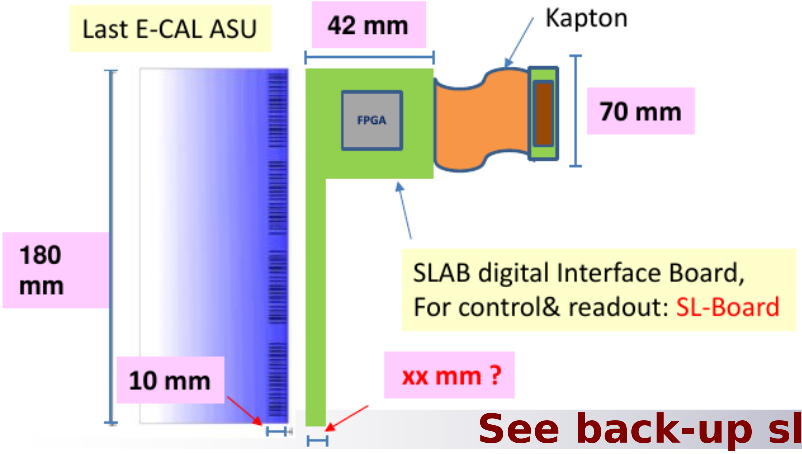


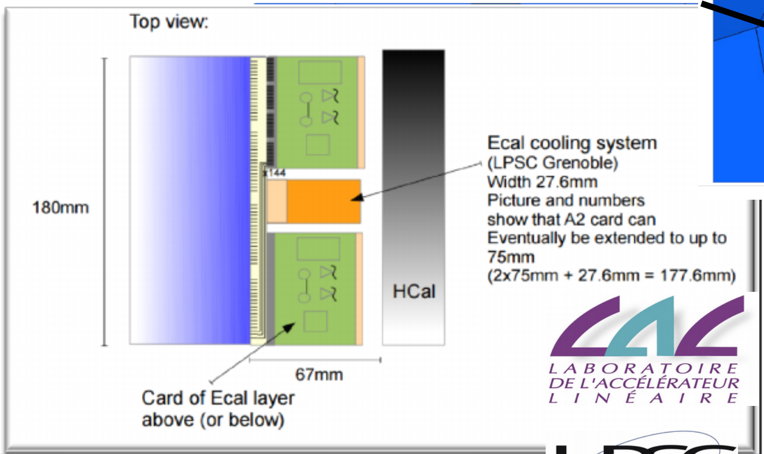


Compactifying the DAQ and passive components of the ASU

- Space constraints for the Slab Interface Board (SL-Board):
  - Power and signal cables and read-out electronics
  - L-shape (even and odd ASUs) Dimensions: see below.







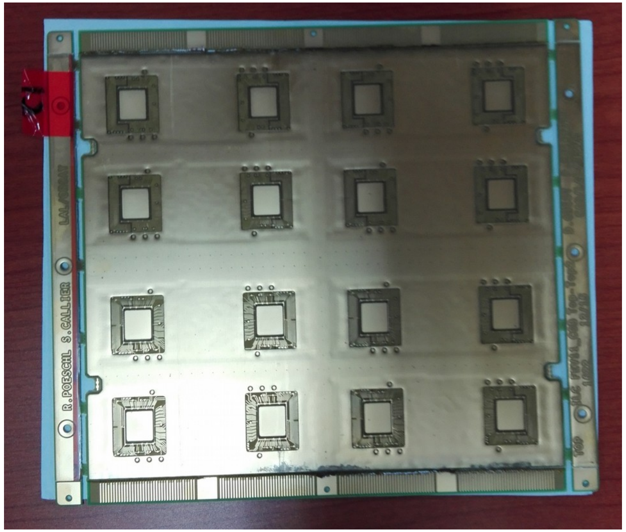
See back-up slides for more info

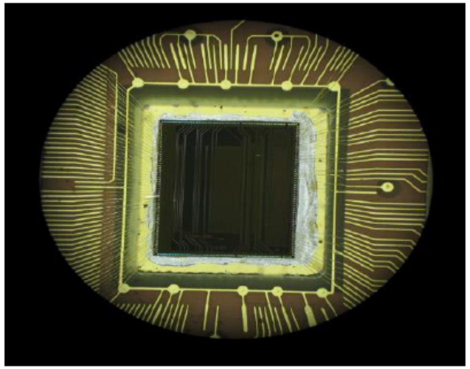
- Space constraints for the Active Sensor Units (ASUs):
  - Maximum Height for Electronics (including PCB): 1.7 mm (depends on number of layers ~20-30?)
  - Current values for prototype: (PCB + components for the SKIROC-2 BGA option) : ~ 3mm

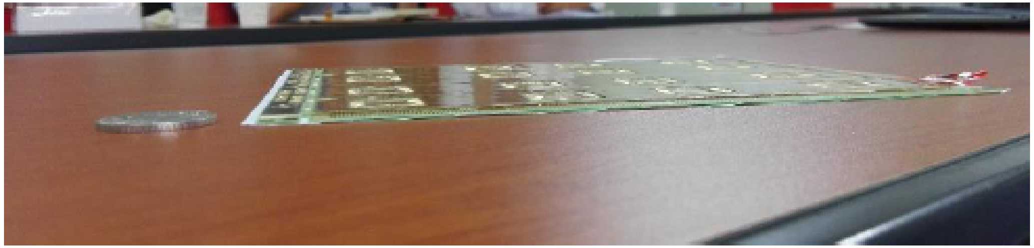
    nex slides →

Compactifying the passive components of the ASU

- Investigating **ultra thin PCB**, with chip on board **COB**
  - Semidonductor packaging, wire bonded.
- LAL/OMEGA collaboration with Corean Group of SKKU, EOS company for the PCB and Kale company for the wire bonding)
  - Strong synergies between university and local companies
  - Testbenchs at LAL and SKKU, training of students done at LAL.
- FEV11_COB production ready (**10 boards of 1.1mm,** good planarity and good electrical response). **3 sent to LAL**
  - Skiroc2a being wire bonded at CERN Bond Lab
  - To be tested in beam this year.



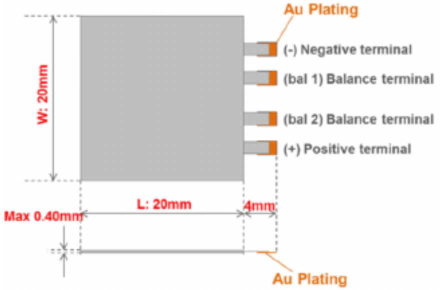


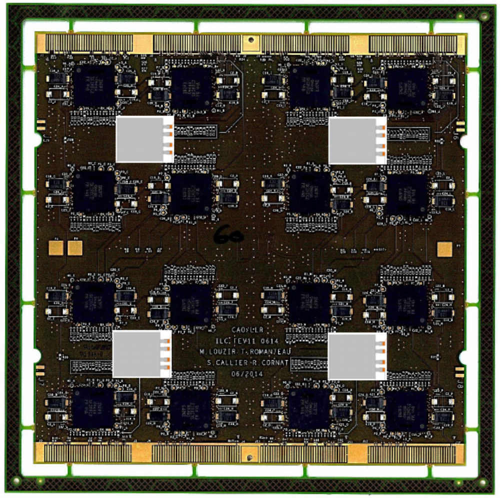


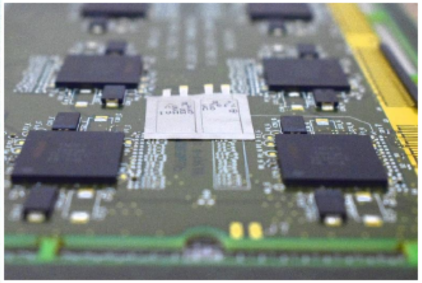
Compactifying the passive components of the ASU

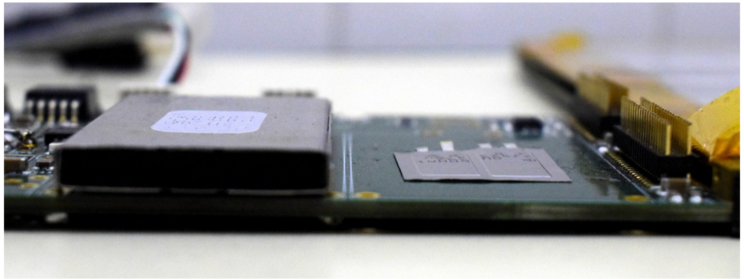
- Proposal to use new ultra-flat capacitors to distribute over the ASUs. This will permit:
  - Peak current reduction: especially through the connectors
  - No more voltage drop along the slab
  - Homogeneous peak power dissipation during power pulsing.
- We go from the 400 mF capacitor/ 12A (peak Current) for the whole SLAB to 140 mF / 1.2 A per ASU.

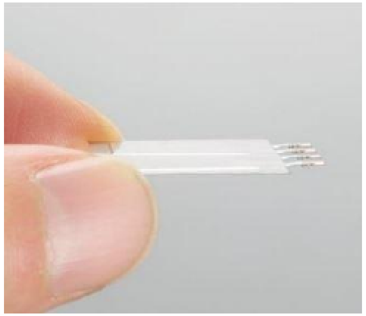
Brand new product, appeared few months ago





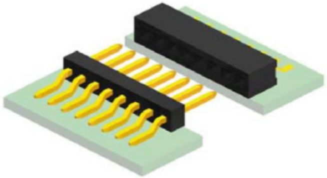


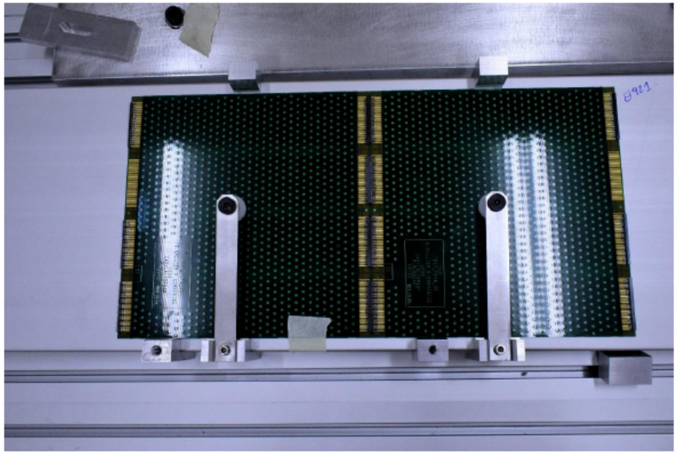




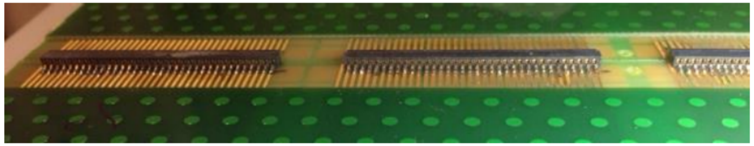
Compactifying the passive components of the ASU

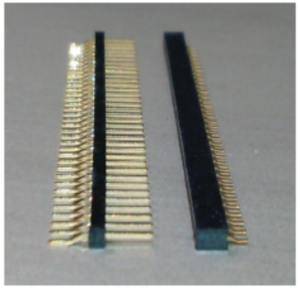
- New interconnection proposal for the ASU with the SKIROC-BGA option
  - old approach based in flat kapton cables seems not feasible at production scales (see back-up slides)
- Gradconn connector BB02-YN
  https://www.gradconn.com/Products/BoardToBoard/MatingHalves/BB02-YN/BB02-WF
  - 35 pins, Height : 1,5 mm possibly 1,27 mm.
  - Pitch 1mm compatible with existing ASUs
  - Current rating : 1 A., AC 300 Volts

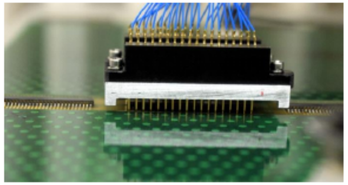




- Still ongoing tests to perform:
  - Connectors resistivity measurement
  - Only one board so far → long slabs? Check ASU alignment.
  - Emulate power-pulsing and measure the effect on the AVDD power supply on the ASUs all along the slab.
  - Signal integrity along the slab: we may need to add buffers on the ASUs
  - Mechanical stress test.



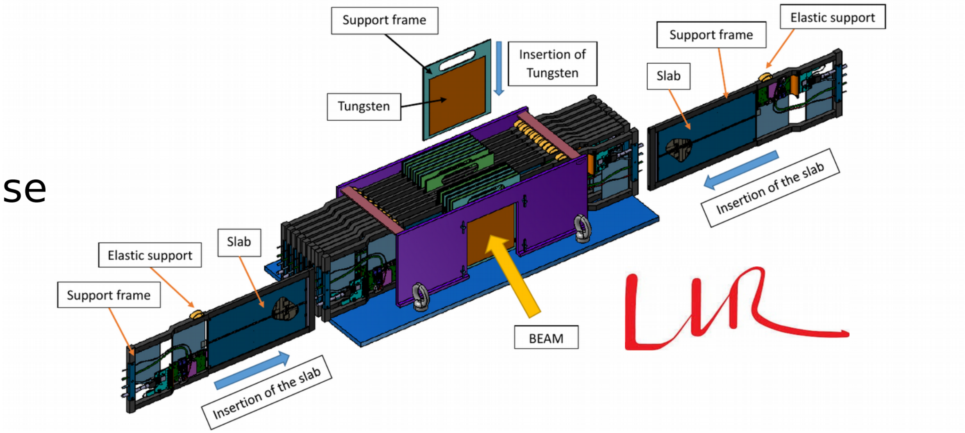




Beam test at DESY, Summer 2018

2 weeks in June 2018 for the SiW-ECAL of ILD/CALICE.

- Using a **new compact structure** allowing for 0 to 24 X0 of Tungsten and 10-20 sensor layers:
  - Test new PCB & Si Wafers & DAQ developments
- A long structure (3.2m) chaining 12 detector units, mounted on a support on wheel, to test the response of a long layer.



Physics program:
- MIP calibration
- Electromagnetic showers
- If possible: photon/electron separation studies (key for Particle Flow understanding)
- Tests with and w/o B field.

Summary

- Successful construction and operation in beam of the SiW-ECAL technological prototype made of short slabs.
- Still some work to be done towards realistic ILD prototype. Many challenges being faced at the moment:
  - Long slab production: it is a complex object electronically and mechanically.
  - Compactification of DAQ and active units.
  - Integration.
- Stay tuned for BT2018 campagin and the news from the R&D!!

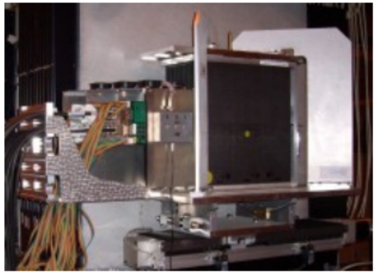
Back-up

Calorimetry for the International Linear Collider (ILC)

Physics Prototype

Proof of principle

2003 - 2011



Number of channels : 9720

Pixel size: 1x1 cm2

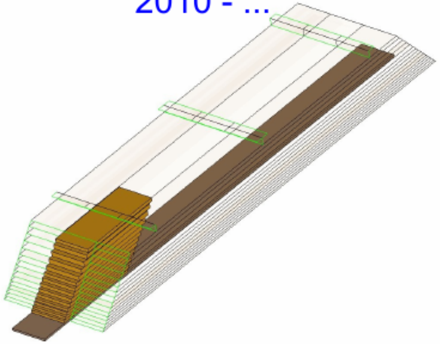
$R_{M,eff}$: ~ 1.5cm

Weight : ~ 200 Kg

Technological Prototype

Engineering challenges

2010 - ...



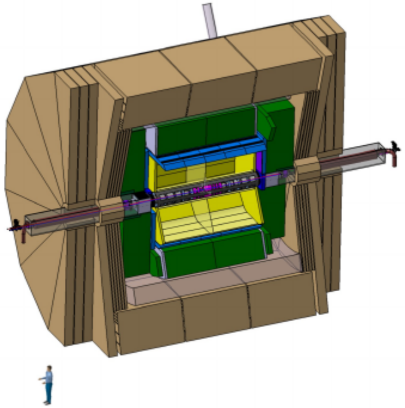
Number of channels : 45360

Pixel size: 0.55x0.55 cm2

$R_{M,eff}$: ~ 1.5cm

Weight : ~ 700 Kg

LC detector



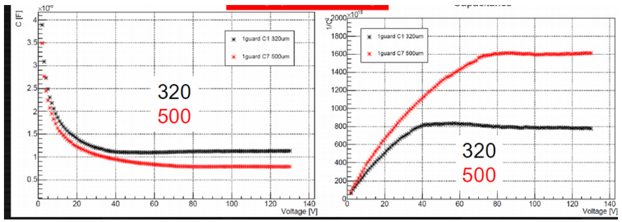
ECAL :

Channels : ~100 10^6

Total Weight : ~130 t

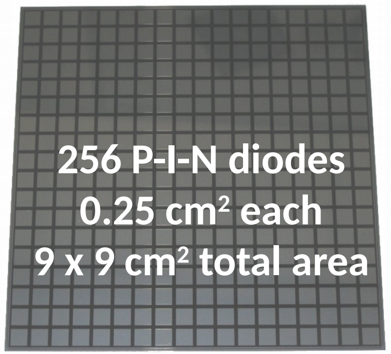
Si wafers

Designed for ILC : Low cost, 3000 m2
Minimized number of manufacturing steps
Target is 2.5 EUR/cm2
Now : 10 EUR/cm2 (Japan)



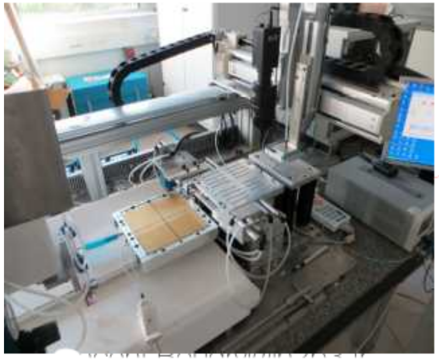
I(V) and C(V) characterization

Breakdown voltage >500V
Current leakage <4 nA/pixel (chip is DC coupled)
Full depletion at <100 V
(~40 V with 320 um, ~70 V with 500um)
Null C(V) slope to avoid dC/dV noise

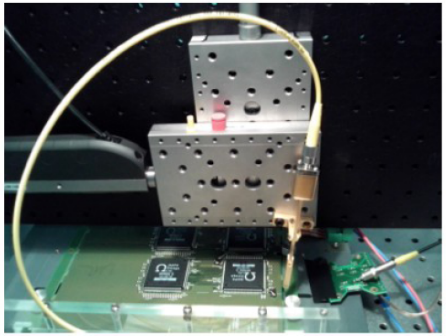


EUDET layout
Prototype from Hamamatsu

Wafers are glued to PCB (robot, LPNHE)
Segmented guard-rings layout as an option

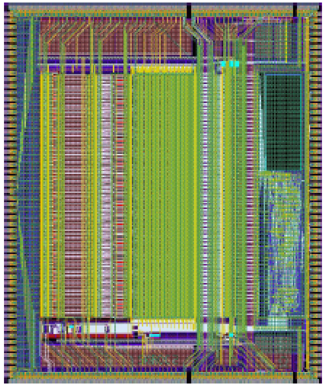


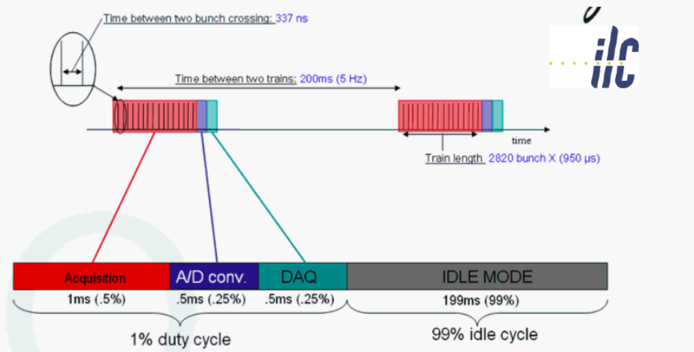
R&D on crosstalk
Segmented guard-rings layout as an option. Systematics studies with laser systems and simulation.



Front end electronics and DAQ

- SKIROC (Silicon Kalorimeter Integrated Read Out Chip)
  - SiGe 0.35µm AMS, Size 7.5 mm x 8.7 mm, 64 channels
  - High integration level (variable gain charge amp, 12-bit Wilkinson ADC, digital logic)
  - Large dynamic range (~2500 MIPS), low noise (~1/10 of a MIP)
  - Auto-trigger at 0.1-0.5 MIP
  - Low Power: (25µW/ch) power pulsing
    switch off electronics bias currents
    during bunch trains

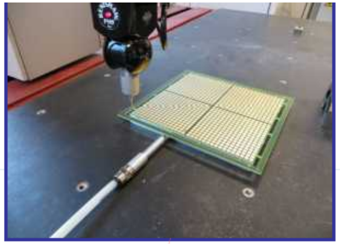




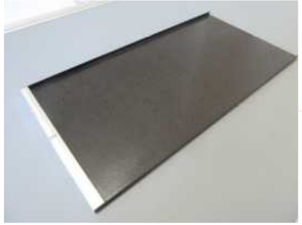
N.B. Final numbers may vary

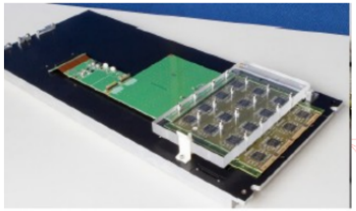
- Prototype version (Skiroc 2 and 2a) for R&D and beam tests
- Definitive version will be optimized for ILC and work in zero supression conditions.

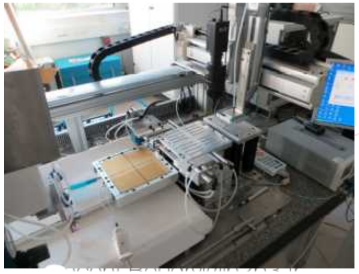
Assembly chain

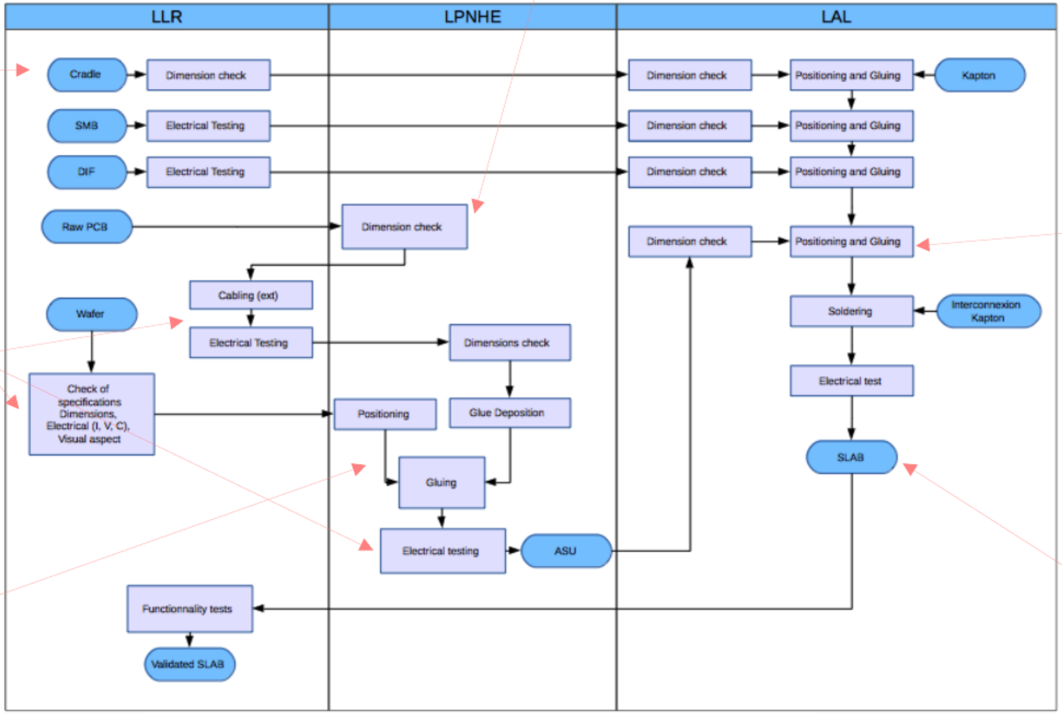


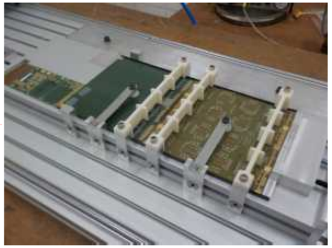
‘Simplified view’





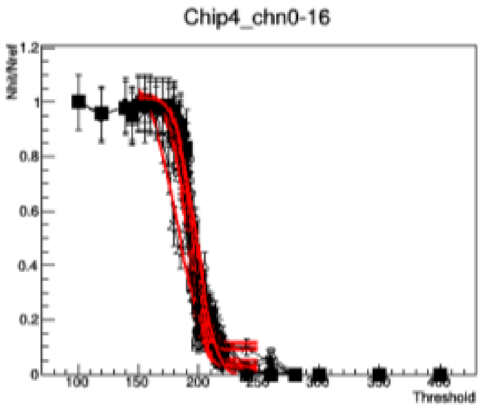


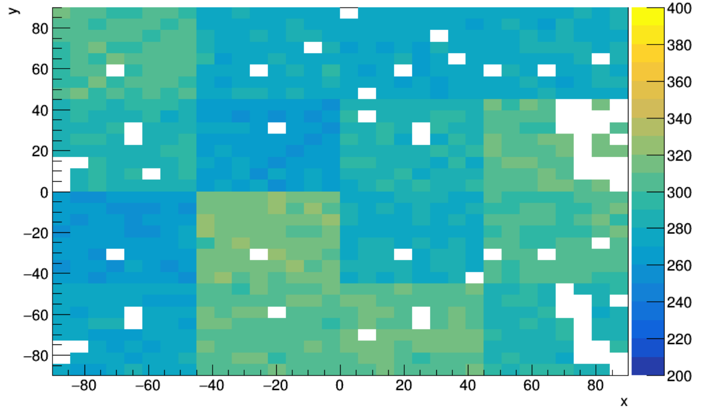




Test Beam at DESY: commissioning

- June 2017, TB24 1 & 2(PCMag) at DESY
- New commissioning procedure with very conservative passports delivery
  - Auto **trigger Threshold** determination through fit of **scurves** to data taken in noise runs.
  - Find **noisy channels**: **7-8%** masked channels (can be reduced by individual threshold settings, sk2A)
  - 7 shorts slabs passed it, the other 3 were rejected for lower performance: under investigation



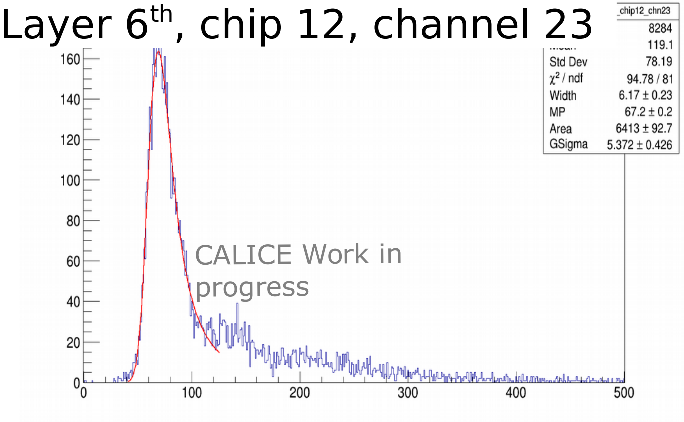


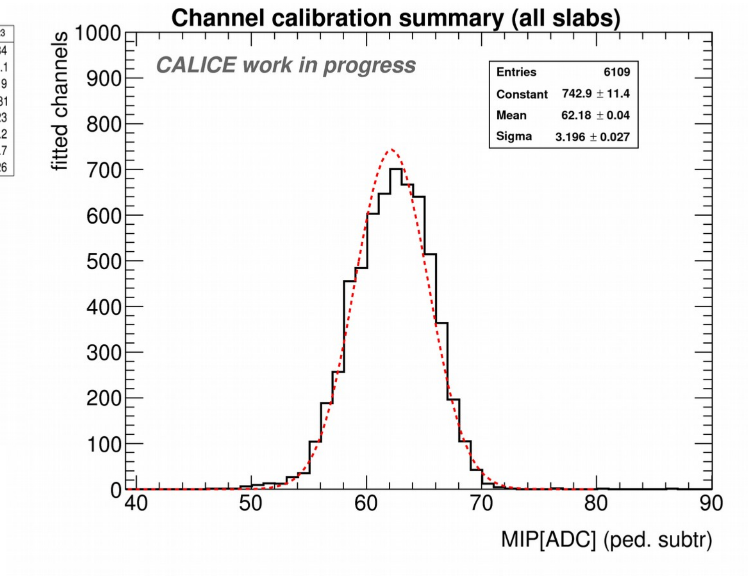
Repetitive patterns on the localization of **noisy channels**

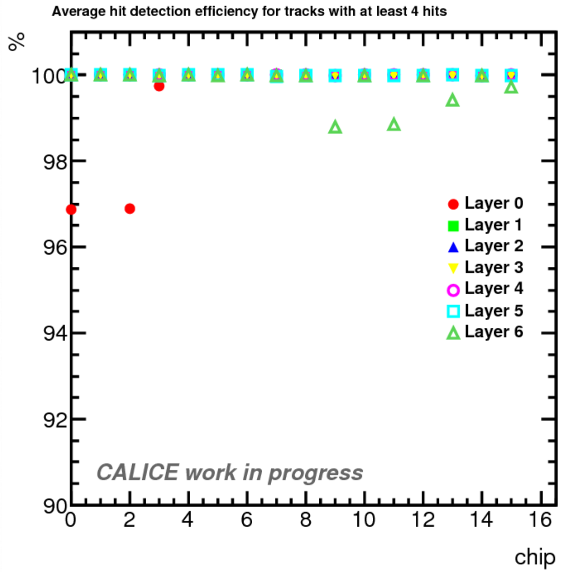
→ **issues on the routing** of pad2ASIC in the PCB have been found after beam test (currently under study)

Si – ECAL (tracker mode)

Layer 6th, chip 12, channel 23



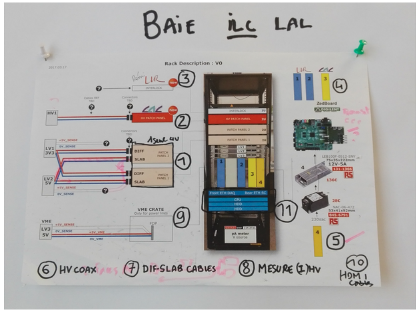


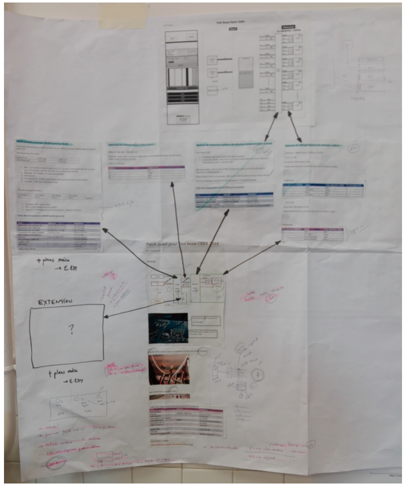


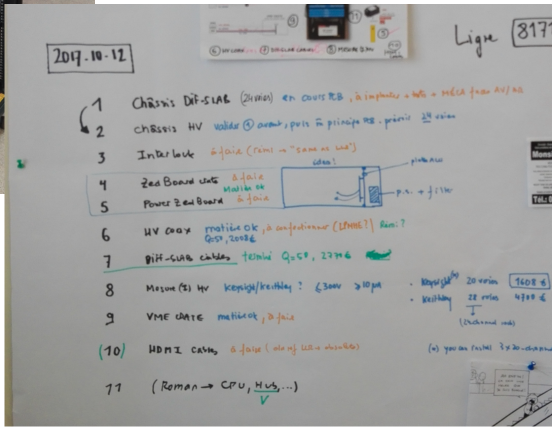
After test beam activities

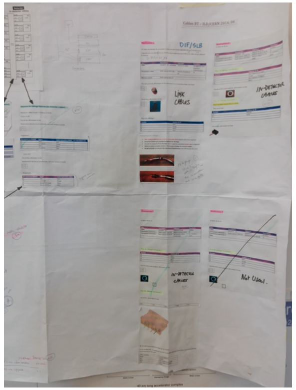
- New LAL Electronic Rack:
  - Up to 20 slabs.
  - Improved groundings/power supplies.
  - Work started by D. Jehanno in close collaboration with R. Cornat.
  - LAL SERDI is taking over.

- Optimized rack is mandatory to investigate noise issues:
  - Noise burst → investigate different setups with optimized power supply and grounding.





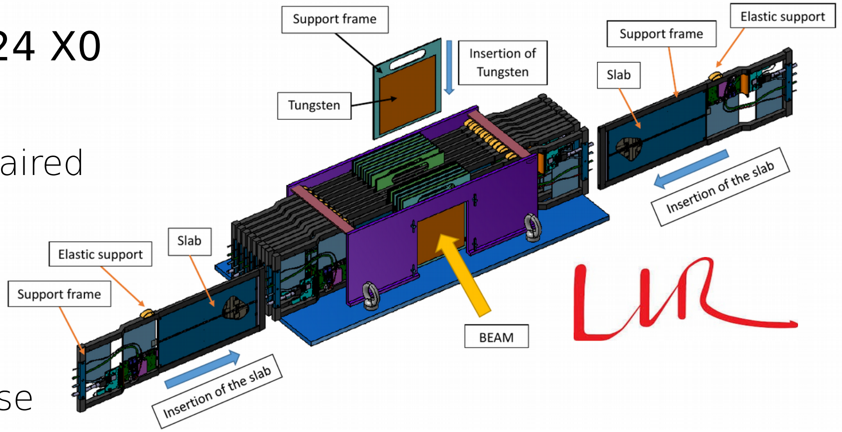




Beam test at DESY, Summer 2018

2 weeks in June 2018 for the SiW-ECAL of ILD/CALICE.

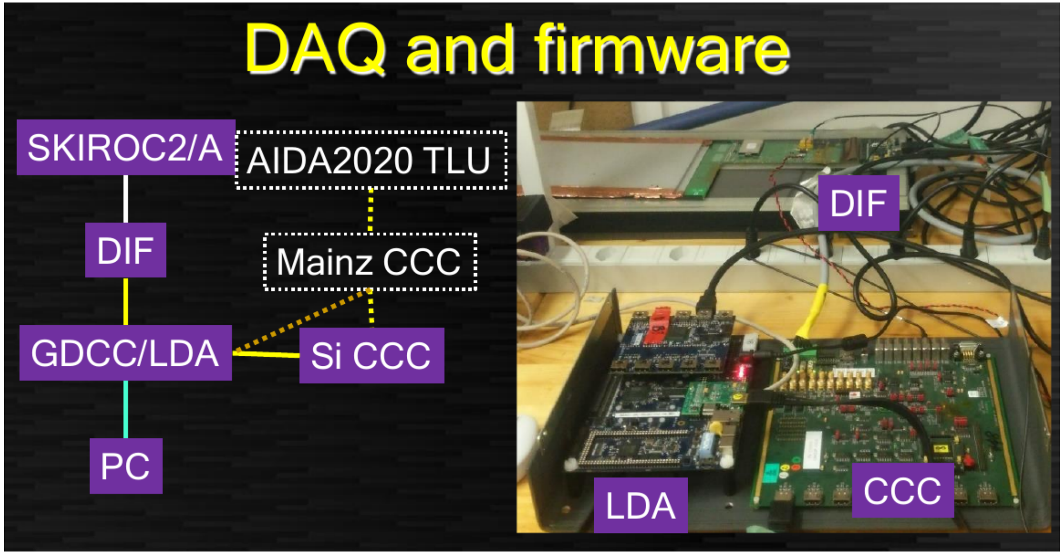
- Using a **new compact structure** allowing for 0 to 24 X0 of Tungsten and 10-20 sensor layers:
  - the existing layers (7 working tested in 2017 + 3 to be repaired
    [FEV11 + 325µm Wafers + SK2]
  - 3 to 4 layers **with improved design (see back-up)**
    [FEV13 + 500µm & 650 µm wafers + SK2a]
  - up-to 5 new layers to be produced in Kyushu (Japan) in close collaboration with industrial partner
    [FEV12-Jp + 650µm Wafers + SK2a]
  - 1 or 2 thin layers with ASICs embbeded in PCB
    [FEV11_COB + baby wafer + SK2a]
- A long structure (3.2m) chaining 12 detector units, mounted on a support on wheel, to test the response of a long layer.



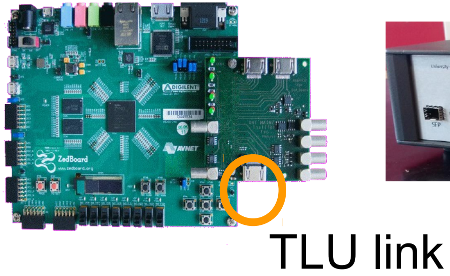
Program:
- MIP calibration
- Electromagnetic showers
- If possible: photon/electron separation studies (key for Particle Flow understanding)
- Tests with and w/o B field.

Towards Combined beam tests

- Start technical discussions and meetings for eventual common beam test with HCAL
  - Internal discussions: Kyushu/LAL/LLR/LPNHE/Omega
  - “External” discussions within the **AIDA2020 WP5** dedicated to DAQ developments for LC-detectors common tesbeams.



- 16 Mainz CCC purchased by LAL, currently distributed as follows:
  - 1 LLR, 1 LNPHE, rest in stock
- 4 AIDA2020 TLU purchased by LAL not yet delivered (to be distributed among LLR, LAL, LPNHE, Kyushu)

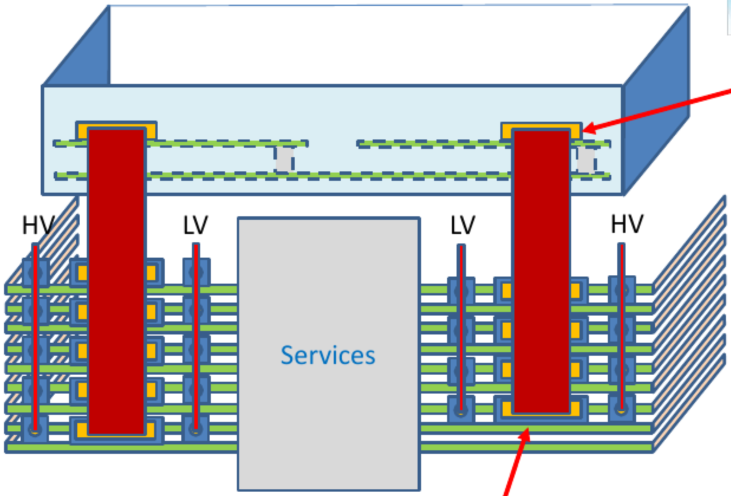


Interconnection with flat kapton cables

- Interconnection is maybe the most involved piece of the assembly
- Current solution with Flat Kapton + Iron Soldering works
  - Proven for short slabs
  - But… Interconnection so far made by hand & Delicate work
- Application for long slab requires automatised (robust) procedure
  - difficulties to find supplier for developing such a procedure…
- Intensive brainstorming at LAL over summer to find solution that
  - is robust, "easy" to implement on short notice and that can be extrapolated
  - Remember also that long slab is electronics/electrotech and mechanical object
  - Tight communication and between LAL electronics and mechanics departments

AIDA 2020 Control & Readout Signals

Core Module connector:
9 common differential pairs for CCC and JTAG, *30 individual pairs* for control and readout, spare, Address, GND



SL-Board Connector
9 differential pairs for CCC and JTAG, 2 individual pairs for control and readout, spare, GND

	Signals
	Clk
	Trigger
	Start/Stop
	Busy
	Control
JTAG	TCK
JTAG	TMS
JTAG	TDI
JTAG	TDO
SPI	SCK
SPI	SDI
SPI	SDO

Signals
Rx_i
Tx_i
Spare …
GND …
ADD[0]
ADD[1]
ADD[2]
ADD[3]

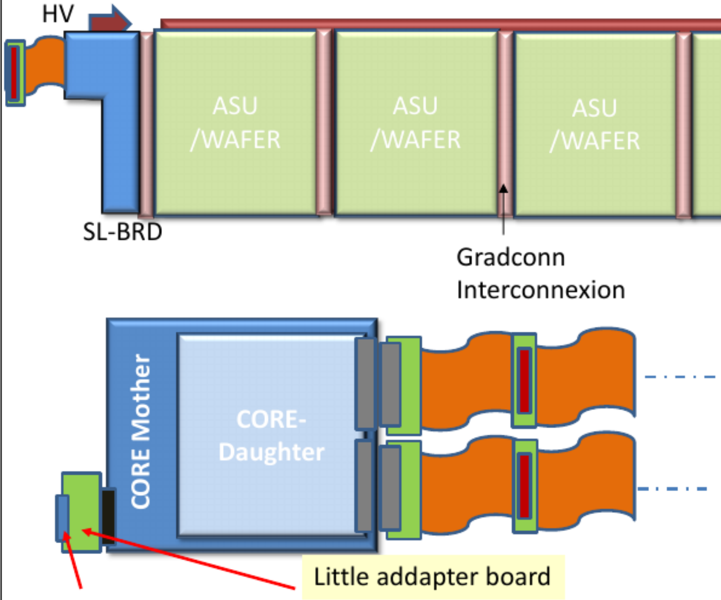
The Acquisition Module

The Control & Readout Acquisition system will be based on an **existing mother board** that handles:

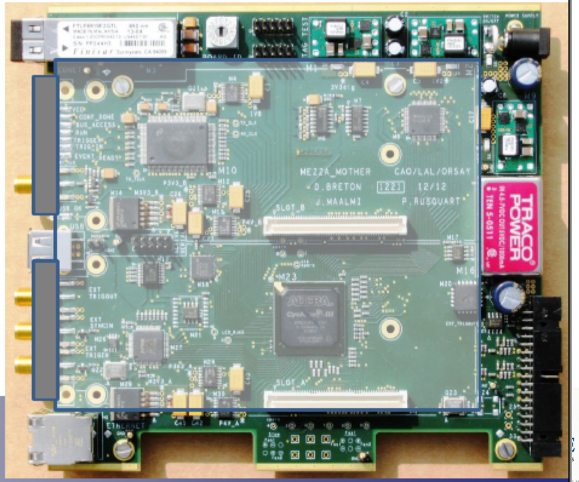
- Control & Readout through **USB/Ethernet/ Optical fiber**
- Distribution of the clock and fast commands

- There are existing low level **C-libraries**. (LAL-ML protocol)
- This LAL development is already used for other experiments.
- The **Detector specific CORE Daughter board is under developement** as well as its **Katpton cable**

Ex of a Long Slab : 8 ASUs

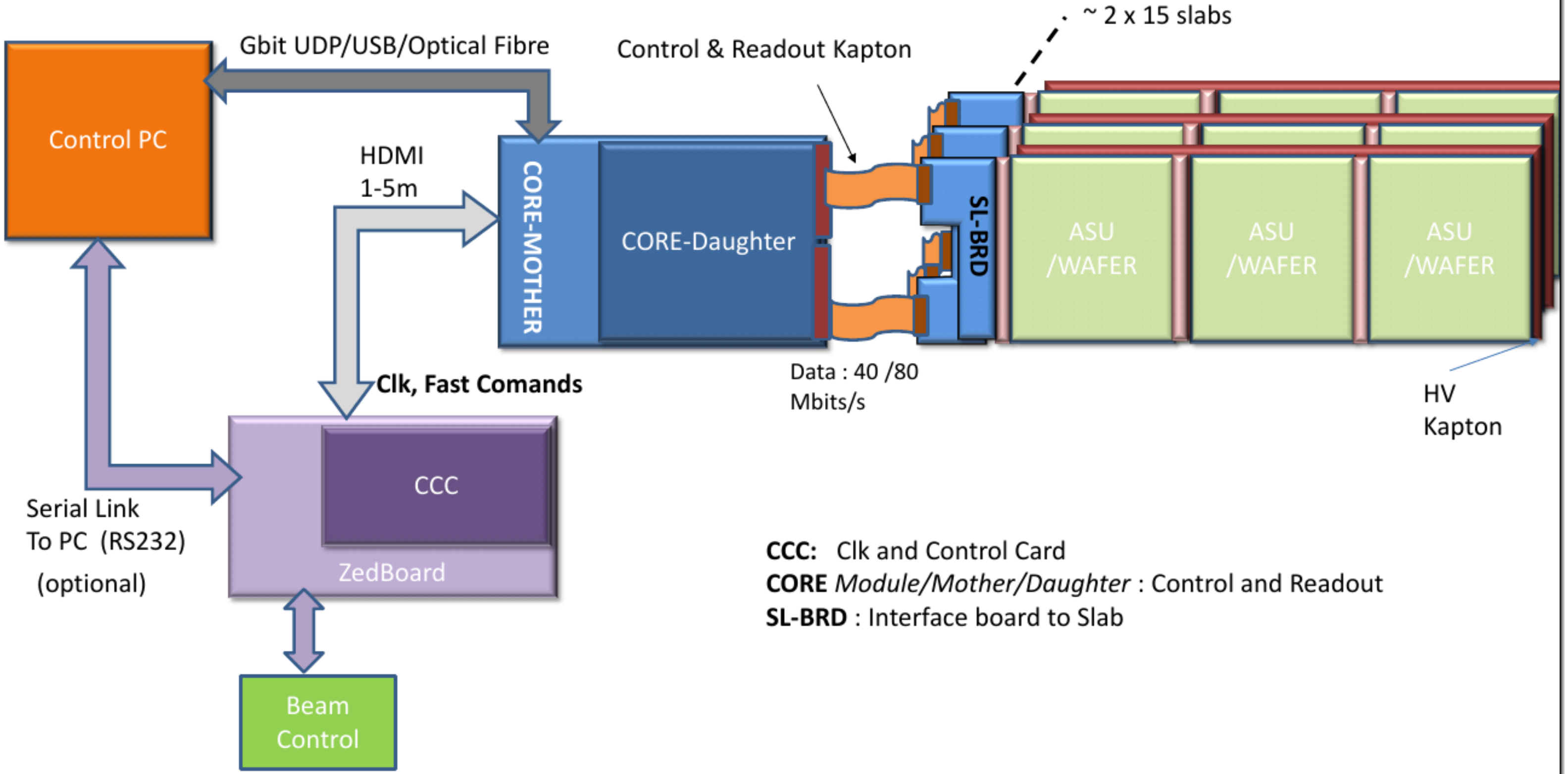


Existing CORE MOTHER



LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Global Architecture Scheme



CCC: Clk and Control Card
CORE *Module/Mother/Daughter* : Control and Readout
SL-BRD : Interface board to Slab

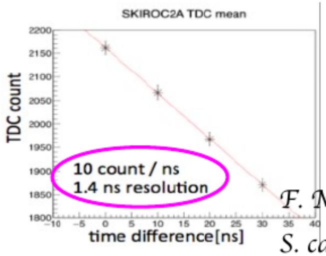
Additional production of shorts SLABs in 2018

2016-17: **10 ASU's produced**: 325 µm Wafers + FEV11 + SK2

- 7 OK for physics
- 3 SLABs are broken (bef. Beam test) : 1 broken, 2 too noisy (1 after manipulation) ⇒ **To be repaired** (if possible)

Material is available for **additional production**

- **Wafers:** 10 ordered by LPNHE from HPK (**525 µm**) + 25 @ LLR + new production in Kyushu (**650 µm**) (~20)
- **ASICs:** ~230 SK2a packaged and tested.
  - include ~1.5ns time resolution; pin-to-pin compatible SK2
- **PBC's**
  - FEV13 ~ 3-4 units ?
  - FEV12_Jp: by *industrial contact* : connectors, thinner design (1.6,1.2, 1.0mm) ~ 5 units ?
  - **FEV11_COB** (next slide) ~ 2 units ?



F. Magniette, J. Nanny, R. Guillaumat [LLR]
S. callier (Omega), T. Suehara (Kyushu)

Expert review of FEV11 after BT

- 15 points of improvements being implemented:
  - Noise: differentiated analog supplies, data routing, phasing of clock
  - Unique Tag, PT100, ...
  - FW: Clock freq, UDP, sync of EventID, ...
  - Adaptor board: new design (SMBv5)

First design review today (11/01/2018)