Results of CLICpix2 + C3PD assemblies

I. Kremastiotis, A. Nurnberg

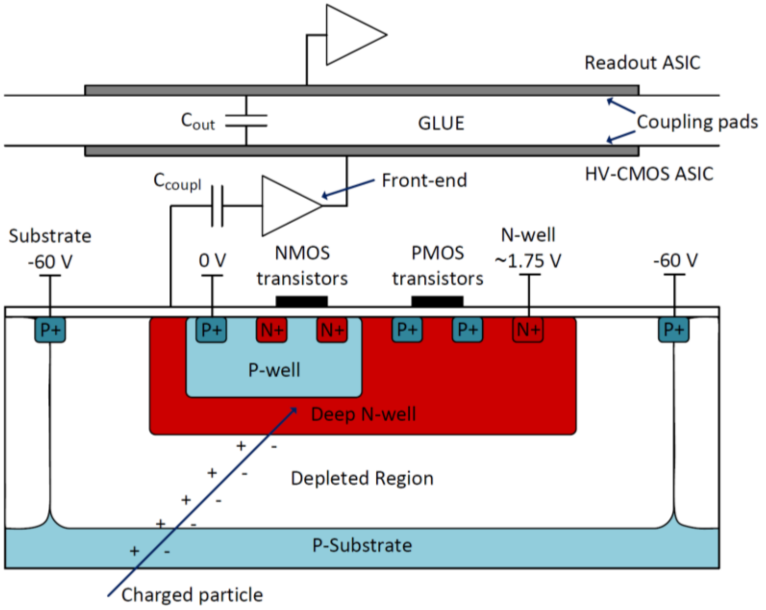
CLIC Workshop 2018
CERN, 22-26 January 2018

Outline

- Introduction: Capacitively coupled pixel detectors
- Standalone C3PD / CLICpix2 characterisation
- Measurements with capacitively coupled assemblies
- Summary and further testing

Introduction to capacitively coupled pixel detectors

- High-Voltage (HV) CMOS sensors:
  - All electronics are placed in a deep N-well, which is also the collecting electrode
  - Due to the reverse applied high-voltage bias, a depletion region with a depth of $\sim 10\ \mu m$ is created under the collection electrode, which leads to fast signal collection through drift
- Capacitively coupled pixel detectors:
  - A thin layer of glue is applied between the sensor and the readout chip
  - The charge collected in the HV-CMOS pixel is amplified by an on-pixel Charge Sensitive Amplifier (CSA) and then transferred to the readout chip



- Two chips have been designed in the framework of the CLIC vertex detector studies
  - The CLICpix2 readout chip *[1]* (65 nm CMOS process)
    - Simultaneous time (8-bit ToA) and energy (5-bit ToT) measurements, 10 ns time tagging
  - The C3PD HV-CMOS sensor chip *[2]*, (180 nm HV-CMOS process)
    - Produced on wafers with 20 and 80 Ωcm resistivity for the substrate
    - 200 Ωcm samples will also be available
  - Both chips feature matrices with 128×128 square pixels, with 25 μm pitch
  - Successors of a 1st generation of chips that have been tested in capacitively coupled assemblies *[3]*

Capacitively coupled assemblies

- Capacitively coupled assemblies with the C3PD HV-CMOS sensor glued on the CLICpix2 readout chip have been produced at Geneva University with an SET Accura 100 flip-chip machine
  - 5 assemblies with the standard substrate resistivity for C3PD (20 Ωcm) have been measured in laboratory and/or beam tests
  - 2 more assemblies with 80 Ωcm C3PD chips have been produced
  - First laboratory results obtained with the 80 Ωcm assemblies. To be further tested in the coming weeks

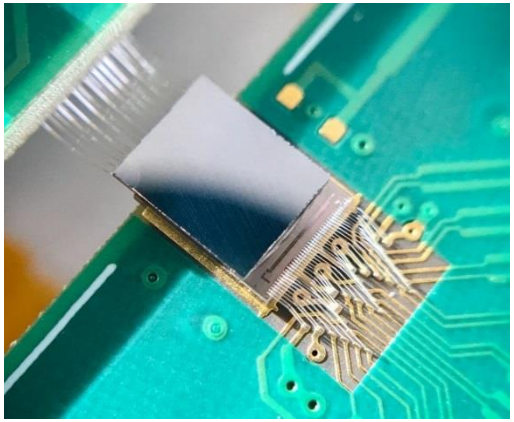
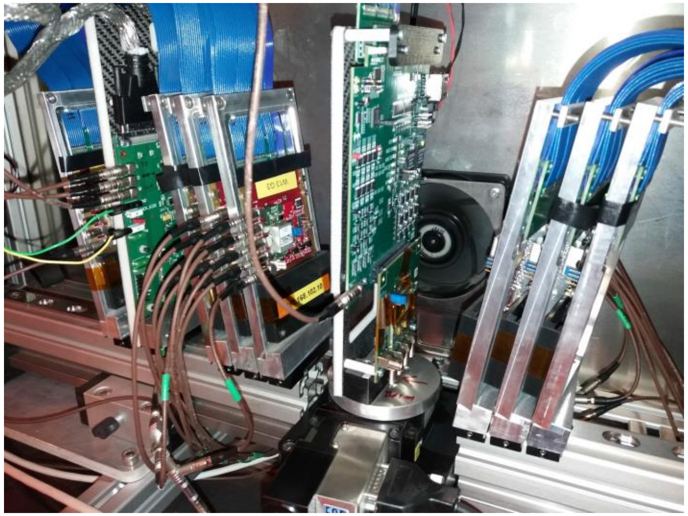


Photo: M. Vicente

- Laboratory and test-beam measurements of capacitively coupled assemblies were performed using the CaRIBOu data acquisition system *[4]*
  - CaRIBOu system improved in stability since August
  - In the test-beam, when the best efficiency is required, decoding is done offline to increase readout data rate
  - For shorter shutters, where the rate is not dominated by the readout, the data rate in test-beam has been increased by a factor of ~10



Test-beam setup (Photo: A. Nurnberg)

https://gitlab.cern.ch/Caribou

Standalone C3PD characterisation

- The chip has been tested using the internal test pulse injection, as well as with a ^{55}Fe source

- The results of the standalone test for bare chips with the standard substrate resistivity (20 Ωcm) *[2]* have shown:
  - Average charge gain: 190 mV/ke^{-}
  - RMS noise: 40 e^{-}
  - Rise time: 20 ns
  - Power consumption: $\sim 5 \mu W$ per pixel (before power pulsing)
  - After power pulsing, the average power consumption over the 50 Hz cycle was estimated to be $\sim 16\ mW/cm^2$
  - These results are close to the ones expected from simulations, and are within the detector requirements

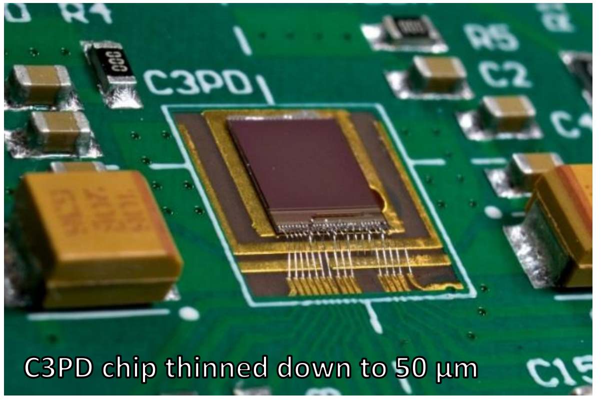


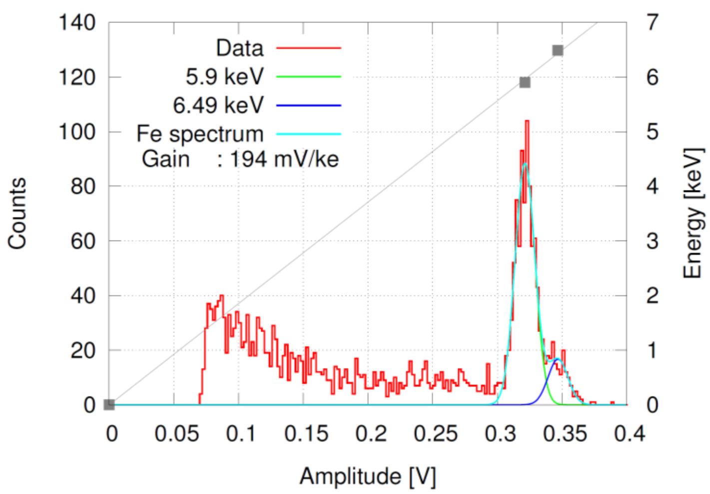
Photo: S. Kulis

- Samples thinned down to 50 µm have been tested, apart from the standard thickness (250 µm)
  - No impact on the chip performance has been observed for the thinned-down samples

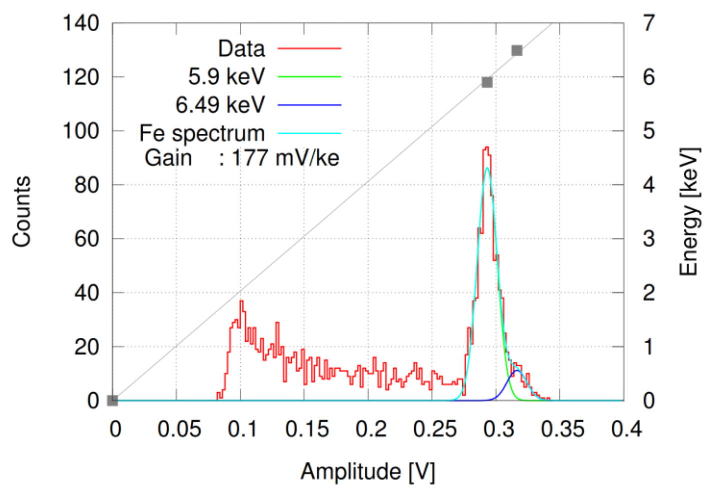
- Samples from the 80 Ωcm wafers have also been tested in standalone mode
  - Higher resistivity wafers have been produced using the same process, but in a different foundry than the ones with standard resistivity

Measurements with ^{55}Fe source

- Measurements with a ^{55}Fe source for one of the monitored pixels of the C3PD chip
  - 20 Ωcm (left) and 80 Ωcm (right)
  - Potentially lower gain for the 80 Ωcm C3PD samples. More statistics are needed in order to investigate further



Resulting amplitude spectrum from a ^{55}Fe source – 20 Ωcm



Resulting amplitude spectrum from a ^{55}Fe source – 80 Ωcm

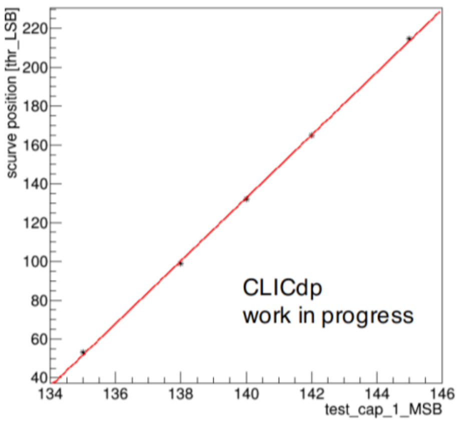
	20 Ωcm (6 samples)	80 Ωcm (2 samples)
Gain [mV/ke$^-$]	190 ± 15%	165 ± 10%
C_{fb} [fF]	0.83 ± 15%	0.96 ± 10%
C_{test} [fF]	0.70 ± 2%	0.62 ± 7%

Work in progress

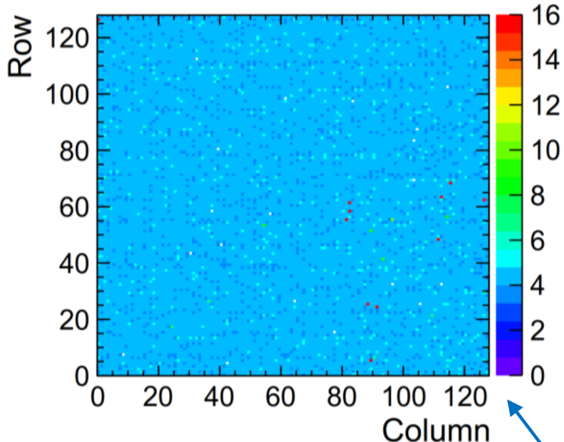
Standalone CLICpix2 characterisation

- 61 e^{-} noise measured (for bare CLICpix2), 67 e^{-} expected from simulations
- Homogenous threshold distribution over matrix after trimming
- Linear front-end response to test pulses
- Noise is increased by a factor of ~2 after powering on C3PD, due to additional noise coupled at the CLICpix2 input

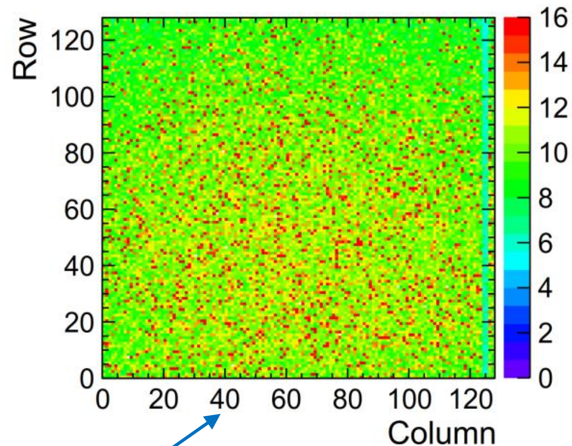
Amplifier linearity



Noise width – C3PD off

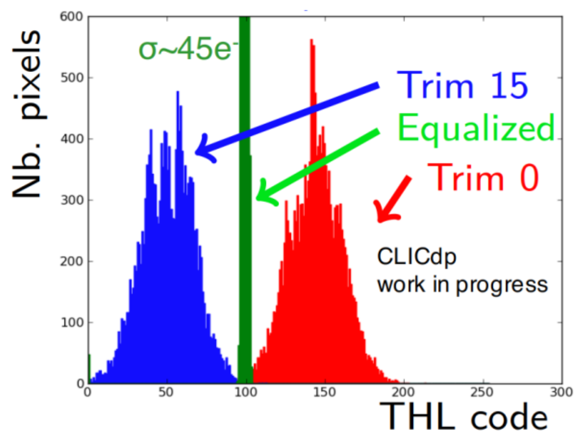


Noise width – C3PD on



Assembly 10

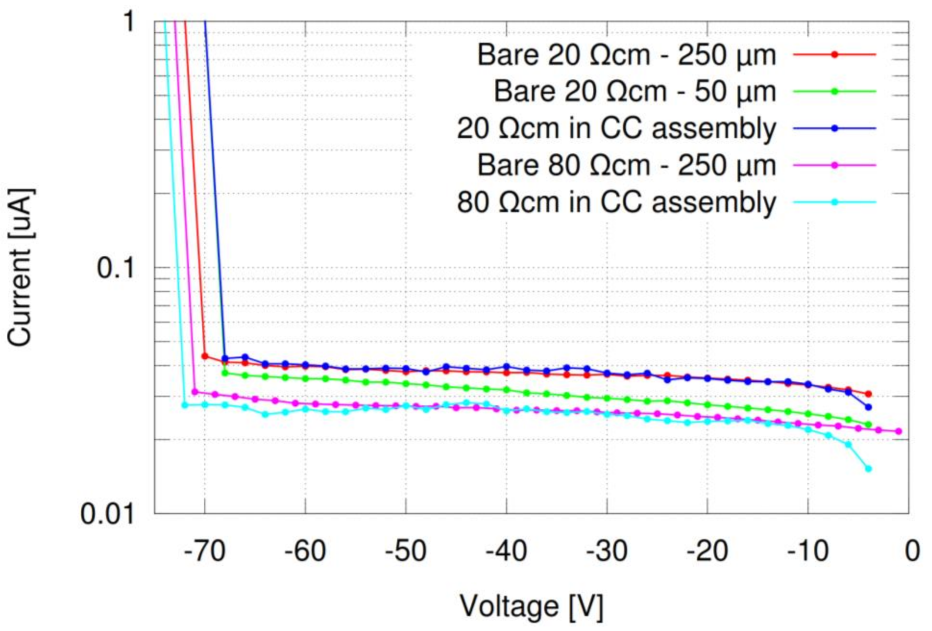
Threshold equalisation



Sensor I-V characteristic

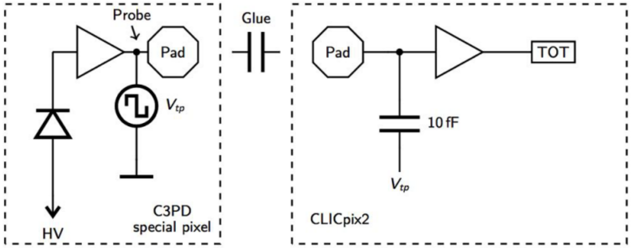
- The leakage current of the C3PD sensor as function of the HV bias has been measured for 5 samples with different resistivities and thicknesses.
  - Capacitively coupled assemblies were produced with standard thickness (250 µm) sensor chips

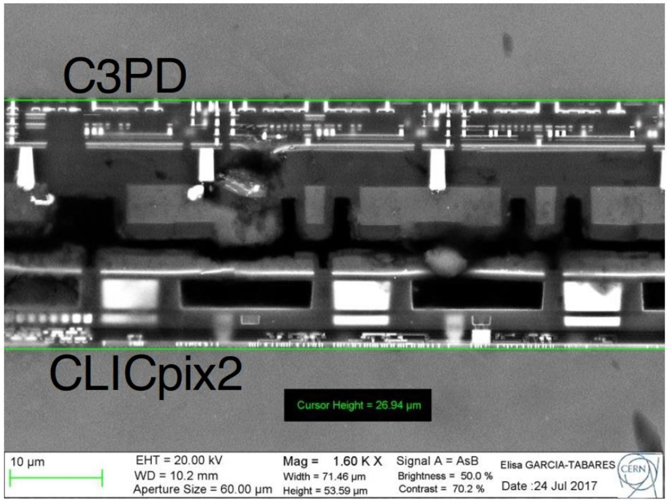
- 80 Ωcm samples show a (slightly) higher breakdown voltage



Measurements on coupling (glue) capacitance

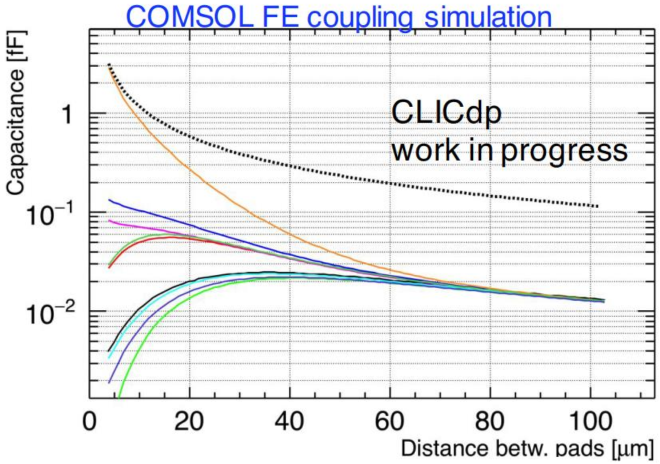
- Following destructive cross-section measurements on two mechanical samples, the pad-to-pad distance is ~3 µm, largely dominated by passivation layers
- The simulated value of the glue capacitance is ~3.5 fF *[5]*
- A “special” C3PD pixel where the injected test pulse signal is connected directly to the coupling pad, was used to measure the coupling capacitance between the two chips





Cross-section of CLICpix2 + C3PD glue assembly

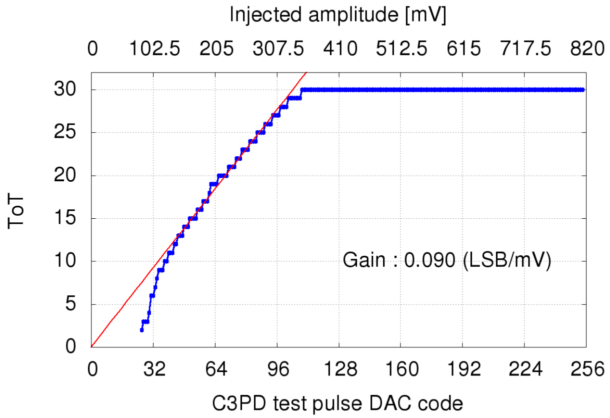
CLICpix + CCPDv3



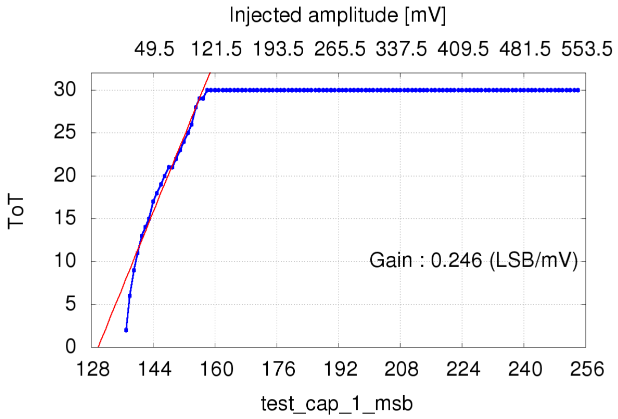
Plot: M. Vicente

Measurements on coupling (glue) capacitance

- The ToT was measured as a function of the injected pulse amplitude
  - First using the C3PD pixel with direct test pulse monitoring (the injected pulse resembles a square waveform)
  - Then using the CLICpix2 internal test pulse
- In both cases, the $\frac{ToT}{V_{inj}}$ was extracted for the linear part of the curve, where V_{inj} is the amplitude of the injected pulse
- The injected charge is $V_{inj} \times C_{coupl}$ for the pulses injected from C3PD and $V_{inj} \times C_{test}$ for the CLICpix2 internal test pulses
- Using the design value for the CLICpix2 test pulse injection capacitance ($C_{test} = 10fF$), one can then estimate the coupling capacitance (C_{glue}):
  - Assembly 1: C_{glue} = 3.66 fF
  - Assembly 6: C_{glue} = 1.43 fF
  - Assembly 7: C_{glue} = 2.95 fF



Measured ToT as a function of the test pulse DAC code injected from C3PD



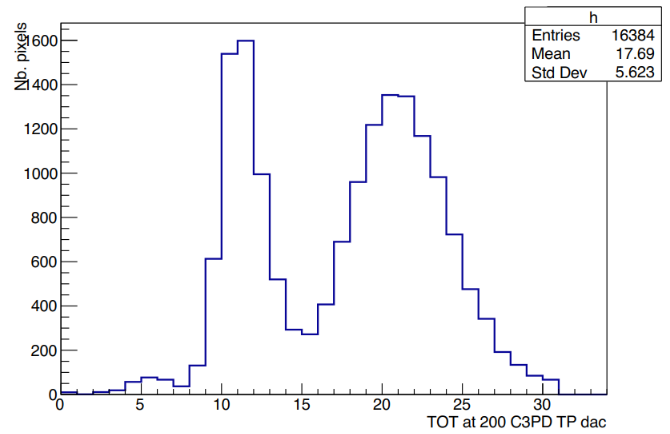
Measured ToT as a function of the test pulse DAC code injected from CLICpix2

** Please refer to back-up slides for detailed calculations*

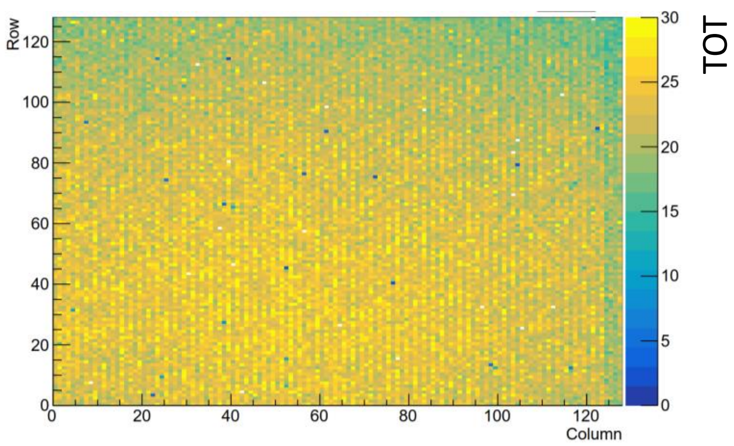
Test pulse measurements

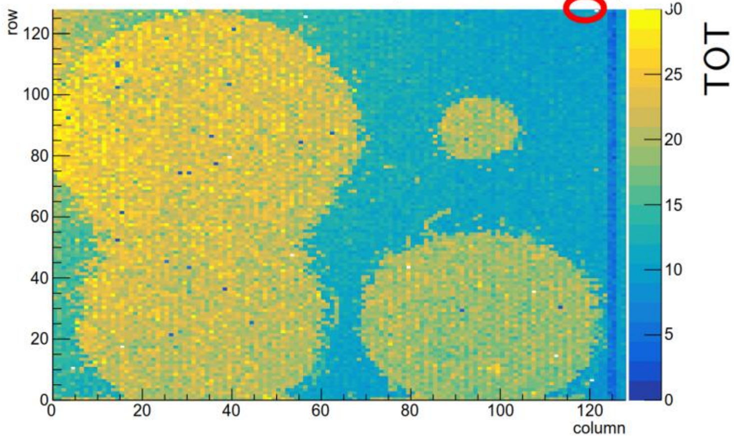
- The above calculation only refers to one pixel at the edge of the pixel matrix
- The ToT has been measured for all CLICpix2 pixels, injecting the same C3PD test pulse amplitude
- Variations in response across the matrix have been observed in some assemblies
  - Assembly 6 shows strong inhomogeneity from glue dots
  - Gluing process to be optimised

CLICpix2 ToT response to C3PD test pulses, assembly 6



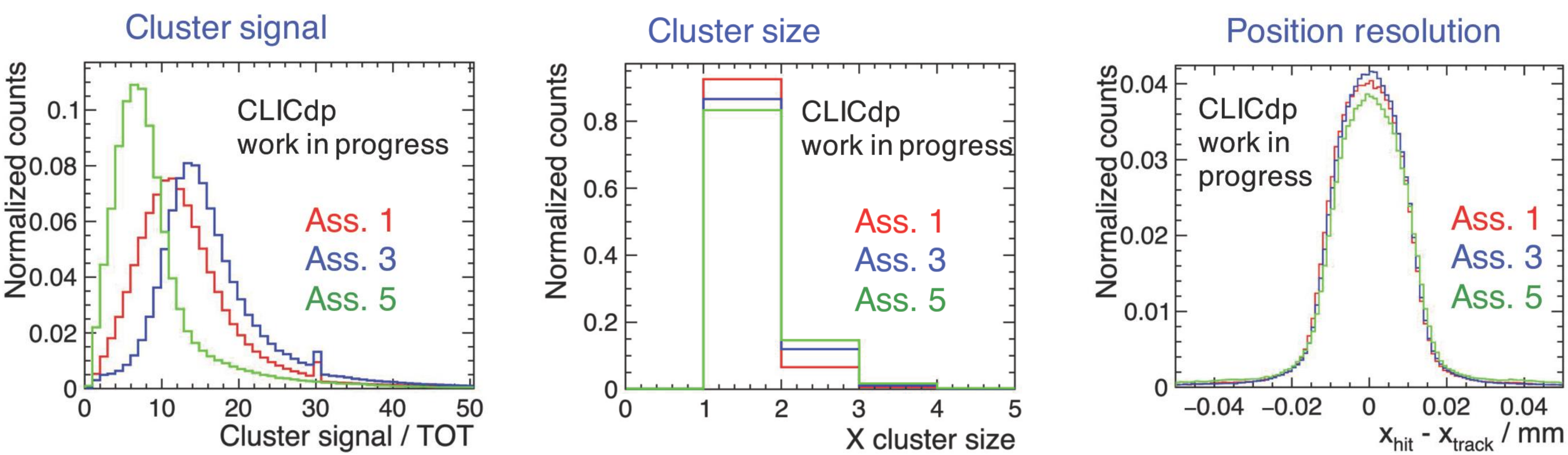
C3PD test pulse, fixed amplitude, assembly 10





Test-beam measurements

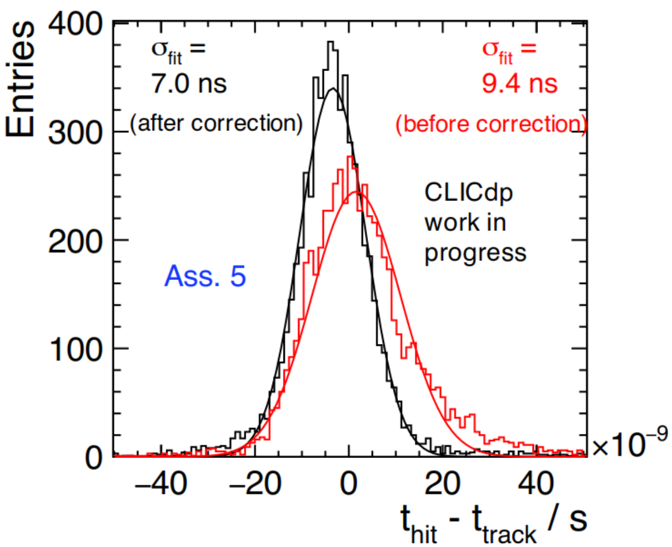
- Test-beam measurements for capacitively coupled assemblies of CLICpix2 + C3PD (20 Ωcm) in CLICdp Timepix3 telescope
- Preliminary results show differences in cluster signals and sizes
  - Expected from varying glue assembly quality
- CLICpix2 threshold set to $\sim 850\ e^-$
- Most dominantly single-pixel hits, limiting factor for spatial resolution
  - 8.5 – 9 µm residual RMS



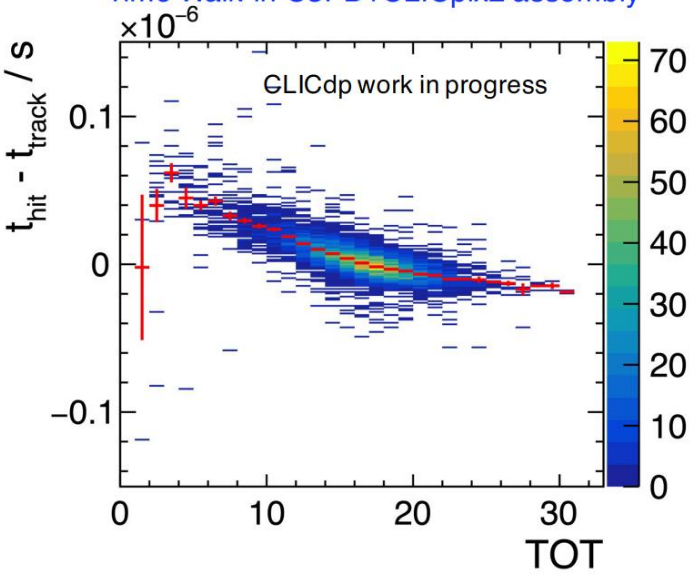
Test-beam measurements

- The ToA counter is 8-bit long with 10 ns steps
  - Shutter is limited to 2.5 µs
- The time difference between reconstructed hit and track is plotted
  - Gauss fit of time residuals shows width of ~9 ns
- ToT information can be used to correct for time walk effect
  - After time-walk correction the time residual is reduced to 7 ns

Hit time residuals in C3PD+CLICpix2 assembly



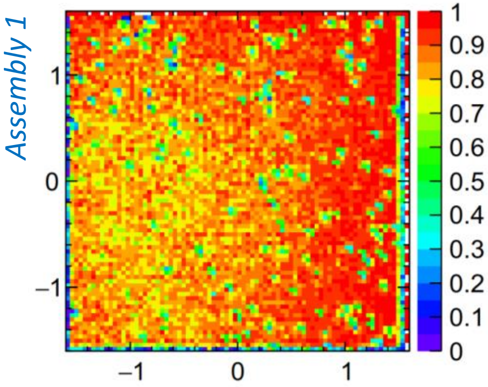
Time Walk in C3PD+CLICpix2 assembly

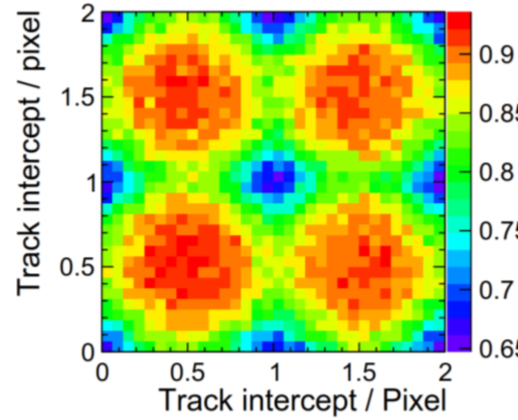


Test-beam measurements

- Efficiency measurement
  - Across the pixel matrix and
  - Folded into a 2 × 2 pixel array
  - Overall efficiency of the assembly: 85 %

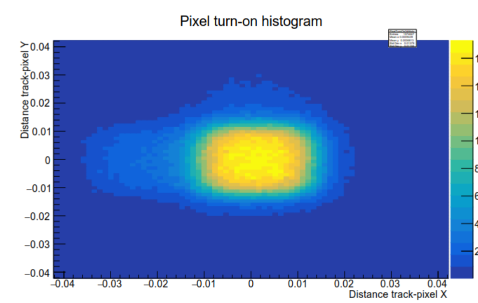
Assembly 1

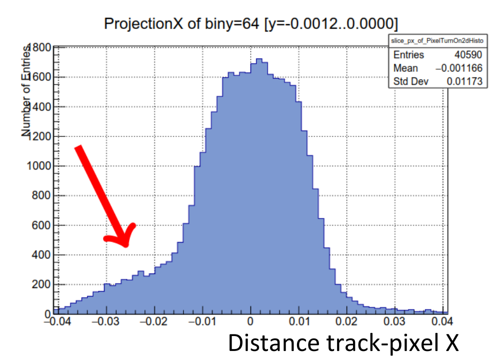




- Cross-talk – asymmetric coupling
  - Asymmetric cross-talk was observed in some cases (eg. Assembly 5)
  - Could be a result of misalignment during the flip chip assemblies
  - To be cross-checked with test pulse data

Assembly 5

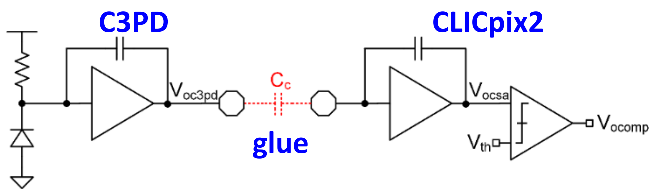




- Charge transferred to the CLICpix2 front-end
  - Assuming a $1\ ke^-$ MIP at the C3PD input, a charge gain of $190\ mV/ke^-$ for the C3PD front-end, and a coupling capacitance $\sim 3.5\ fF$, the expected charge at the input of the CLICpix2 front-end would be $\sim 4\ ke^-$
  - The detected charge is $\sim 40\%$ less than expected (based on the ToT calibration and the CLICpix2 test pulse capacitance – slide 10)
  - Many uncertainties, calculations based on simulated/design values (MIP charge at C3PD, glue capacitance, charge to ToT conversion)

Simulations on signal transfer

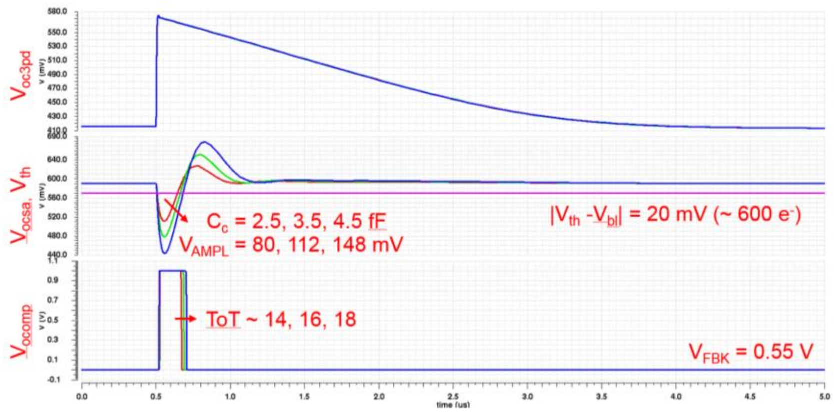
- The signal transfer from C3PD to the CLICpix2 front-end was simulated using extracted netlist for both circuits
  - The coupling is assumed as an ideal capacitor C_c
  - A charge of 1 ke^- was used as the input of C3PD (rough approximation for a MIP charge)
  - Simulation performed for different pulse shapes. No significant degradation observed



- Simulated C3PD + CLICpix2 chain seems to behave as we would expect
- It is still not clear why the measured signal transferred from C3PD to CLICpix2 is weaker than expected
  - Measured values of the coupling capacitance are close to expected
  - The response to MIPs needs to be further studied

Signal transfer including noise

Signal transfer for different glue capacitance



Plots: E. Santin

Summary and further testing

- Thanks to the capacitive coupling, it was possible to test the CLICpix2 readout chip with particles, before receiving assemblies with planar sensors

- The CLICpix2 and C3PD ASICs have been characterised in standalone mode as well as in capacitively coupled assemblies:
  - C3PD samples with 80 Ωcm substrate resistivity show similar performance to the ones with standard resistivity (20 Ωcm) in terms of noise, rise time and leakage current.
  - First 80 Ωcm C3PD samples show a gain ~10% lower. More statistics are needed in order to investigate further
  - The amount of charge collected by drift is expected to be larger for the higher substrate resistivity – to be confirmed in beam tests
  - Variations in glue uniformity and alignment have been observed
  - The measured response to MIPs is weaker than expected from simulations and calibration measurements

- Next steps:
  - C3PD samples with 200 Ωcm substrate resistivity will be characterised in beam tests (wafers are produced, chips are expected in the coming weeks)
  - Testing CLICpix2 with planar sensors is needed in order to fully characterise the chip. Single chip bump bonding of CLICpix2 and planar active-edge sensors is in progress at IZM. First assemblies expected in February.

Thanks to everyone who contributed to this work!

References

[1] E. Santin, P. Valerio and A. Fiergolski: CLICpix2 User's Manual (2016)
https://www.overleaf.com/4621916xdqqmb#/13998870/

[2] I. Kremastiotis et al: Design and standalone characterisation of a capacitively coupled HV-CMOS sensor for the CLIC vertex detector (2017),
https://arxiv.org/pdf/1706.04470.pdf

[3] N. Alipour Tehrani et al., Capacitively coupled hybrid pixel assemblies for the CLIC vertex detector (2016)
https://doi.org/10.1016/j.nima.2016.03.072

[4] A. Fiergolski: A multi-chip data acquisition system based on a heterogeneous system-on-chip platform (2017),
https://cds.cern.ch/record/2272077/

[5] M.Vicente: Finite-element simulations of coupling capacitances in capacitively coupled pixel detectors (2017),
https://cds.cern.ch/record/2267848/

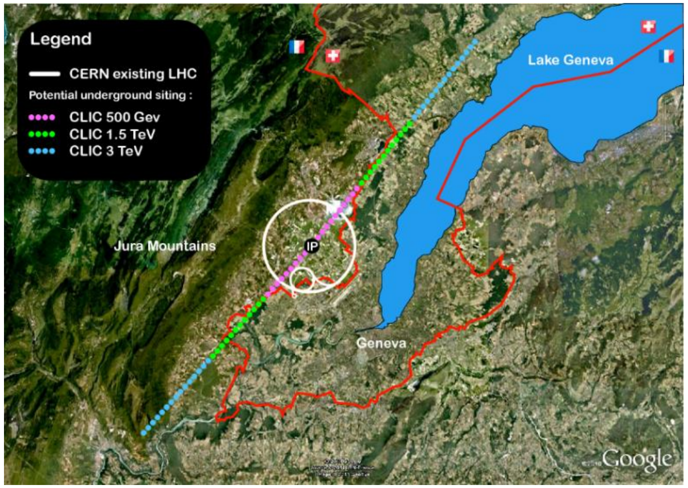
Back-up slides

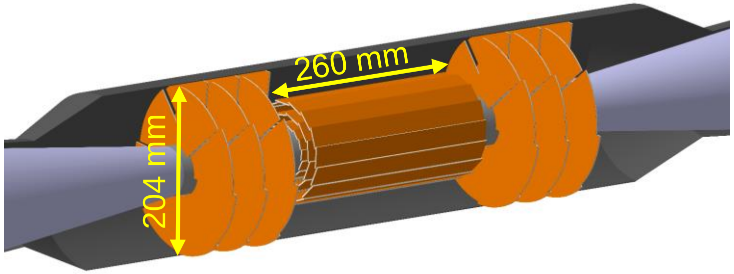
The CLIC vertex detector requirements

- Requirements for the CLIC vertex detector:
  - Single point resolution: 3 µm
  - Material budget: $< 0.2\% \, X_0$ per detection layer (corresponding to $100 \, \mu m$ for silicon sensor and readout chip)
  - Time-stamping resolution: 10 ns
  - Power consumption: $< 50 \, mW/cm^2$ (after power pulsing)

- The CLIC beam structure consists of bunch trains at a repetition rate of 50 Hz
  - Each bunch train consists of 312 bunch crossings separated by 0.5 ns
  - Thanks to the low duty cycle of the CLIC beam ($156 \, ns/20 \, ms$), a power pulsing scheme can be introduced in order to power down the main driving nodes of the front-end between subsequent bunch trains. The average power consumption over the $50 \, Hz$ cycle can therefore be minimised

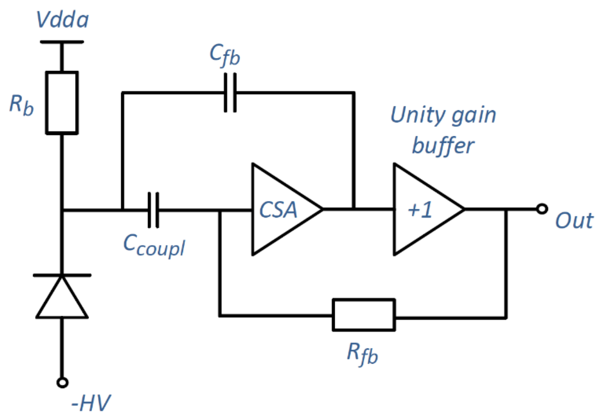
- The capacitive coupling between an active HV-CMOS sensor and a readout ASIC has been considered in the framework of the CLIC vertex detector study



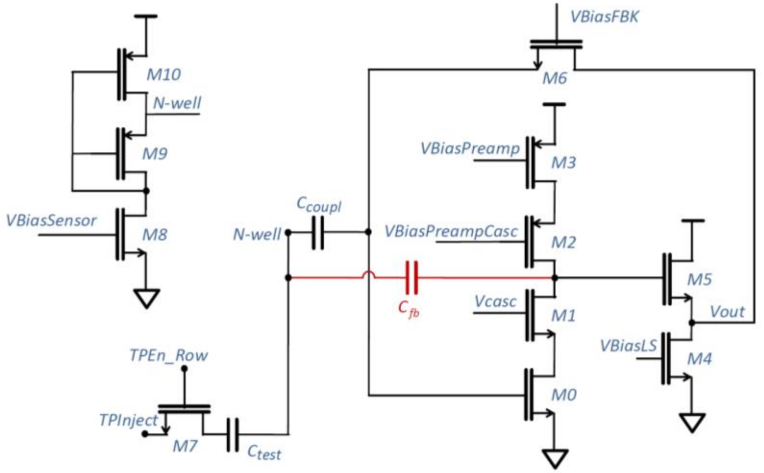


The CLICpix Capacitively Coupled Pixel Detector (C3PD)

- Active HV-CMOS sensor to be used in capacitively coupled assemblies with the CLICpix2 readout chip
  - Produced in a commercial 180 nm HV-CMOS process
  - Requirements:
    - 128×128 square pixels with 25 μm pitch
    - Rise time: $\sim 20\ ns$
    - Charge gain: $> 120\ mV/ke^{-}$
    - Power consumption: $< 50\ mW/cm^2$ (both for sensor and readout chip, after power pulsing)
  - The analog front-end is based on a charge sensitive amplifier (CSA), followed by a unity gain buffer



Block diagram of the C3PD pixel



Schematic of the C3PD pixel

ToT vs C3PD test pulse (for 'tot_clk_div = 0')

- The ToT was measured as a function of the injected pulse amplitude, using the C3PD pixel with direct test pulse monitoring (so that the injected pulse resembles a square waveform)

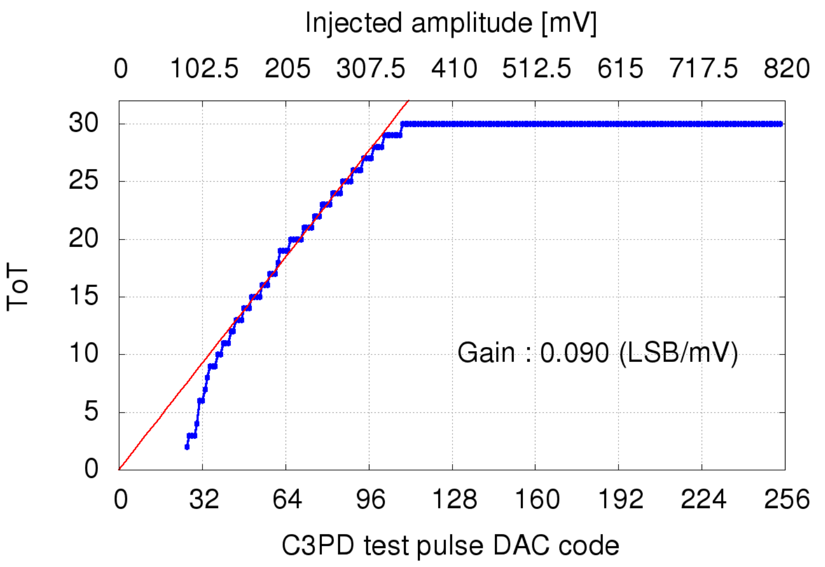
- As extracted from the slope of the curve, the 'gain' of the ToT is: $0.09\frac{LSB}{mV}$, or $90\frac{LSB}{V}$

- $ToT = 90\,V_{inj}$ (1)

- $V_{inj} = \frac{Q_{inj}}{C_{coupl}}$ (2)

  where V_{inj} is the pulse amplitude injected to the coupling capacitance, Q_{inj} the injected charge, and C_{coupl} the coupling capacitance

- From (1) and (2): $ToT = 90\frac{Q_{inj}}{C_{coupl}}$ (3)



ToT vs CLICpix2 test pulse (for 'tot_clk_div = 0')

- The ToT was measured this time as a function of the CLICpix2 injected pulse amplitude

- As extracted from the slope of the curve, the 'gain' of the ToT is: $0.246\,\frac{LSB}{mV}$, or $246\,\frac{LSB}{V}$

- $ToT = 246\,V_{inj}$ (4)

- $V_{inj} = \frac{Q_{inj}}{C_{test}} = \frac{Q_{inj}}{10 \cdot 10^{-15}}$ (5)
  where V_{inj} is the pulse amplitude injected to the test pulse capacitance, Q_{inj} the injected charge, and C_{test} the test pulse capacitance (10fF by design)

- From (4) and (5): $ToT = 24.6 \cdot 10^{15} Q_{inj}$ (6)

- From (3) and (6): $90\,\frac{Q_{inj}}{C_{coupl}} = 24.6 \cdot 10^{15} Q_{inj}$

→ $\boldsymbol{C_{coupl} = 3.66\ fF}$