The thermo-mechanics of ultra-thin, integrated silicon ladders

CLIC workshop
CERN, Jan. 2018

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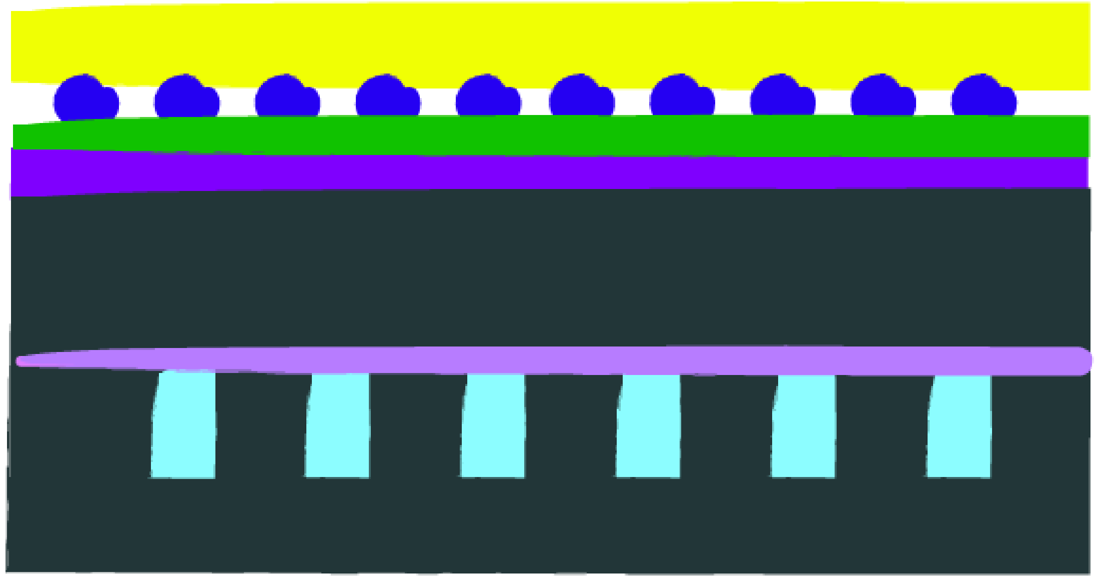
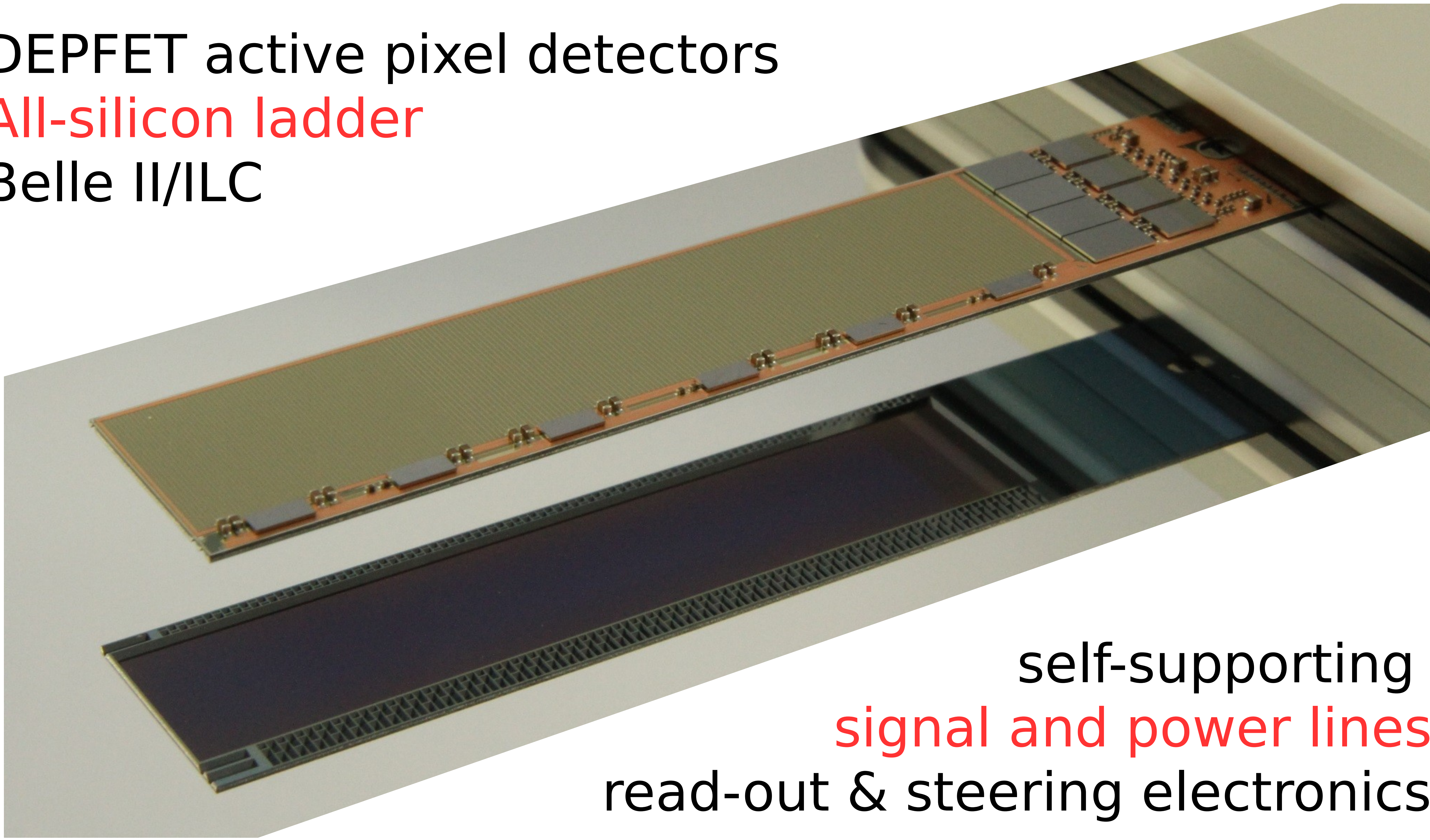


This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168

Thin silicon

DEPFET active pixel detectors
All-silicon ladder
Belle II/ILC



self-supporting
signal and power lines
read-out & steering electronics

Air cooling

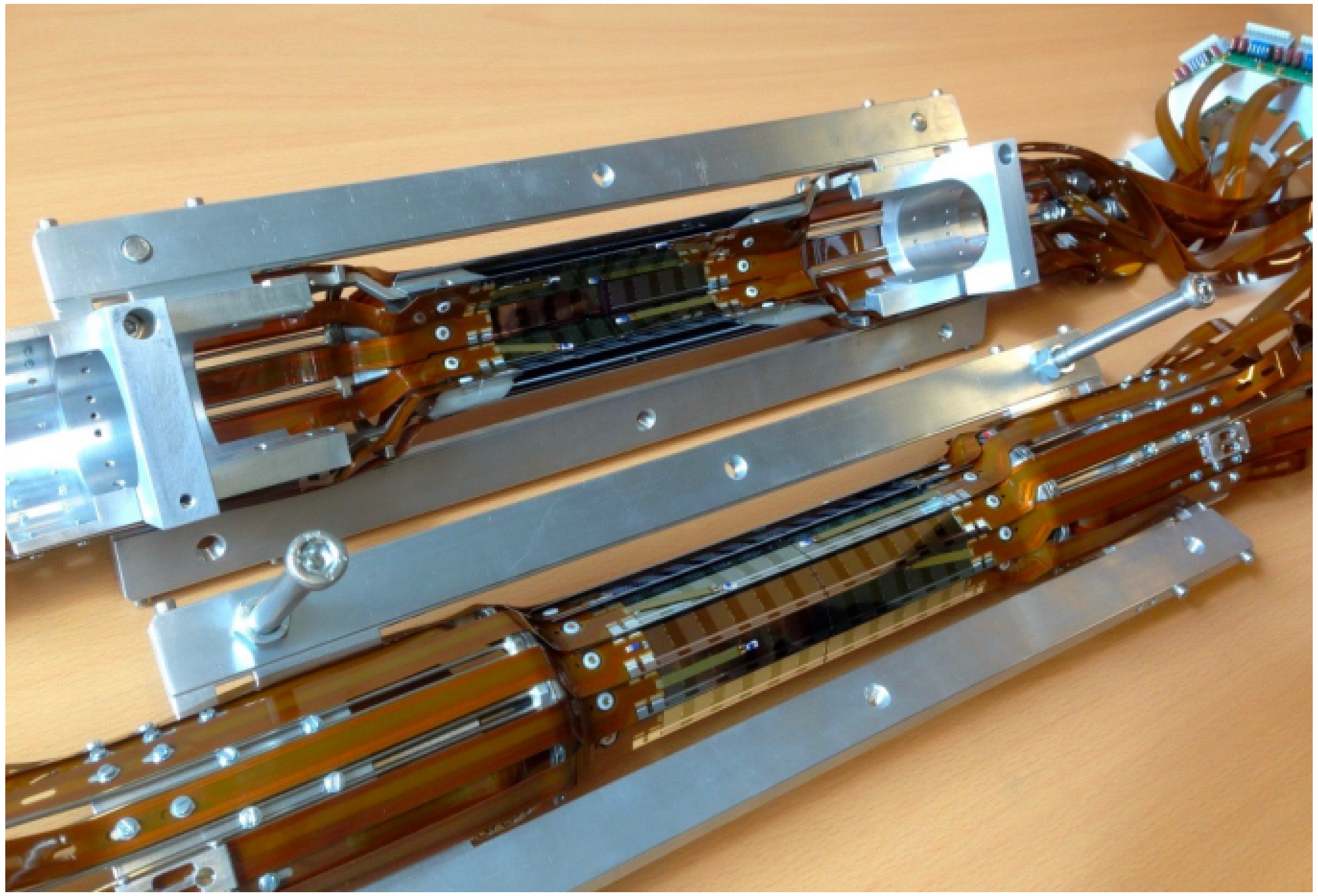
Ultra-thin silicon, power pulsing and air cooling?

Keep the silicon cool without affecting the stability or compromising the integrity!

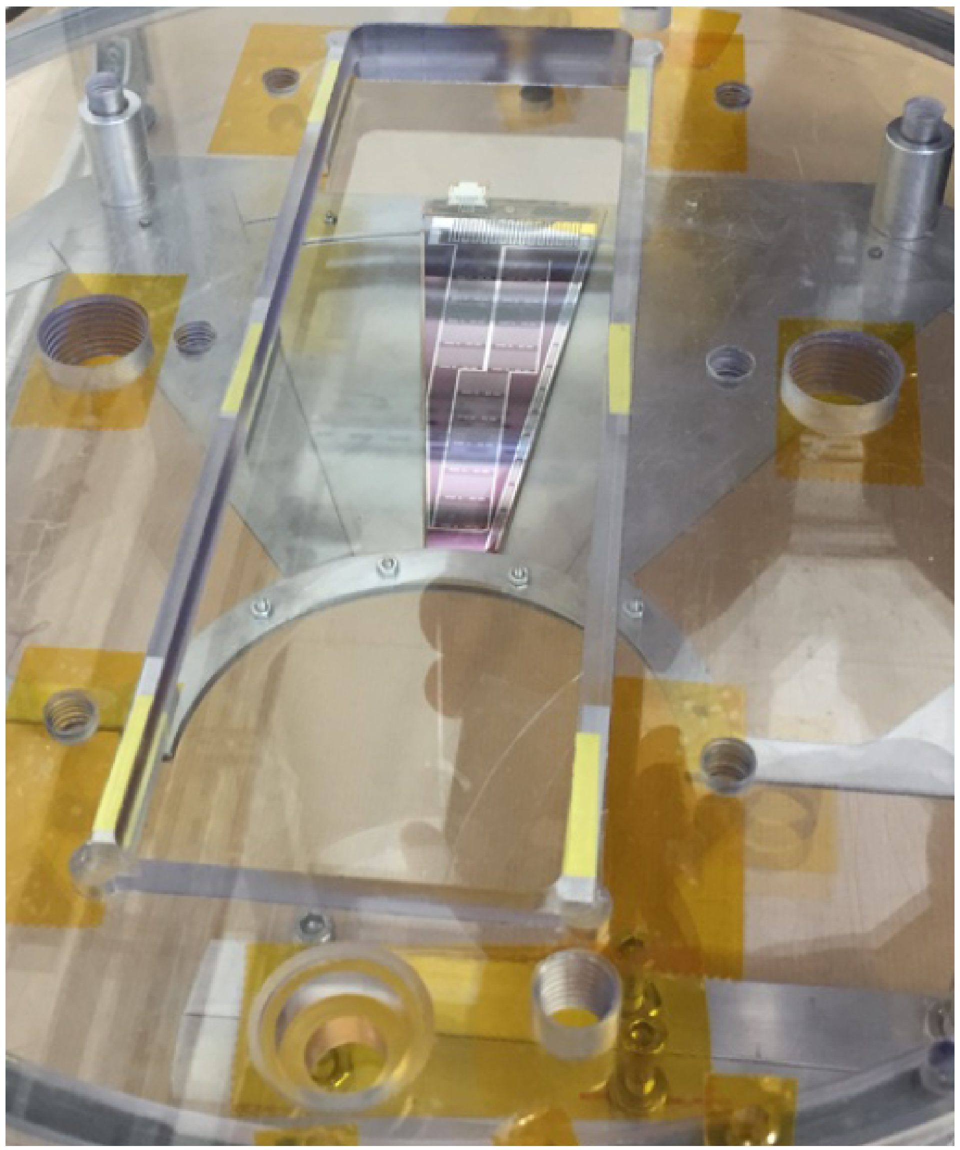
Experience with air cooling in STAR
arXiv:1710.02176

Extensive studies in Belle II mock-up,
arXiv:1607.00663

Aggressive plans for Mu3e!
arXiv:1610.02021

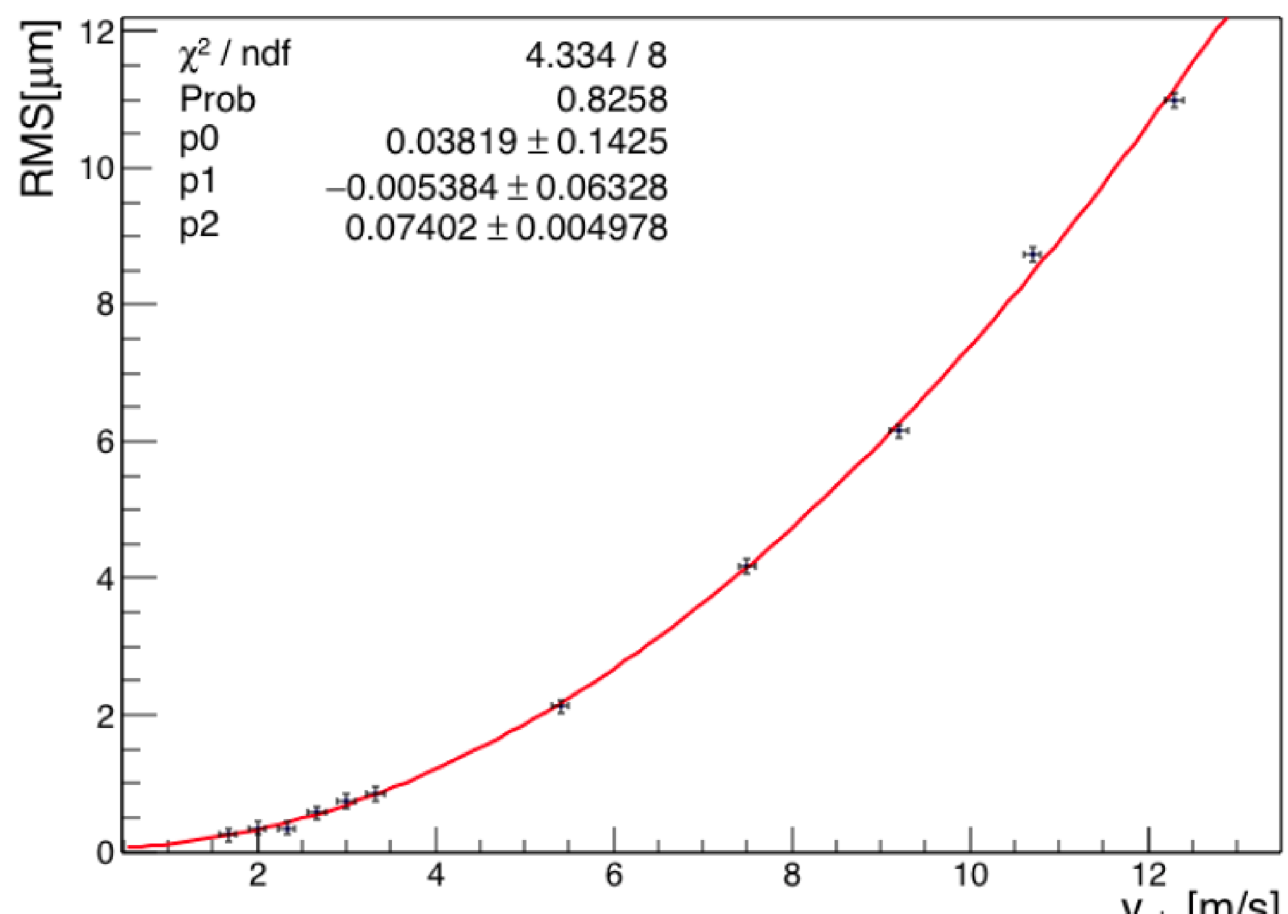


Air cooling & mechanical stability



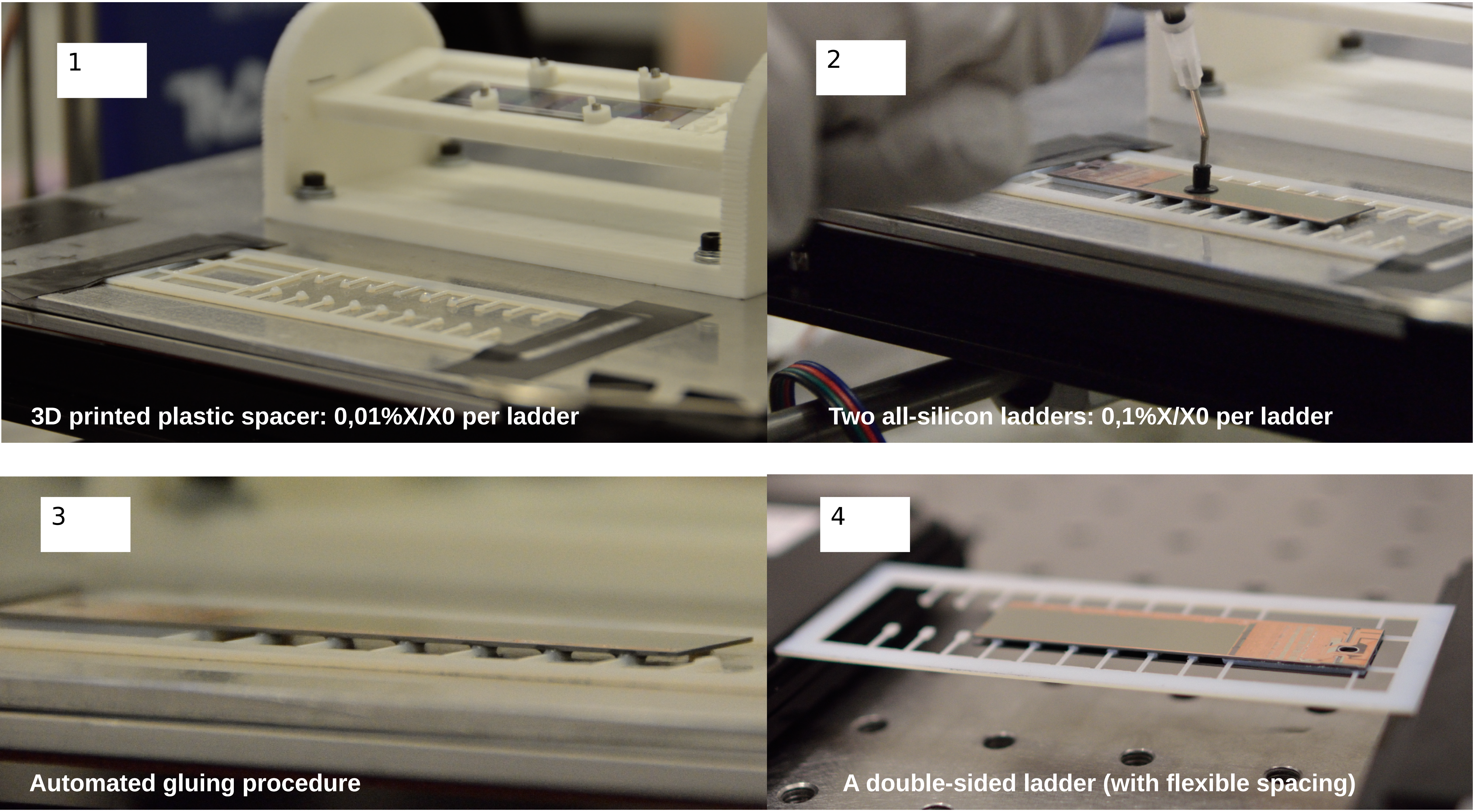
Dummy petal in CERN wind tunnel

Vibrations remain acceptable for air speed up to several m/s



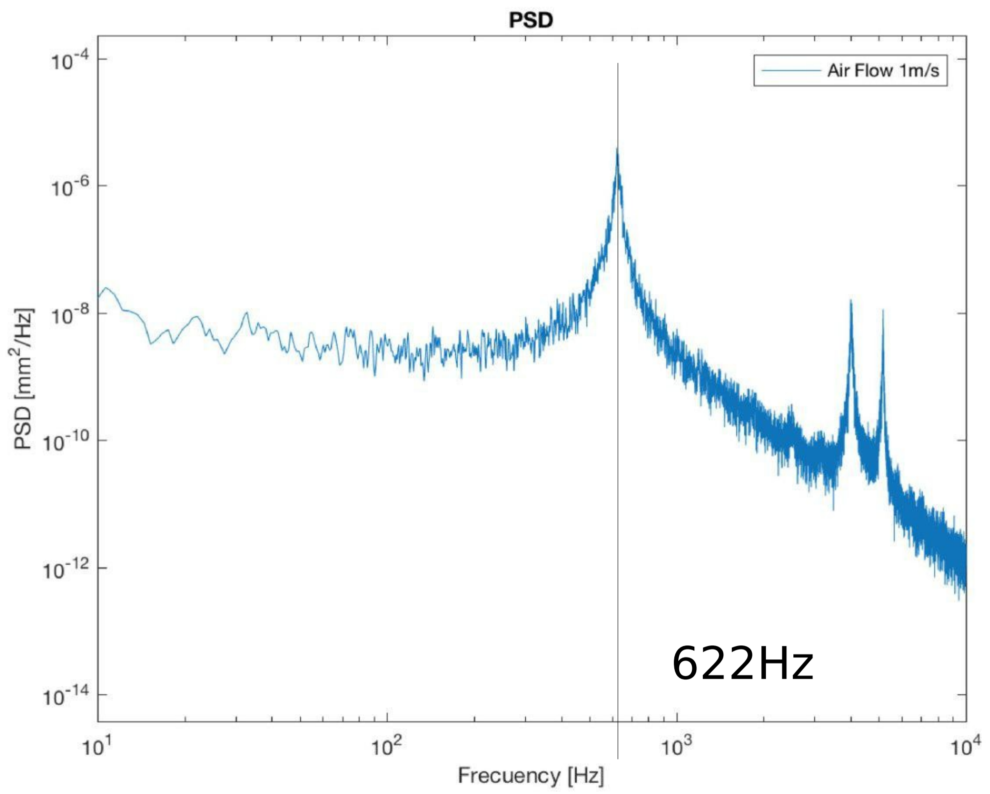
Ph.D. thesis Nacho Garcia,
U. Valencia, 2016

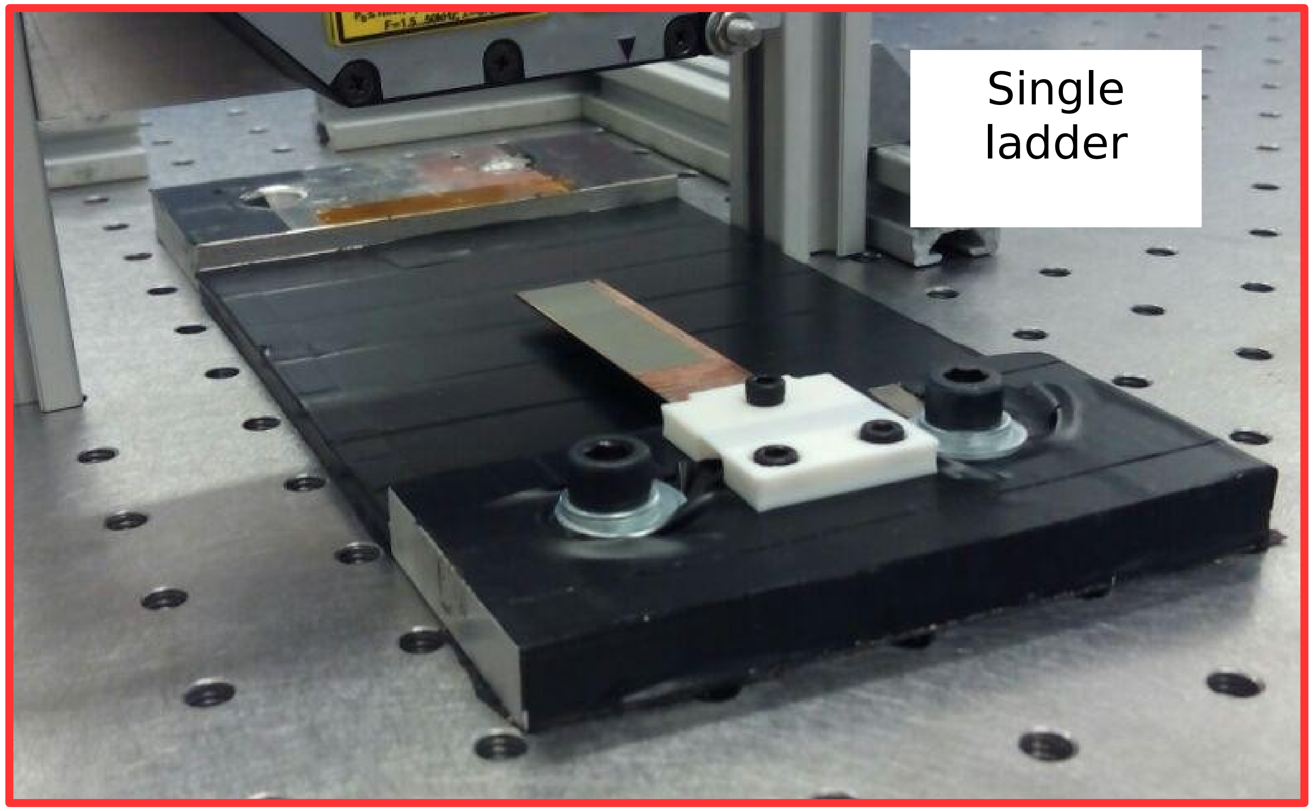
Double-sided structures

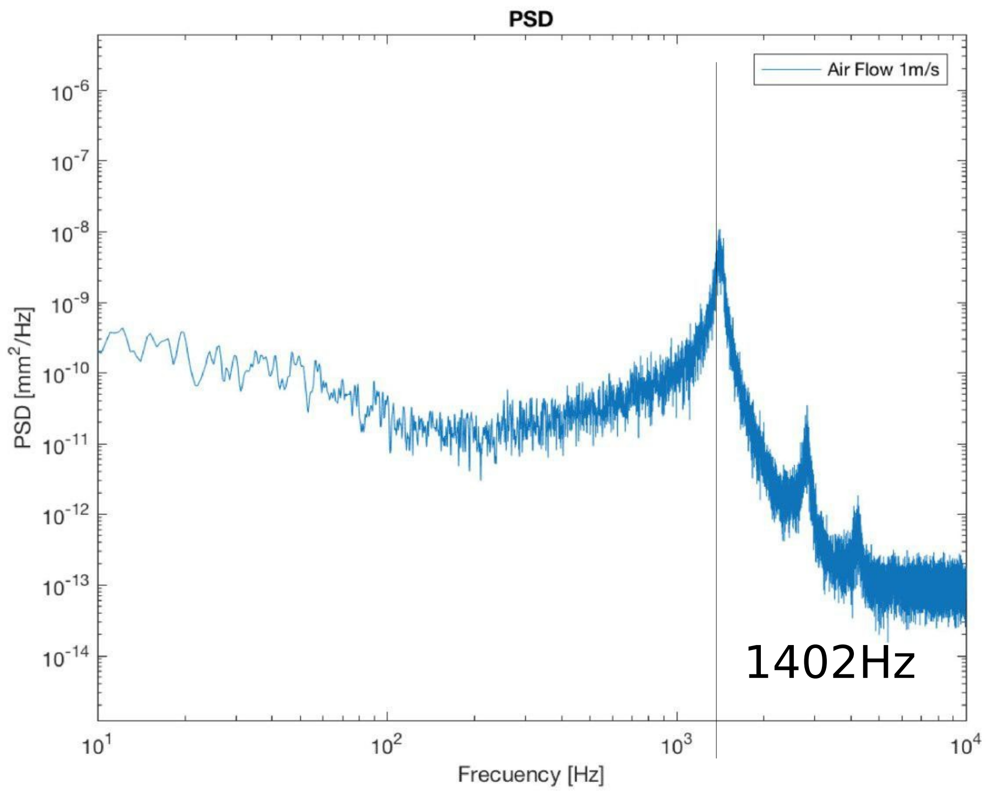


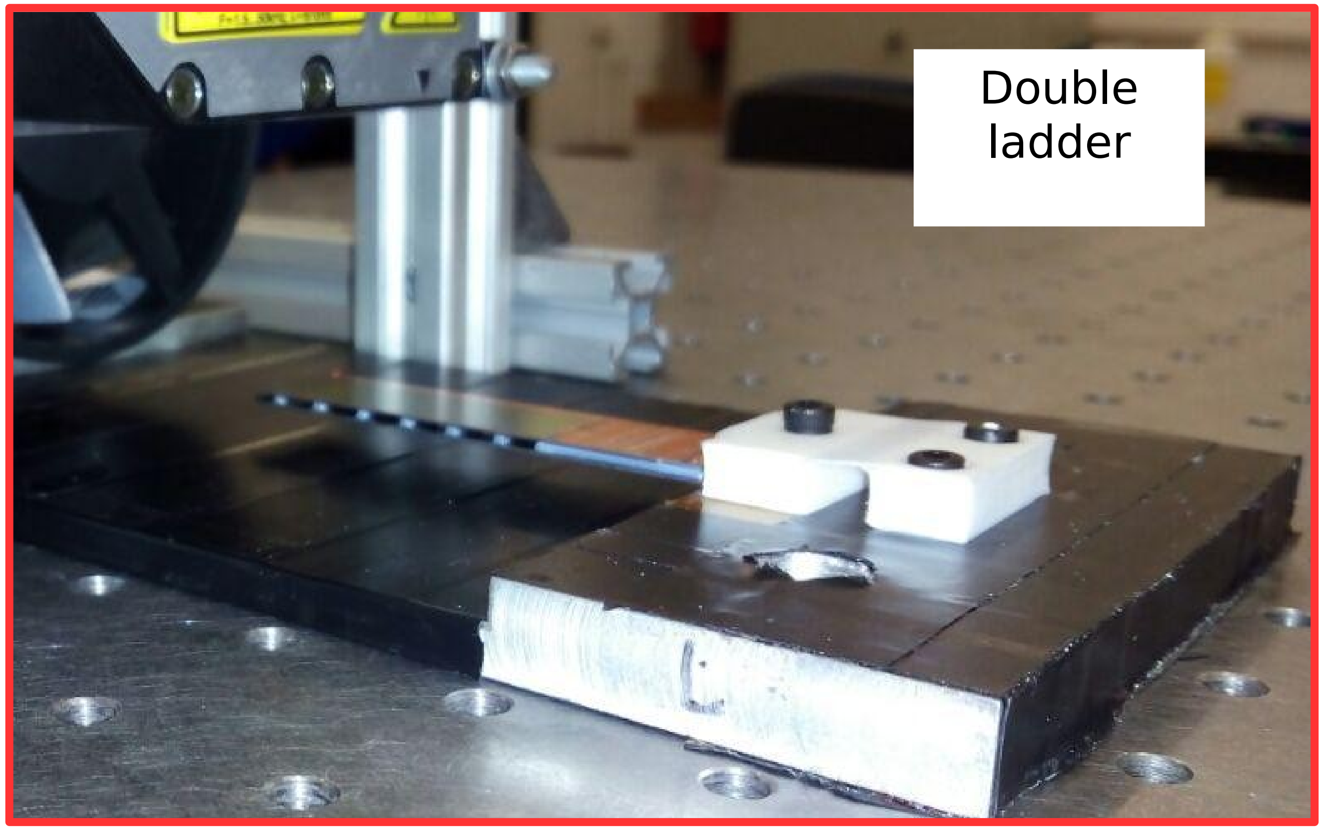
Double-sided structures based on all-silicon ladders

Air cooling









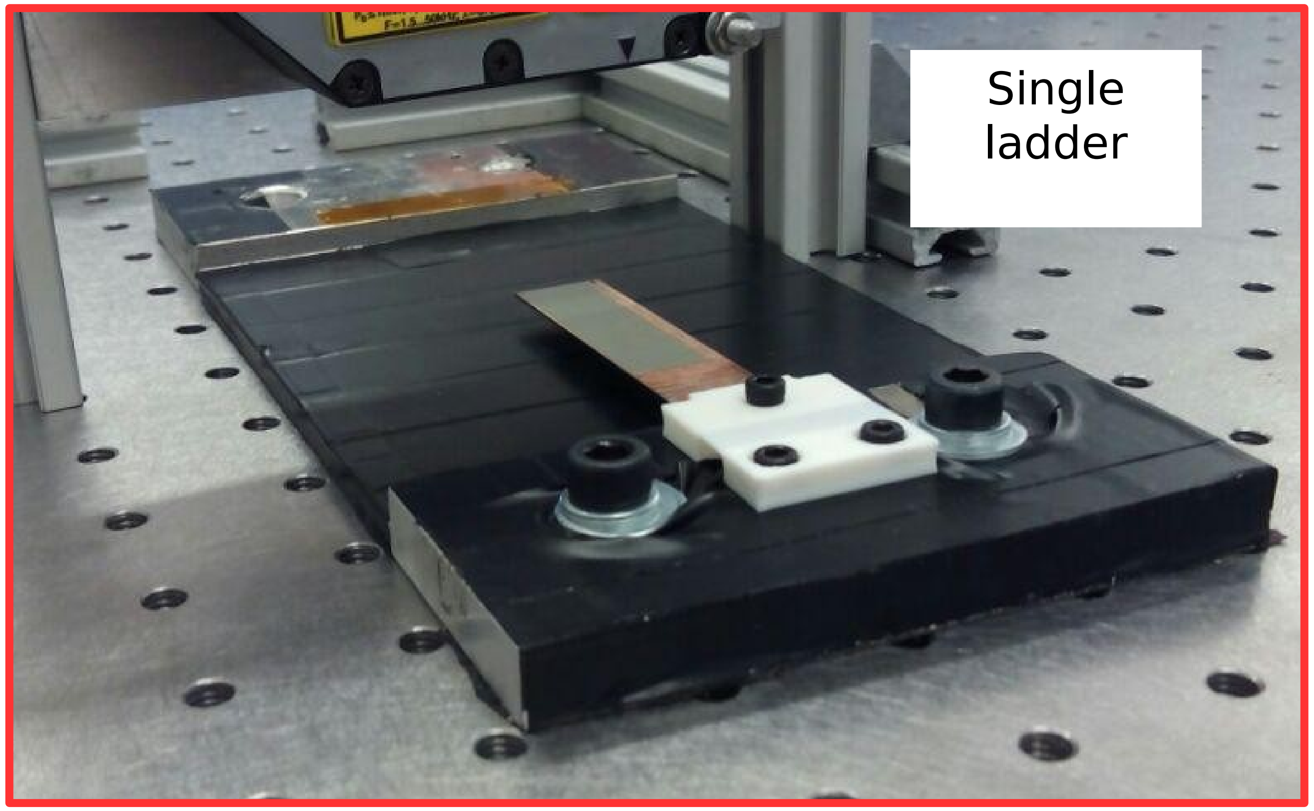
Double-sided structures have considerably higher eigenfrequency

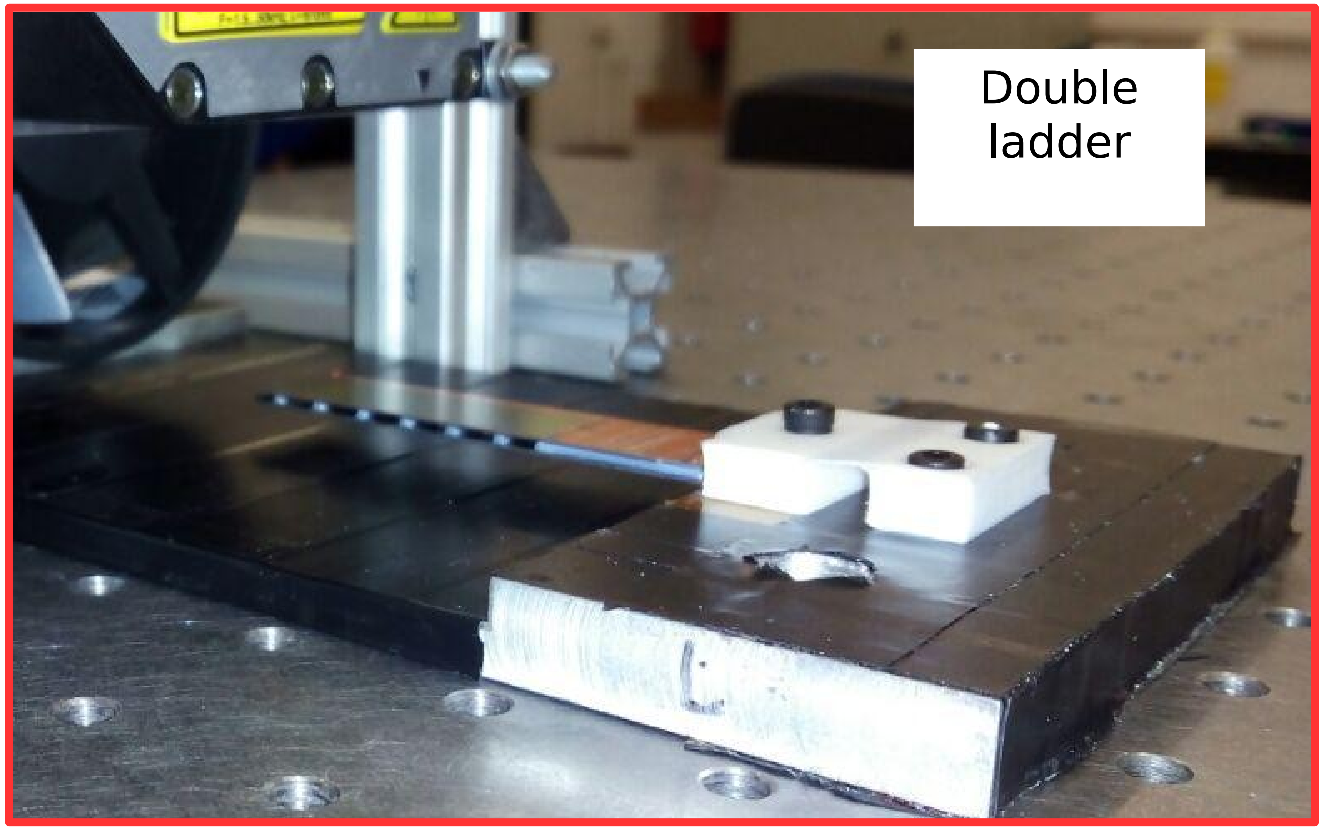
Air cooling

Double-sided structures improve resilience against air-induced vibrations

v=1m/s	Peak2Peak	RMS
Single ladder	68um	7,2um
Double ladder	8,1um	2,2um

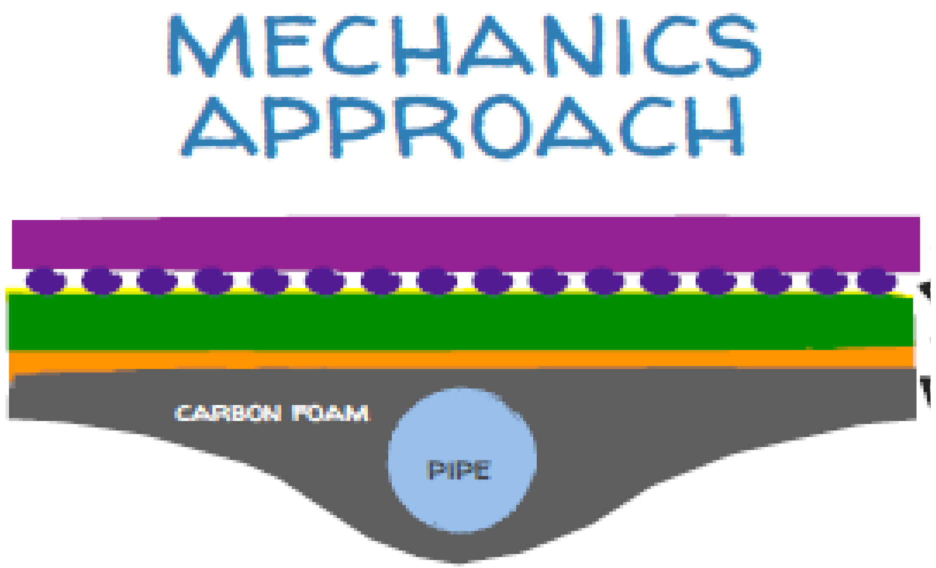
Note: ladders supported on one side only to amplify effects
Note: thick silicon (thinned assembly soon)
Note: petal-shaped structure to follow later





The case for MCC in HEP

Large channel density
→ power consumption
Tightly coupled FE and sensor
→ FE heats up sensors
Control sensor temperature
→cold or uniform
Minimal material!!!!!!



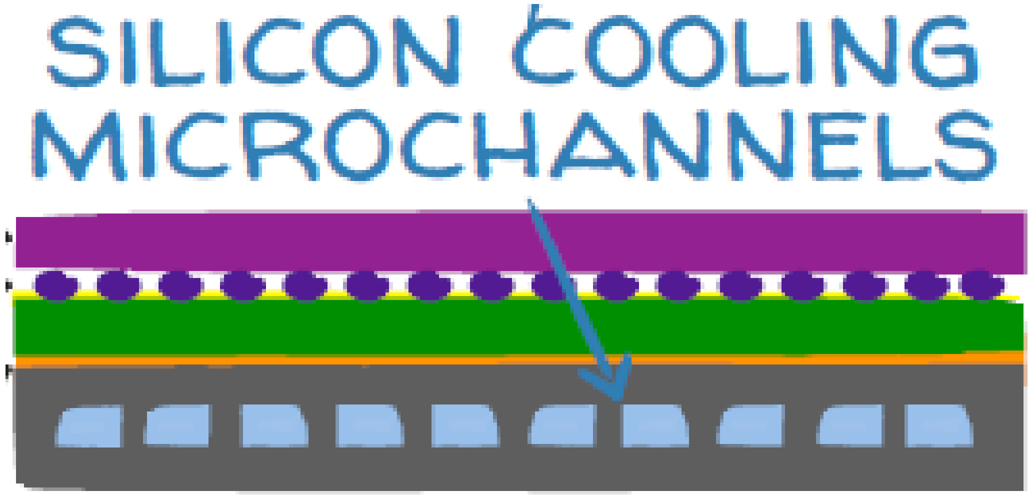
Issues with traditional approach:

→ glue layers and interfaces (thermal barriers)
→ high-Z materials (material budget)
→ small coolant contact area (bottle-neck)
→ CTE mismatch (cf. ATLAS IBL experience)

Cooling of silicon detectors

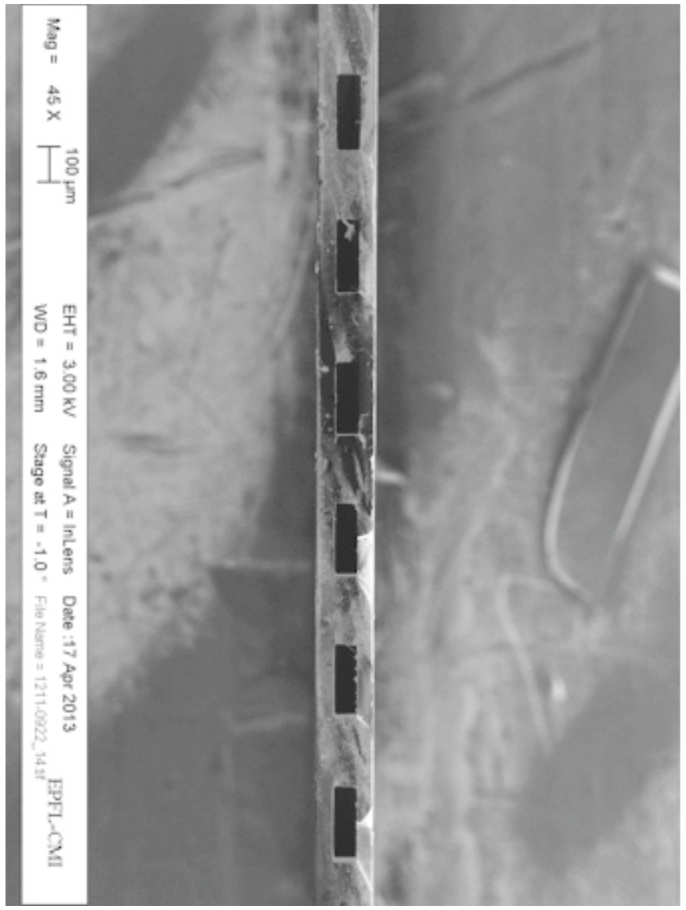
Micro Channel Cooling seems to be the natural solution

Direct large-area contact
→ minimal thermal barriers
Silicon as support material
→ CTE matched
Advanced μ-electronics techniques
→adapted to very small
Minimal material!!!!!



And, indeed, quite some interest in HEP
Na62, LHCb, ALICE, ATLAS, DEPFET
AIDA2020-WP9 provides a forum,
“standards” & generic R&D

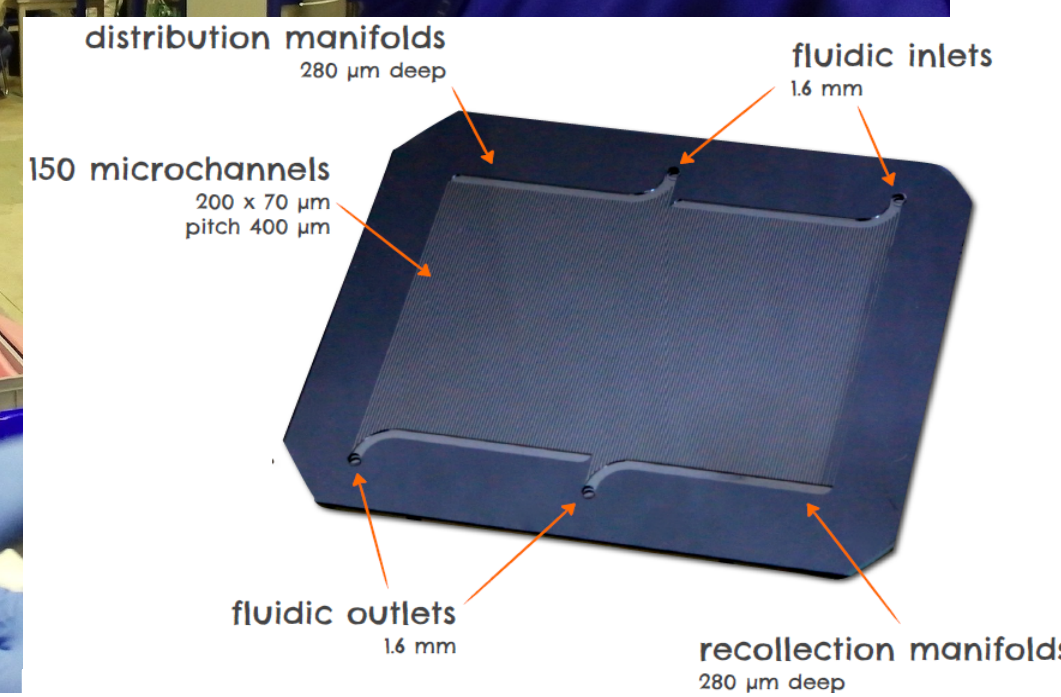
NA62 GTK: first MCC in HEP



Experiment running since 2014

Hybrid pixel detector: 40 W on 3x6 cm^2

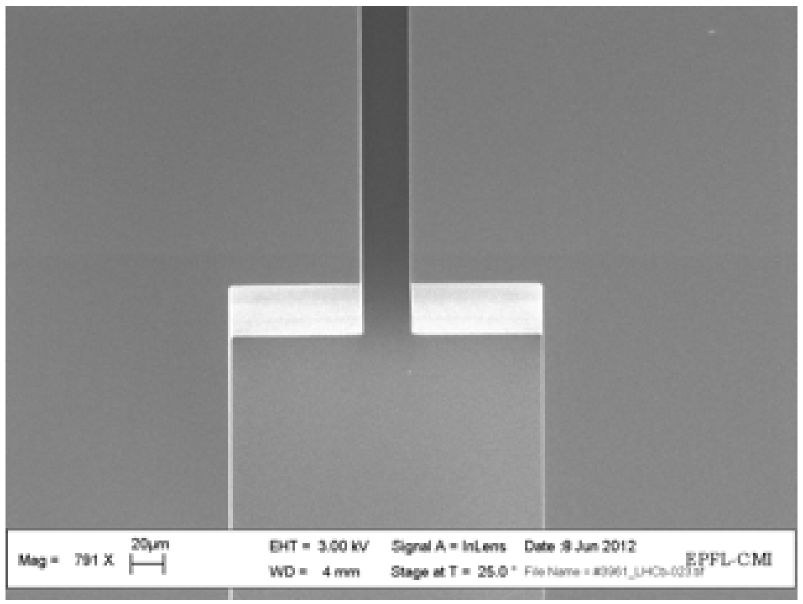
Liquid cooling (mono-phase C6F14 at -20C)

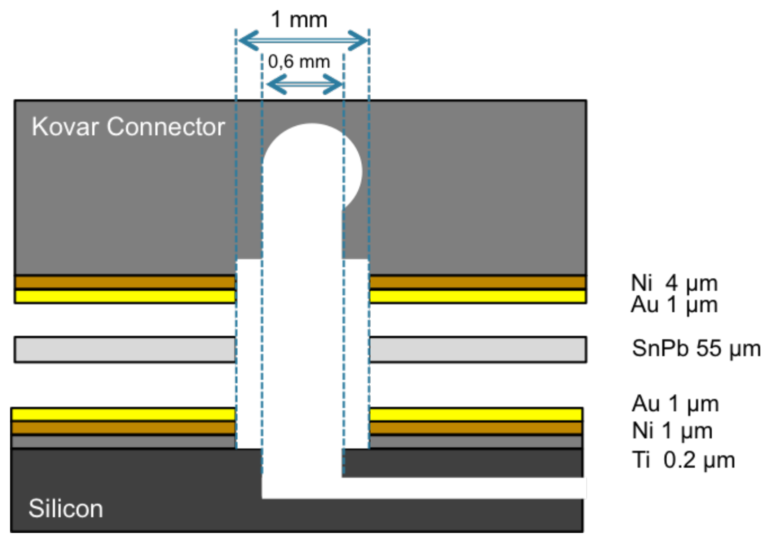


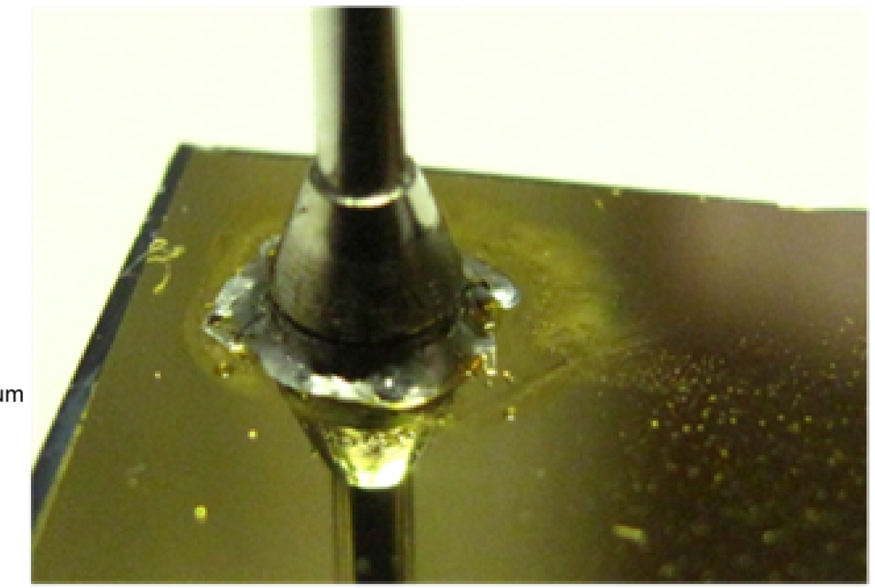
A.Francescon et al:
Application of micro-channel cooling to the local thermal management of detectors electronics for particle physics,
Microelectronic Journal, Volume 44, Issue 7, July 2013, Pages 612–618

Who’s next?

LHCb → CO_2 cooling plate → high pressure MCC!!



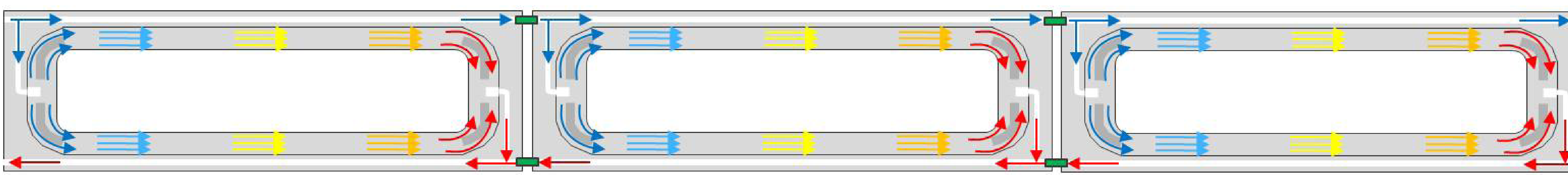




LHCb VELO upgrade, JINST 11 C05014

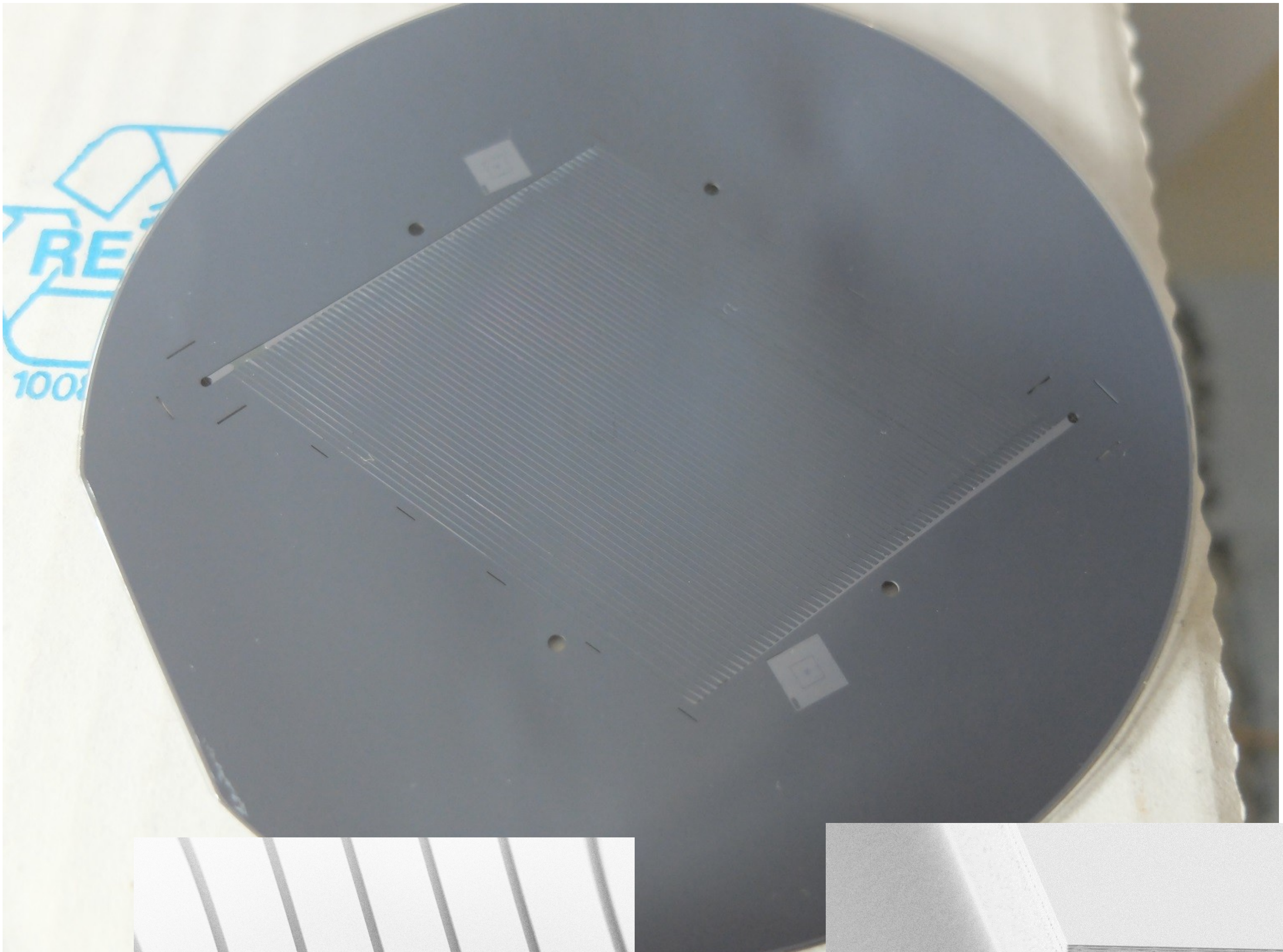
ALICE-ITS upgrade alternative design → MCC in acceptance

No place to hide: long ladders in acceptance require low-X_0 connectors

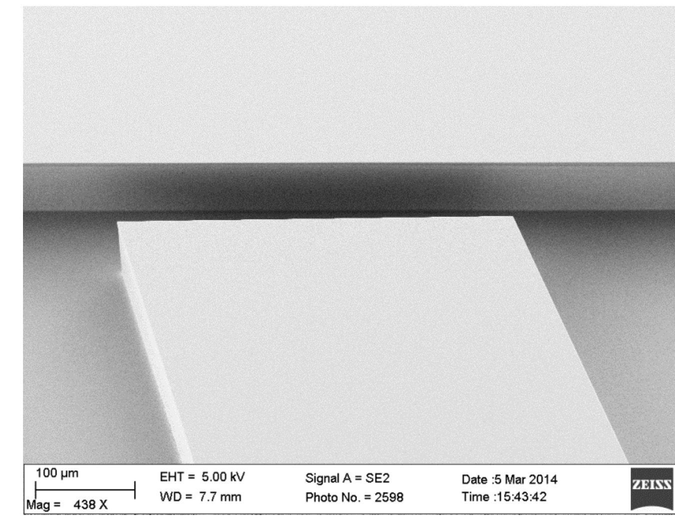


CNM/DESY

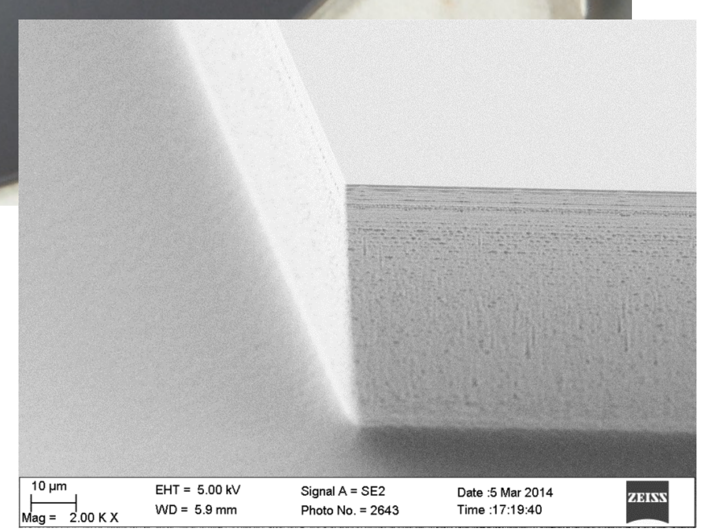
Courtesy of Nils Flaschl, DESY

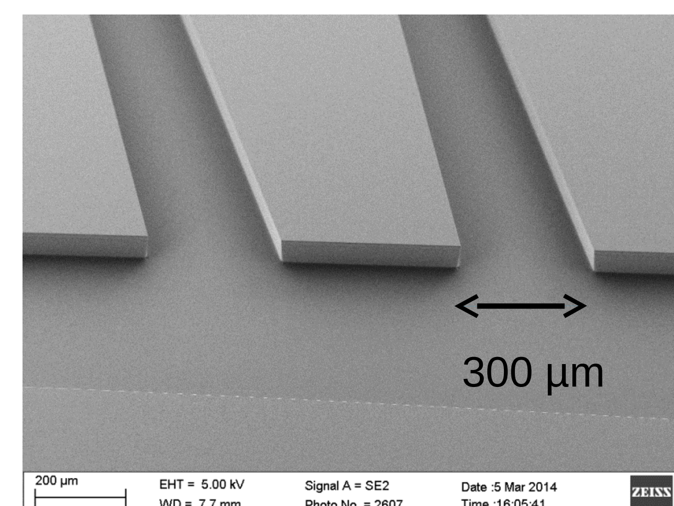


Sample with a Pyrex top to close the channels
Silicon thickness: 375 μm
Pyrex thickness: 500 μm



Electron microscope images of the channels after being etched into the silicon





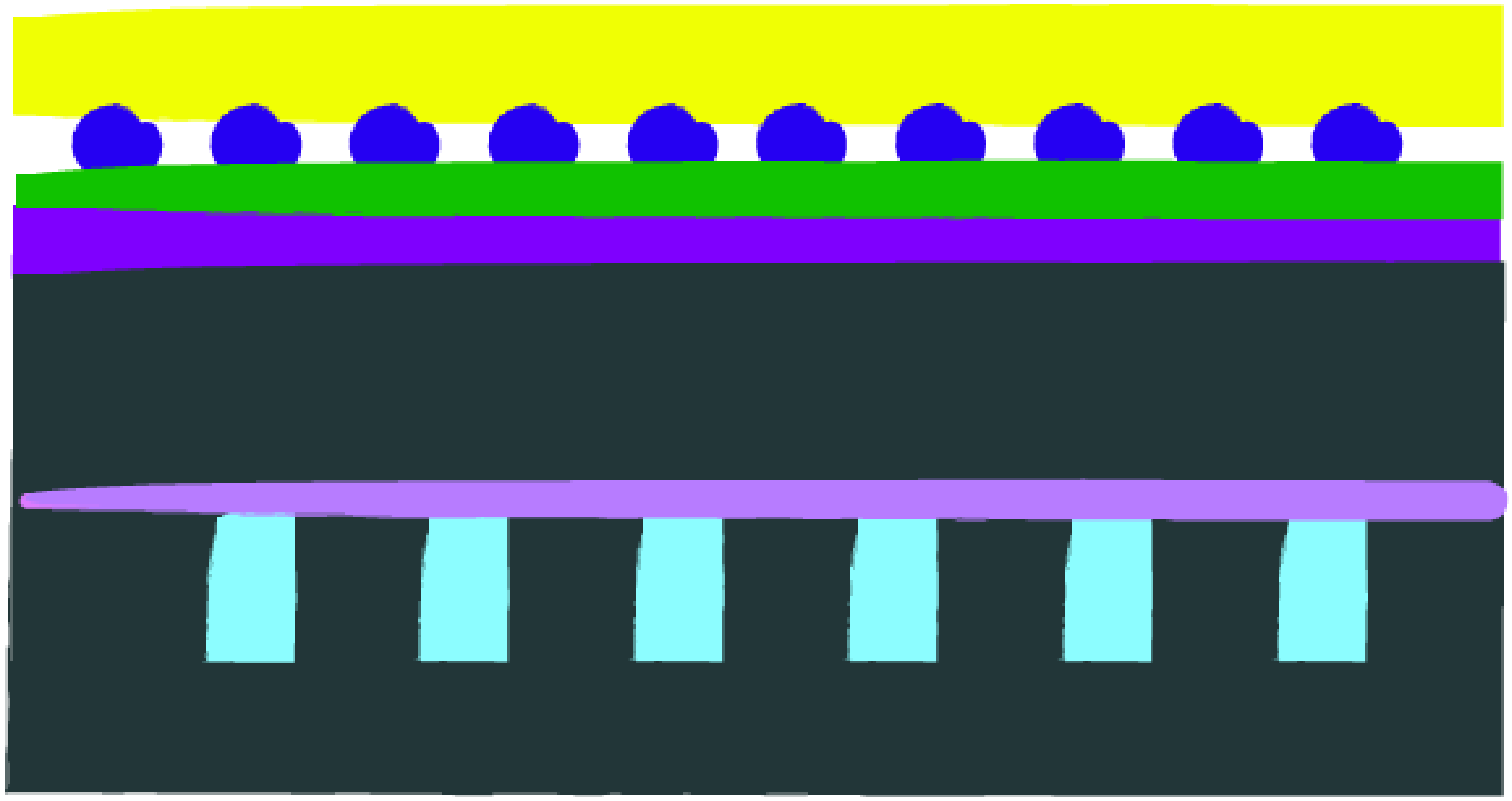
Integrating MCC in active silicon

Integrated cooling channels in position-sensitive silicon detectors,
JINST 11 (2016) no. 06, P06018

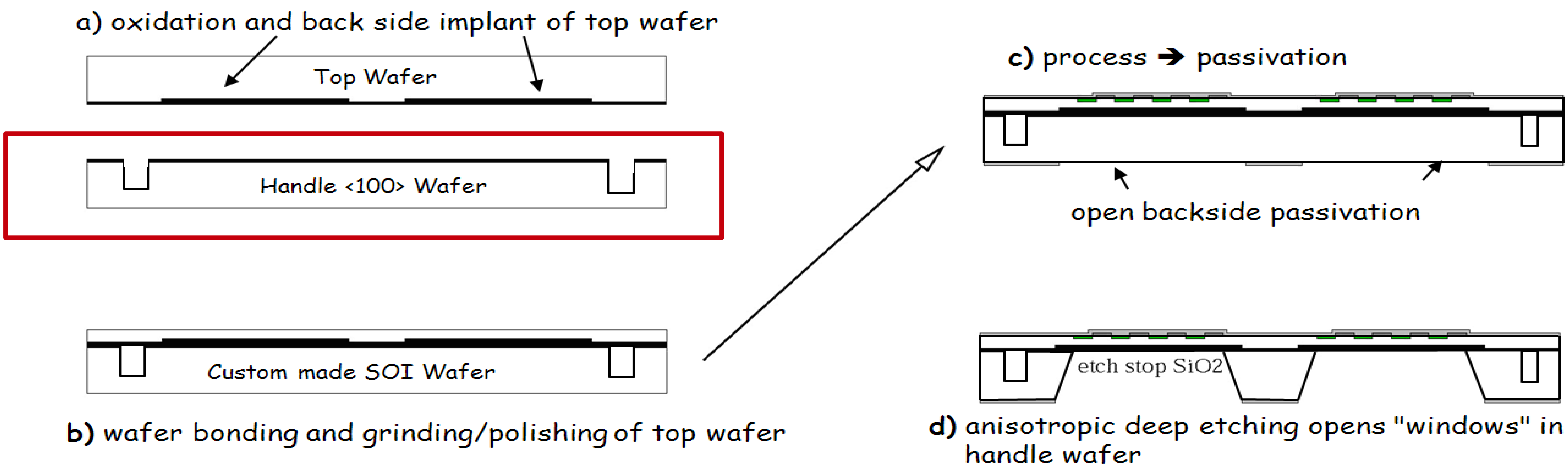
L. Andricek[1], M. Boronat[3], J. Dingfelder[2], J. Fuster[3], I. Garcia[3], P. Gomis[3], C. Lacasta[3], G. Liemann[1], C. Marinas[2], D. Markus[2], J. Ninkovic[1], M. Perelló[3], E. Scheugenpflug[1], M.A. Villarejo[3], M. Vos[3]
[1]MPG Halbleiterlabor Munich, [2]Bonn University, [3]IFIC Valencia

Go one step further: circulate the liquid in the sensor!!

Cartoon by A. Mapelli



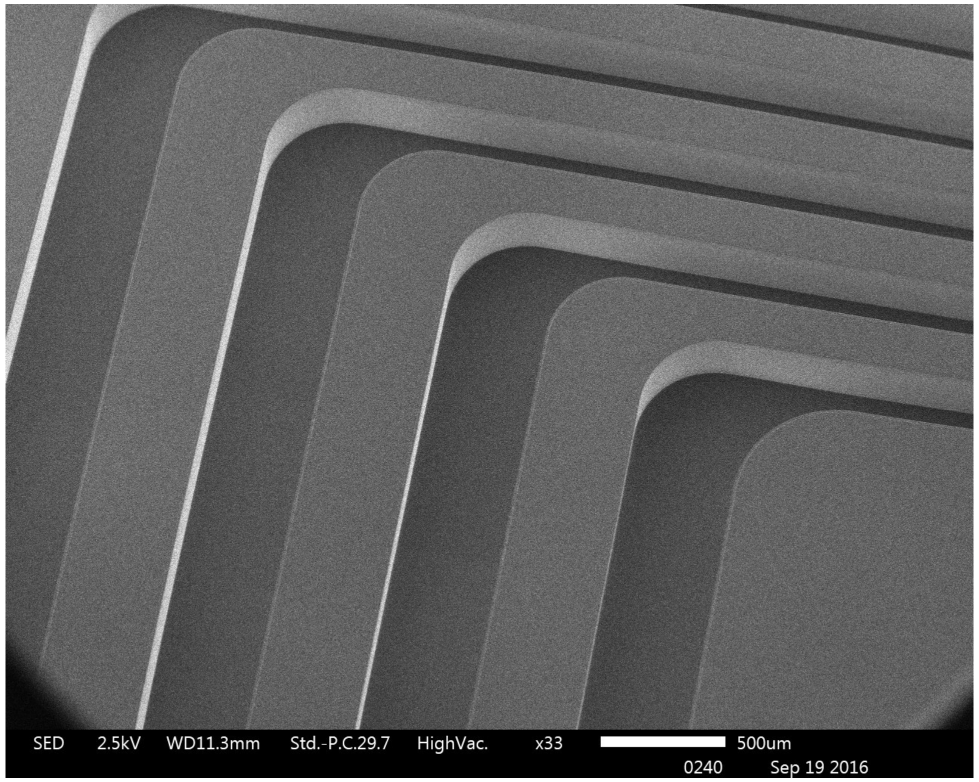
All-silicon ladder with integrated cooling

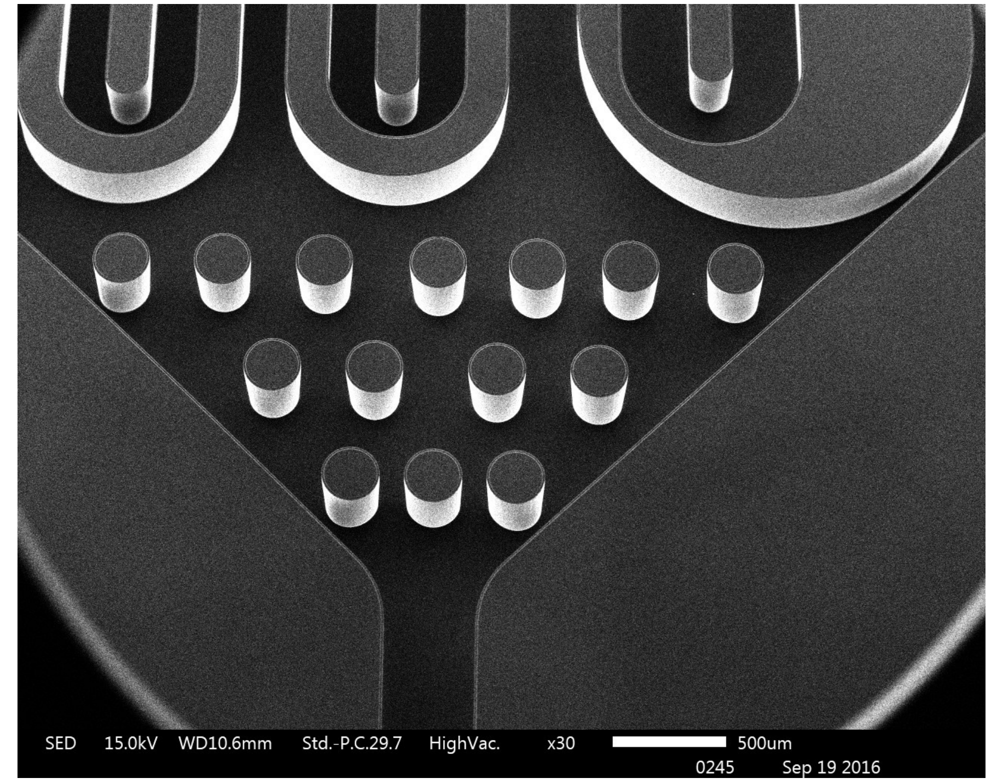


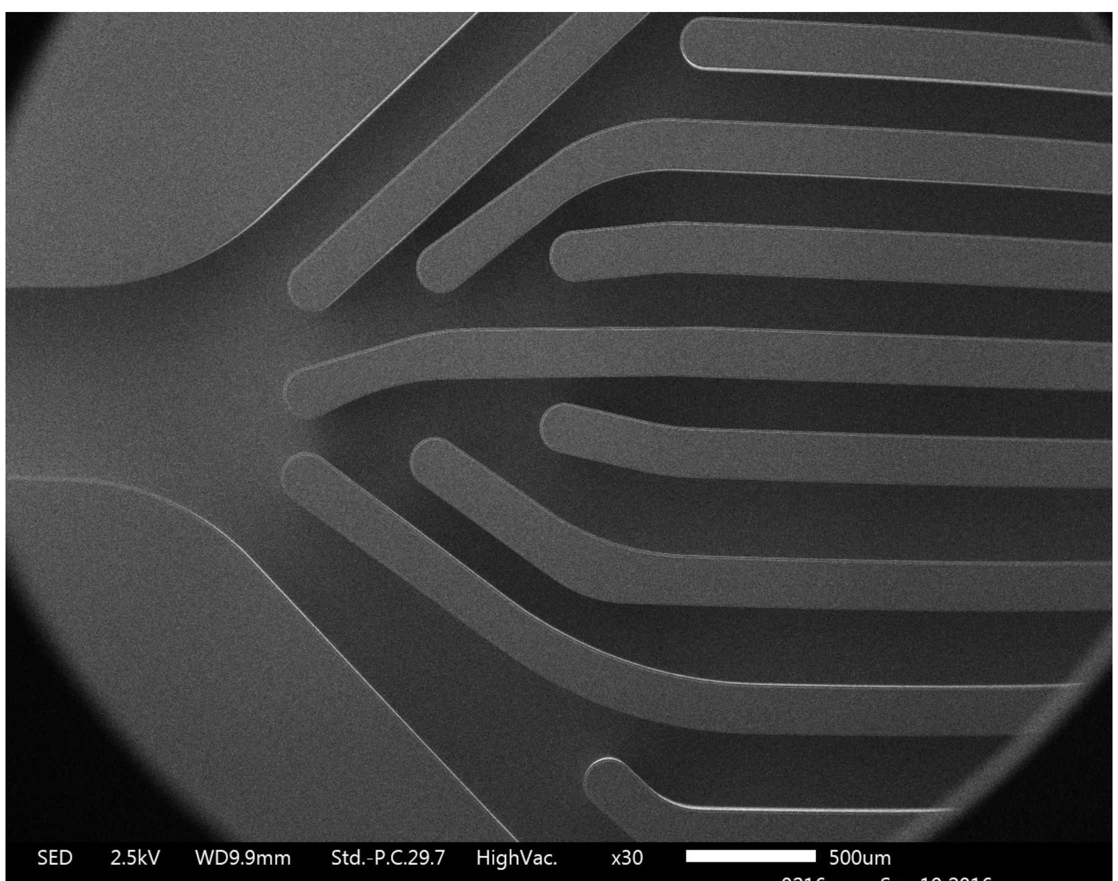
thinned all-silicon module with integrated cooling channels

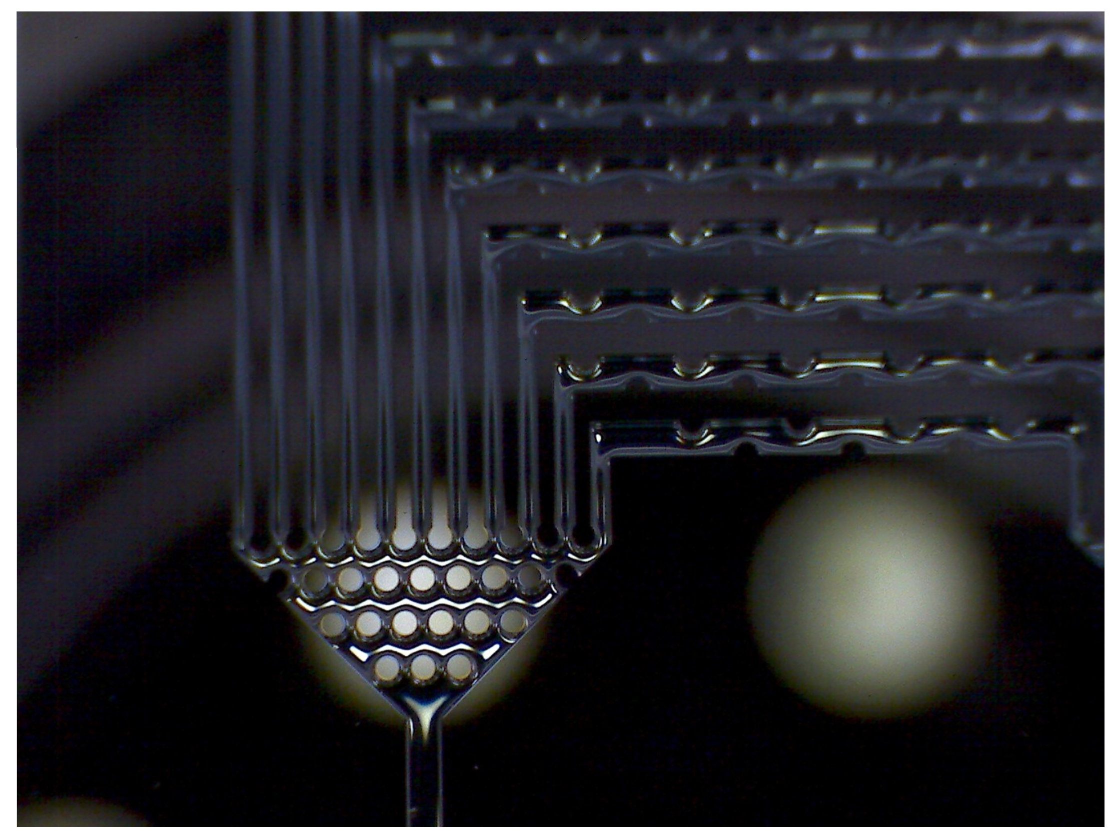
:- integrate channels into handle wafer beneath the ASICs
:- channels etched before wafer bonding → cavity SOI (C-SOI)
:- full processing on C-SOI, thinning of sensitive area
:- micro-channels accessible only after cutting (laser)

Micro-channel manifolds

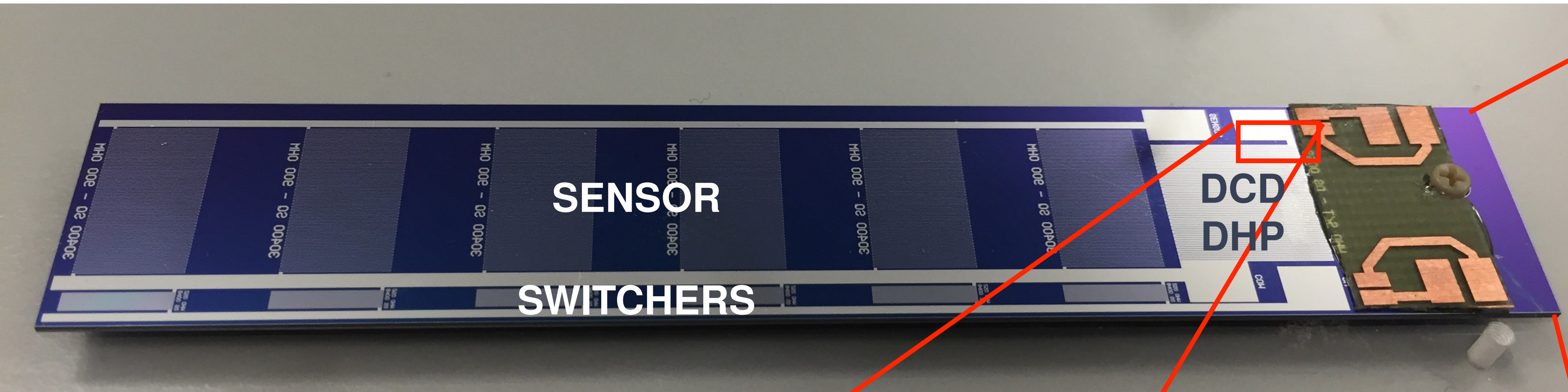


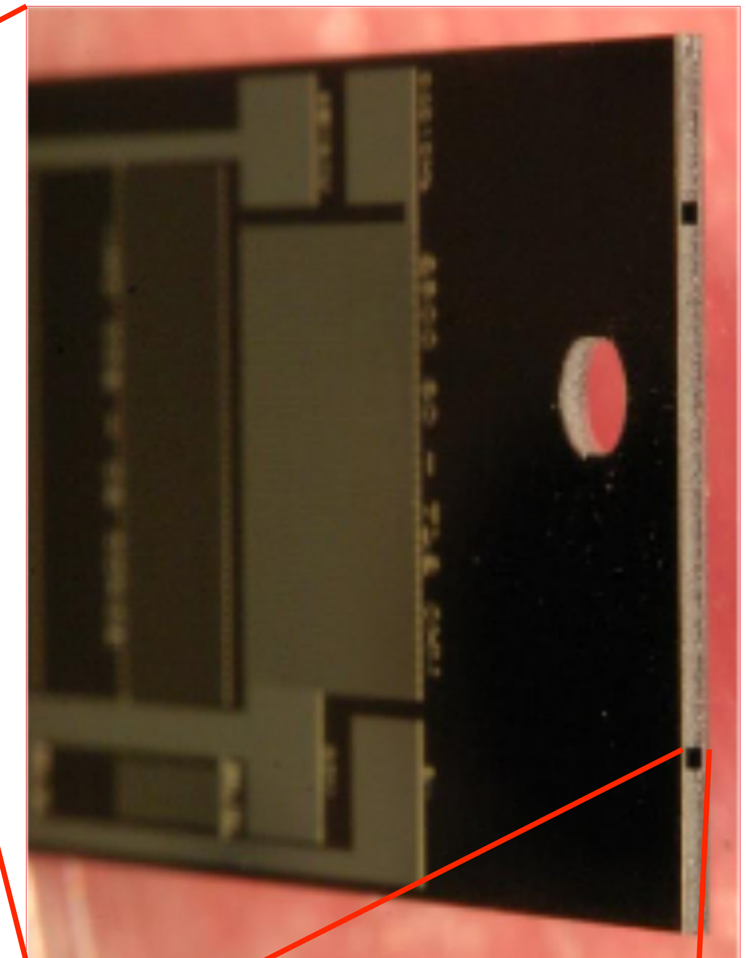






All-silicon ladder with integrated cooling

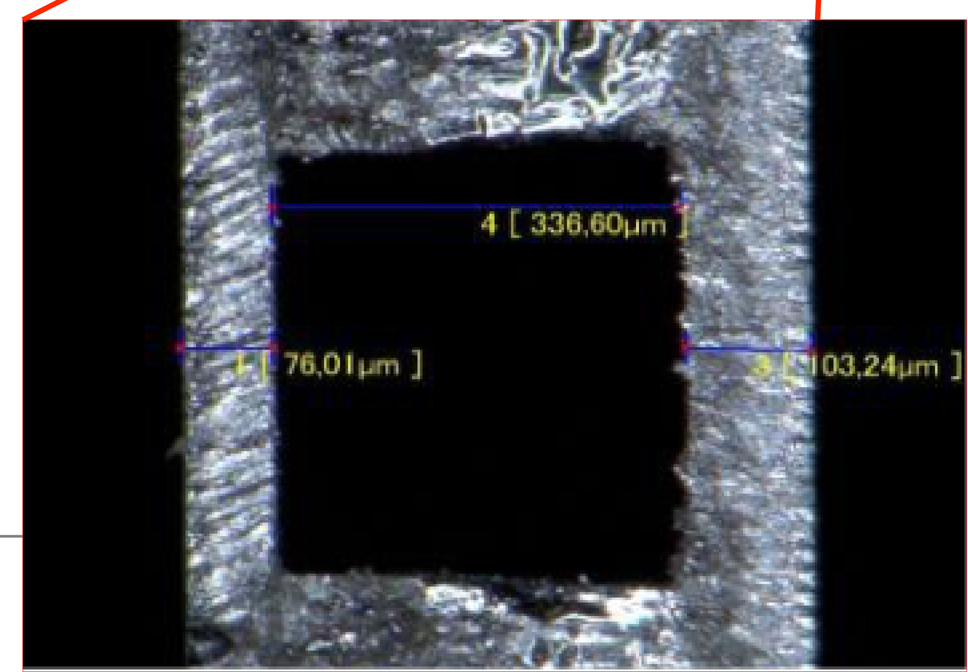




Resistor circuits to mimic DEPFET power dissipation

Thermo-mechanical DEPFET half-ladder

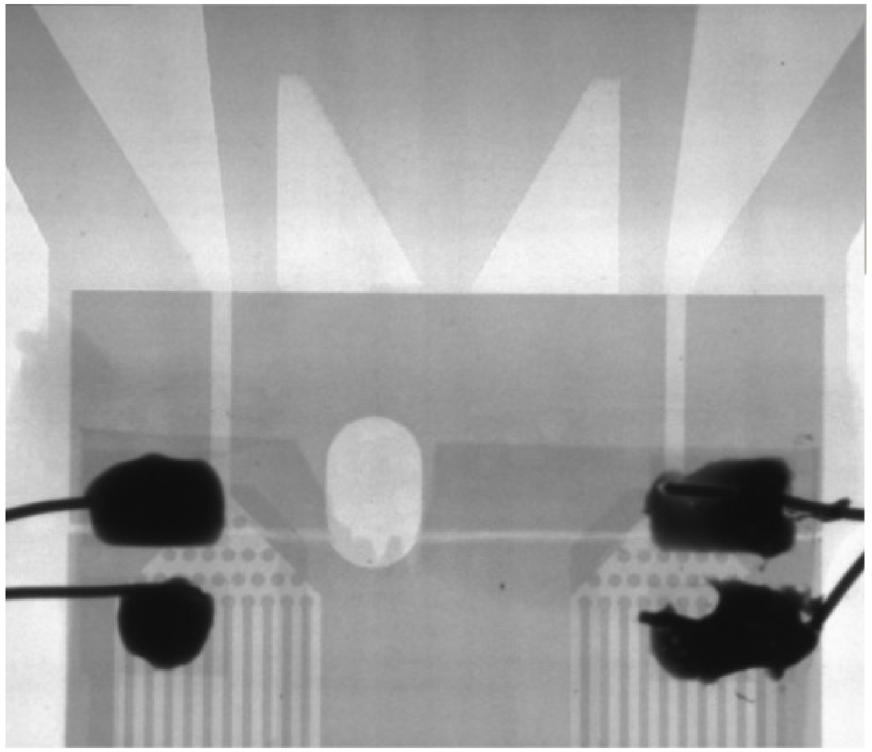
Inlet and outlet visible after wafer cutting



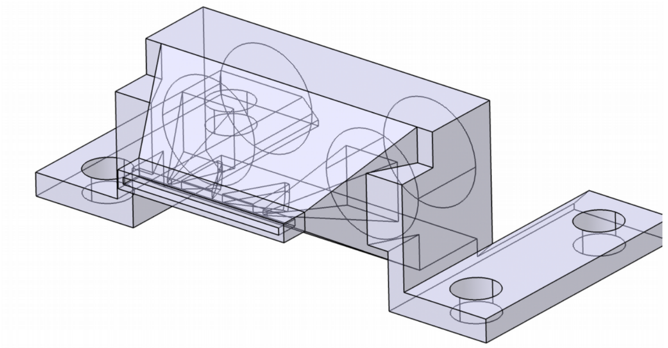
Low-mass in-plane connectors

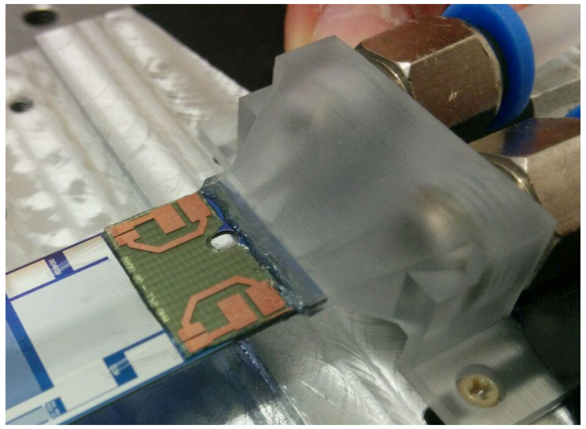
Low-Z 3D-printed connectors

Arbitrary complexity, 30 μm tolerance
→ self-aligned with silicon channels
Very rapid prototyping, very cheap
Pressure-tested to >100 bars

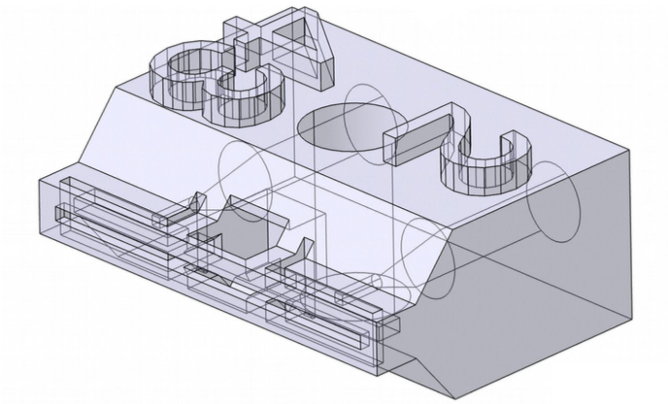


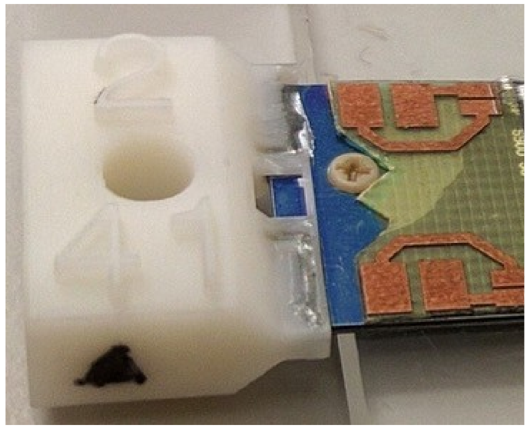
First attempt (0.81% X/X_0)
standard Swagelok fittings



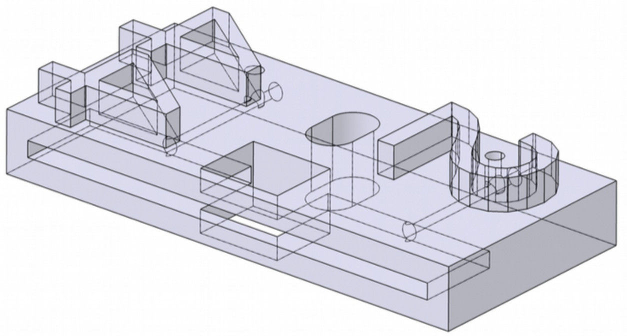


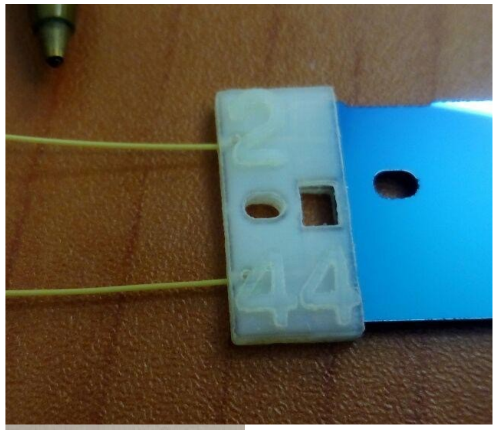
Past (0.21% X/X_0)
Smaller fittings





Present (0.05% X/X_0)
Glued PEEK tubes



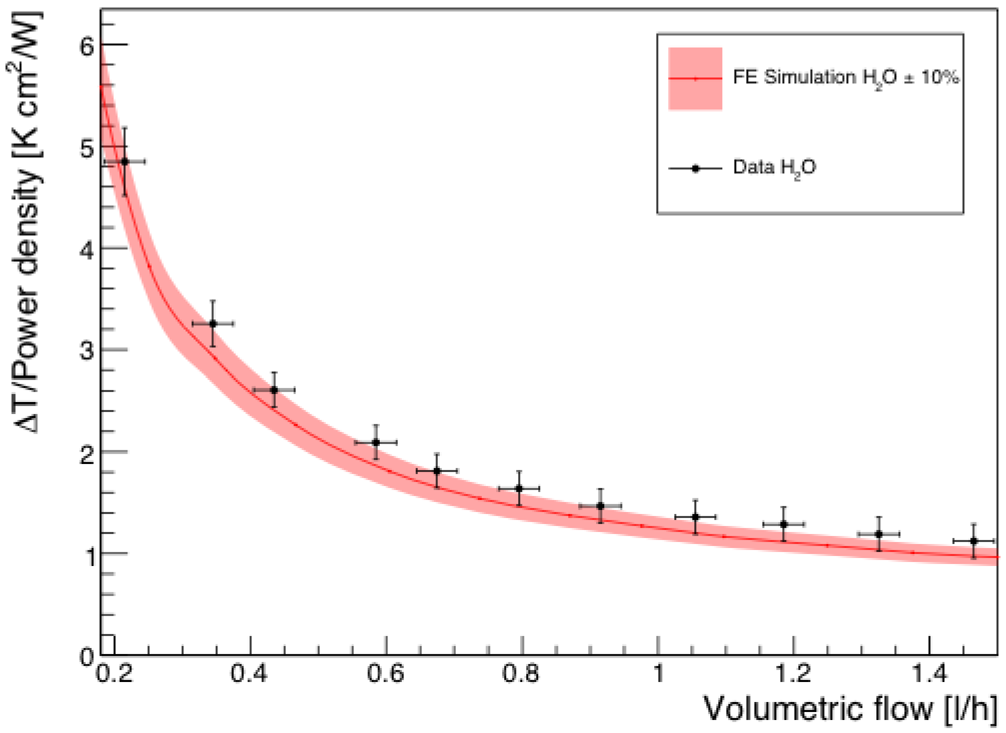


Future

?

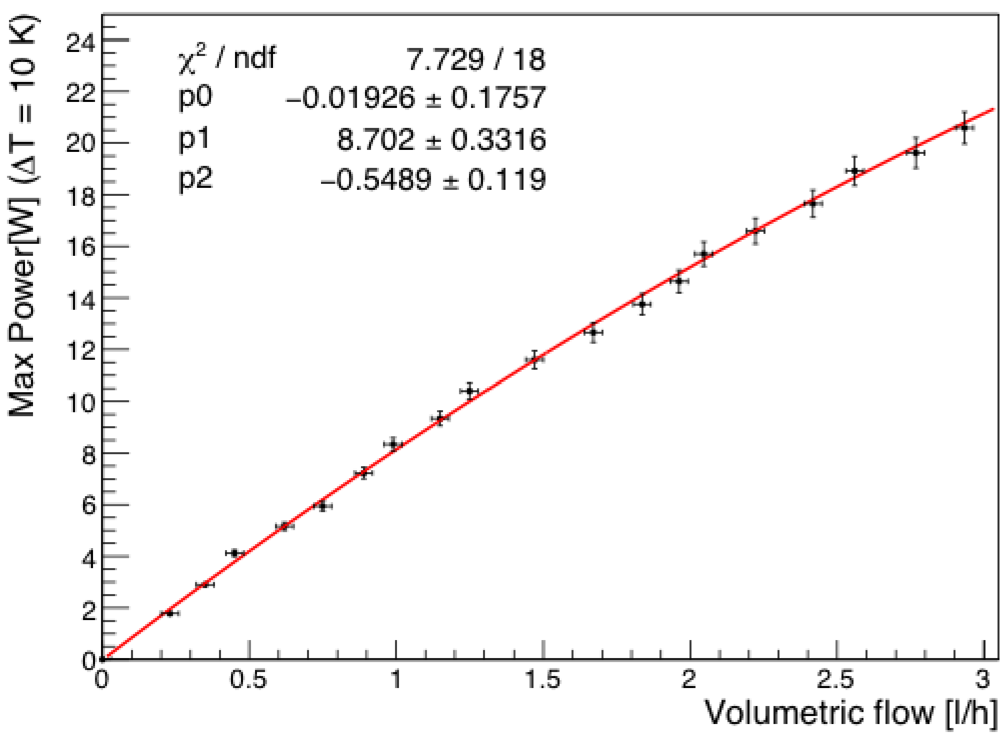
Integrated manifold
and support structures

A low-pressure mono-phase cooling solution

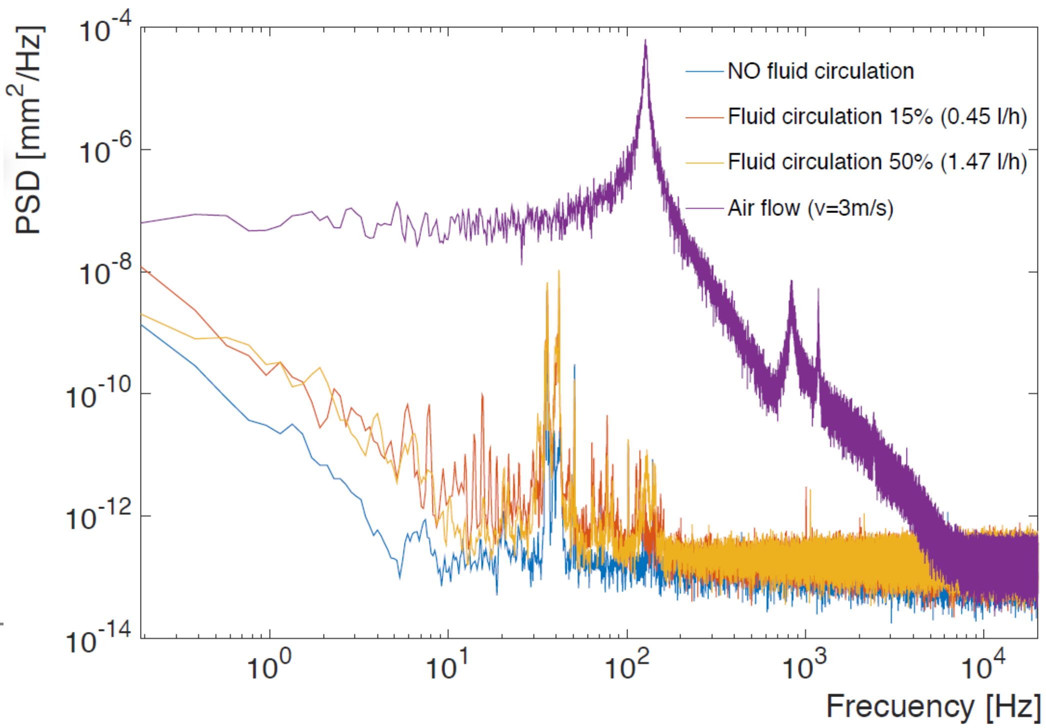


Good agreement with **FE simulation** (<10%)

Thermal figure of merit ~ 1
(way beyond classical solutions)

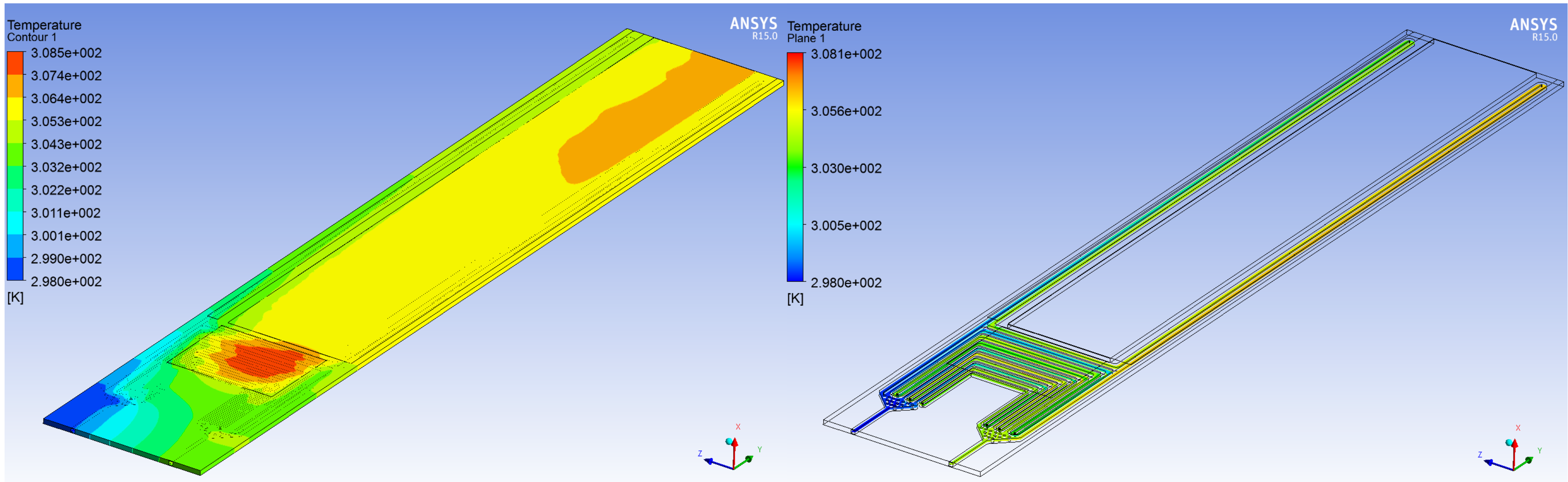


- Up to 25 W/cm² with flow rate of 3 l/h
- Low-pressure mono-phase: 0.2 - 1.5 bar



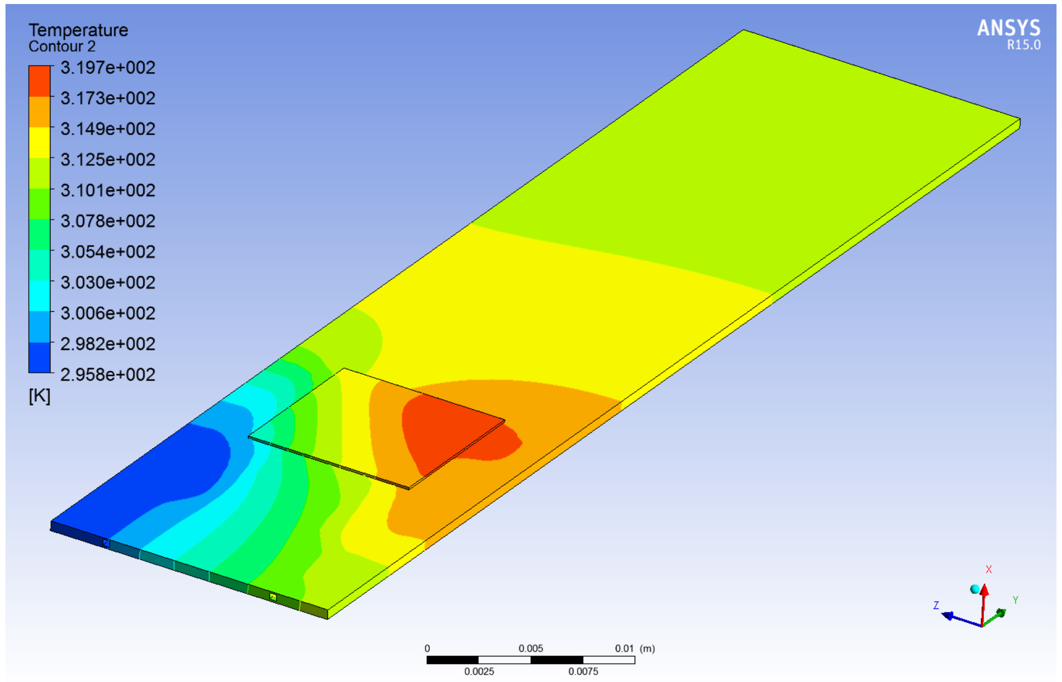
- No impact on mechanical stability

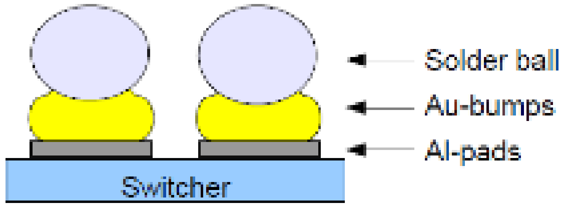
Next generation in FE simulations



Full-ladder MCC

Run a single channel around the sensor:
ΔT~5 K (nominal load)





Thermal barrier formed by bump bonds

300 μm Si ASICS + 100 μm Bump-bonds
thermal resistivity of 6 W/m·K
Figure of merit increases by 5 K cm^2 / W

C.Mariñas PhD thesis link

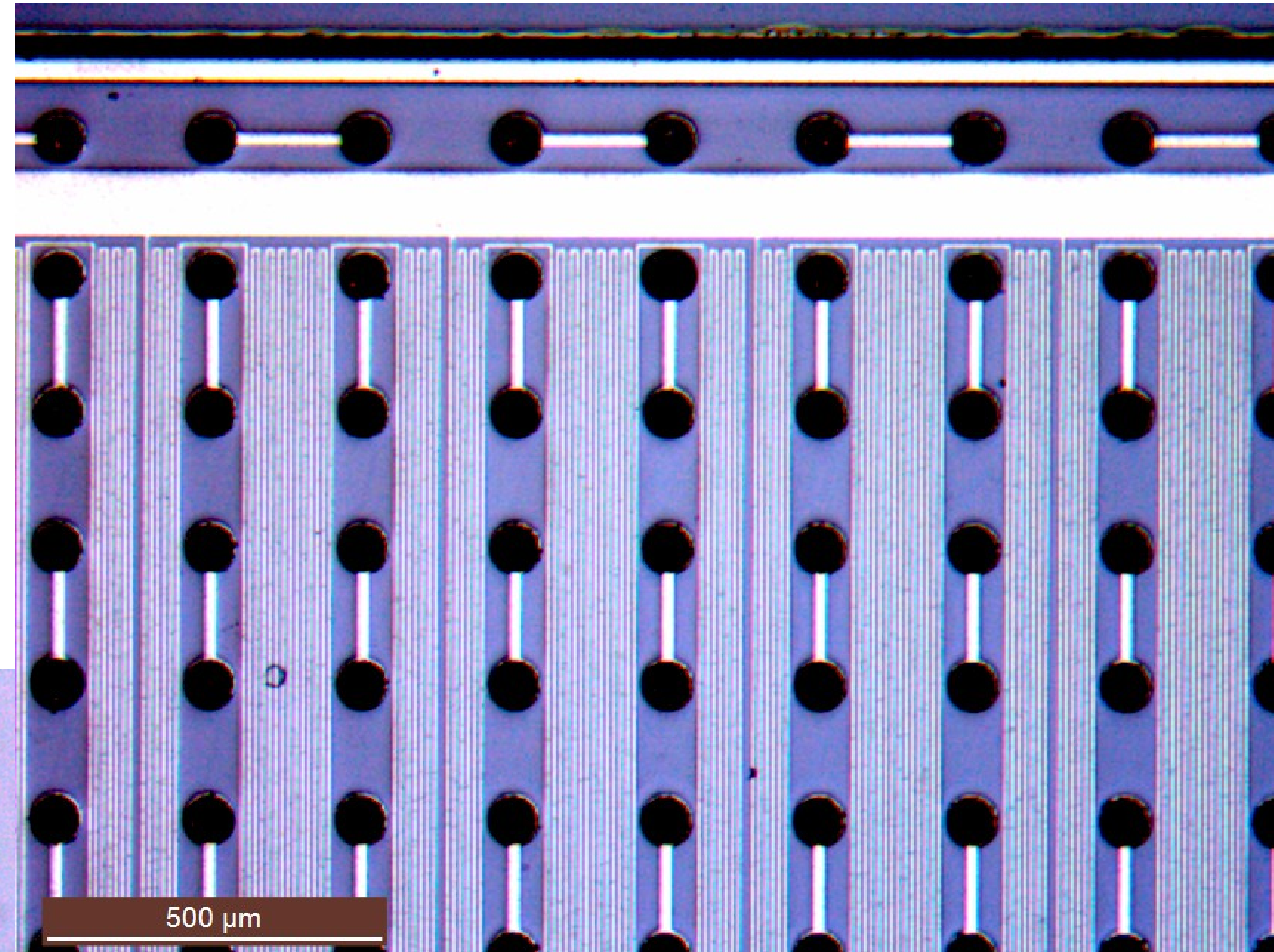
New production has all these structures

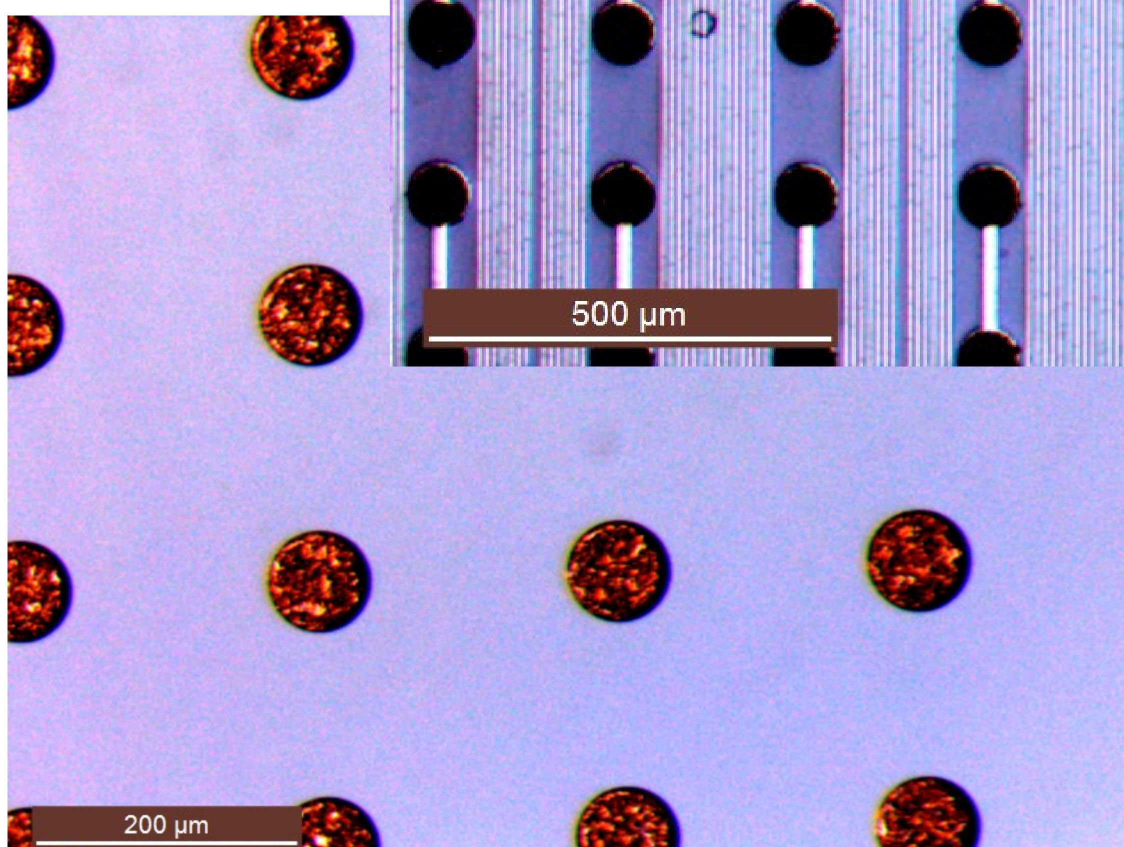
Dummy chips

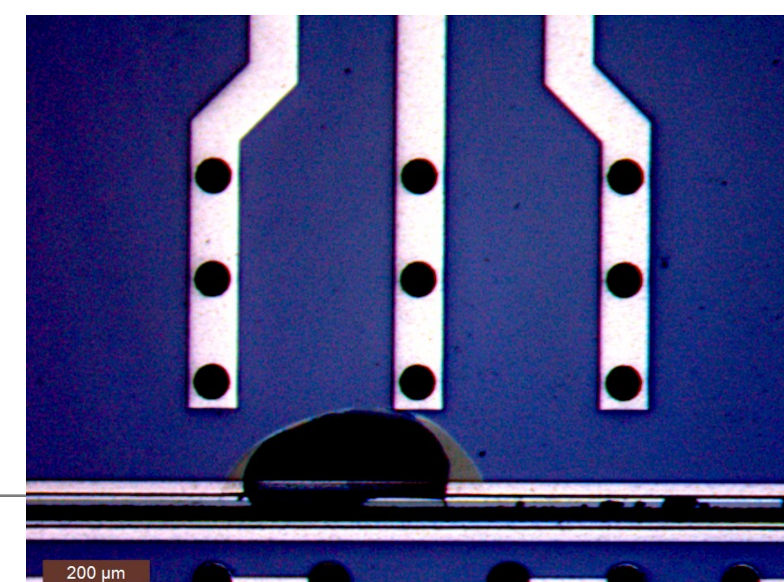
The “chips” are simple Si pieces
Dimensions: 1 cm x 1 cm 500 μm

The chips are equipped with Indium solder balls, distributed in a 200 x 200 μm² grid

A resistor “heater” circuit covers the area of the chip, which allows to dissipate heat



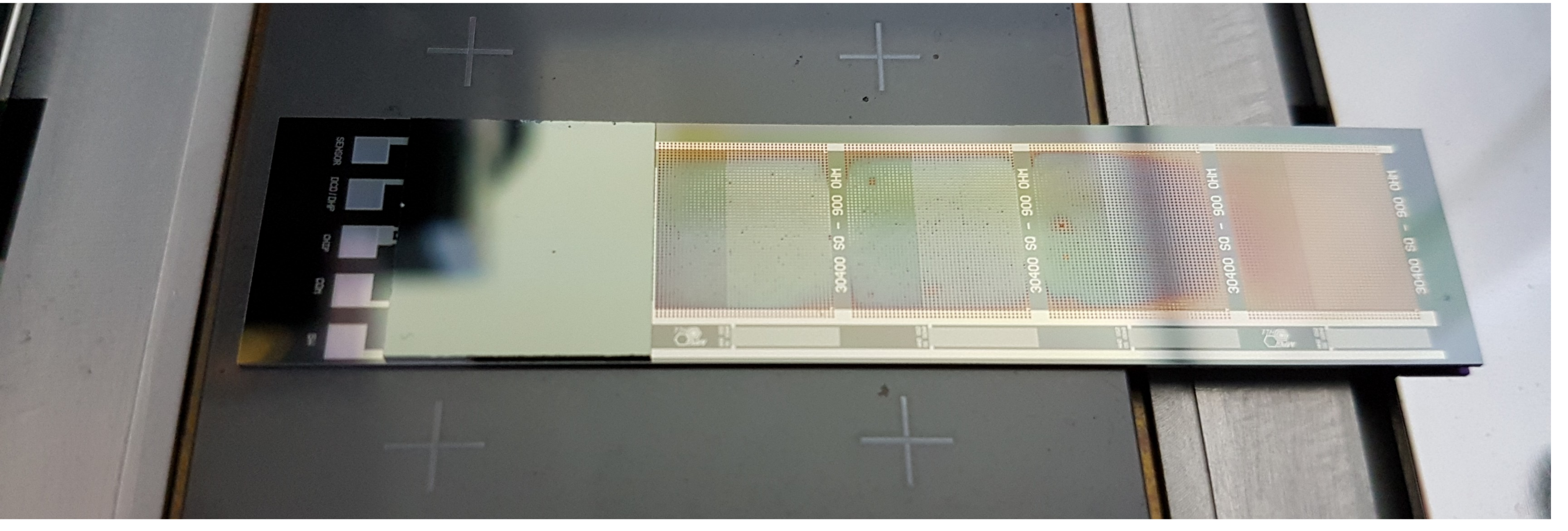




New structures

AIDA2020 production: three wafers with 3x2 “sensors” each

First “sensor” sample bump-bonded to “chip” at NTC-UPV



Conclusions

All-silicon ladder offers versatile, integrated solution

→ not limited to DEPFET technology, any traditional sensor (+ CMOS?)

MCC embedded in silicon cooling plates succesfully demonstrated in HEP

→ NA62 (2014) + LHCb VELO upgrade (~2020)

MCC can be integrated in the active silicon!!

→ process demonstrated (*JINST 11 (2016) no. 06, P06018*)

→ low-power, low-material solution looks promising for CLIC

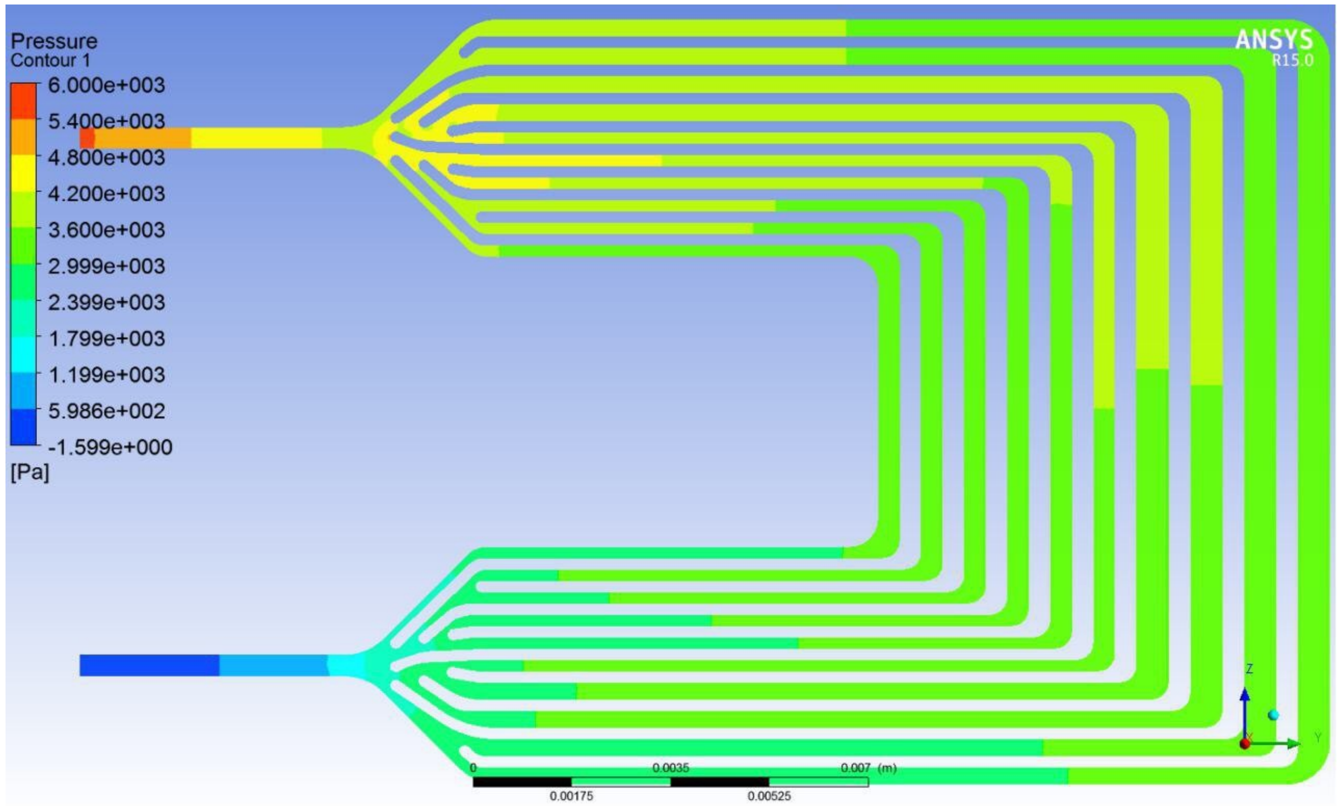
2018 forum on tracker mechanics

The 2018 edition of the yearly forum on tracker mechanics will take place in Valencia, end of June.

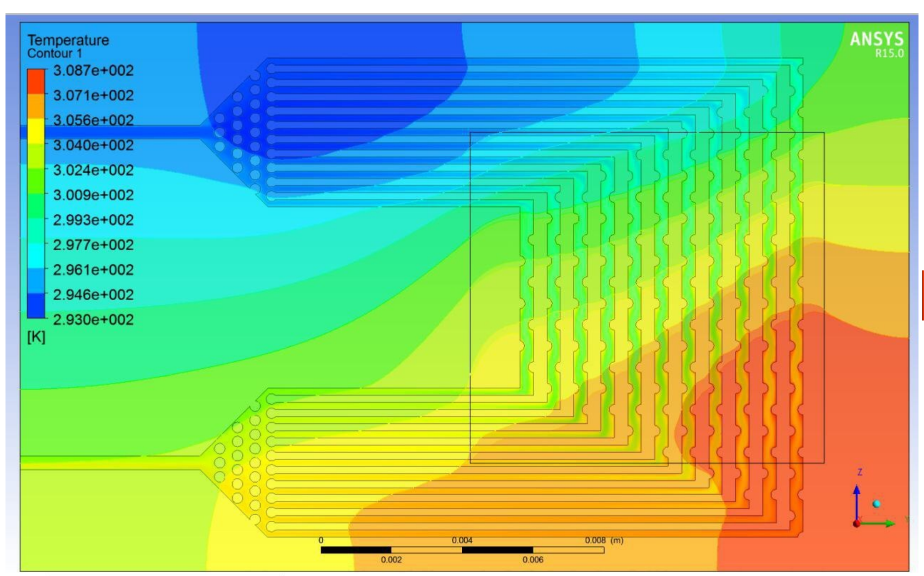
We hope to see many of you there!

Thank you for your attention

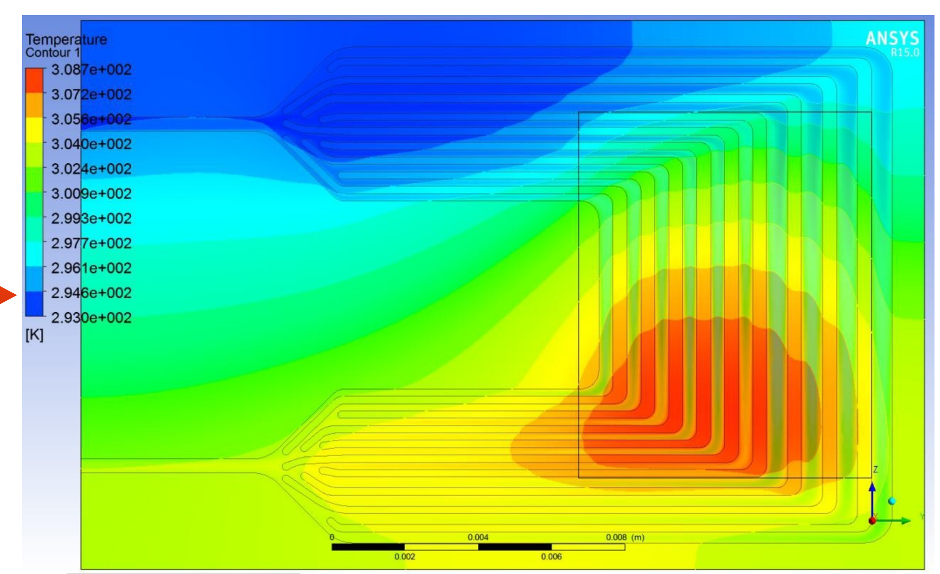
Optimized MCC geometry



- More homogenous flow
- Reduce pressure gradients
- Minimize and confine the heat spread



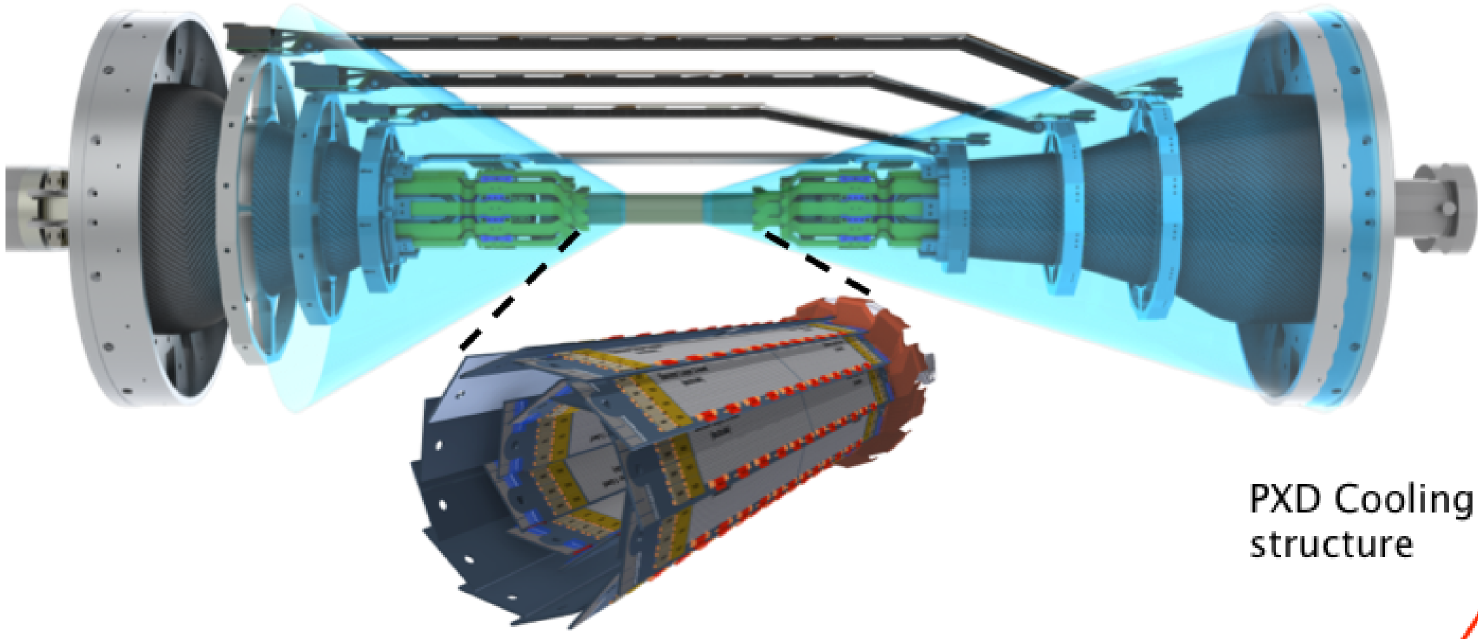
Recent geometry

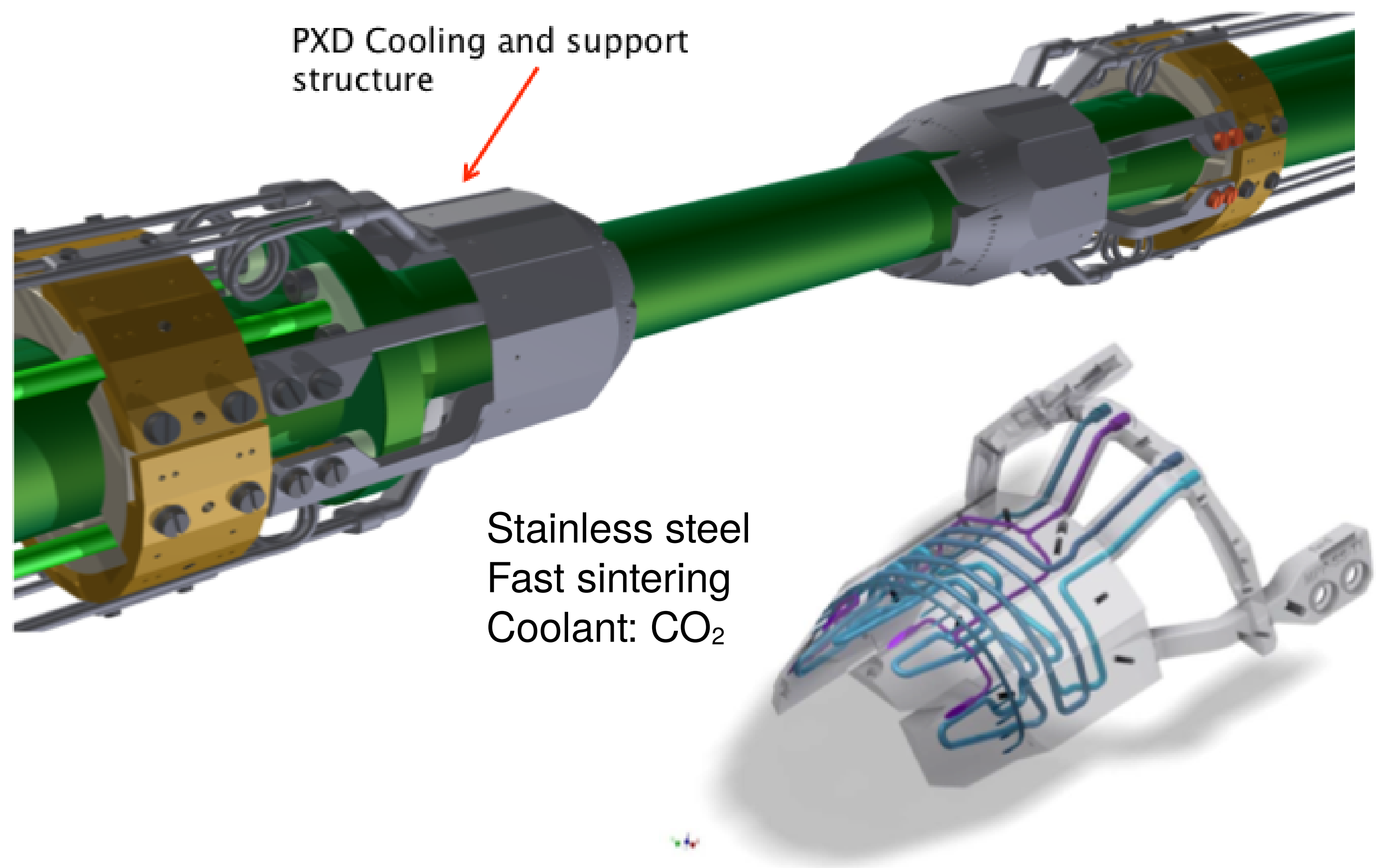


Optimized geometry

Cooling strategies

Belle II





Massive structures outside the acceptance to cool down the readout chips