A MONOLITHIC CHIP FOR THE CLIC SILICON TRACKER

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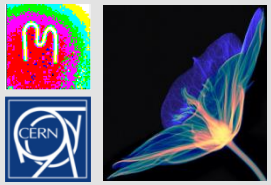


Outline

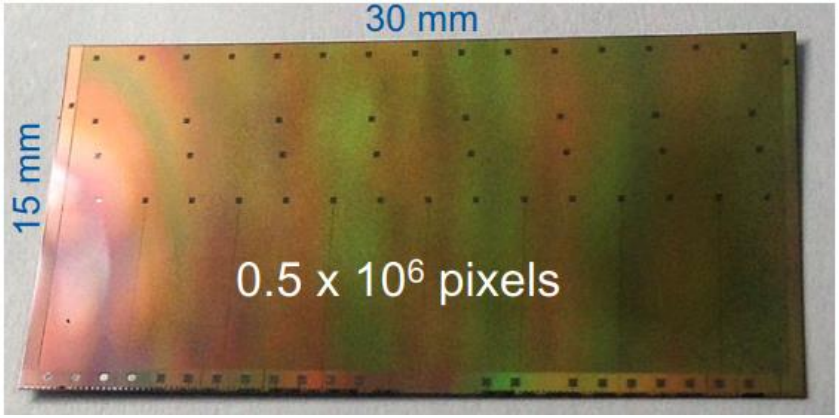
- Requirements
- The ALPIDE chip
- The sensor
- Analog front-end
- Digital strip, chip architecture and periphery
- Summary and conclusions

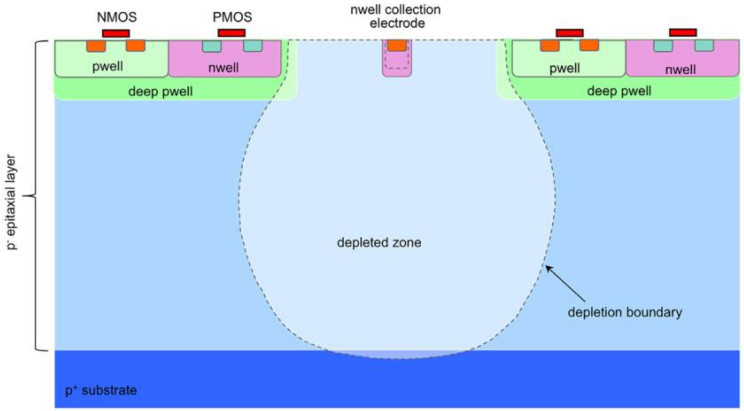
Requirements for a chip for the CLIC silicon tracker [1]

- Channel dimensions:
  - Single point resolution in one dimension ≤7 μm (transverse plane)
  - Length of short strip/long pixel: 1mm -10mm (1mm fulfils the requirements for the different barrels)
- Energy measurement (For time walk correction and improving spatial resolution)
  - 5-bit resolution
- Time measurement:
  - 10ns bin, 8-bits
  - No multi-hit capability
- Material budget 1-1.5% X_0 (i.e. ~200μm for silicon detector and readout)
- Power consumption below 150mW/cm^2 (Power pulsing, duty cycle ~500ns/20ms (25×10^{-6}))
- Radiation hardness (NIEL< 10^{10} neq/cm^2/yr, TID < 1 Gy/yr)
- Monolithic sensor in Tower Jazz 180nm CMOS imaging process (Expertise in design due to ALPIDE effort)

[1] D. Dannheim, A. Nürnberg: Requirements for the CLIC tracker readout (CLICdp-Note-2017-002)

ALPIDE CHIP





- ALPIDE chip: ALICE Inner Tracking System Upgrade
- Size 15mmx30mm, 512x1024 pixels
- Pixel size 29.24x26.88 μm^2
- Pixel includes sensing diode, front-end, shaper, discriminator, digital section (ENC ~4e^-, C_D=2.5fF, τ_p=2μs)
- Total pixel consumption ~300nW (~150mW/chip or 35mW/cm^2)

- Tiny collection electrode, deep P-WELL (Full CMOS), 30μm epitaxial layer (High resistivity wafers (>1kΩcm)

- Extensive tests before and after irradiation done to characterize the technology

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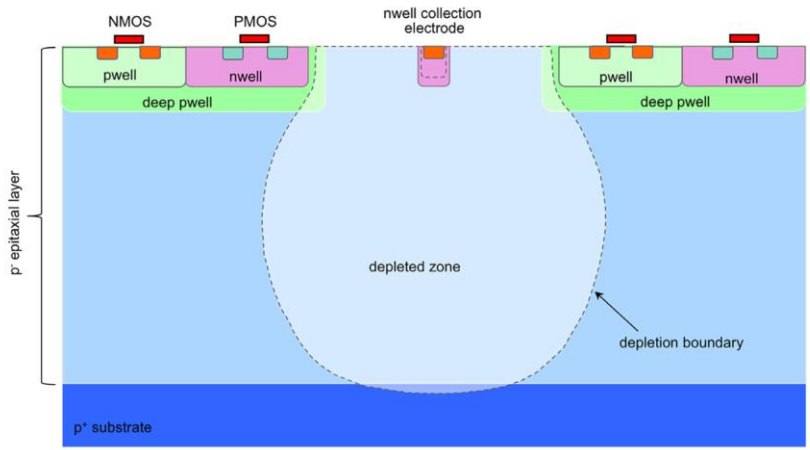
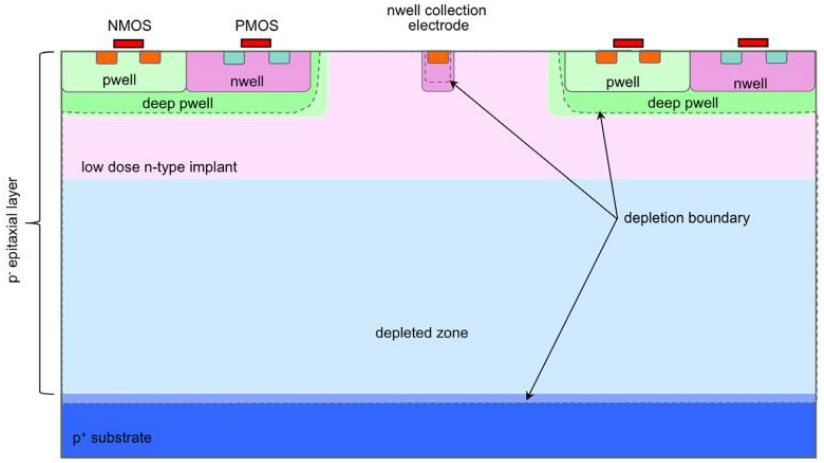
The sensor



ALPIDE CHIP PROCESS

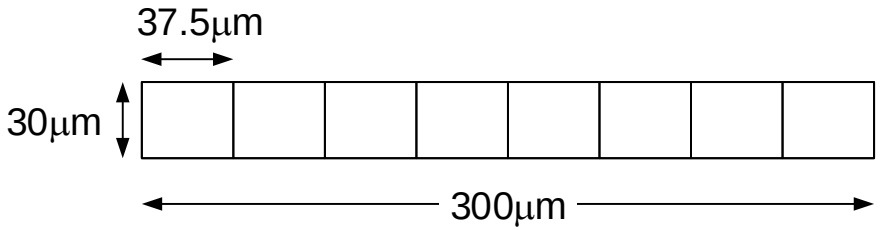


MODIFIED PROCESS

- Tower Jazz HR CMOS 180nm (2 versions of the process: Original/modified)
- Original:
  - Does not allow full depletion of the sensitive layer
  - Charge collection by diffusion and drift
- Modified process
  - N-type implant to fully deplete the epitaxial layer
- Choice for CLICTD. Advantages: low sensor capacitance, improved timing and improved radiation hardness
- MIP Signal in thin Si layer ~50$e^-/h^+/\mu m$, 30μm depleted region i.e. 1500e-

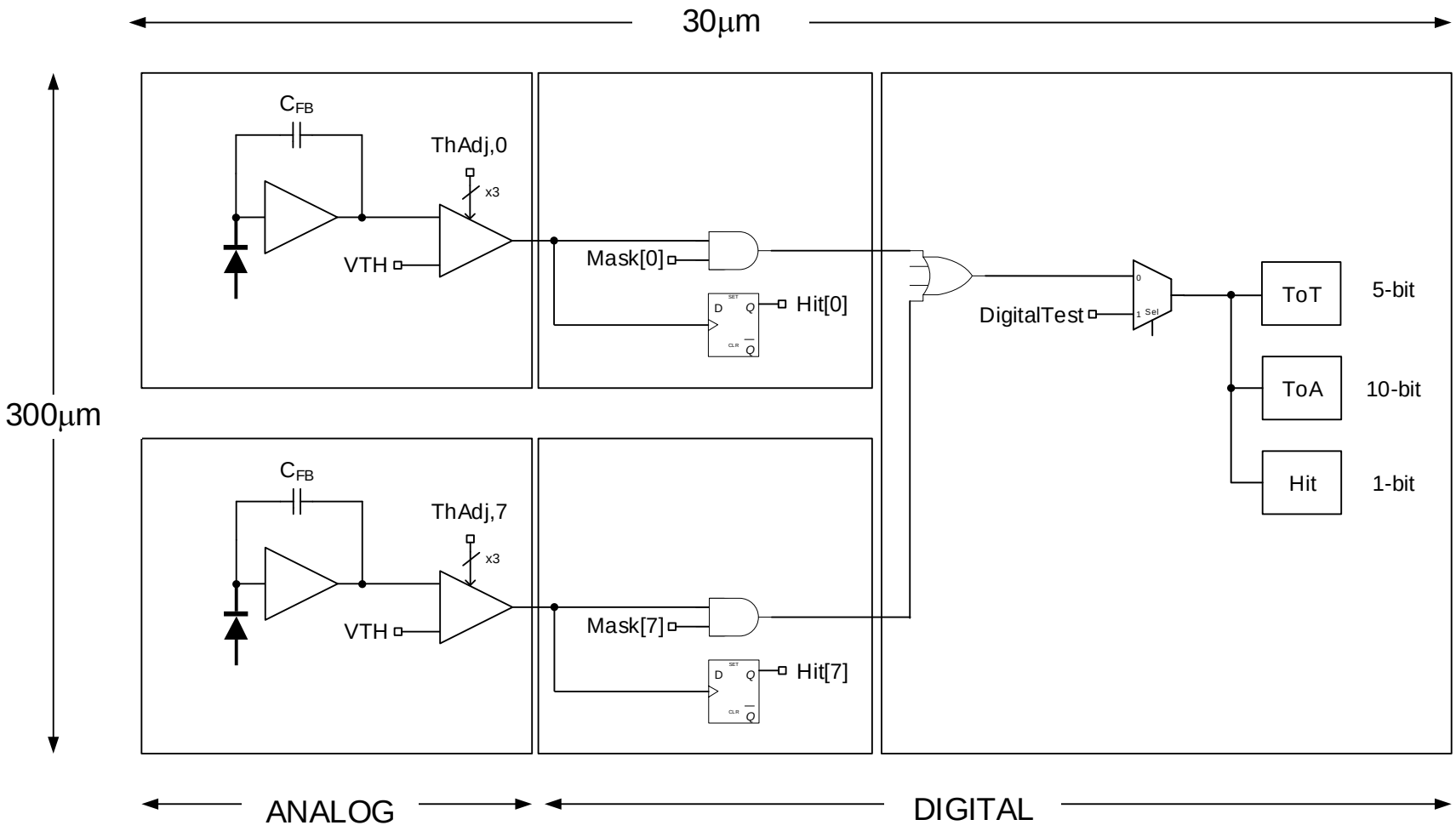
W. Snoeys et al. Nuclear Inst. and Methods in Physics Research, A 871 (2017) 90–96

The detector channel



- The detector unit cell consists of a strip of 30μm x 300μm
- It is segmented in 8 pixels
  - To ensure prompt charge collection in the diodes
- Measurement
  - Pixel hit within strip (8 bits)
  - Time of arrival of the signal at the strip (10ns bin, 8 bits) (first hit)
  - Energy deposit (Time over Threshold), 5 bits (pixel with largest deposition)
- Considered other architectures (e.g. analog summing but penalty in minimum threshold)

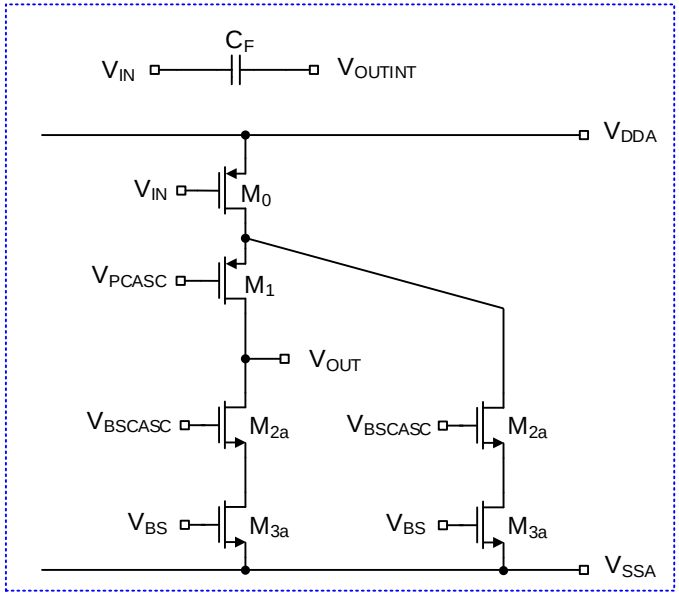
The readout channel



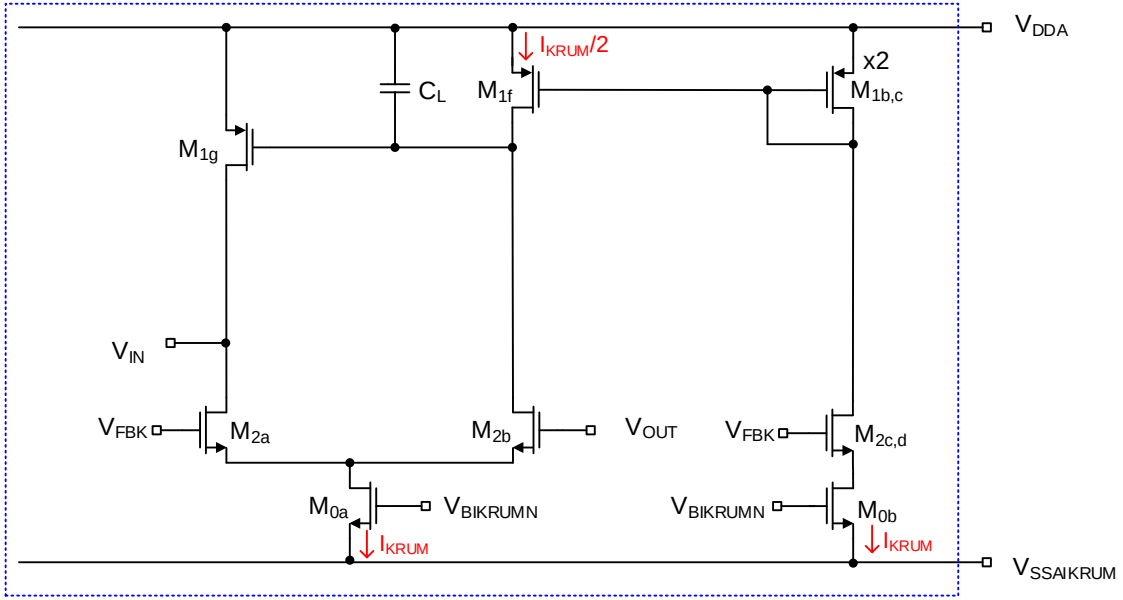
Individual pixel hit information, possibility to mask pixels

Charge sensitive amplifier

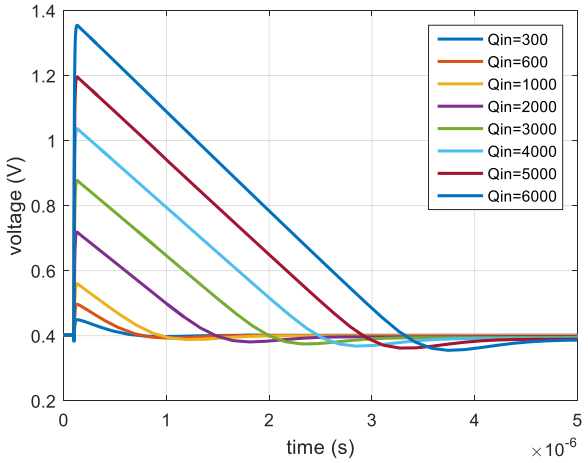
CSA

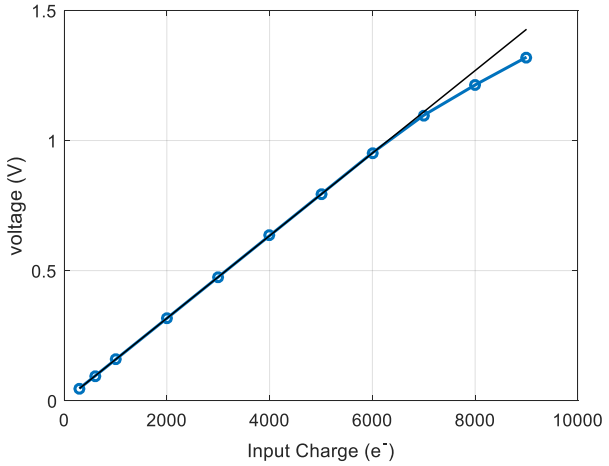


FEEDBACK



Charge sensitive amplifier



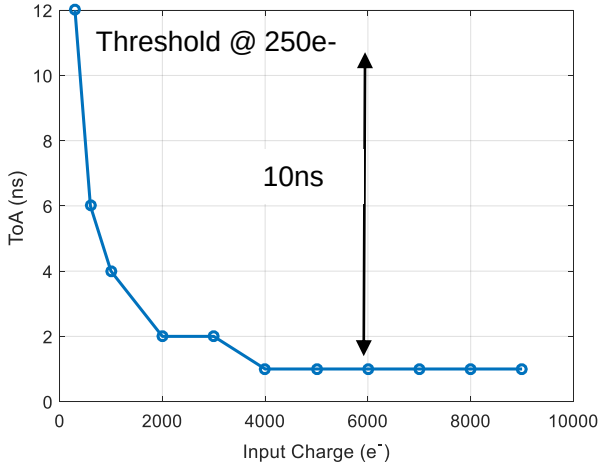


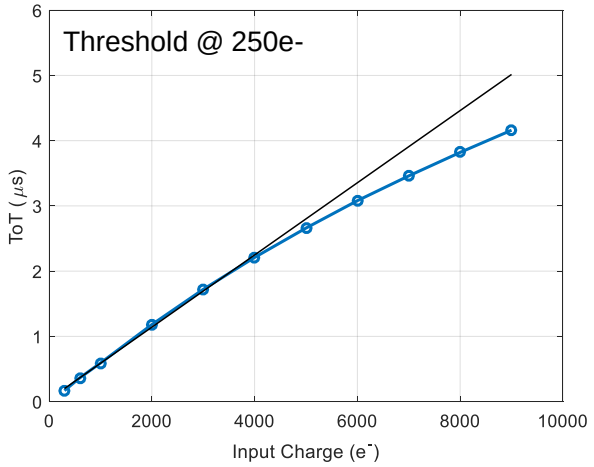
C_F=1fF (min value limited by the architecture)
C_D=2fF (detector and interconnections)

I_{PREAMP}=150nA (10mW/cm^2 (preamp only/30um pixels))

Gain=160mV/ke$^-$

Noise=35e$^-$ r.m.s





Unequalized threshold=70e$^-$ r.m.s.

Equalized (3bits)=15e$^-$ r.m.s.

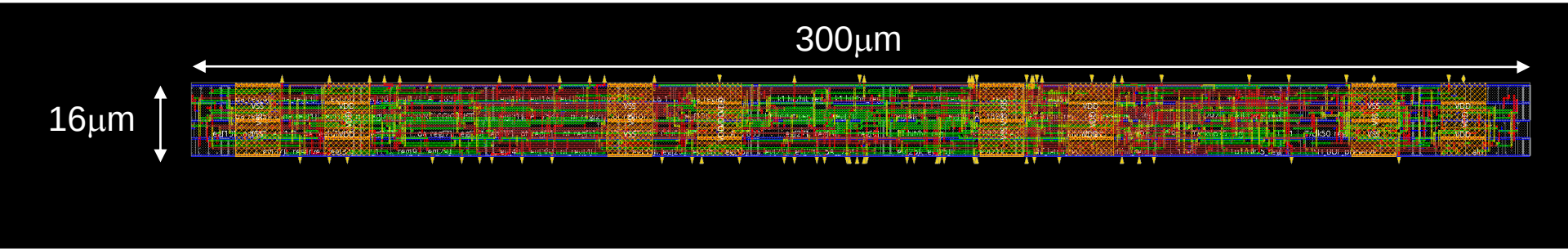
Minimum detectable charge=230e$^-$

Slope=16MV/s
(Jitter=noise/slope~0.4ns (@1ke$^-$))

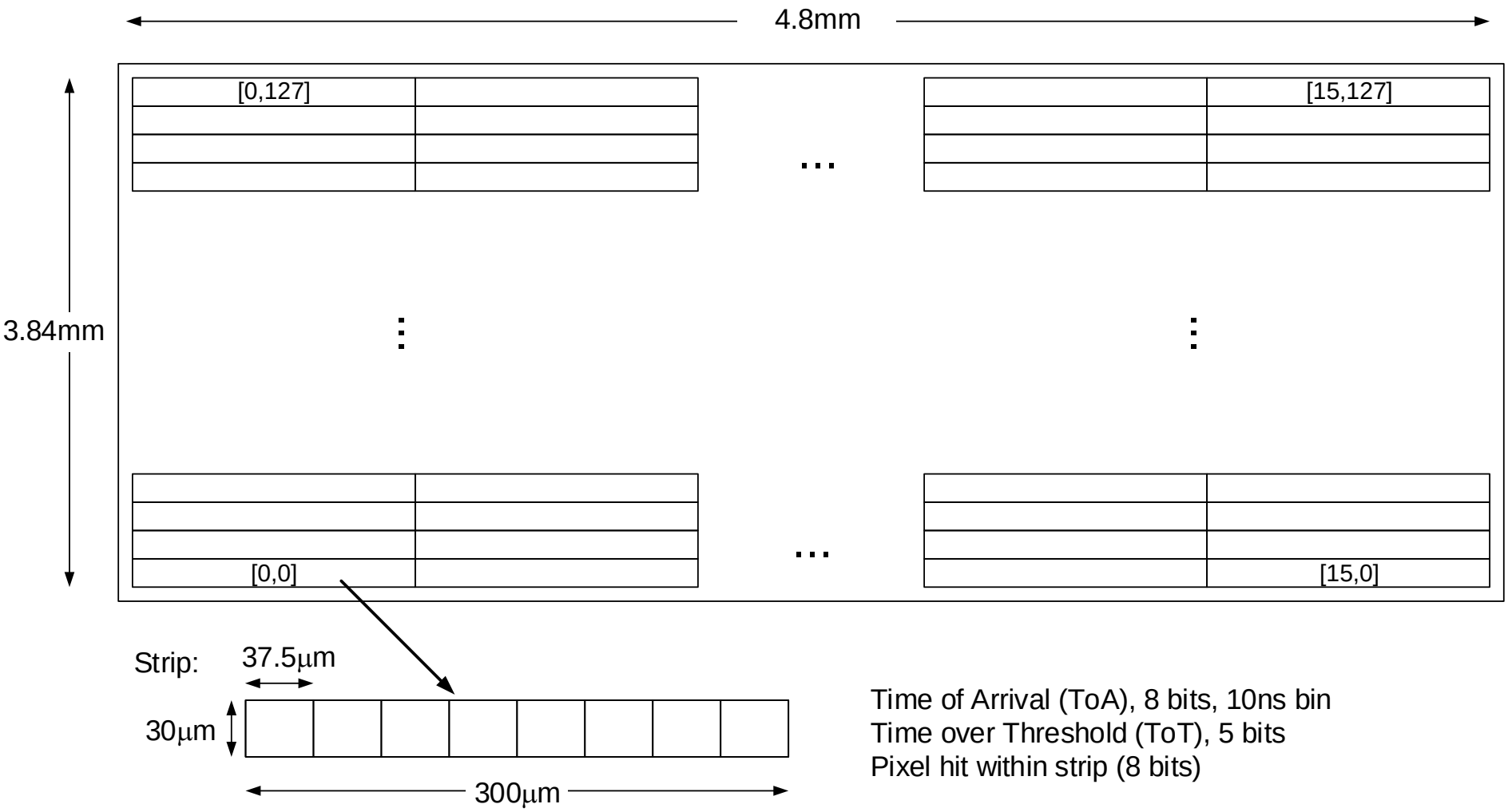
Comparator under study

Strip working modes

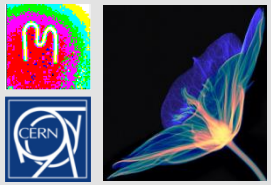
- Configuration
- Acquisition
  - 8 bits ToA, 5 bits ToT, individual hit information (8 bits)
    - ToT clock is generated by dividing the ToA clock (/2, /4, /8, /16 i.e. 50MHz, 25MHz, 12.5MHz or 6.25MHz)
  - 13 bits ToA, individual hit information (8 bits)
  - 13 bits hit counting (mainly for threshold equalization purposes)
- Readout
  - Zero compression is available



Chip sensitive area



Time of Arrival (ToA), 8 bits, 10ns bin
Time over Threshold (ToT), 5 bits
Pixel hit within strip (8 bits)



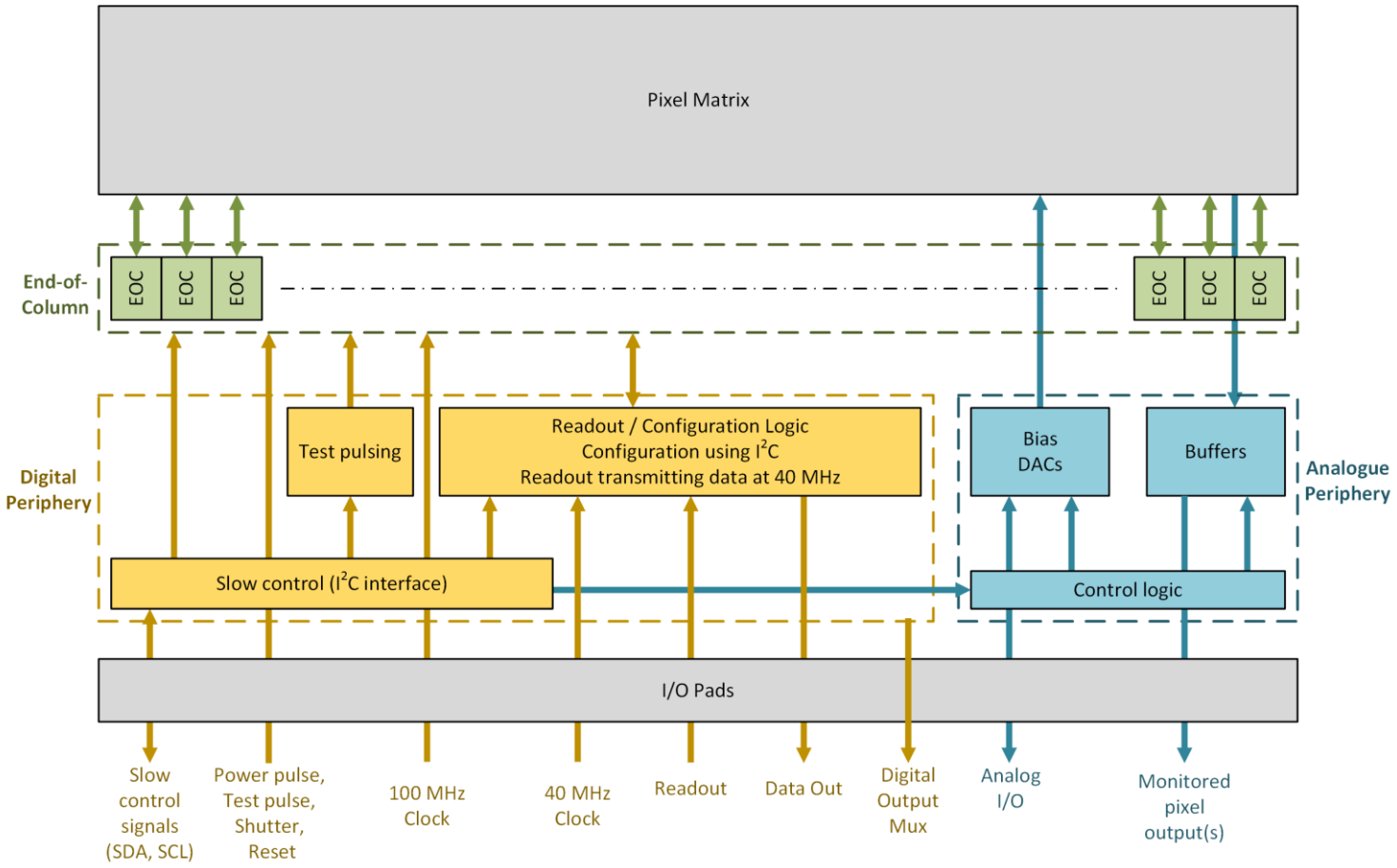
Readout

- **Readout frequency 40Mhz, 8b/10b encoding**
- **Zero compression can be enabled**
  - **No compression:**
    - **21 bits are read out per strip**
  - **Compressed readout at pixel level:**
    - **22 bits are read out for hit strips. 1 bit read out for strips that are not hit**
  - **Compressed readout at strip and column level:**
    - **1 bit is read out for the columns that are not hit**

	Data per frame *		Readout time	
	With hit map (21 bits/pixel)	Without hit map (13 bits/pixel)	With hit map (24 bits/pixel)	Without hit map (14 bits/pixel)
No compression	43 kbits	26.6 kbits	1.34ms	831us
Pixel compression	3.3 kbits	2.78kbits	103us	87us
Pixel and column compression	3.2 kbits	2.78kbits	100us	87us

* Calculated assuming an occupancy of 3%, and a matrix area of $4.8 \times 3.84\ mm^2$ (16×128 pixels)
The readout time is calculated assuming a readout at 40 MHz and 8b/10b encoding

Chip periphery

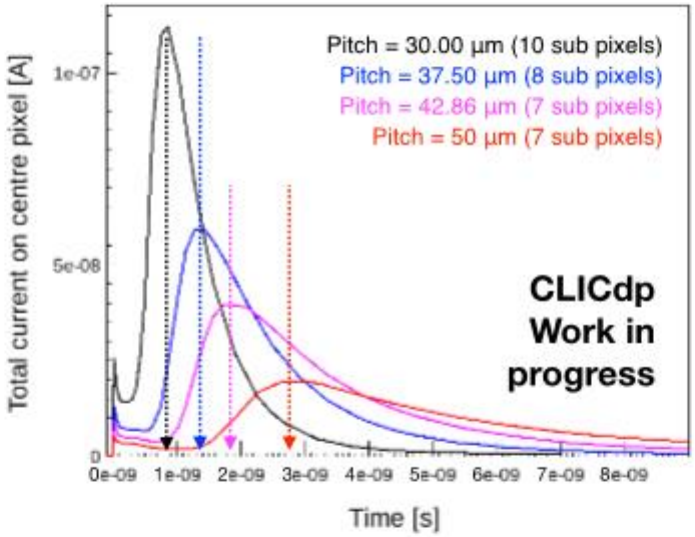


Summary and conclusions

- The CLICTD design status has been presented
- The design is done in TJ 180nm (monolithic) and using the “modified” process
- The chip sensitive area contains 128 rows and 16 columns of detector elements
- The detector channels are organized in segmented strips of 30μmx300μm measuring 8 bit ToA (10ns bin), 5 bit ToT and the individual pixel hit information (8 bits)
- The front-end has a gain of 160mV/ke$^-$, noise of 35e$^-$, minimum detectable charge 230e$^-$, fast timing characteristics and a power consumption of 2.16μW/strip
- The readout clock frequency will be 40MHz

2d TCAD simulation / **electric field for different pitch**

Particle incident pixel edge (worst case):



- Shift of time pulse needs to reach maximum differs by ~ 1 ns if we go from 10 to 8 sub pixels.

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