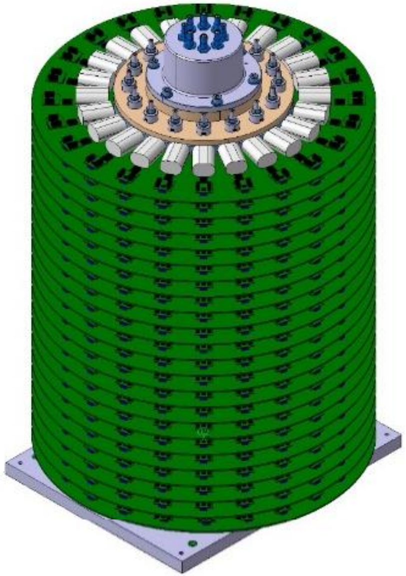
Inductive adder prototype pulse generator for FCC-hh kickers

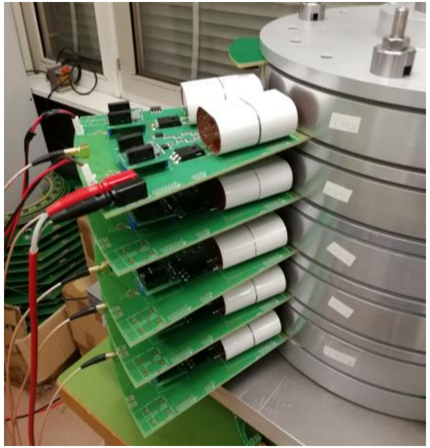
D. Woog

Acknowledgements:
M.J. Barnes, J. Holma, T. Kramer

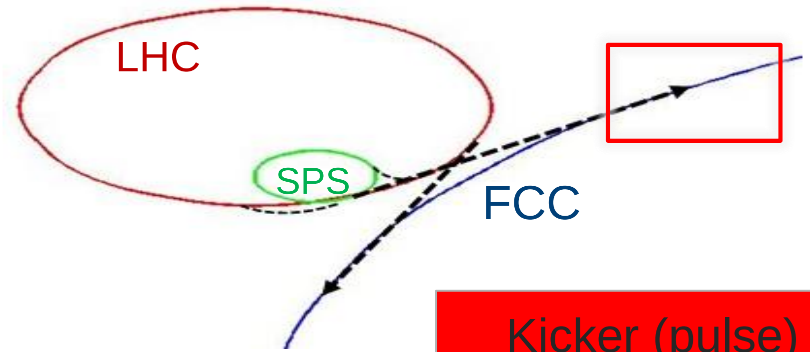
Content

- Inductive adder introduction
- Requirements and Design
  - General overview
  - Pulse length limitation
  - Stack design
  - PCB design
- Hardware status
- Summary and outlook

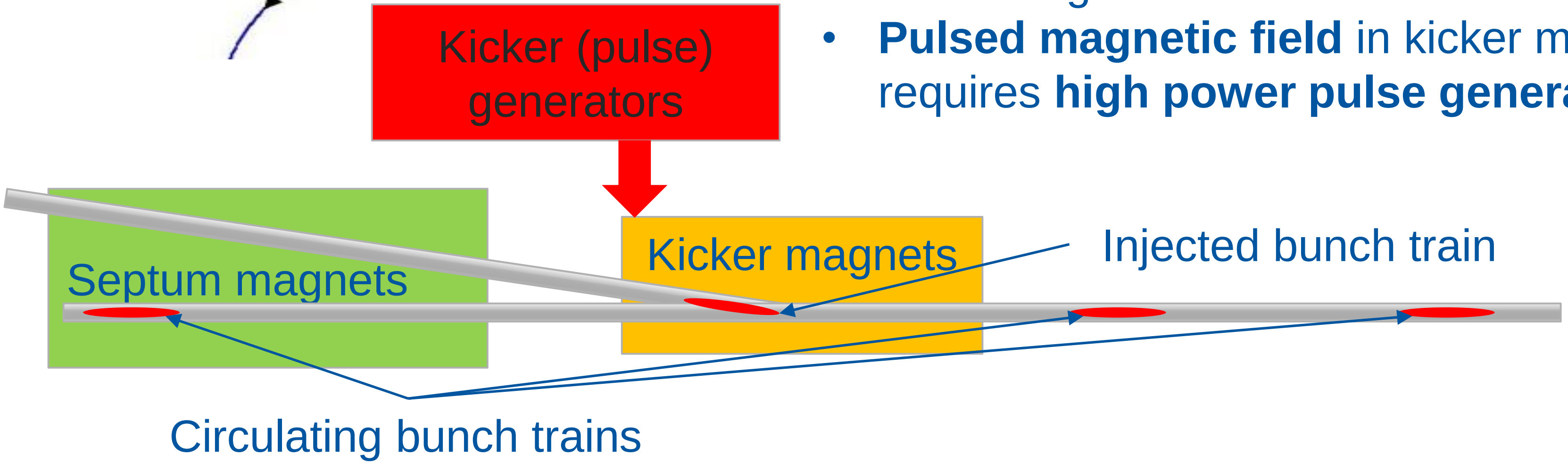




FCC-hh injection system



- Injection from high energy booster (HEB) into FCC
- Injected bunch train needs to be deflected onto the circular orbit
- Circulating bunches must not be kicked
- **Pulsed magnetic field** in kicker magnet requires **high power pulse generator**



Thyratron replacement

For machine protection reasons **high reliability** of the kicker system is necessary!!

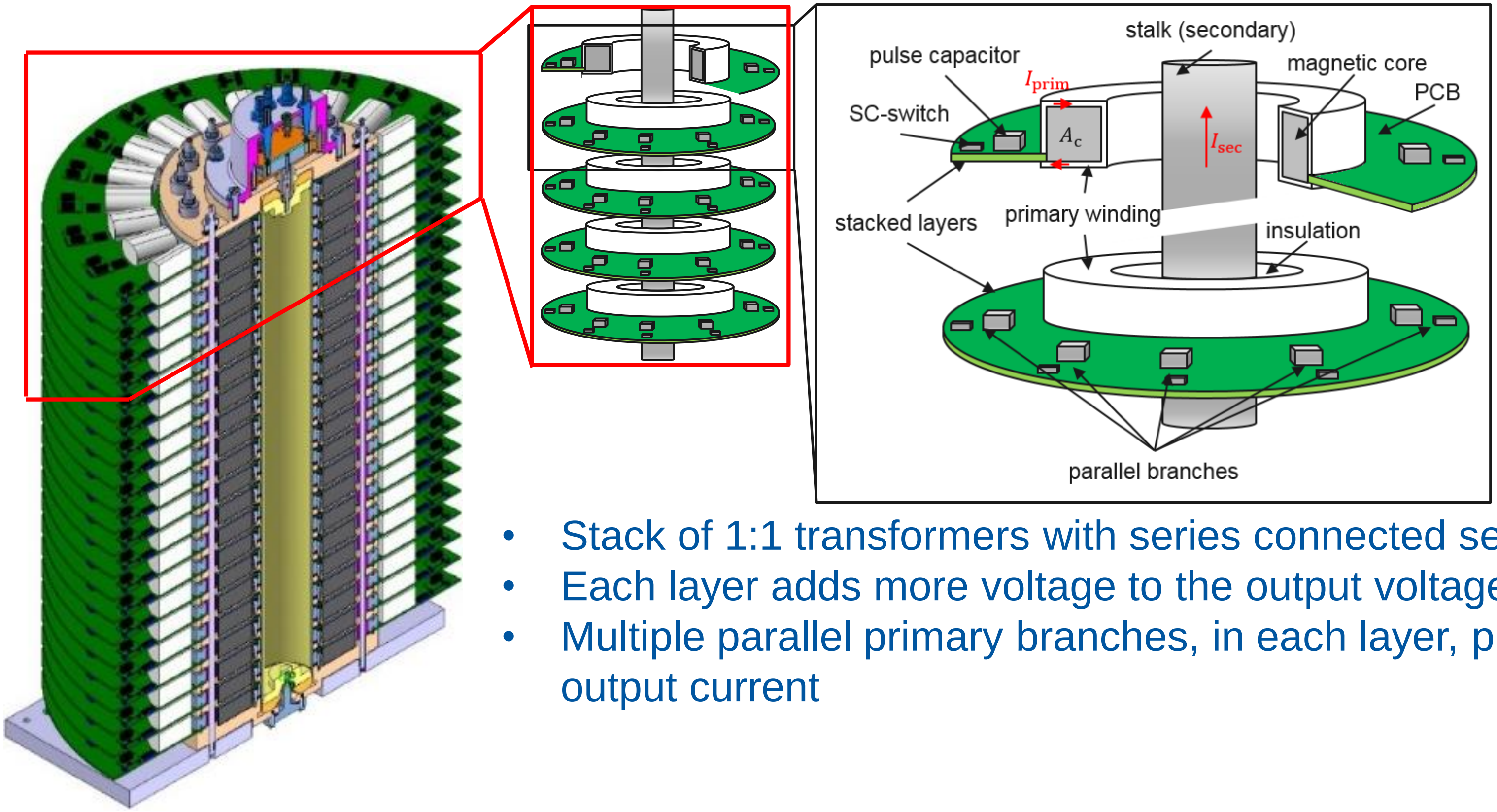
→ Thyratron **pre-firing** problems are unacceptable for FCC

- Thyratrons must be avoided as switch
- New pulse generator design is needed
- **Semiconductor (SC) switches** are a promising alternative
- Two main pulse generator designs based on SC-switches under consideration:
  - **Inductive Adder** (IA)
  - Solid state Marx generator

Presentation by Mike Barnes this morning:
"Marx prototype pulse generator design and initial results"

High voltage thyratron

Inductive adder



- Stack of 1:1 transformers with series connected secondary winding
- Each layer adds more voltage to the output voltage
- Multiple parallel primary branches, in each layer, provide the high output current

Requirements for the FCC injection Inductive Adder

Injection parameters (from LHC at 3.3 TeV):

Parameter	Unit	Value
Kinetic Energy	[TeV]	3.30
Angle	[mrad]	0.18
Pulse flat top length	[µs]	2.00
Flat top tolerance	[%]	±0.50
Voltage	[kV]	15.0
Current	[kA]	2.4
System impedance	[Ω]	**6.25**
Field rise time	[µs]	**0.43**

355 ns magnet fill time +
75 ns current rise time

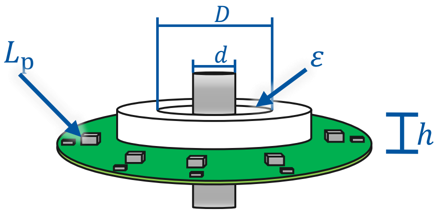
Inductive Adder prototype parameters:

Parameter	Unit	Value
Nr. of constant voltage layers	-	20
Nr. of modulation layers	-	2
Nr. of branches per layer	-	24
Characteristic impedance	Ω	6.25
Voltage per layer	V	960
Current per branch	A	100
Total height	mm	~1200
Output voltage	**kV**	**15.0**
Output current	**kA**	**2.4**

Impedance matching of the stack

Factors influencing the layer impedance:

- Ratio of primary inner diameter (D) and stalk diameter (d)
- Insulation material between primary and secondary (ε)
- Layer height (h)
- Inductance of primary winding (L_p)



Impedance of IA:

$$C_{\text{layer}} = \frac{2\pi\varepsilon h}{\ln\frac{D}{d}} \qquad L_{\text{layer}} = \frac{\mu \cdot h \cdot \ln\frac{D}{d}}{2\pi}$$

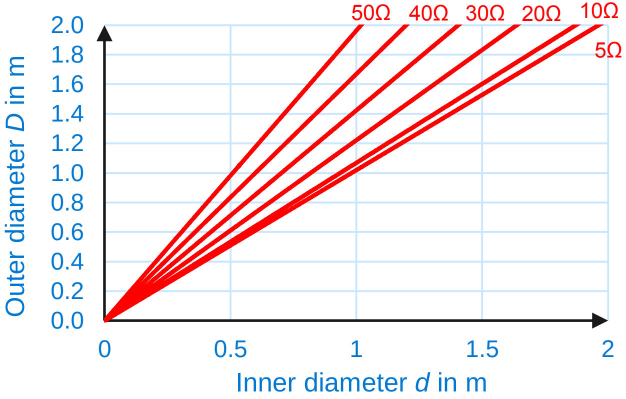
$$Z_{\text{IA}} = \sqrt{\frac{L_p + L_{\text{cell}}}{C_{\text{cell}}}} = \sqrt{\frac{L_p}{2\pi\varepsilon h}\ln\frac{D}{d} + \frac{\mu}{4\pi^2\varepsilon}\ln^2\frac{D}{d}}$$

Examples for insulation materials:

- Air
- **Oil**
- Water
- Epoxy
- FC-77
- SF6
- Vacuum

Outer diameter D over inner diameter d for different Z_{IA}

$$D(d) = d \cdot e^{-\frac{L_{p1}\cdot\pi}{h\mu} + \sqrt{\left(\frac{L_{p1}\cdot\pi}{h\mu}\right)^2 + Z_{\text{IA}}^2 \cdot \frac{4\pi^2\varepsilon_0\varepsilon_r}{\mu}}}$$

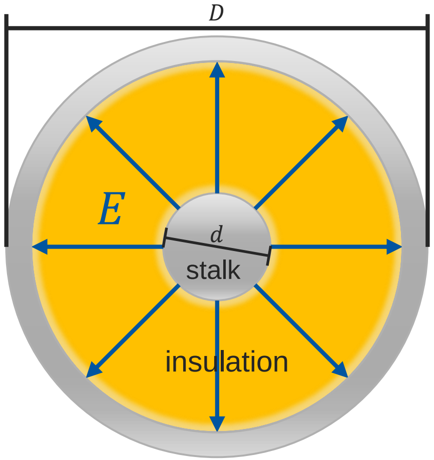


Low impedance -> small insulation gap

Electric field in insulation:

$$E(r) = \frac{V_{\text{out}}}{r \cdot \ln\frac{D}{d}}$$

$$E_{\max} = \frac{V_{\text{out}}}{\frac{d}{2} \cdot \ln\frac{D}{d}}$$



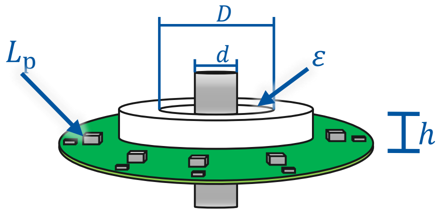
inner primary winding

Layer design for fast rise time

Propagation time of IA layer: $t_{\mathrm{p,layer}} = \sqrt{(L_\mathrm{p} + L_\mathrm{cell}) \cdot C_\mathrm{cell}} = \sqrt{\left(L_\mathrm{p} + \frac{\mu \cdot h \cdot \ln\frac{D}{d}}{2\pi}\right) \cdot \frac{2\pi\varepsilon h}{\ln\frac{D}{d}}} = \sqrt{L_\mathrm{p} \cdot \frac{2\pi\varepsilon h}{\ln\frac{D}{d}} + \mu\varepsilon h^2}$

Propagation time of IA stack (n layers): $t_{\mathrm{p,stack}} = 2n \cdot t_{\mathrm{p,layer}} = 2n \cdot \sqrt{L_\mathrm{p} \cdot \frac{2\pi\varepsilon h}{\ln\frac{D}{d}} + \mu\varepsilon h^2}$

$C_\mathrm{cell} = \frac{2\pi\varepsilon h}{\ln\frac{D}{d}}$ $\quad L_\mathrm{cell} = \frac{\mu \cdot h \cdot \ln\frac{D}{d}}{2\pi}$



Factors influencing the rise time:

- Stack height
- Insulation material
- Primary inductance
- Output voltage, layer voltage
- Switching time of switching device

Use of *Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistor* (**SiC MOSFET**) as switching device

Pulse length limitation in case of erratic

Problem:

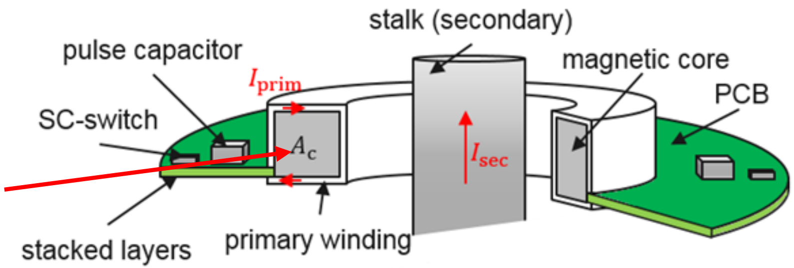
- Large amount of energy stored in the pulse capacitors
- **Long pulse length** in case of an erratic (capacitor discharges completely)
- For machine protection reasons a maximum of **80-100 bunches** (~2 µs) can be accepted by the injection protection system

In case of pulse forming network / line (PFN/PFL) only the energy for one kick is stored in the system
-> impossible to generate longer pulses (hence limited number of circulating bunchs at risk)

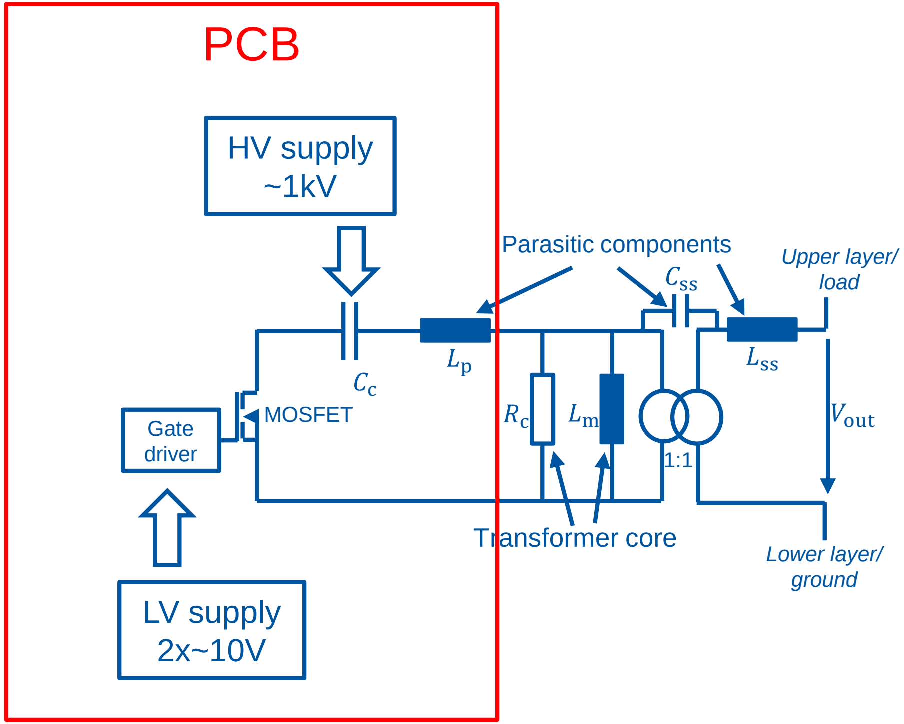
Possible solution:

- Design of the **magnetic core cross sectional area** without significant margin
- In case of too long pulses the **cores saturates** and the output drops to zero

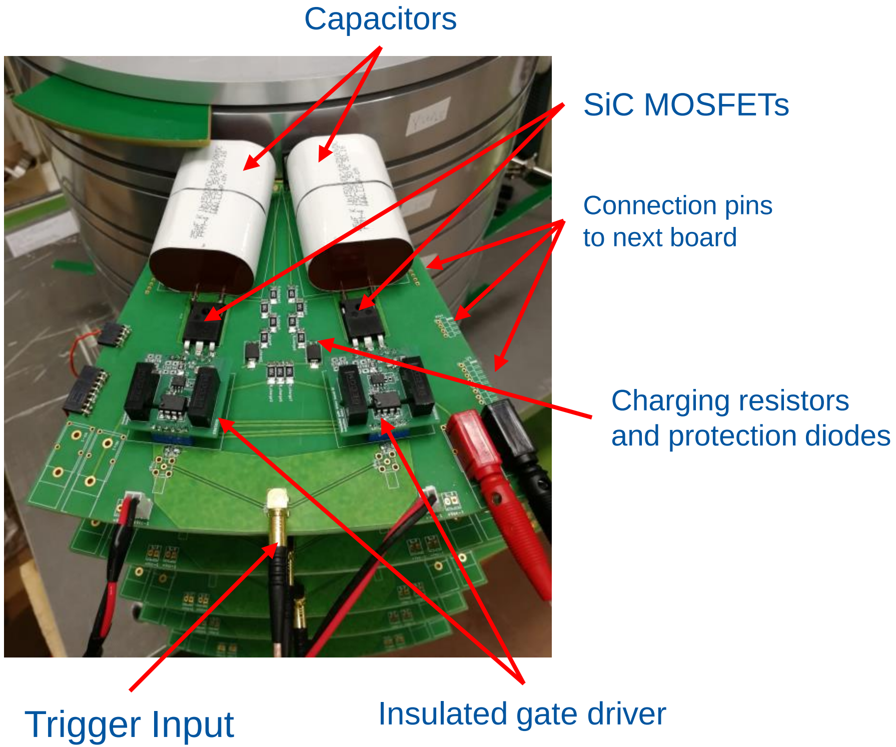
$$A_c = \frac{\int V_c \, dt}{\Delta B}$$



PCB design



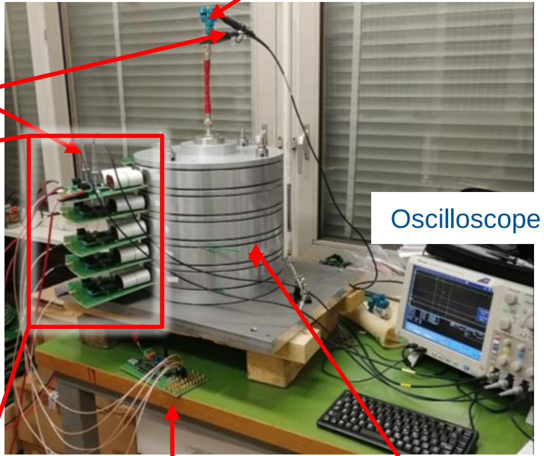
PCB
HV supply
~1kV
Parasitic components
Upper layer/
load
C_{ss}
C_c
L_p
L_{ss}
MOSFET
Gate
driver
R_c
L_m
1:1
V_{out}
Transformer core
Lower layer/
ground
LV supply
2x~10V



Capacitors
SiC MOSFETs
Connection pins
to next board
Charging resistors
and protection diodes
Trigger Input
Insulated gate driver

Hardware status

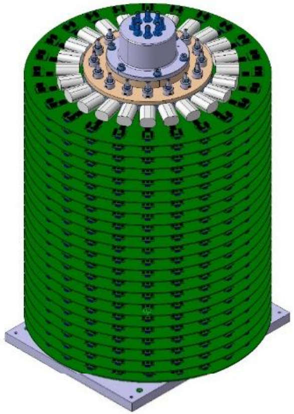
Test setup, with FCC PCBs, on CLIC prototype cores



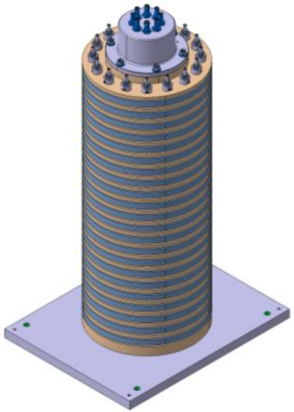
Measurement results	
V_{layer}	1 kV
V_{out}	5 kV
R_{load}	50 Ω
I_{out}	100 A
t_{rise}	40 ns

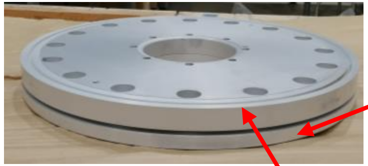
Hardware status

Inductive adder with PCBs

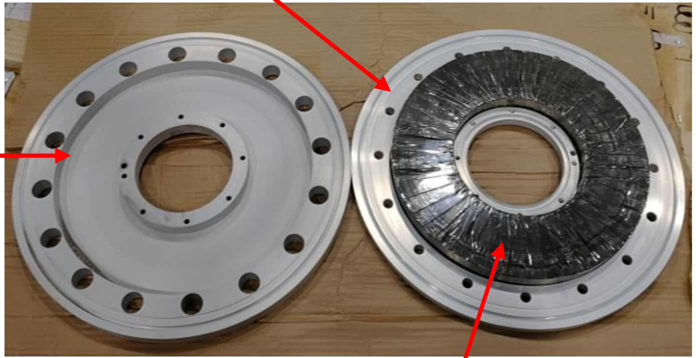


Inductive adder without PCBs

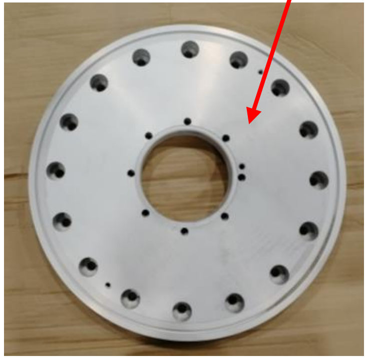




Lower layer part



Upper layer part



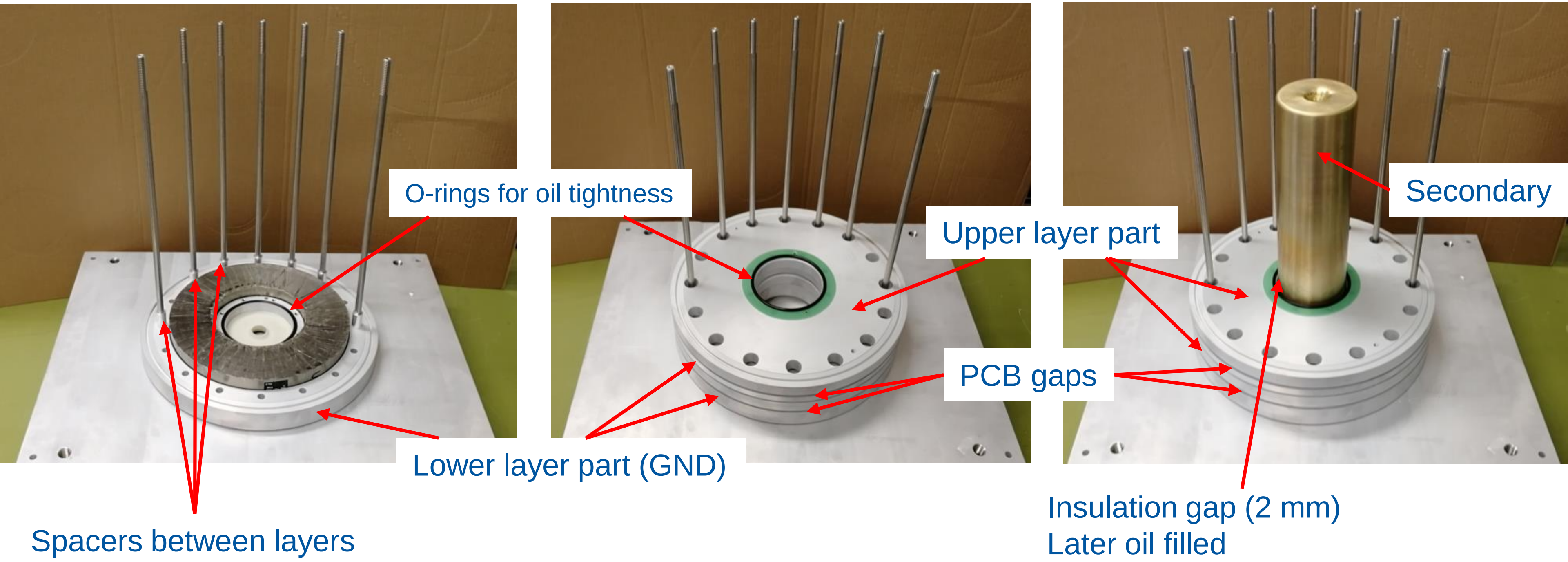
Tape wound, nanocristalline magnetic core (insulated)

Hardware status

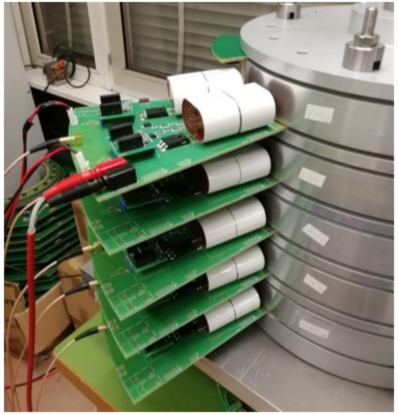
Magnetic core of first layer

Two layers of the IA

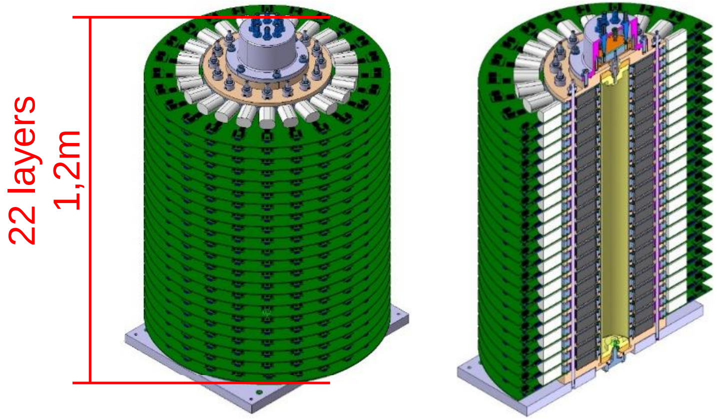
Two layers with secondary



Summary



- Injection kicker pulse generator design is complete
- System impedance of 6.25 Ohm (2.4 kA, 15.0 kV) with oil insulation
- Testing and developing of components is complete
- Components are received
- Setup of first prototype has started (10 layers)



Outlook:

- Verification of simulation results on 10 layer prototype, until June
- Upgrade to 22 layer prototype by end of 2018 / beginning of 2019

Thank you for your attention!

Questions?