

Mass Chip Test (MCT) and Hybrid Integrated Circuit (HIC) production in PNU for ALICE-ITS Upgrade

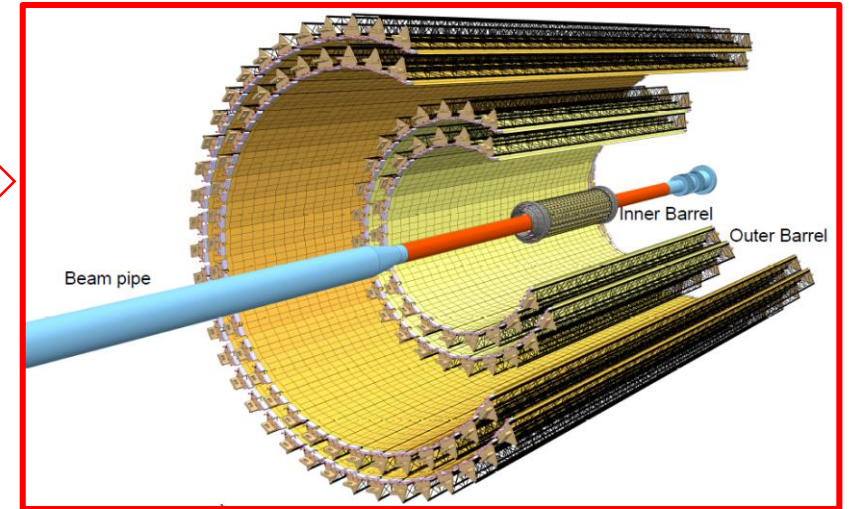
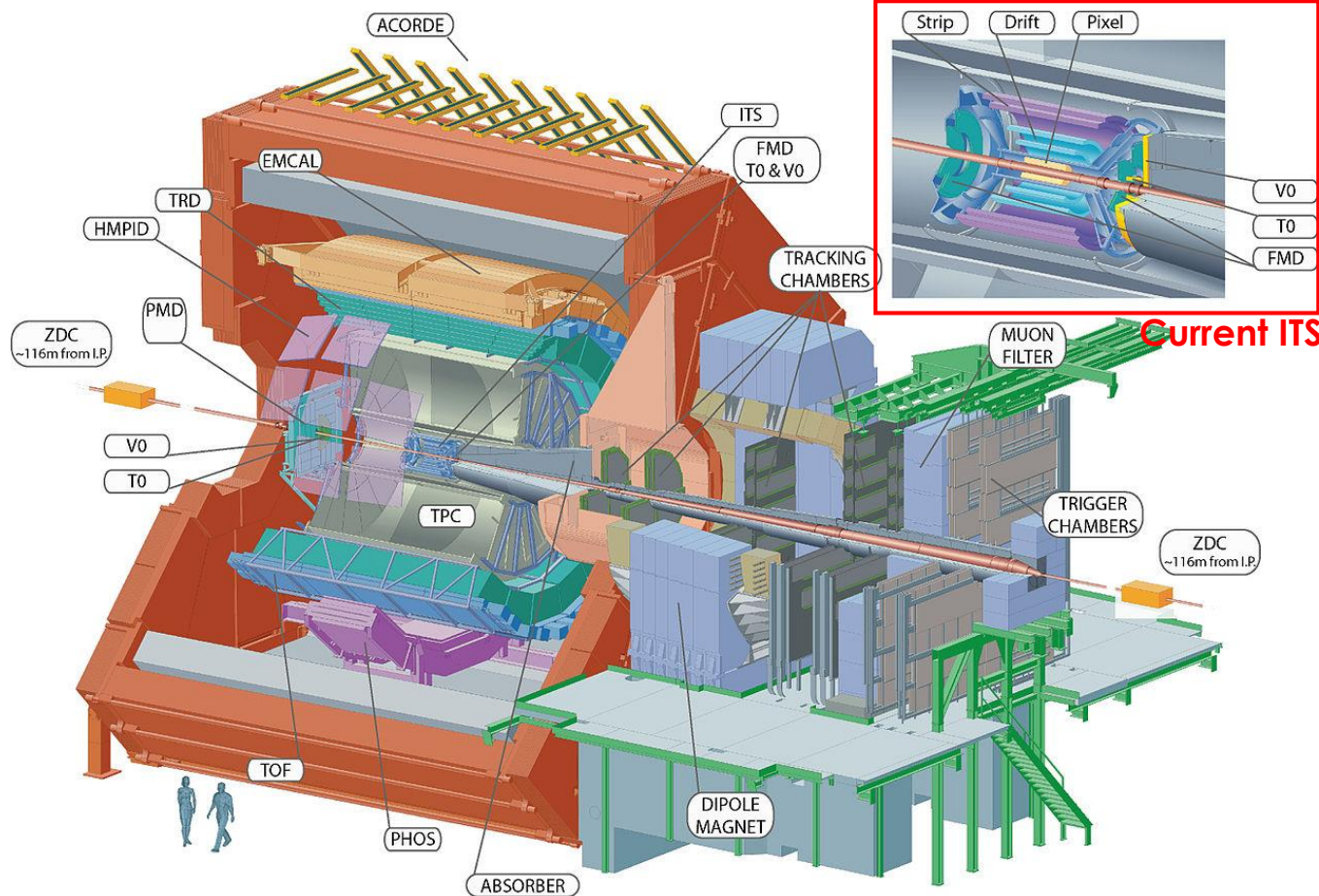
Bong-Hwi Lim

Pusan National University

2017-08-16

A Large Ion Collider Experiment

ALICE and Inner Tracking System



New ITS (Inner Tracking System)

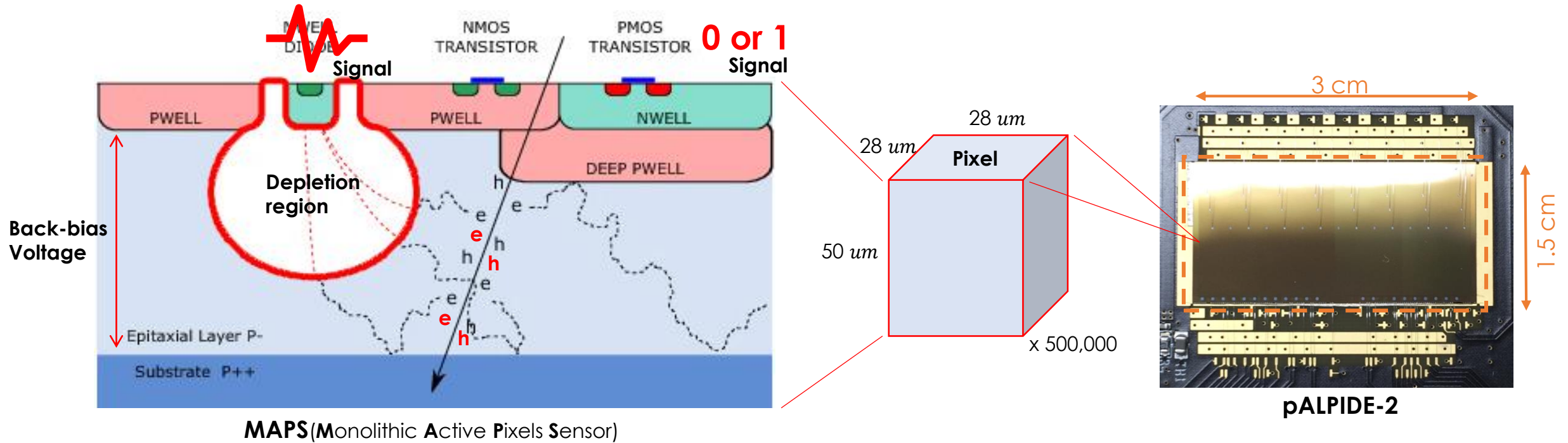
Upgrade Motivation

- Increase position resolution and tracking efficiency for heavy quark
- Increase readout rate capabilities(x100)



The way how we can track the particles

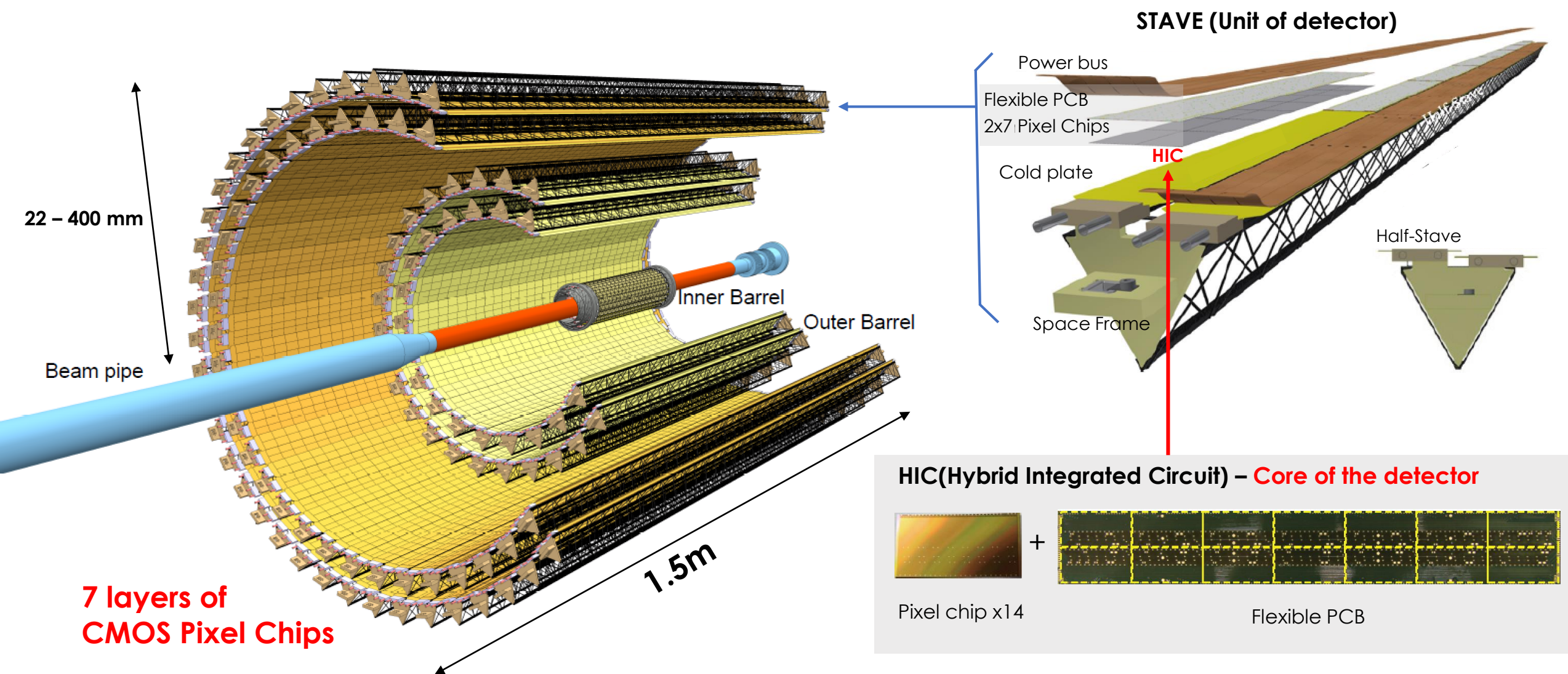
ALPIDE and MAPS technology



- CMOS MAPS (Monolithic Active Pixels Sensor) technology
 - **Integrated Signal Processing Circuit into the Pixel**
 - **High granularity** → High Position resolution
 - **Low material budget and power consumption**
- 3 x 1.5 cm² size, 50 μm thickness, 500,000 Pixels
 - 28 μm x 28 μm pixel size

Appearance of the new ITS

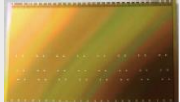
ITS Outer Barrel



ITS Upgrade Project

Outer Barrel Construction Workflow

Mass Chip Test



x 30k

- Electrical Test
- Visual Inspection

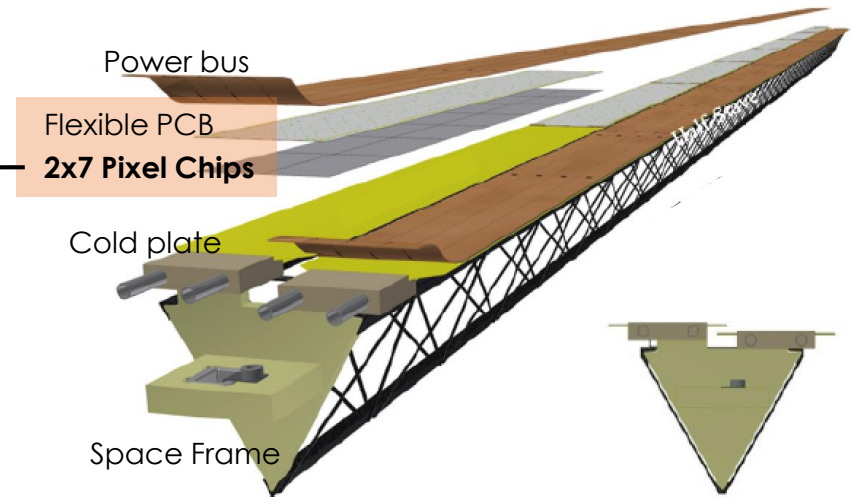
Distribute to each site

Test period: 5.5 min/chip x 30k chips → ~1 year
 From **August 2017** to **August 2018**


Pusan-Inha Univ.
Yonsei Univ.

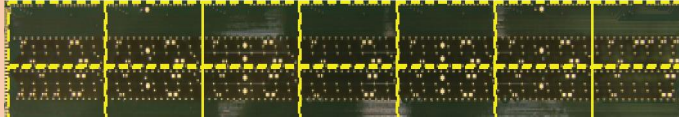
Flexible PCB

Trieste



HIC(Hybrid Integrated Circuit) Assembly



+ 

Pixel chip x14 Flexible PCB

Test period: 0.6 day/HIC x 400 HICs → ~1 year
 From **Sept. 2017** to **July 2018**

Pusan-Inha Univ.
Bari, Liverpool, Strasbourg, Wuhan

Power Bus

Kharkov

Cold Plates & Space-frames

CERN

Stave Assembly, Test

Daresbury, LBNL, NIKHEF, Turin

Outer Barrel Assembly

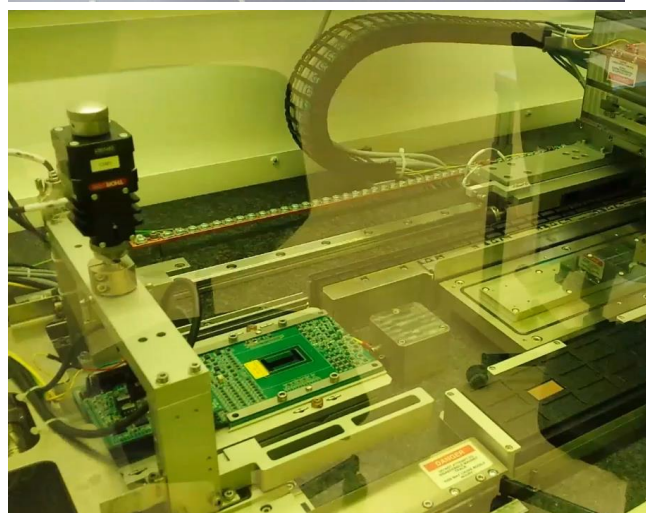
All@CERN

- Worldwide 14 countries participant / 16 Million USD
- Time plan:
 2012 ~ 2016 (R&D) / **2017 ~ 2018 (Prod.&Test)** / 2019 ~ 2020 (Install)

Preparation in HIPEx

Lab preparation for MCT/HIC Assembly

- ALICIA (~180k CHF)

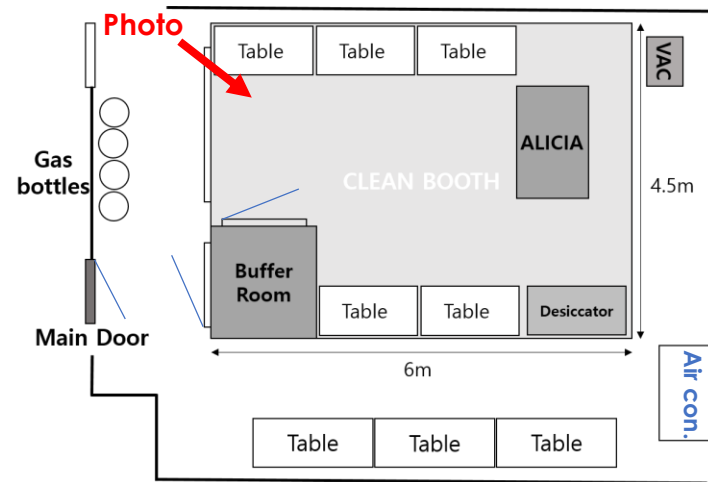


Lab Preparation in PNU



- **We built the lab from (almost) zero**
 - When we start the preparation, we had only a room with an air conditioner. (June of 2014)
- **Our achievement**
 - Install the clean booth and the contents
 - Lab Environment: Electrical support, Gas support, ESD Protection, Floor vibration level check

Installation & Specification



2017-08-16

• Installation the clean booth

- We installed **the clean booth** in the room.
 - Merits – Movable, moderate price, looks good!
 - Demerits – Needs an additional air conditioner for temp. & humidity control
- Installed in 25th of October, 2016
 - Need maintenance of the filters by half or a year

• Specifications

- Cleanness level: 10,000 Class*
- ESD Protection
- Clean booth size: $6 * 4.5 \text{ m}^2$
 - Height: 2.3 m
- Buffer room without air shower
- Temp. & Humidity are controlled by room air conditioner
 - Power: $21,000\text{W}^*$, Room area $\sim 55 \text{ m}^2$
 - Temp. & Humidity logger(testing)
 - The record can be shown in the web site.
 - Possibly log the cleanness level.

*Detailed results are in back-up slide

*For active area, the appropriate power of air conditioner per square meter: $\sim 125\text{W}/\text{m}^2$
2017 Pusan-Inha Physics Workshop

Facilities



Inside the clean booth



Desiccator



Air Conditioner



Gas bottles



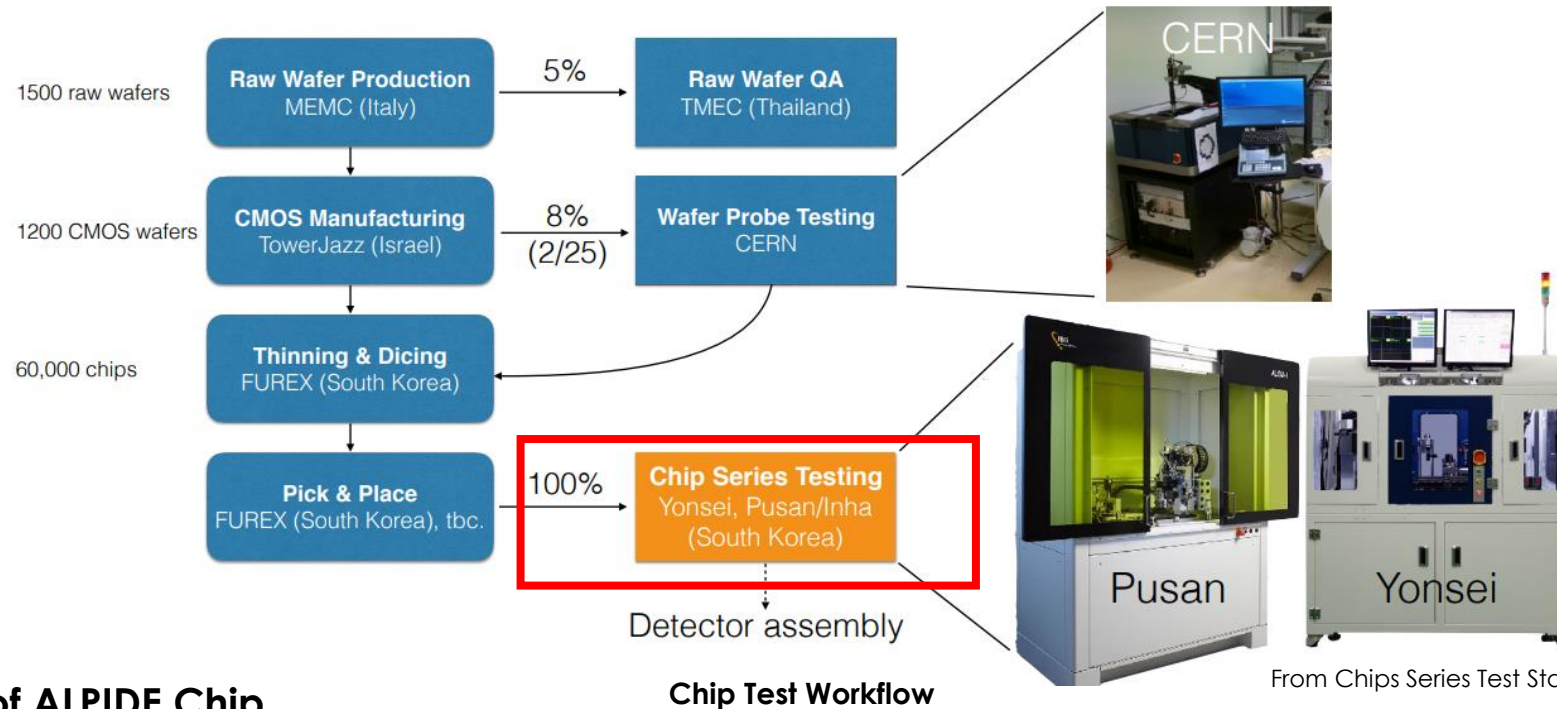
Microscope



Vacuum Pen (Feb.2017)

Details of each equipment are in back up slide

General



- **Series Test of ALPIDE Chip**

- Test amount: **30,000 chips**
(50% of total chip needed for whole ITS upgrade project)

- **Using ALICIA with Probecard**

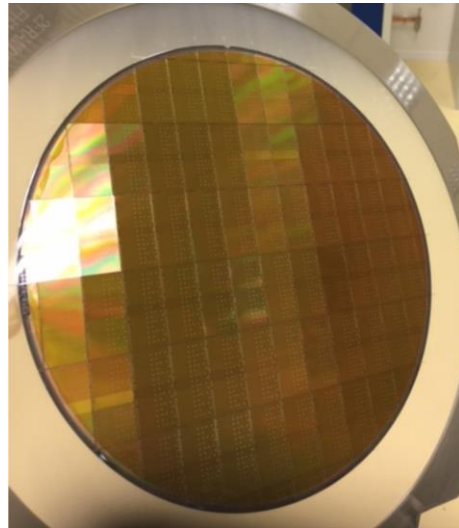
- Test sequence: Chip Dimension Measurement (Visual Inspection) -> Probecard Measurement (Electrical Test)
- Test time: 2.5 hour / 23 chips
(can be optimized later..)

- **Test period: August 2017 ~ August 2018**

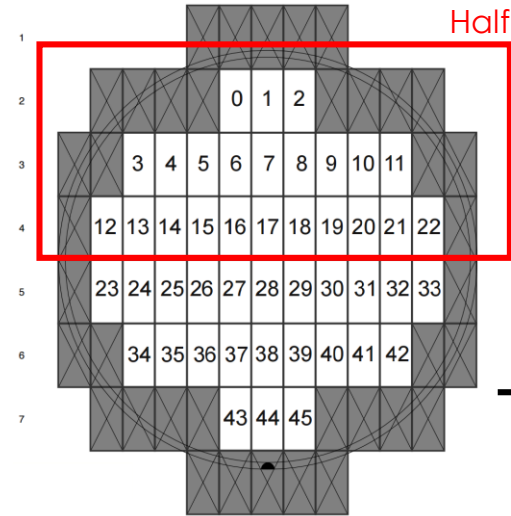
- 4 shifters in 2 shift per day (6 hour for a shift) from **Mon.** to **Fri.**

Preparation of the Chip

From wafer to the chip tray



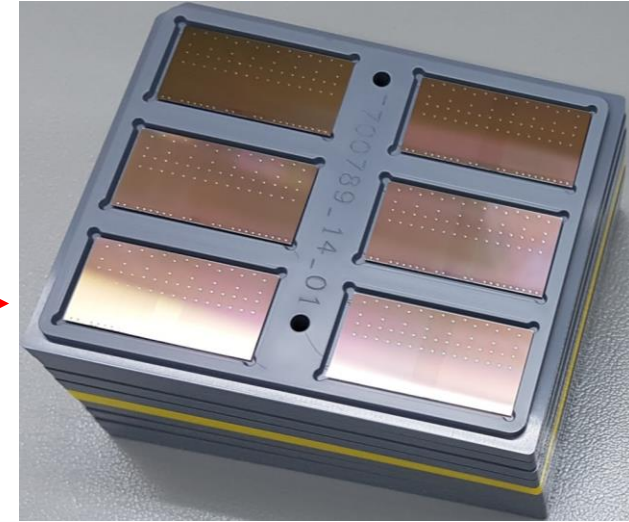
Wafer



Wafer layout



8 trays



6 chips in a tray

- **One wafer (46chips) is distributed into 8 trays**
 - Yellow tray: Cover tray
 - Top 4 trays: chips from top of wafer
- **A 4-tray-set has it's own barcode for ID (Wafer, ship ID etc.)**

Insert



4-tray-set with 4 trays

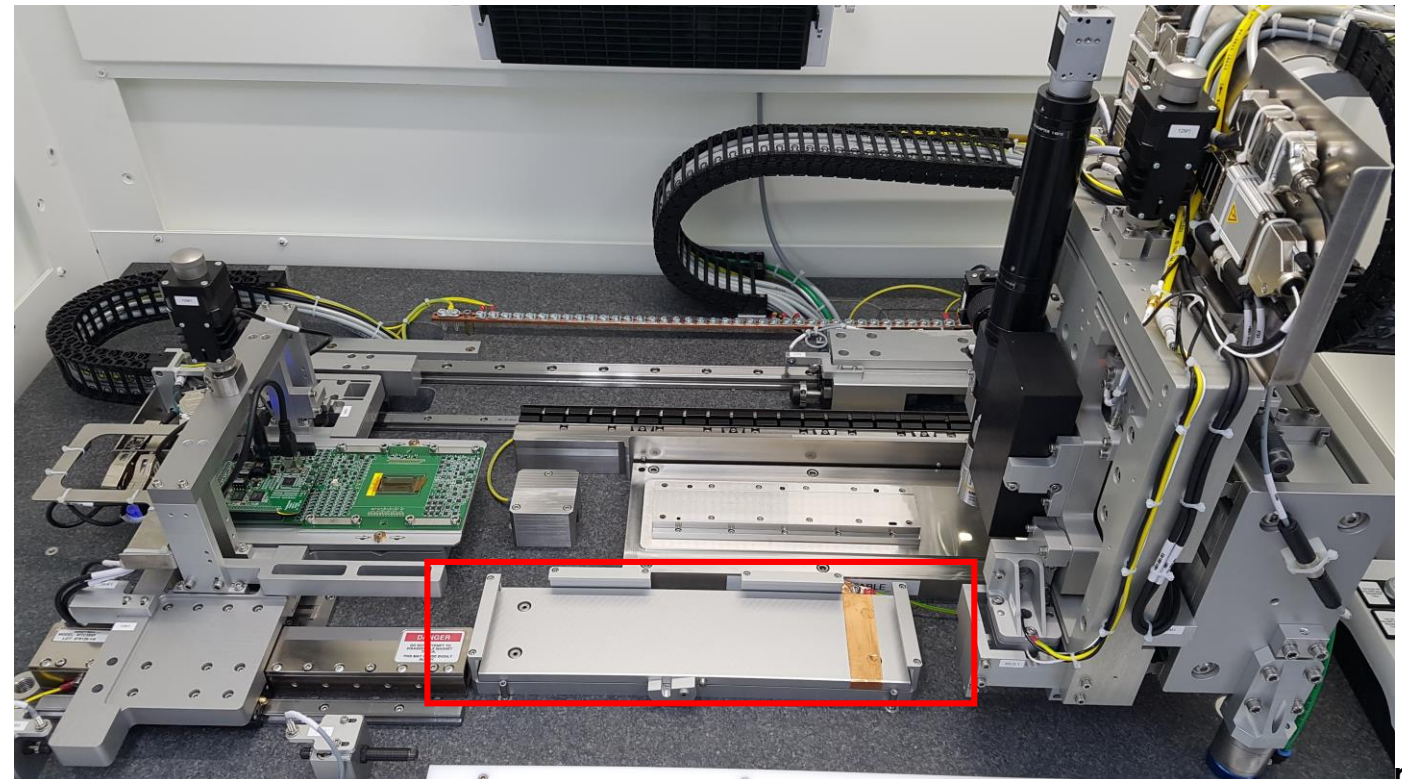
Mass Chip Test

In Pusan



- Chip Test Procedure:

- 1. Chip Placement(Tray to PPC)



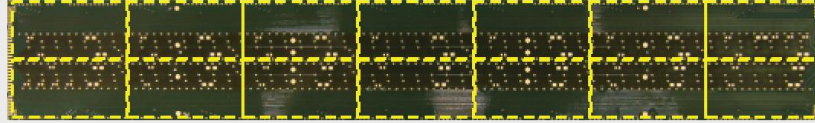
General

HIC(Hybrid Integrated Circuit) – Core of the detector

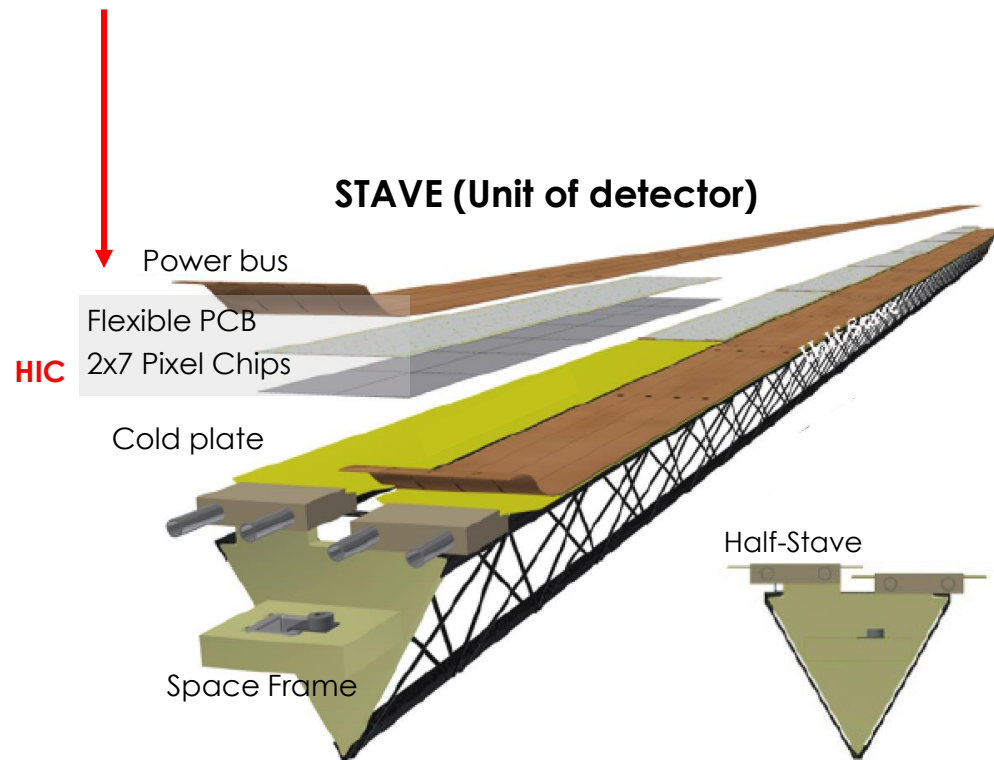


Pixel chip x14

+

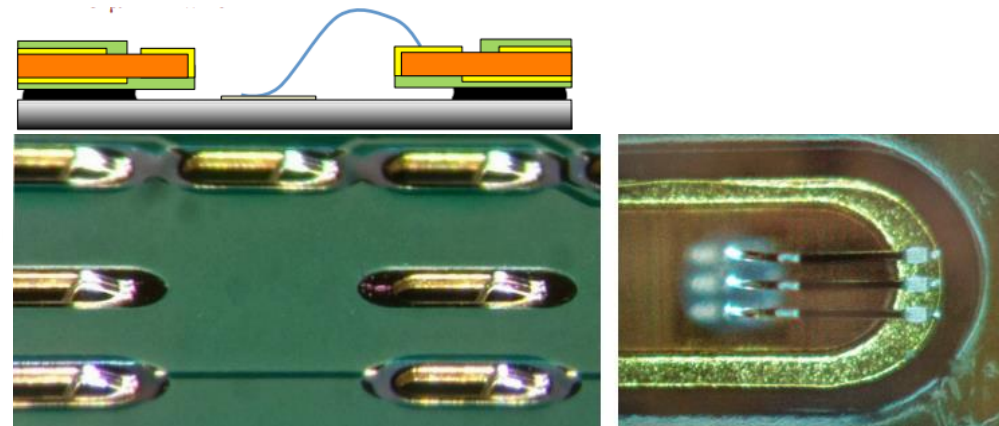


Flexible PCB



• HIC

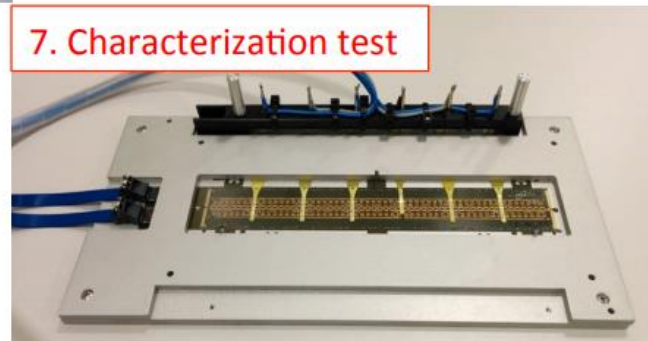
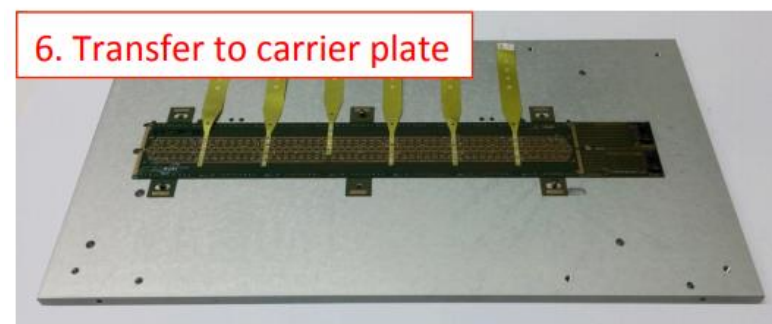
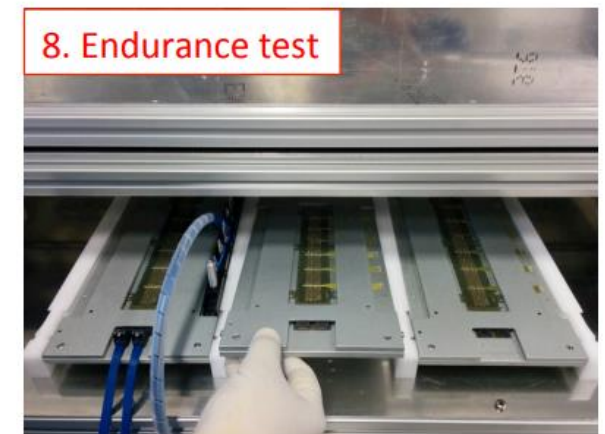
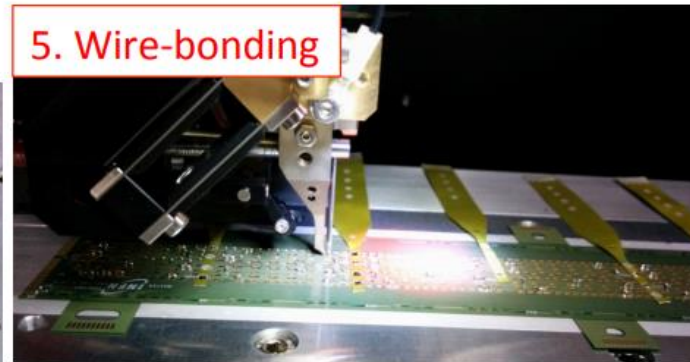
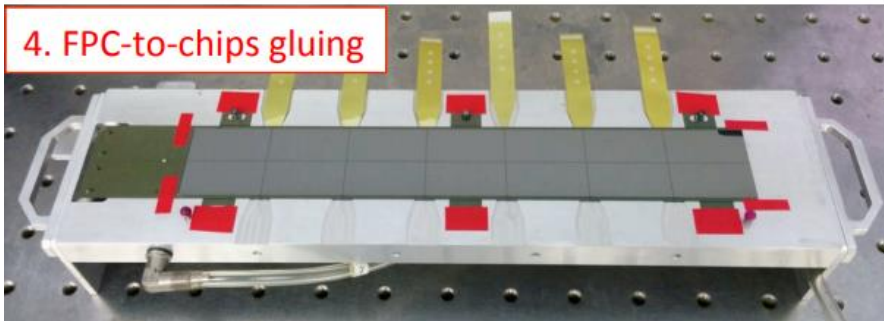
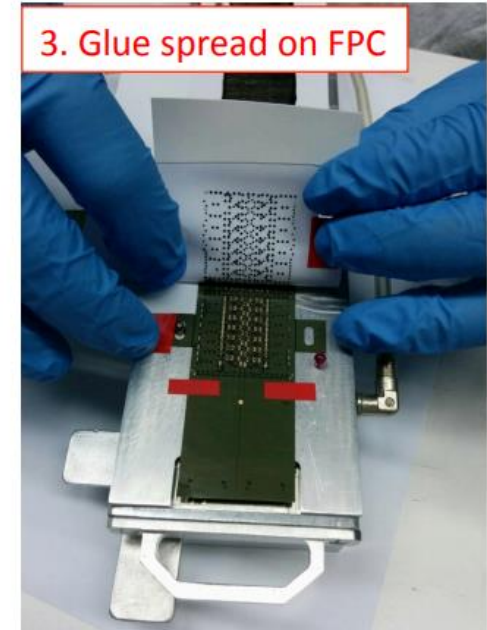
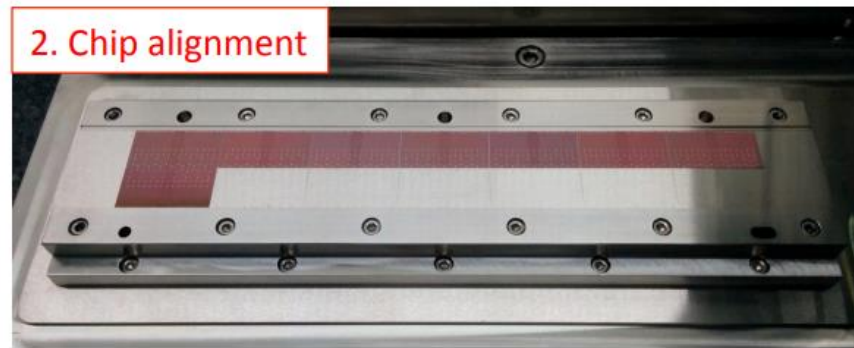
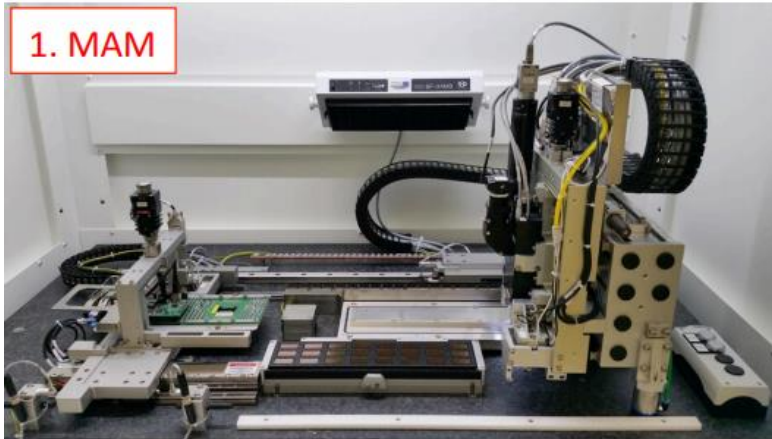
- 14 Pixel chips + 1 Flexible PCB
 - Using the chip from MCT
 - Bonded by wire-bonding technique
- **Total ~ 2000 HICs are needed for OB Stave**
- **PNU/INHA team will cover 20% of them**
 - ~ 400 HICs
- **Due to the MCT, we should produce 1 HIC per day**
- **Wire-bonding will be done by external company**



Wire-bonding

HIC Assembly

Procedure

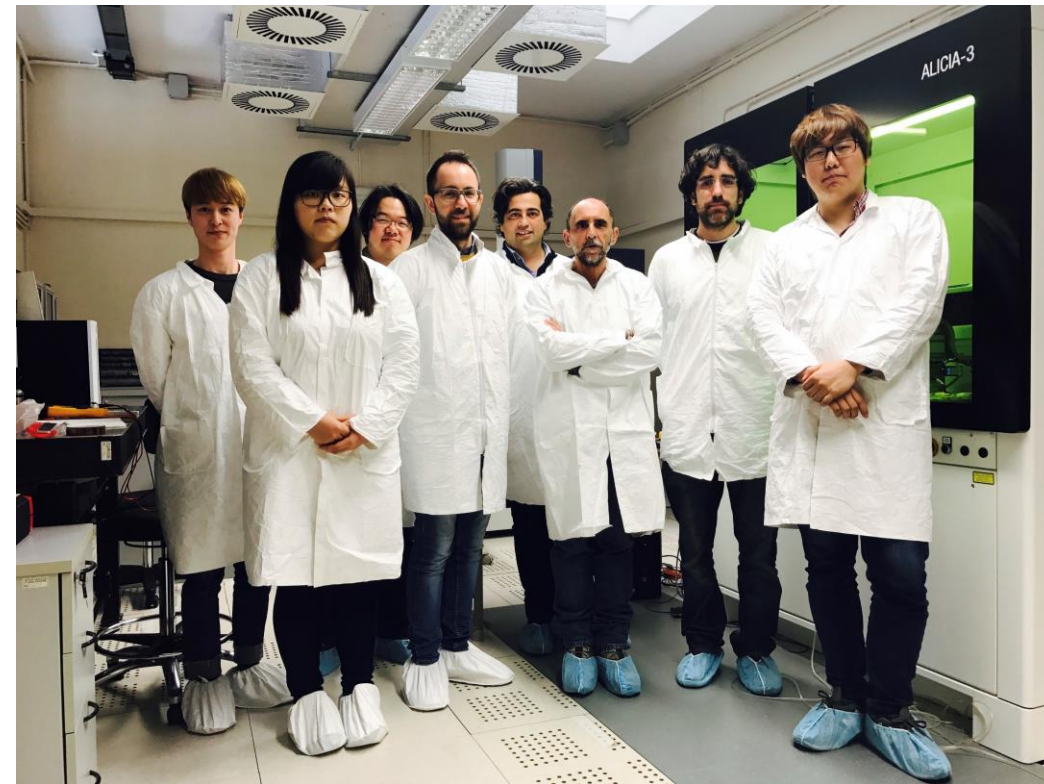


From OB HIC Production Overview(Vito Manzari) 2017.06.26.

Preparation for HIC Assembly

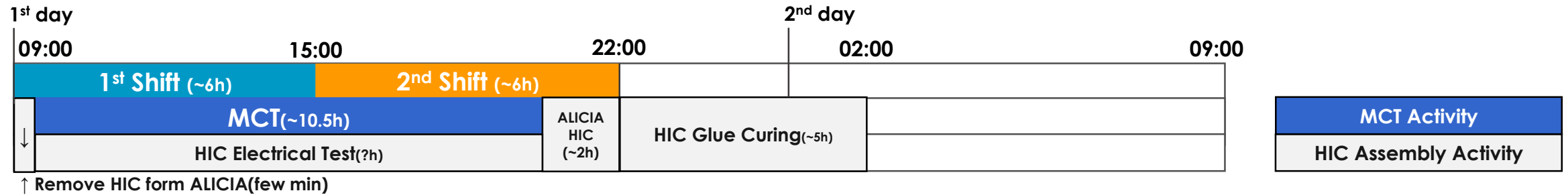
Traninging

- **Date:** 20th ~ 24th Feb. 2017 (5 days)
- **Location:** Bari
- **Participant:** Bong-Hwi Lim, Jongsik Eum, Hyesun Bang, Jonghan Park
- **Main Activities:**
 - Training Gluing Procedure with Dummy HIC module
 - Making Check List of the Tools
 - Briefing the HIC Test



Daily Schedule

For MCT/HIC Assembly



- **We need to compose the daily shift schedule with MCT and HIC Assembly.**

- HIC assembly needs ~ 5 hours of curing time.
- MCT mainly doesn't need such a effort for manual procedure.

- **2 shift plan**

- 1st shift will test ~ 3 chip trays
- 2nd shift will test ~ 2 chip trays
 - And prepare the HIC assembly and start HIC Glue curing
 - Leave the HIC in the machine and finish the shift
- 1st shift will remove the HIC from the machine at the beginning

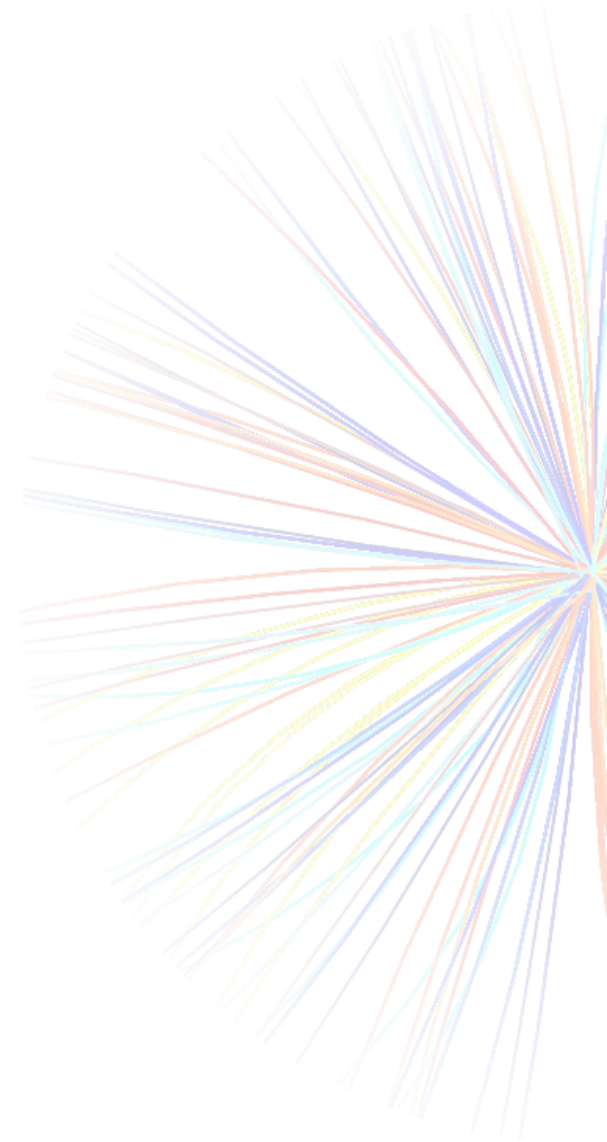
and Outlook

- **Mass Chip Test**

- It's very remarkable and important mission for ALICE ITS upgrade project
 - All tested chip will be used for the whole detector
- We've prepared the lab environment such as clean room
- The MCT has been started from this month.

- **HIC Assembly**

- HIC is the core part of the whole detector parts
- PNU/INHA team will cover the 20% of total HIC
- Along with the preparation of MCT, lab environment is ready for the assembly.
- It will be started in next month



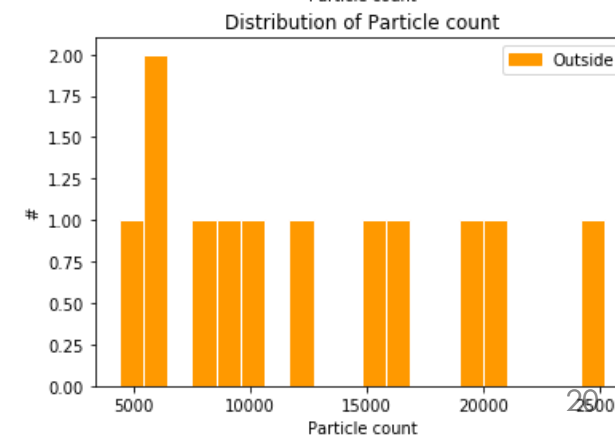
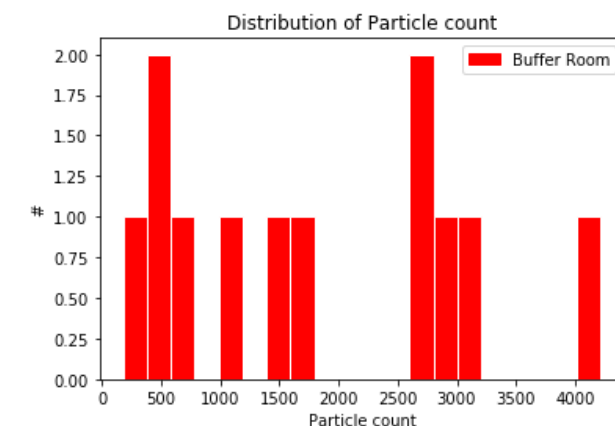
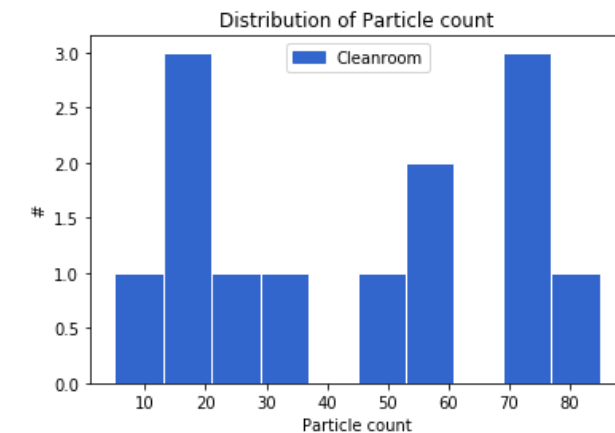
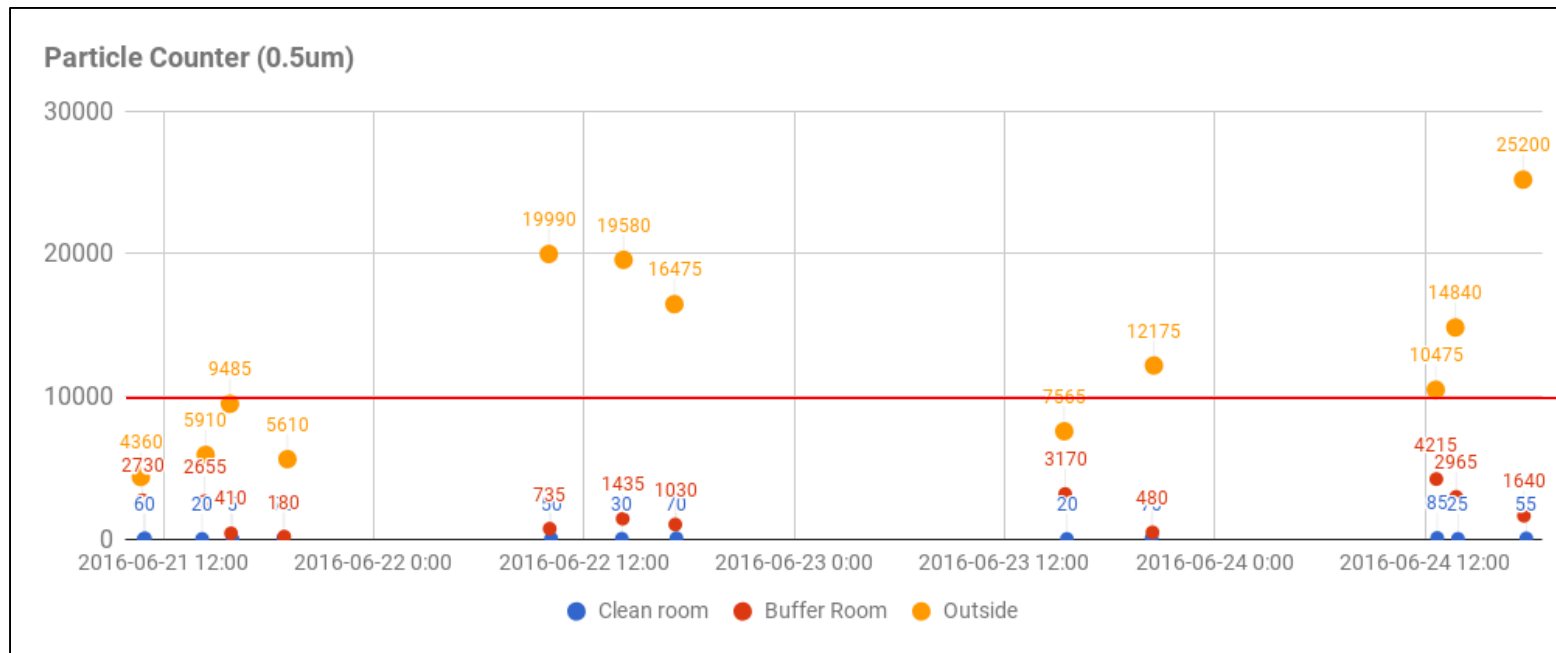


Thanks for your attention!!

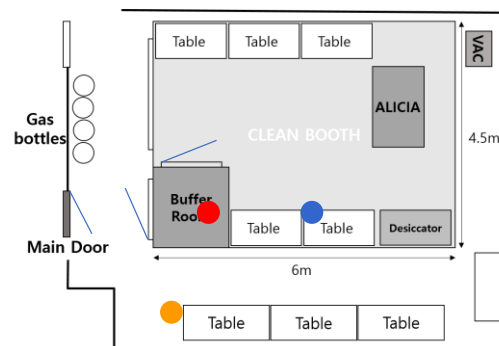
Back up

Cleanness level measurement

Using Particle counter



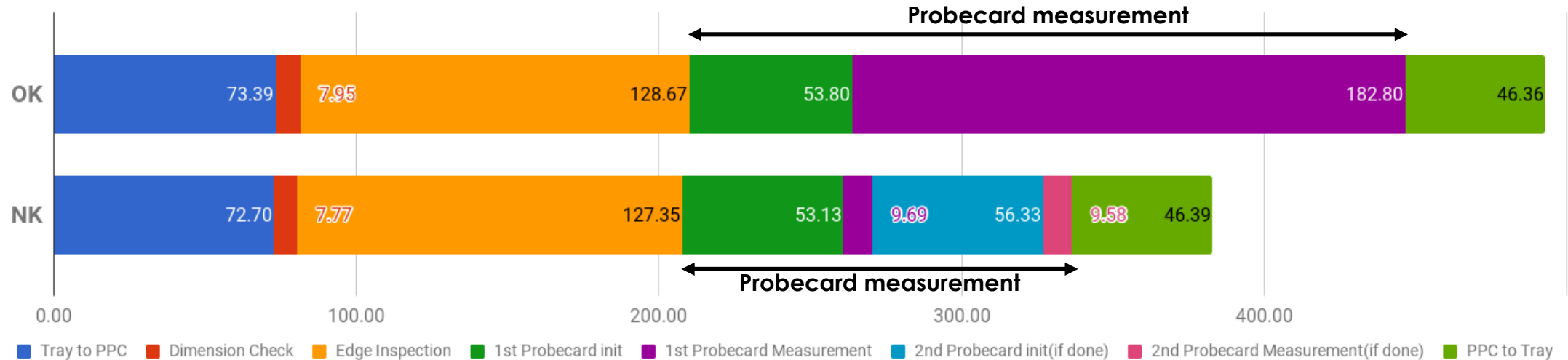
- **Cleanness level:** determined by # of 0.5 um size particles in $1ft^3$
 - Measured with Particle Counter (Airy Technology P311)
- **Result:**
 - **Inside of the Clean Room:** 44 ± 26 counts
 - **Buffer Room:** 1804 ± 1308 counts
 - **Outside of the Clean Room:** 12639 ± 6628 counts
 - We could see a **clear separation of each position**
 - further data needed for study
- **On-line monitoring is planned**



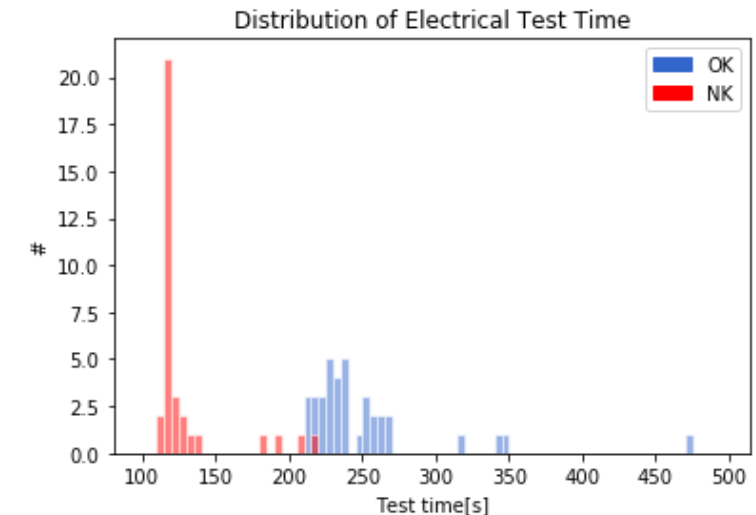
Result: Chip Test Time Measurement

Overall test time with status of chips

Chip Test Time



- **Average Test Time** (Except ~10% of outlier)
 - OK: 492 ± 18 s
 - NK: 382 ± 25 s
 - Average: 433 ± 60 s (**7 min 13s**) (Yield ~50% Case)
 - If we set the yield to 75%, average test time will be 465 s
- **Probecard Measurement time**
 - **Initializing time** + **Measurement time**
 - NK Case always has **2nd attempt**
 - Most **critical time** for the total test time
 - ~ 10 % of outlier data are needed to be understood



Thanks to Minjung Kim