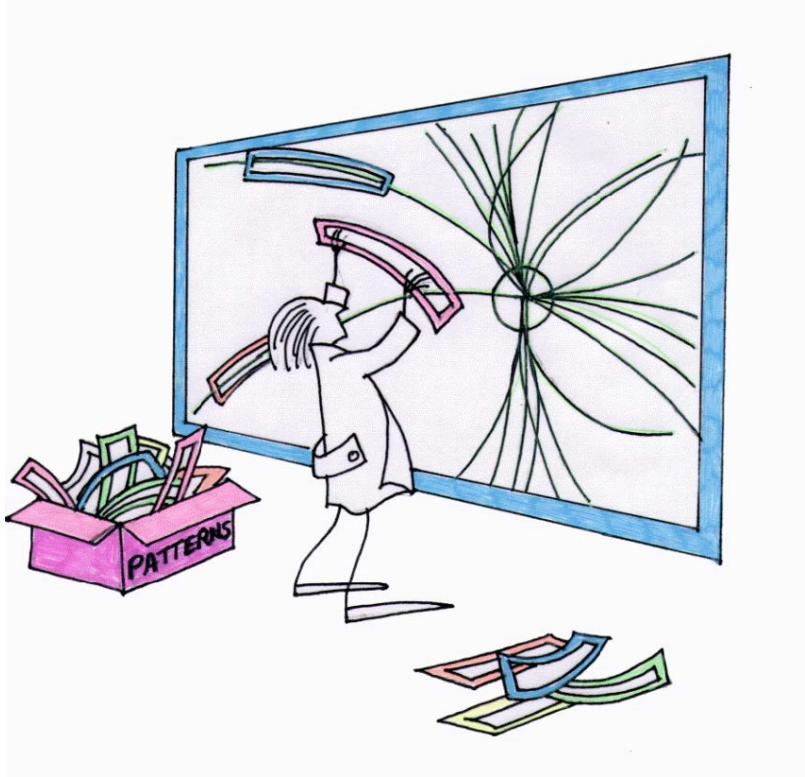
The Fast TracKer

A hardware track processor for the ATLAS trigger system



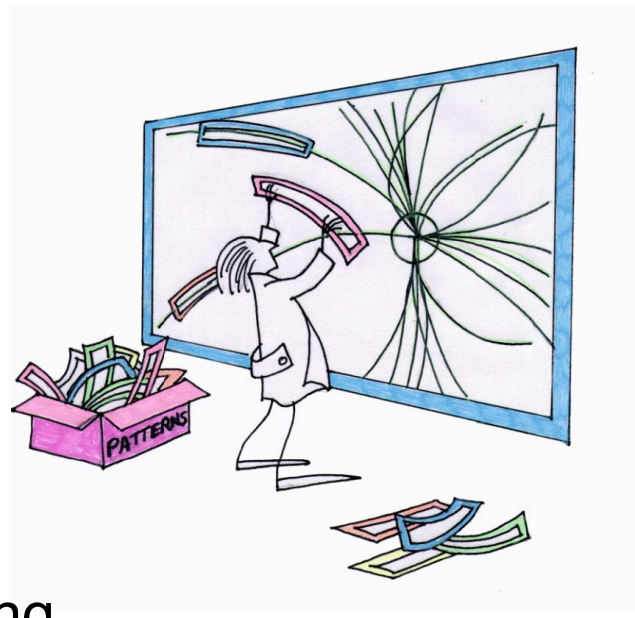
Karolos POTAMIANOS, on behalf of the ATLAS Collaboration
Connecting the Dots, UW, Seattle, USA
March 20, 2018

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

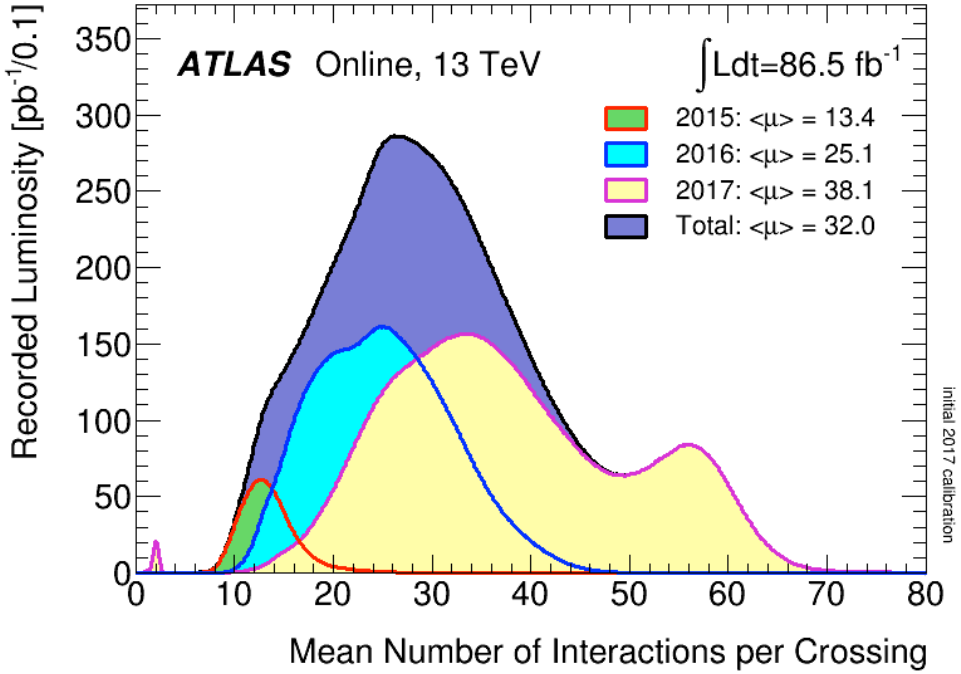
ATLAS EXPERIMENT

DESY

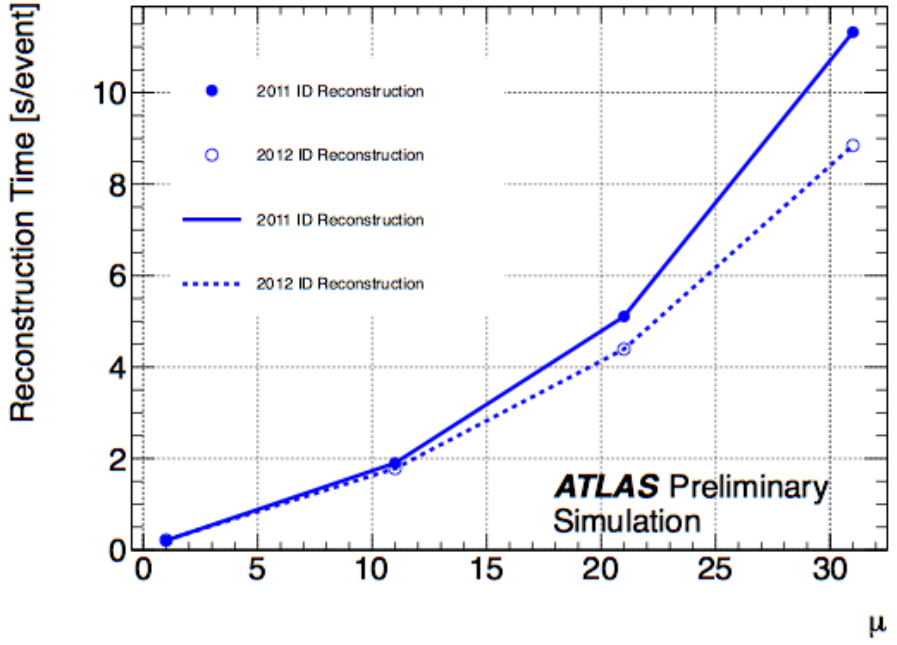
Introduction



- **Efficient and fast tracking is essential for many physics analyses (not covered in this talk)**
- LHC conditions (luminosity, pile-up) have become more and more challenging, and pose a significant challenge to tracking

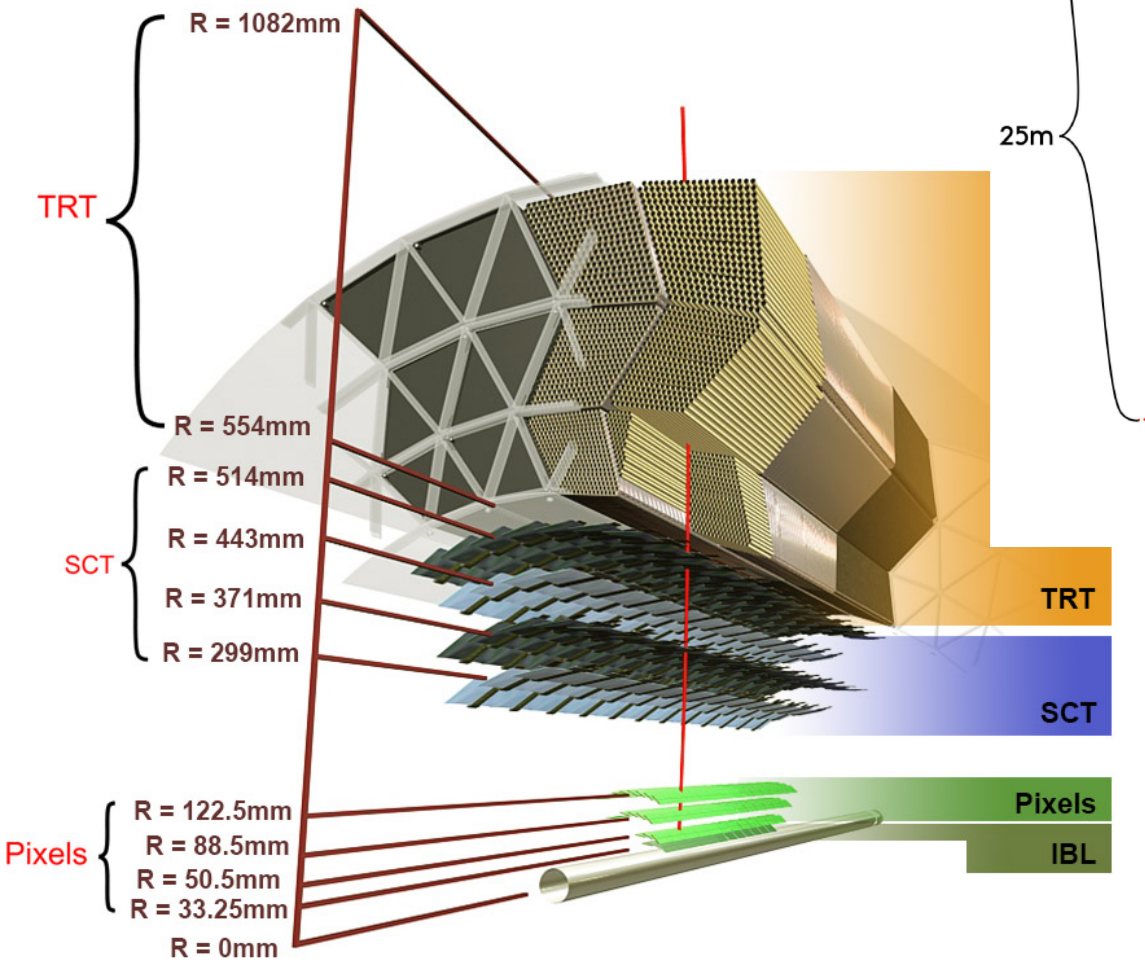


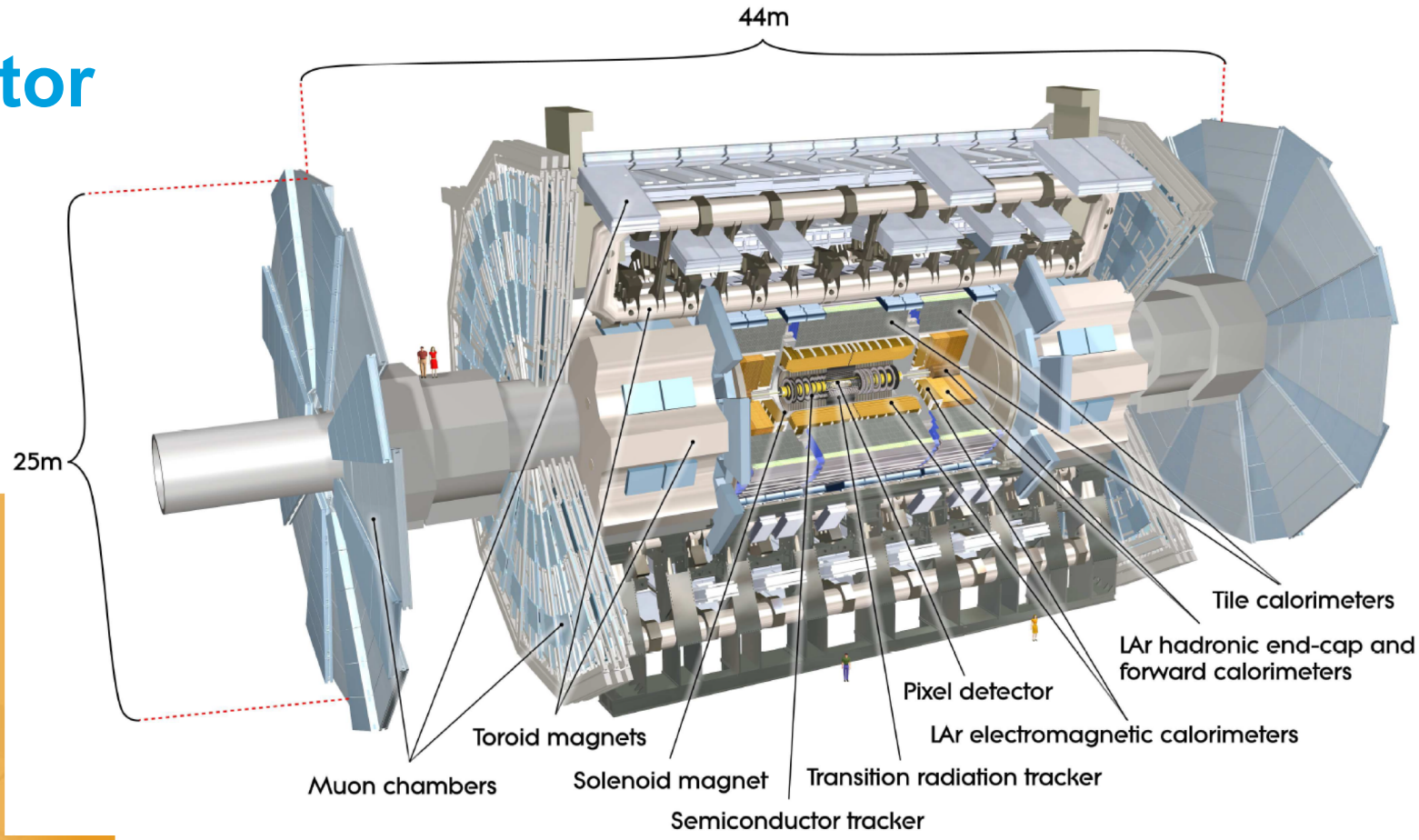
ATLAS-CONF-2012-042



The ATLAS Detector

And its Inner Detector

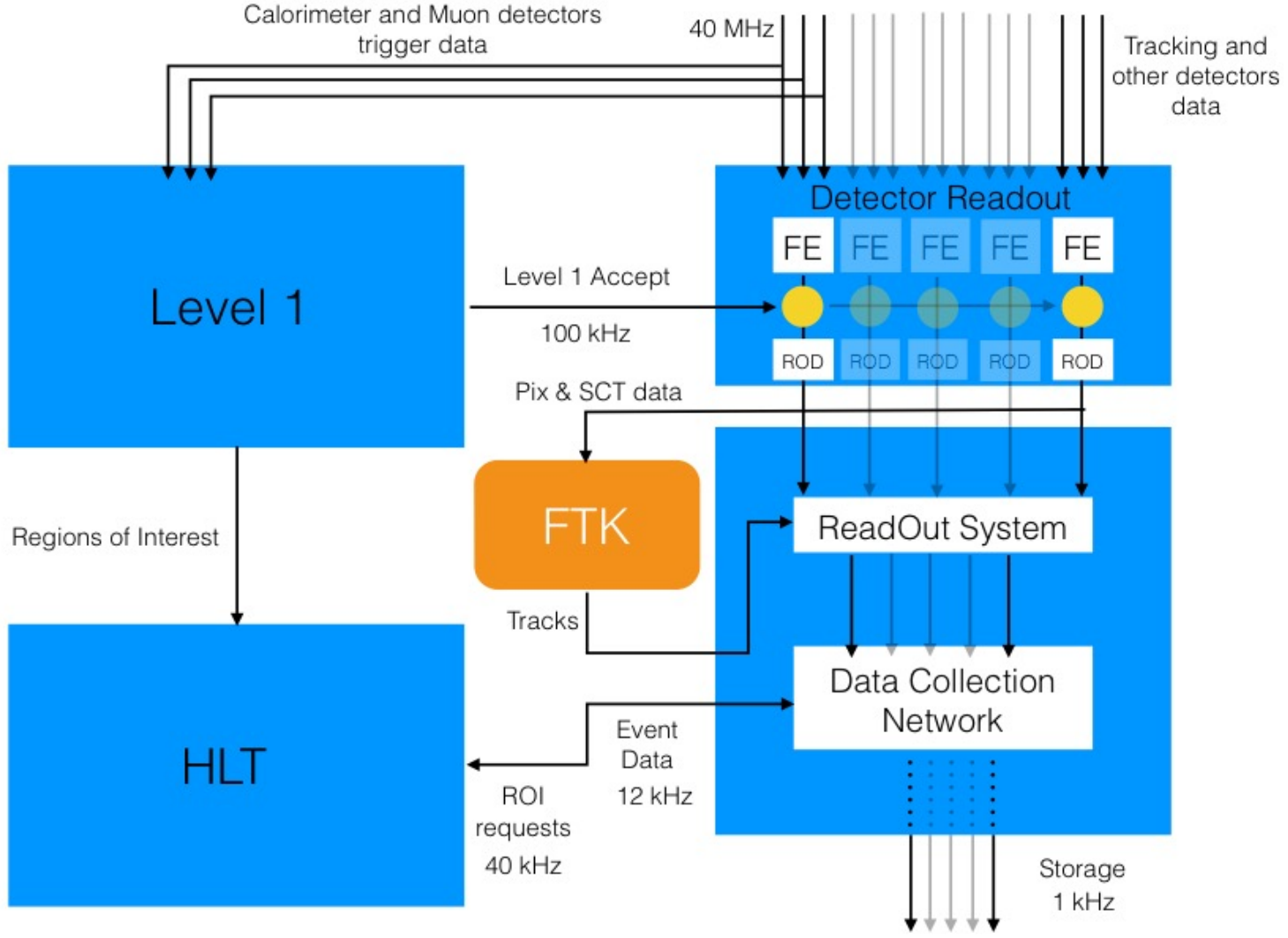




O(100M) channels in ATLAS SCT, Pixel and IBL detectors

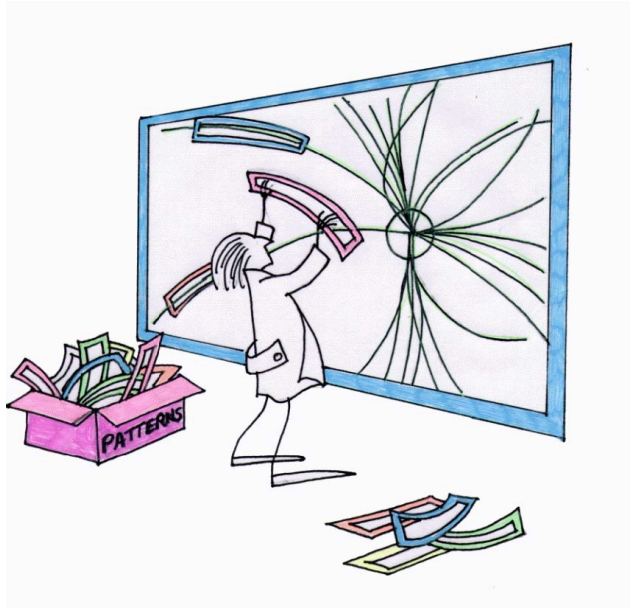
The Fast TracKer (FTK) In ATLAS Data Taking

A hardware-based tracker, input to the High-Level Trigger (HLT)



The Fast TracKer (FTK) In a Nutshell

A hardware-based tracker, input to the High-Level Trigger (HLT)



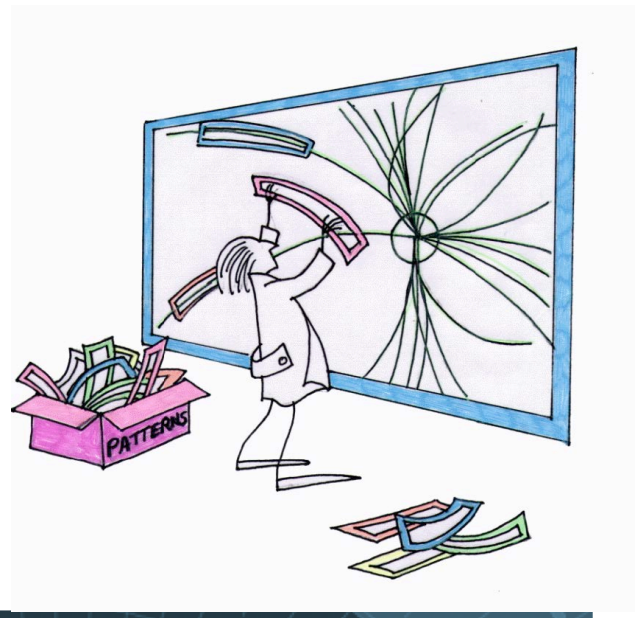
- **Hardware-based tracker, fitting full silicon detector tracks with p_T > 1 GeV, making them available to the High-Level Trigger within O(100 μs)**

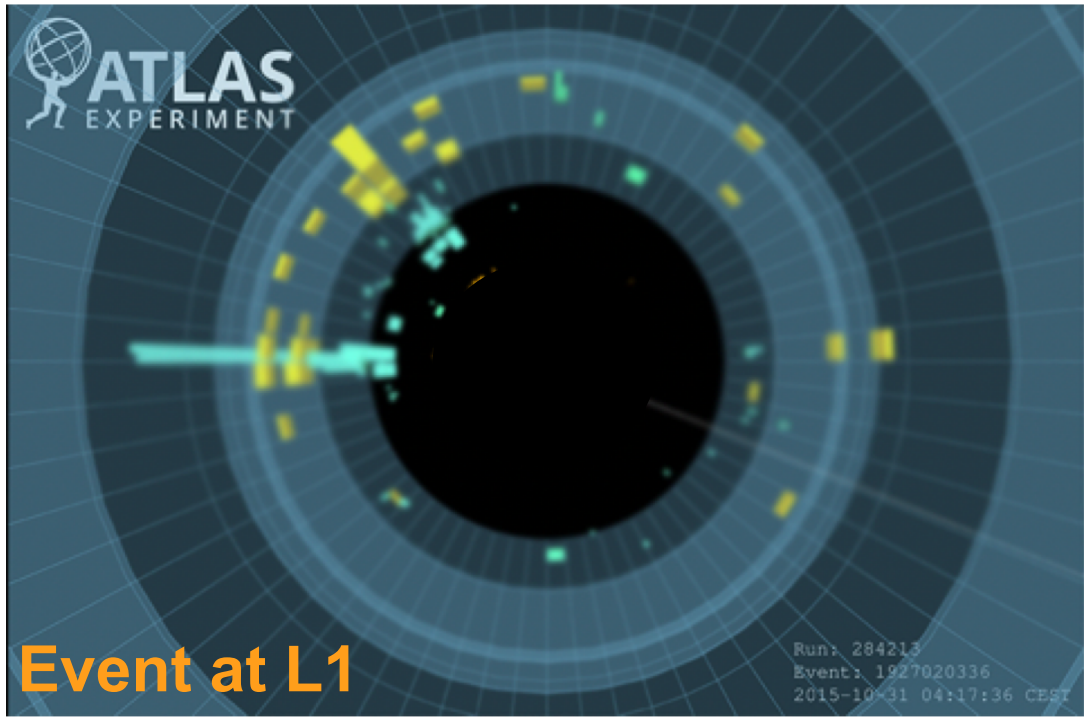
- Massively parallel: 450 boards, 8000 ASICs, 2000 FPGAs and thousands of high-speed I/O links (up to 10 Gbps)

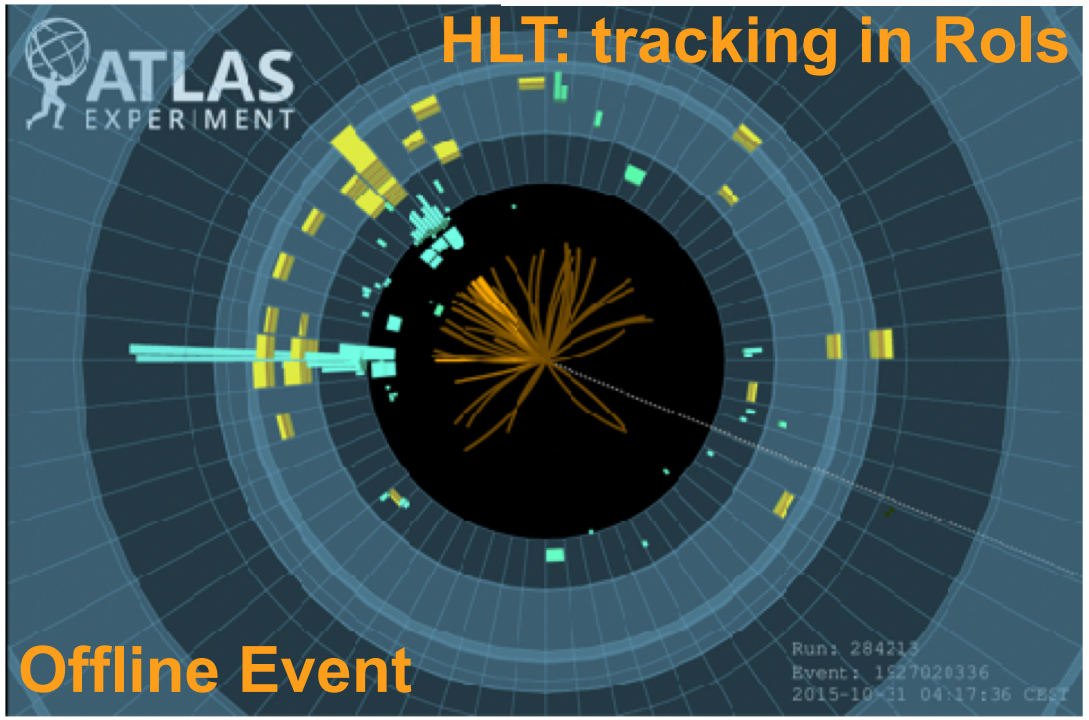
The Fast TracKer (FTK) In a Nutshell

A hardware-based tracker, input to the High-Level Trigger (HLT)

- **Goal: provide HLT with offline-quality tracks**



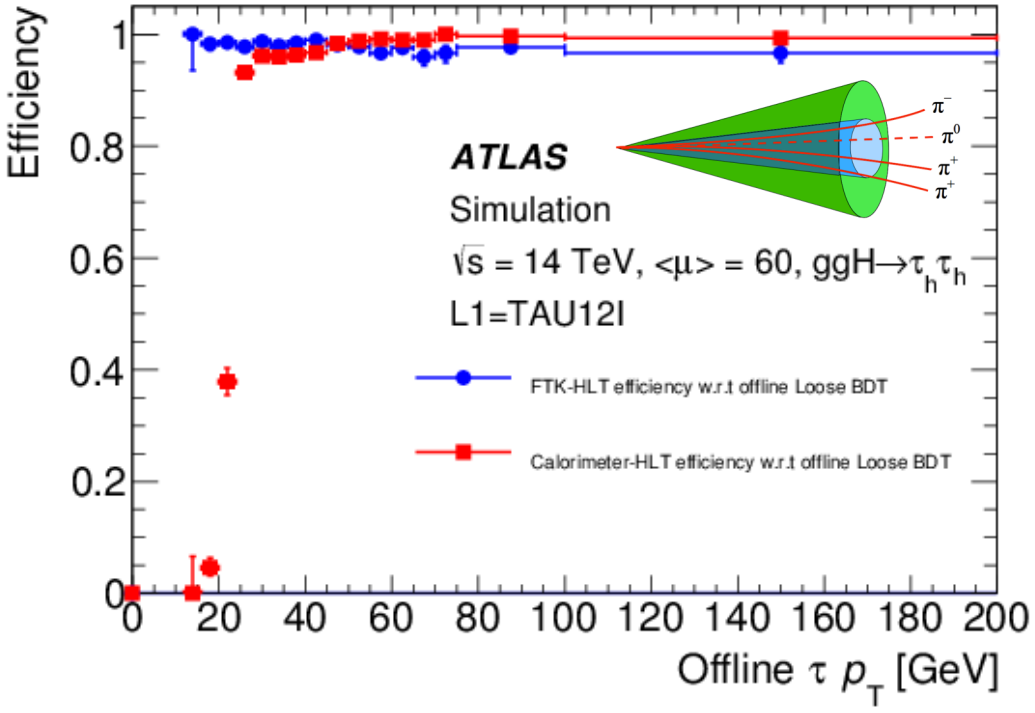


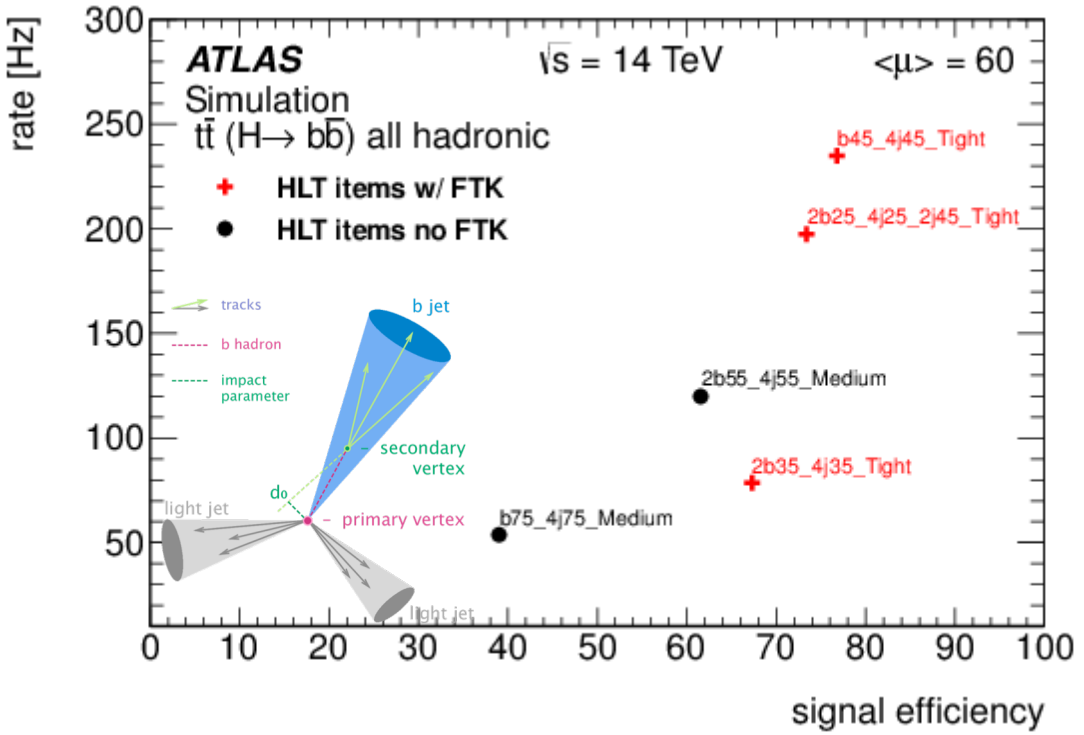


The Fast TracKer (FTK) In a Nutshell

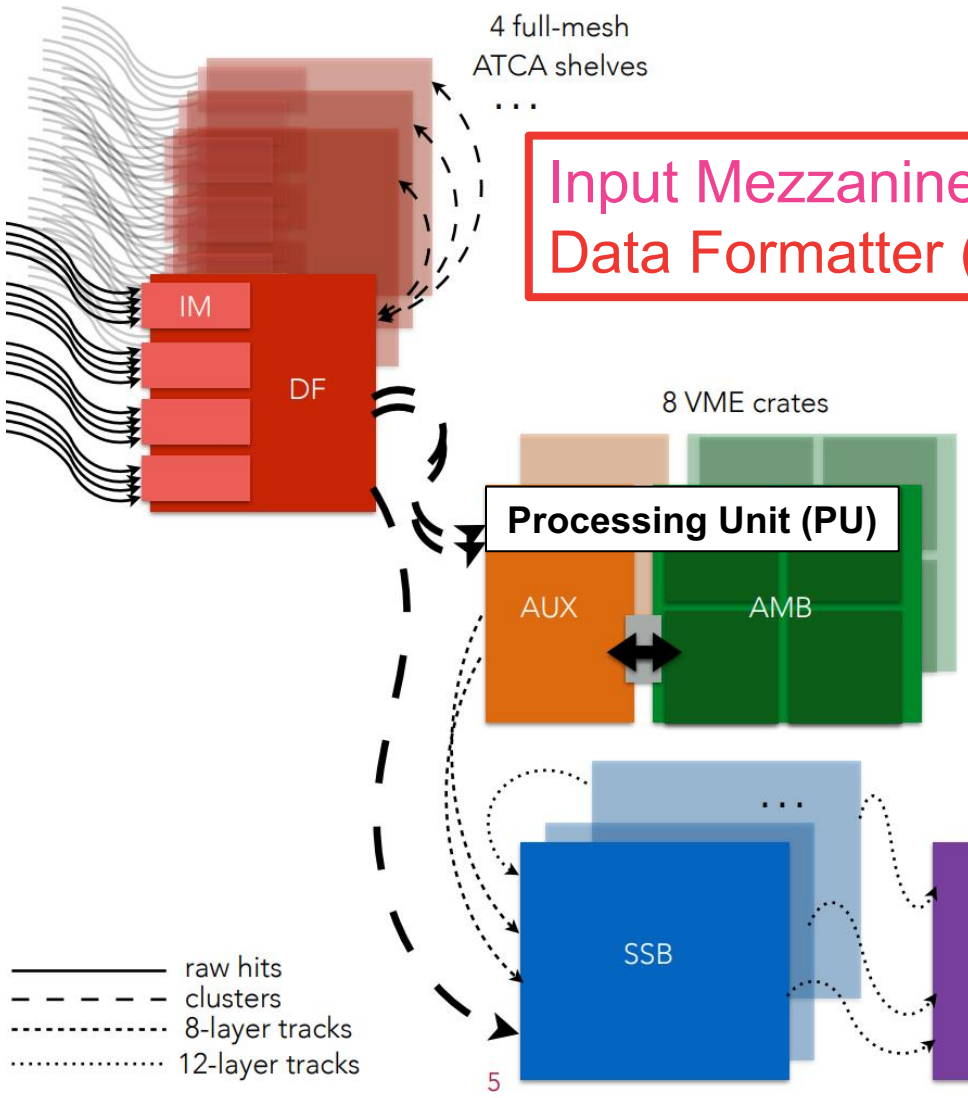
A hardware-based tracker, input to the High-Level Trigger (HLT)

- **Goal: provide HLT with offline-quality tracks, allowing**
  - **reconstructing hadronic taus**
  - **finding displaced tracks and secondary vertices**
  - **for MET & jet corrections, PV reconstruction, beamspot finding, etc.**
  - **Allows developing pile-up resilient triggering strategies**





FTK System Overview



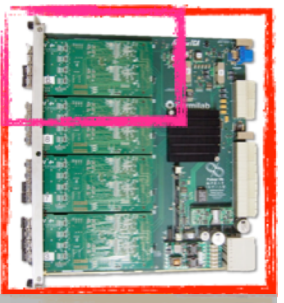
Input Mezzanine (IM): input from ID + hit clustering
Data Formatter (DF): clustering data organisation

Associative Memory Board (AMB): ~instant track road finding

Auxiliary Card (AUX): first-stage fit; 8L(ayers): 3 PIX, 5 SCT

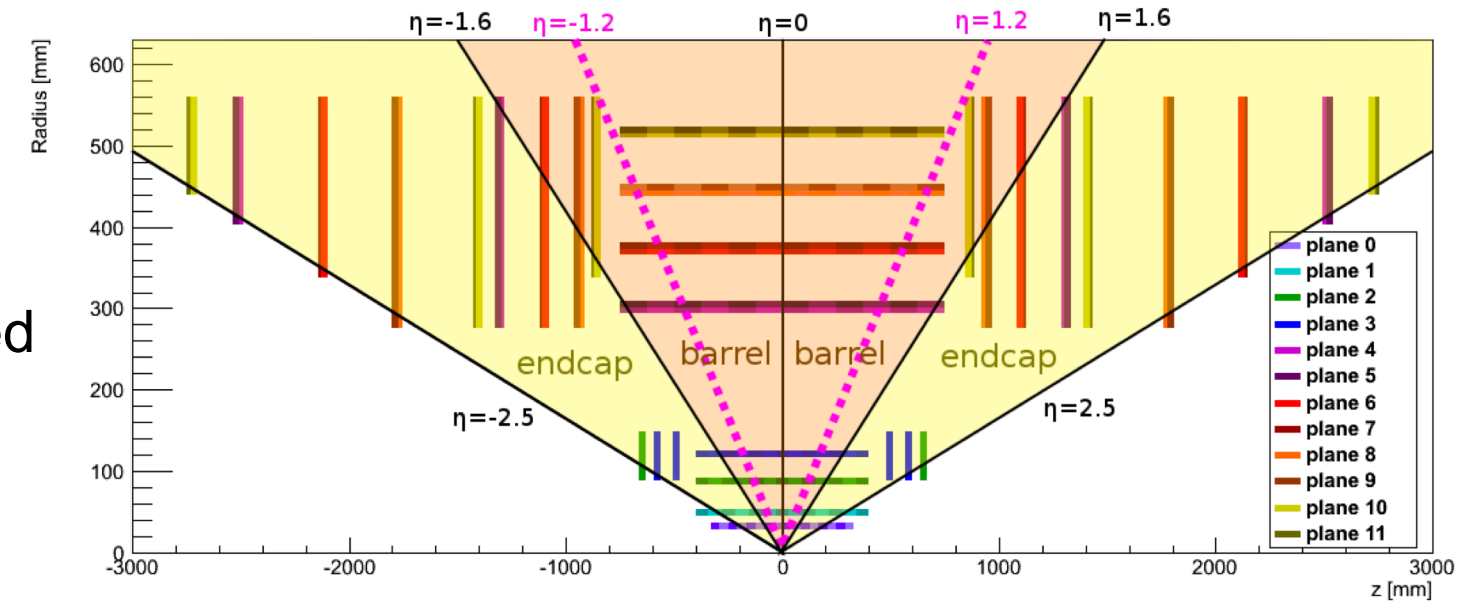
Second Stage Board (SSB): 8L → 12L extrapolation + 12L fit

FTK to Level-2 Interface Card (FLIC): data formatting for HLT

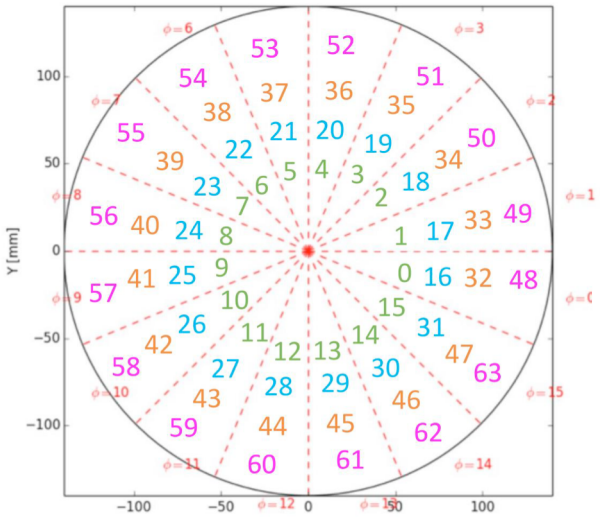


The ID Seen By FTK

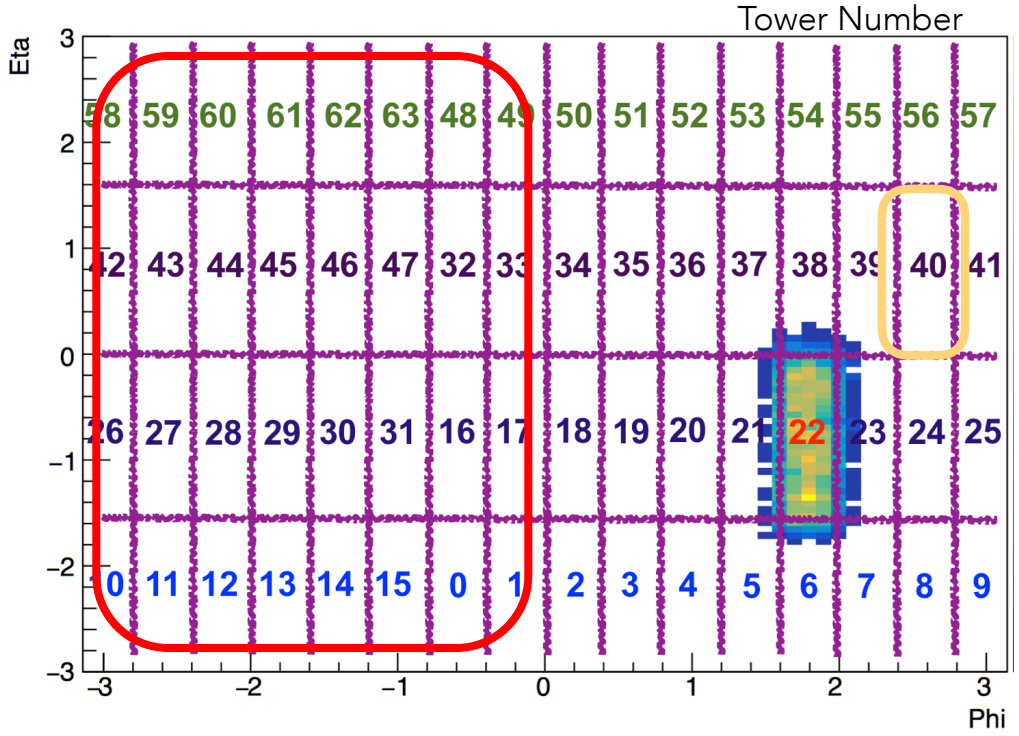
- ID (IBL/Pixel + SCT) mapped into 64 η-φ towers (4x16)

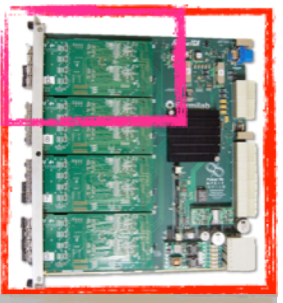


Divide into independent regions that are **processed simultaneously**



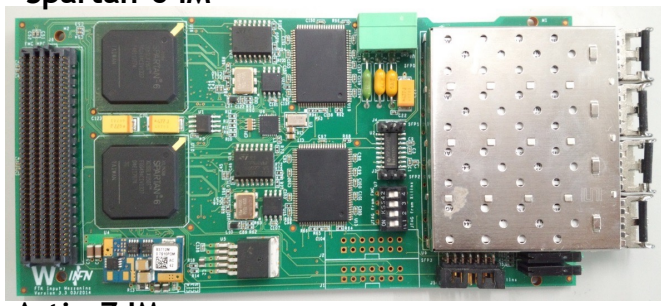
Endcap (η<0: 0-15)
Barrel (η<0: 16-31)
Barrel (η>0: 32-47)
Endcap (η>0: 48-63)



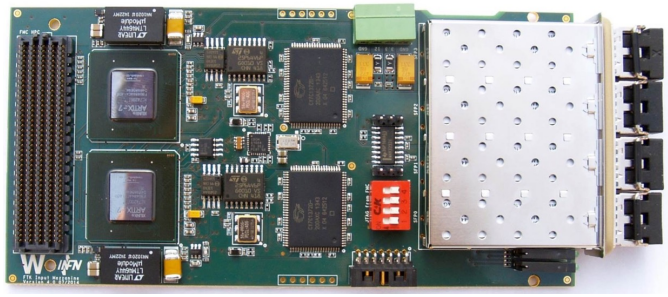


FTK Input Mezzanine and Data Formatter

Spartan-6 IM

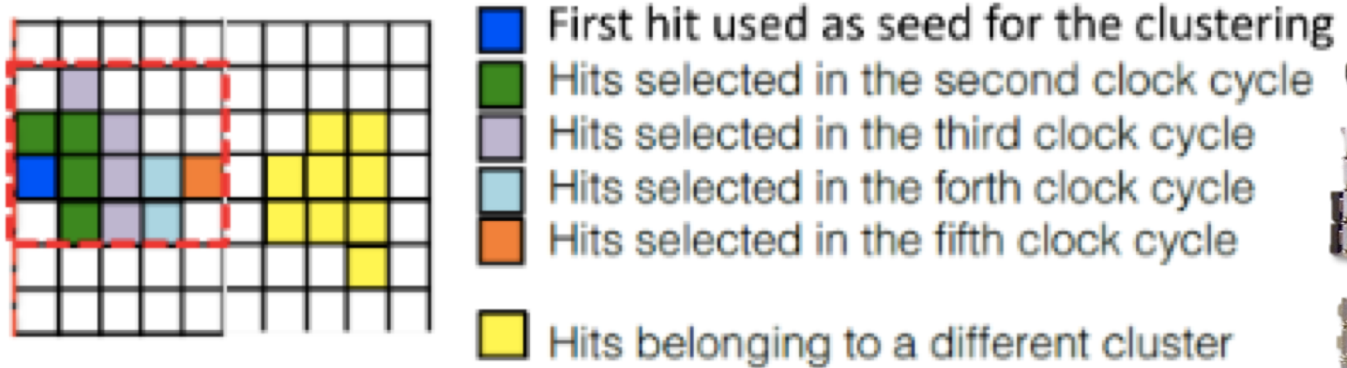


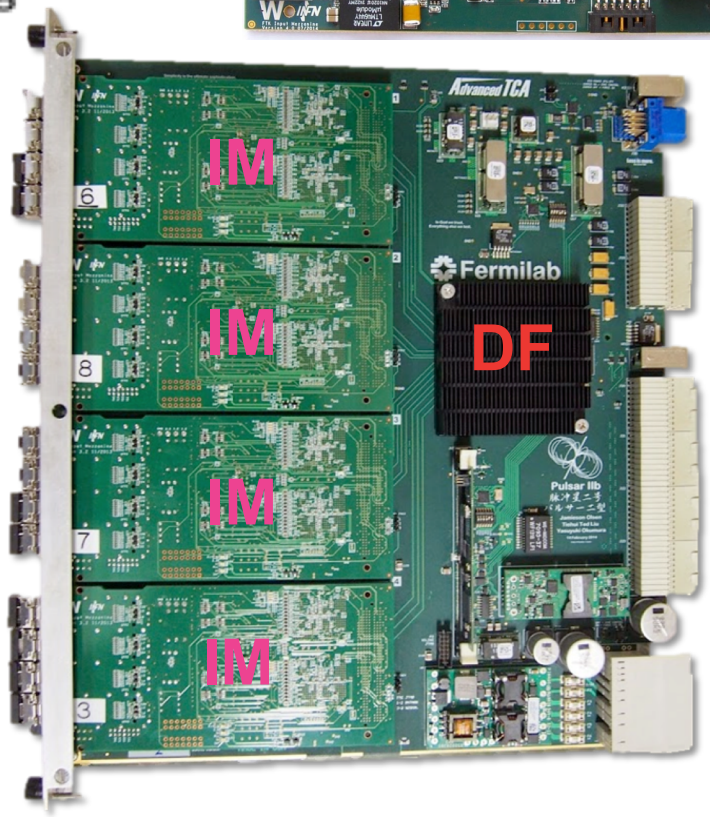
Artix-7 IM



Input Mezzanine (IM)

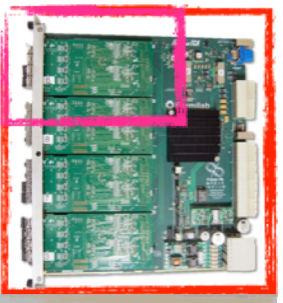
- Handles input from ID and performs clustering
- Can provide pre-loaded events for system tests





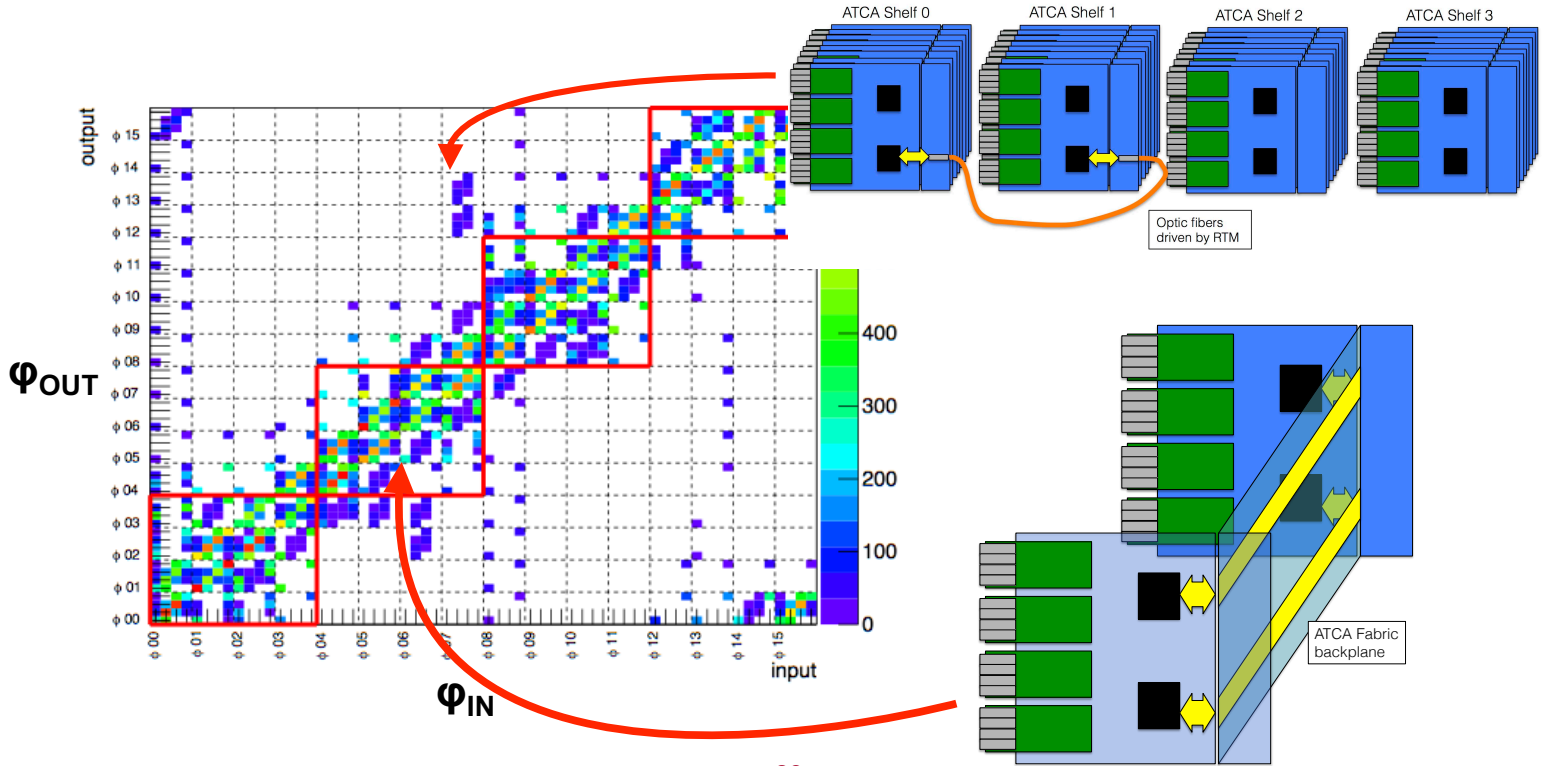
Data Formatter (DF)

- Receives data from IM
- Distributes clusters to FTK towers



FTK Input Mezzanines (IM) and Data Formatters (DF)

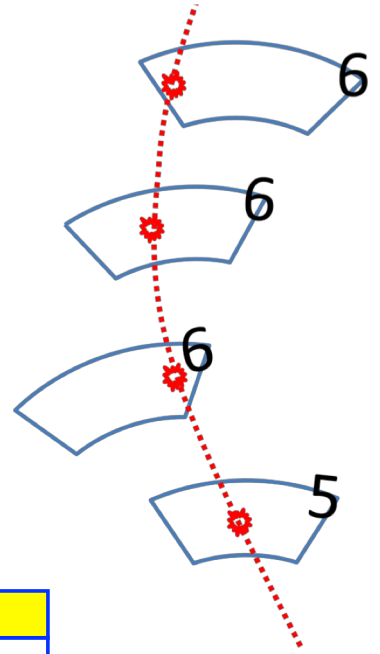
- ID readout per stave (constant r or z), but FTK processes towers in η-φ
  - Inter-DF routes to access the appropriate data
  - Using ATCA backplane (intra-shelf) and fibre links (inter-shelf)



32 DF boards in 4 shelves with full mesh 40 Gbps backplane

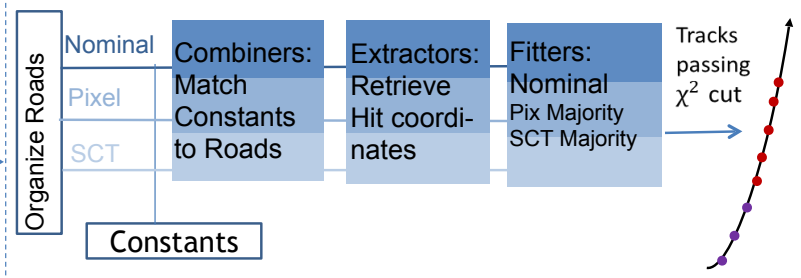
Associative Memory Board (AMB) and Auxiliary Card (AUX)

- Hits are ganged together into coarse resolution hits
- All possible patterns determined from simulation
- Custom associative memory chips are used to **compare hits** to O(10^9) patterns **simultaneously**
- First-stage 8-layer track fitting



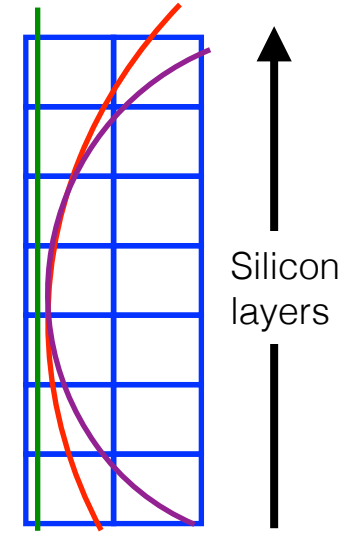
Data Organizer (DO) FW: Associates roads to SS using ext. memory, sends hits to TF

Track Fitter (TF) FW
Allows for 1 missing layer (Pix/SCT majority hit)



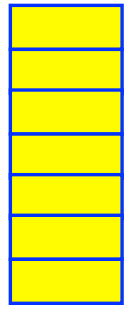
More details in talk by Rui Zou

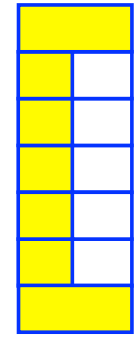
3 types of tracks



Silicon layers

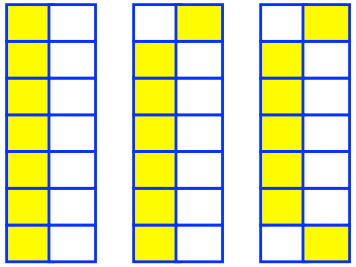
1 wide pattern: more fakes



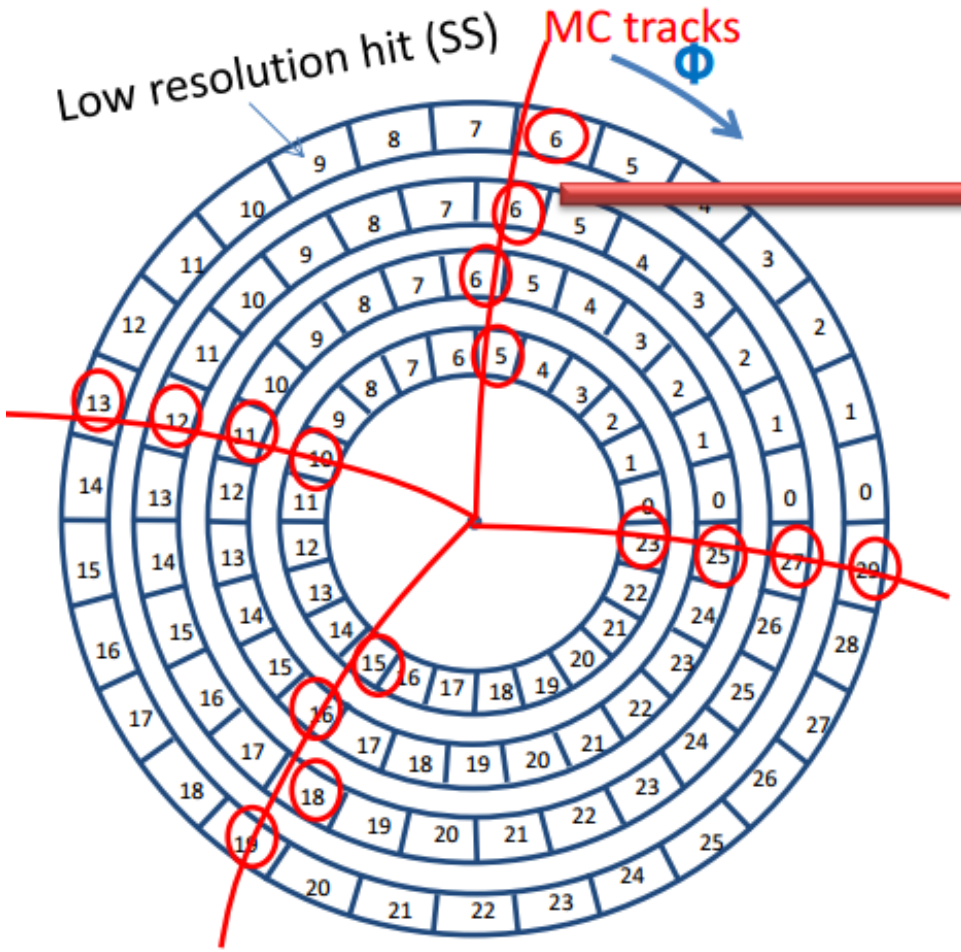


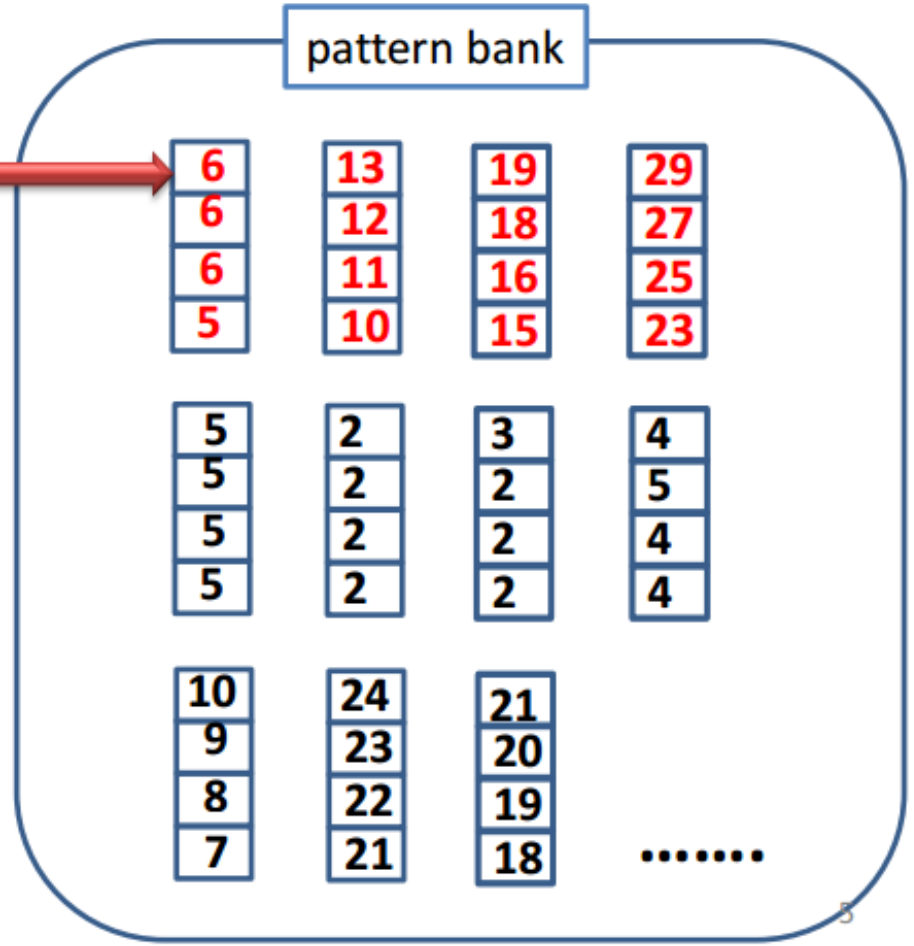
Good tradeoff of efficiency + fake rate using DC bits

3 narrow patterns, need large number for good efficiency

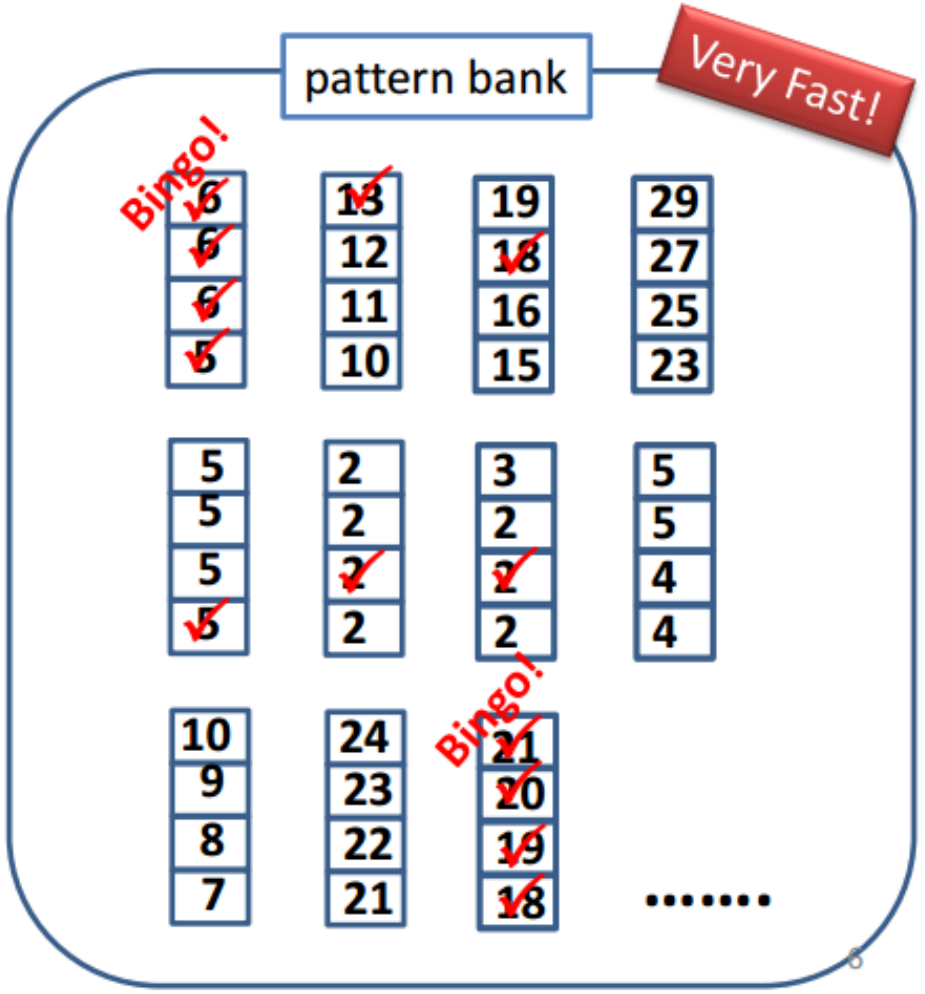


Associative Memory Board (AMB) and Auxiliary Card (AUX)



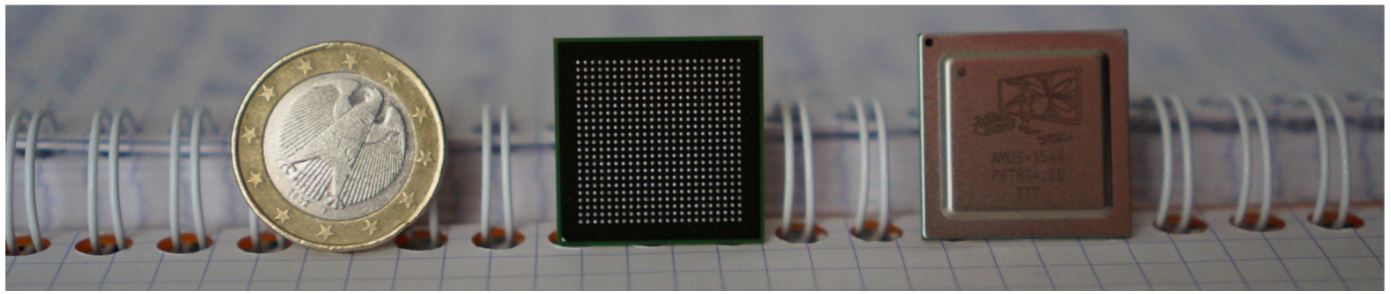


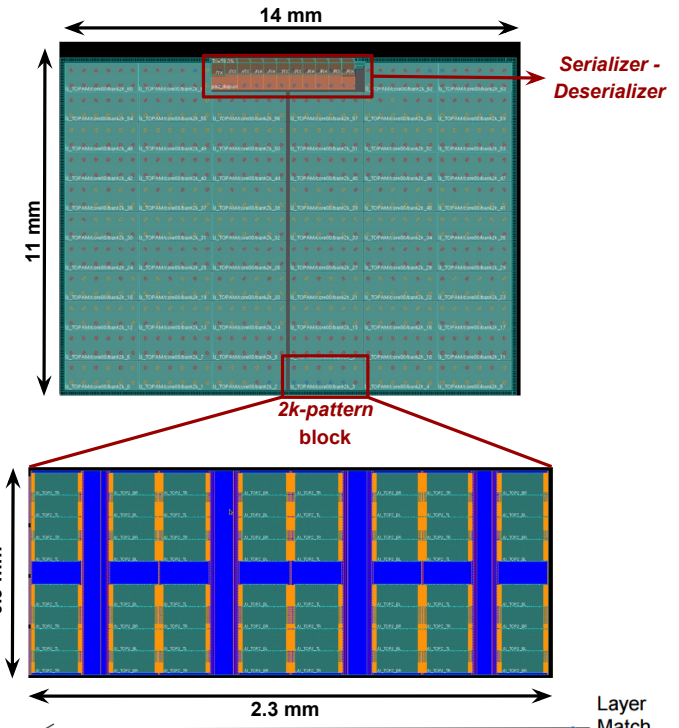
Associative Memory Board (AMB) and Auxiliary Card (AUX)

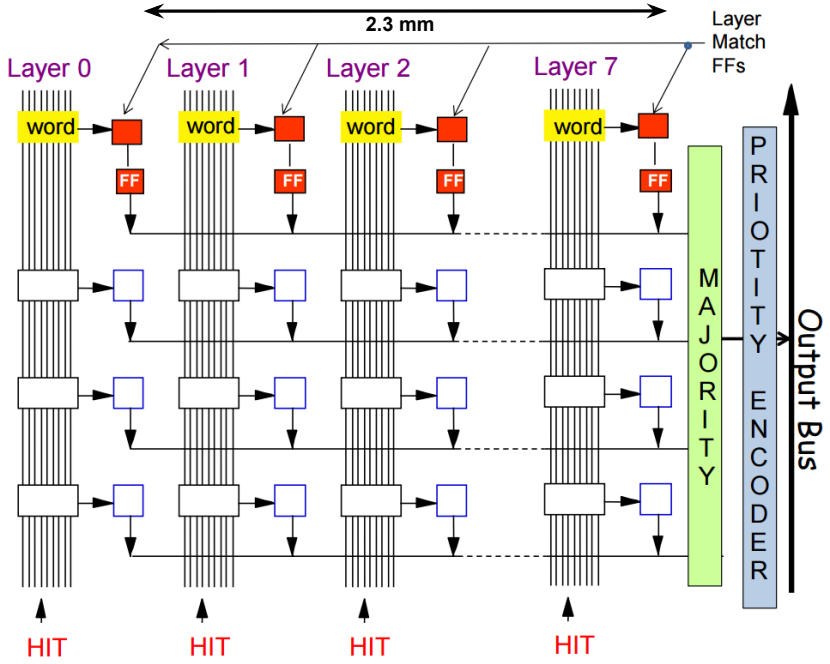


Associative Memory Board (AMB)

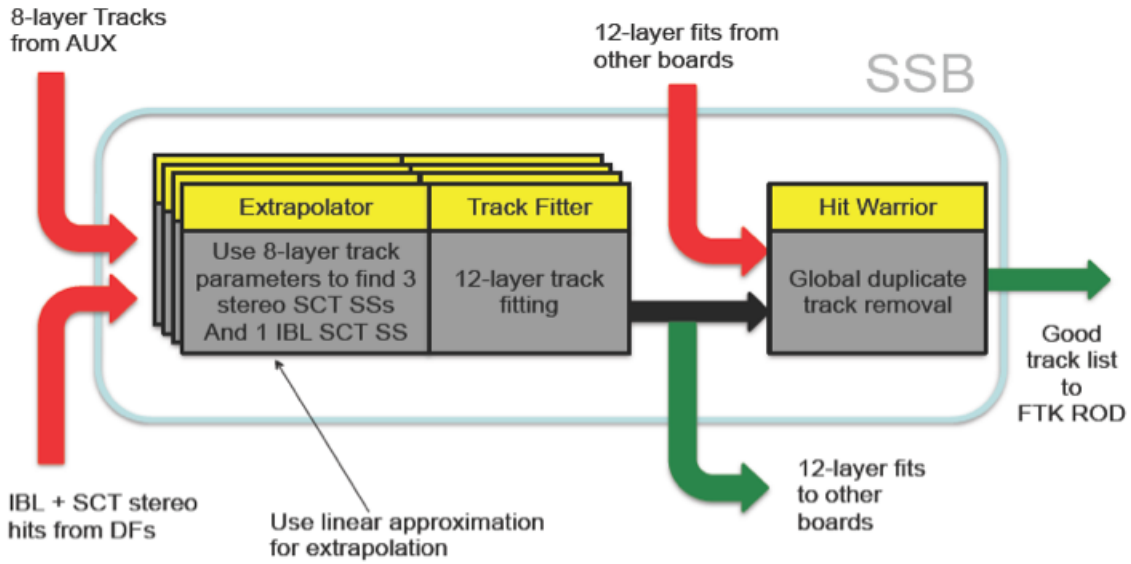
- AM chip is a custom designed ASIC
  - AM06, 65nm technology, largest area ASIC in HEP
- Content Addressable Memory (CAM) with 128 000 patterns / chip (1 billion in system)
- Low voltage (1.2 V) / low power (3 W)
  - Energy usage: 2.3 fJ / comparison / bit
  - Important effort, to minimize heat
- Stores the pre-calculated tracks and makes bit-wise comparisons

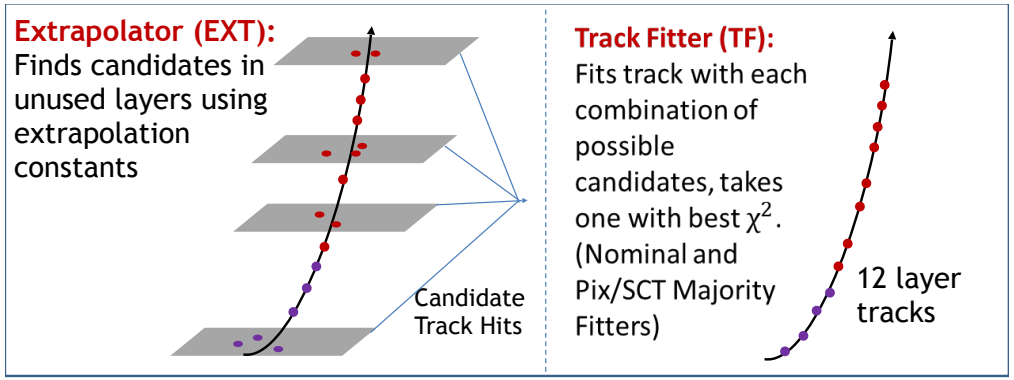






FTK Second Stage Board (SSB)



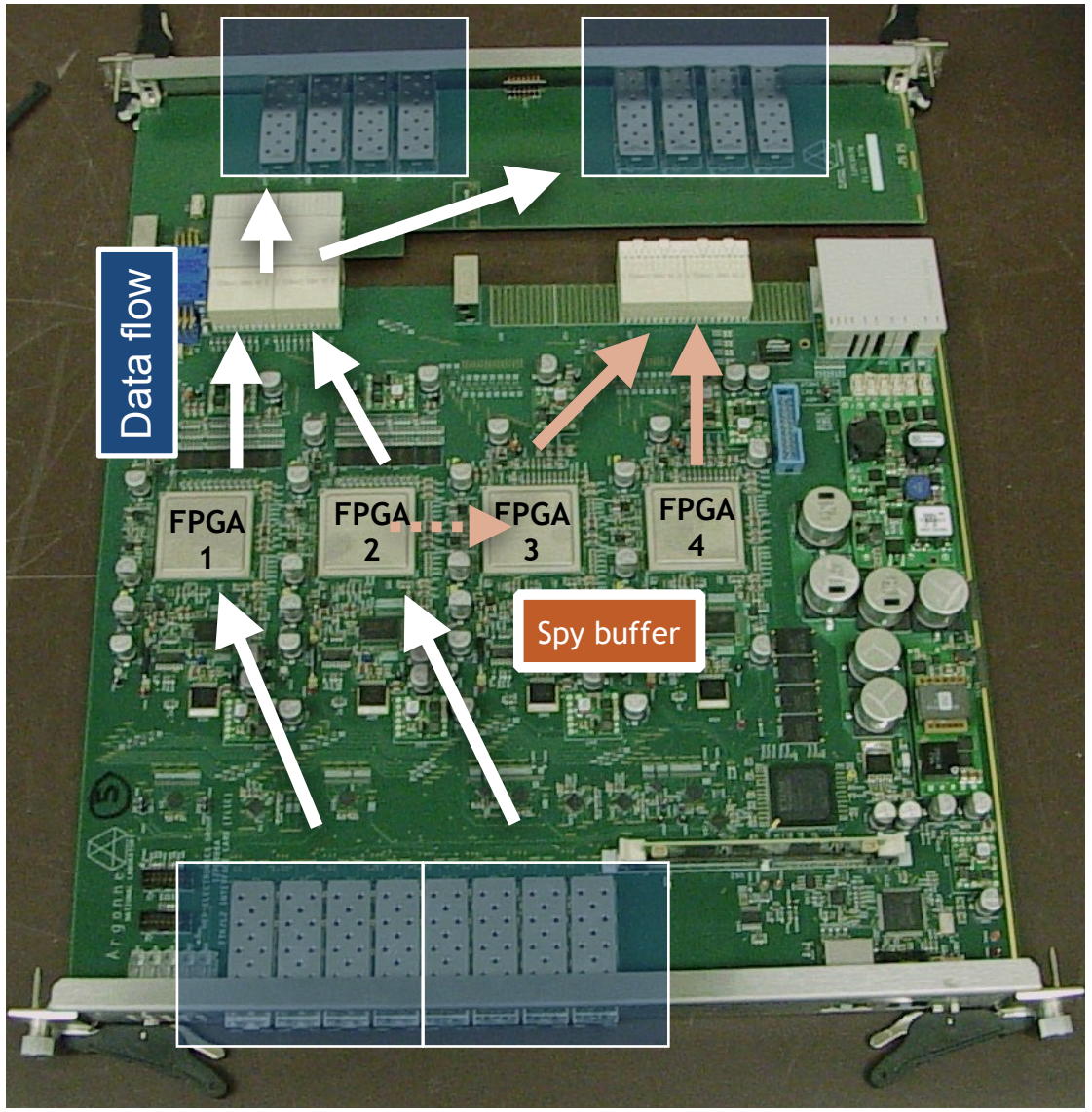


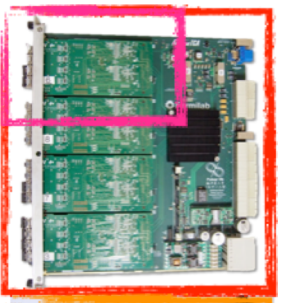
More details in talk by Rui Zou

- Receives 8L data from 4 AUX cards
- Receives IBL and stereo SCT hits from DF (2 towers)
- Extrapolates 8L fits, retrieving candidate hits to use in the 12L track fitting
- Performs 12L fit
- Retrieves intra- and inter-crate SSB 12L tracks, removing duplicates
- Merges FTK data and outputs to FLIC

FTK to Level-2 Interface Card (FLIC)

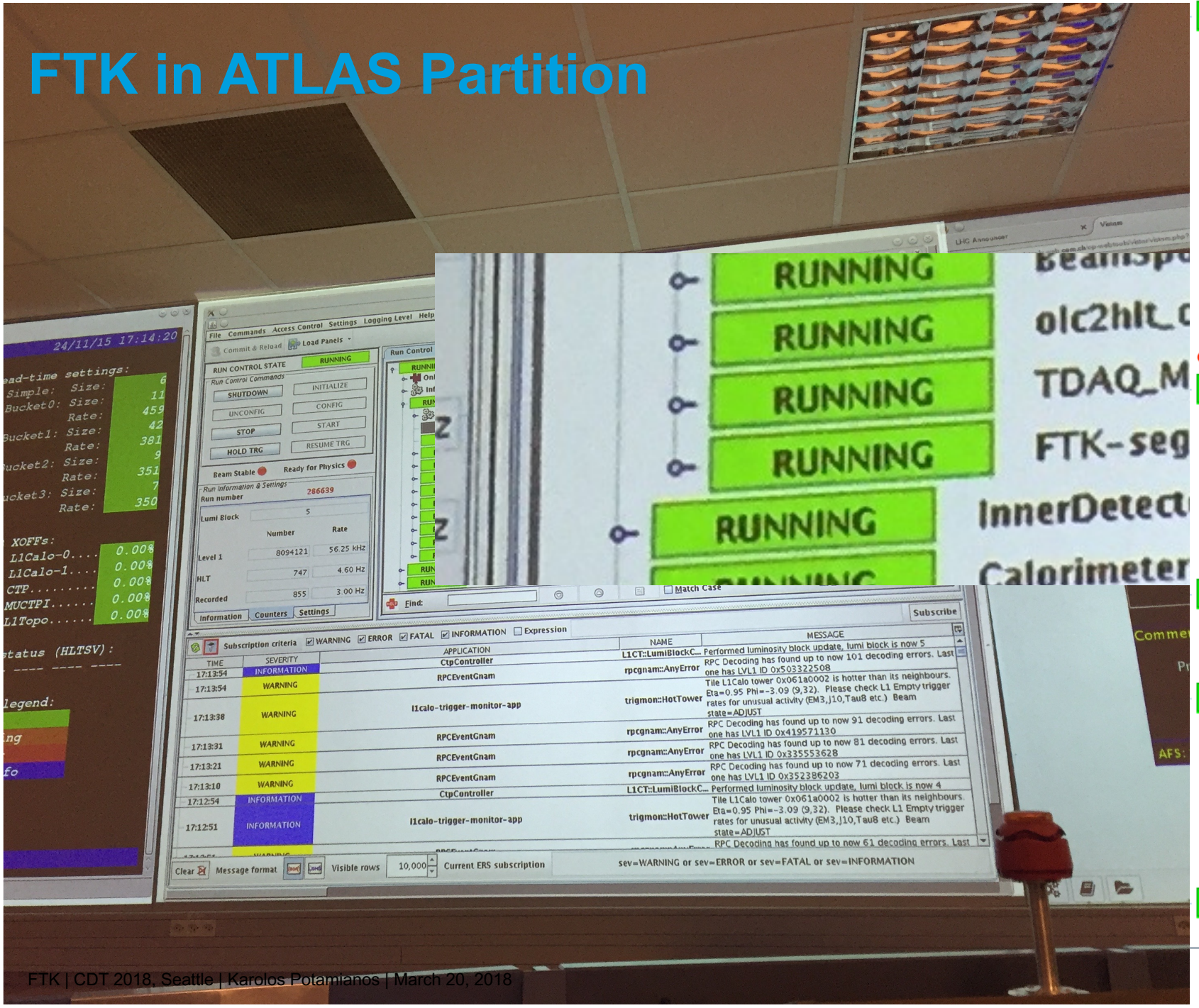
- Receives event records from upstream FTK boards (1/16th of ID per channel)
- Converts FTK identifiers and event records to the ATLAS formats
- Sends records to the HLT and receives backpressure and propagates it to the other FTK boards
- Baseline bandwidth from the FLIC to the FTK: 300 tracks per event @ 100kHz







FTK in ATLAS Partition



RUNNING TDAQ
- Infrastructure
  - UP ddcdtATLAS_ATLGC
  - ABSENT AppOks2Coral
  - RUNNING L1CentralTrigger
  - RUNNING L1Calo
  - RUNNING HLT
  - RUNNING TriggerConfig
  - RUNNING TRP_Segment
  - RUNNING TDAQ_Monitoring
  - RUNNING FTK

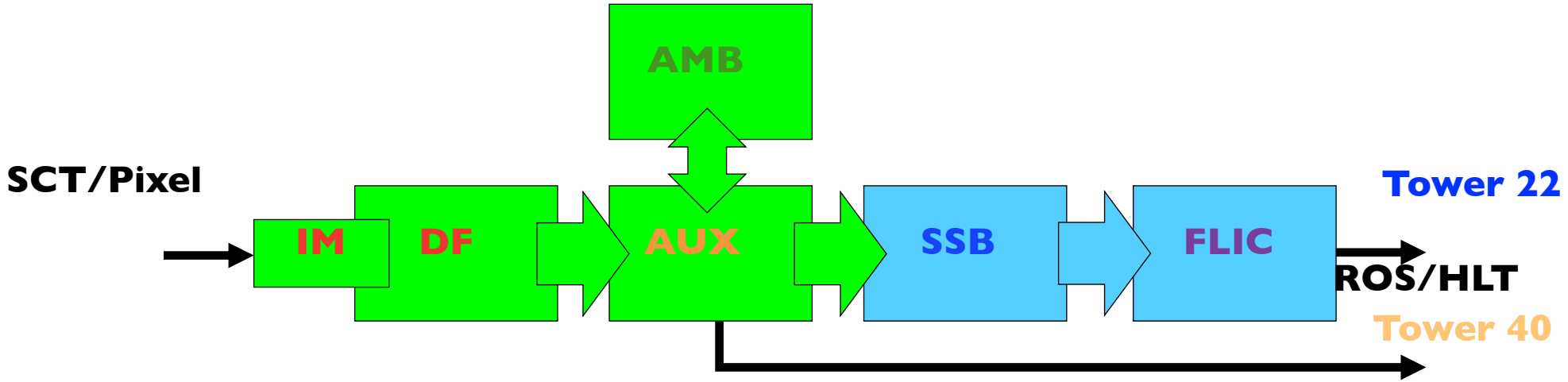
RUNNING InnerDetectors
- Infrastructure
  - RUNNING TRT
  - RUNNING BCM
  - RUNNING Pixel
  - RUNNING SCT

RUNNING Calorimeters
- Infrastructure
  - RUNNING Tile

RUNNING MuonDetectors
- Infrastructure
  - RUNNING CSC
  - RUNNING MDT
  - RUNNING RPC
  - RUNNING TGC

RUNNING ForwardDetectors
- RUNNING LUCID

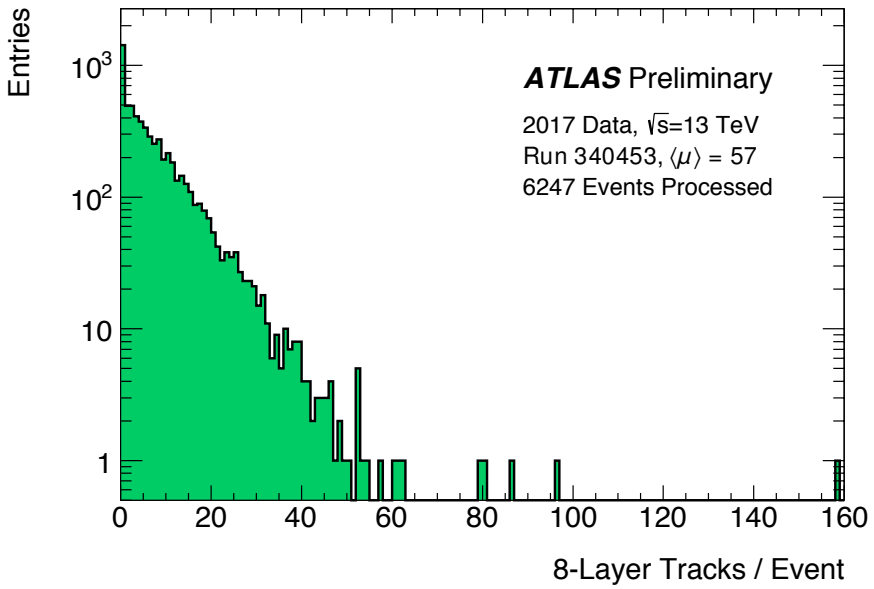
First Data with FTK

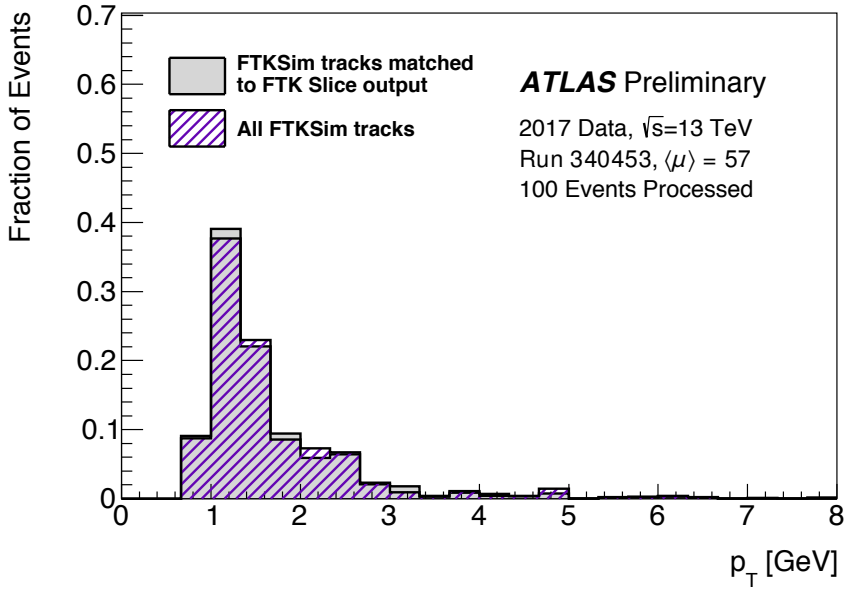


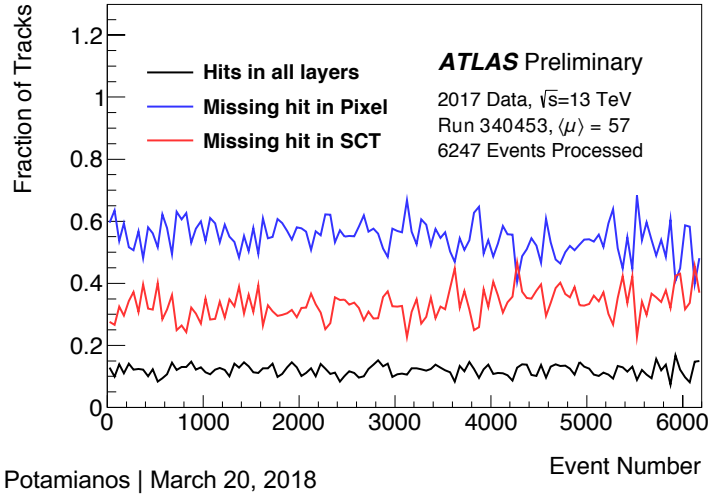
- **Two test configurations:**
  - **AUX → ROS (Tower 40): saving 8-layer tracks to ATLAS stream**
  - **Full slice (Tower 22): saving 12-layer tracks to ATLAS**

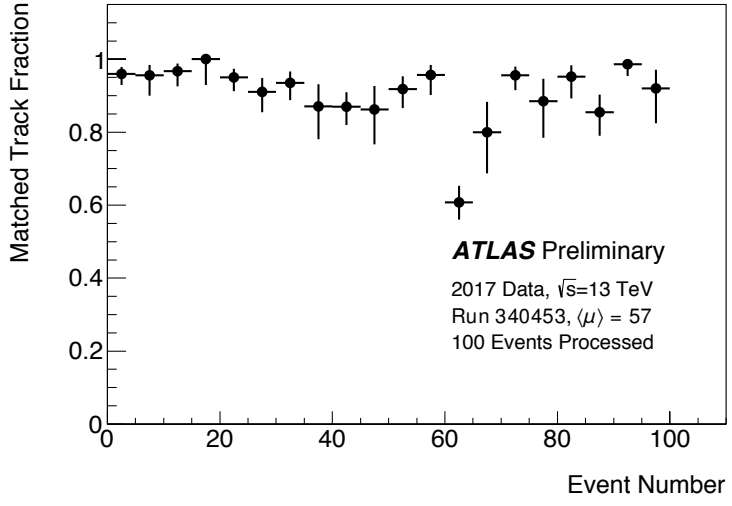
First Data with FTK

13 TeV run, <μ> ~ 60 , data taking with Tower 40 (AMB/AUX)





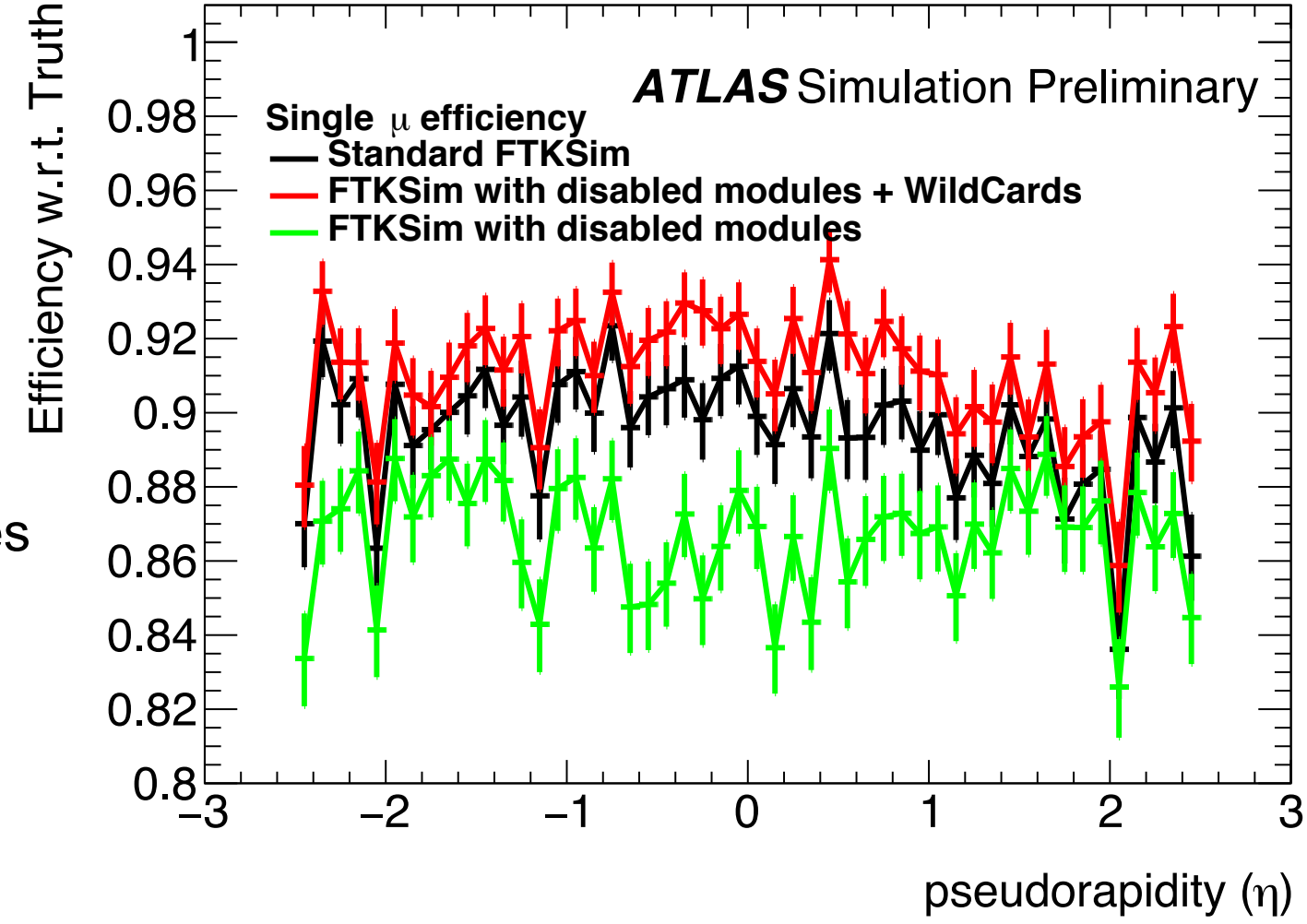




See talk by Stefan Schmitt at CDT/WIT 2017

FTK Software and Pattern Banks

- Continuous improvements to core software
- Using "wildcards" (module mask ON) in patterns to account for disabled modules
  - Updated pattern banks with 2017 disabled modules



FTK-HLT Integration

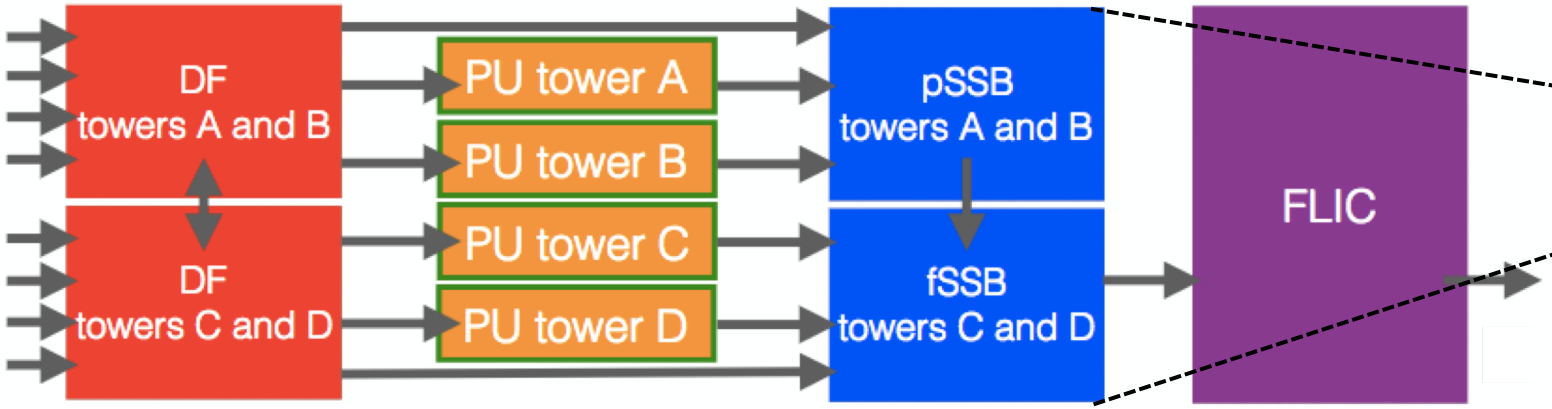
- FTK items being integrated in trigger menu
  - Items for muon, tau, bjet, jet, b-physics, and MET triggers
  - Covering commissioning, performance & physics trigger signatures
  - Currently validated using simulated FTK datasets

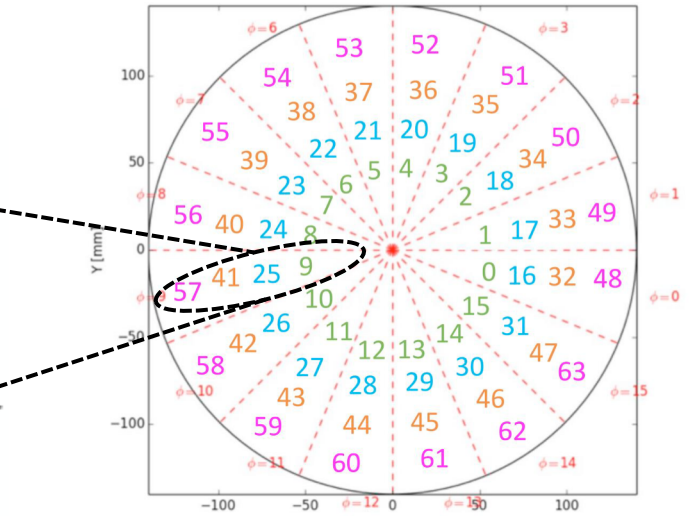
- Plans for 2018
  - Further validation and optimization with simulated data samples
  - Validation of patterns by running with FTK Simulation on data
  - Evaluation of the performance of FTK with FTK data when available

  - **Validate FTK so that HLT can trigger on its output in Run-3**

FTK Run 2 Configuration

- 32 DFs (2 η-adjacent towers: barrel & endcap) send data to 2 AUX, and 1 SSB
- 64 PUs (AUX, AMB) receive data from one tower **(x2 to 128 for Run-3)**
- 32 SSBs receive 2 η-adjacent towers (B&E) from 1 DF and 2 AUX
- 16 FLIC channels total on 2 FLIC boards receive 4 towers each (adjacent in η), and then send their data to the HLT

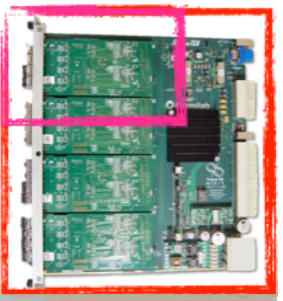




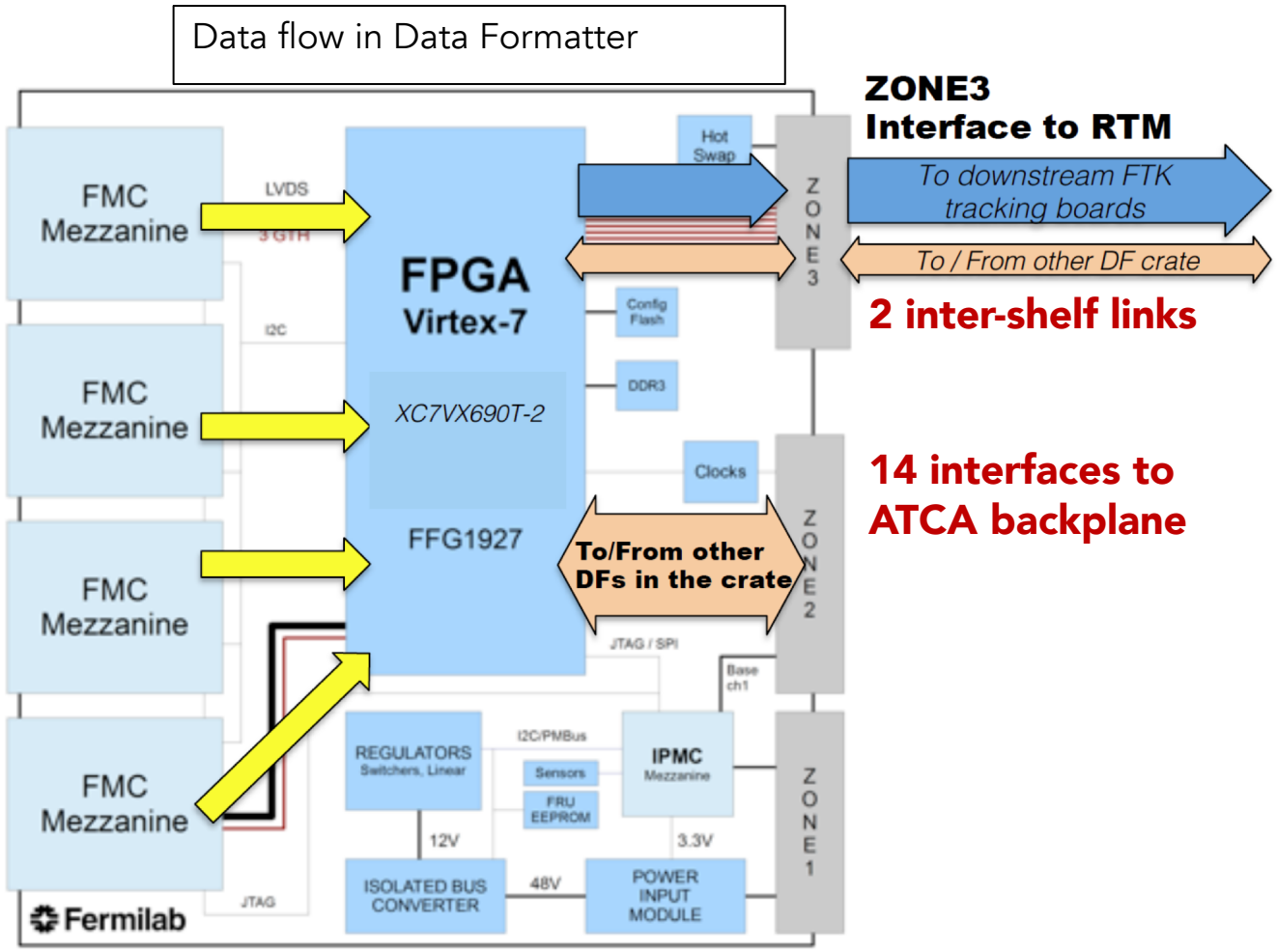
Summary and Outlook

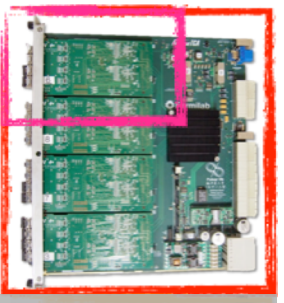
- Continuous development of FTK towards full inclusion in ATLAS
  - Cabling up in progress
  - First 8-layer tracks output to ATLAS in 2017
  - Commissioning FTK with cosmic data until first collisions in 2018
  - Improved simulation of ATLAS data, scaling up to include all boards
- During Long Shutdown 2 (2019-2020) FTK will be further improved for increased capabilities for LHC Run-3, when FTK will be used to trigger!
- Looking forward to collecting more data in 2018 and to providing input to the HLT (to be used for validation)

ADDITIONAL MATERIAL

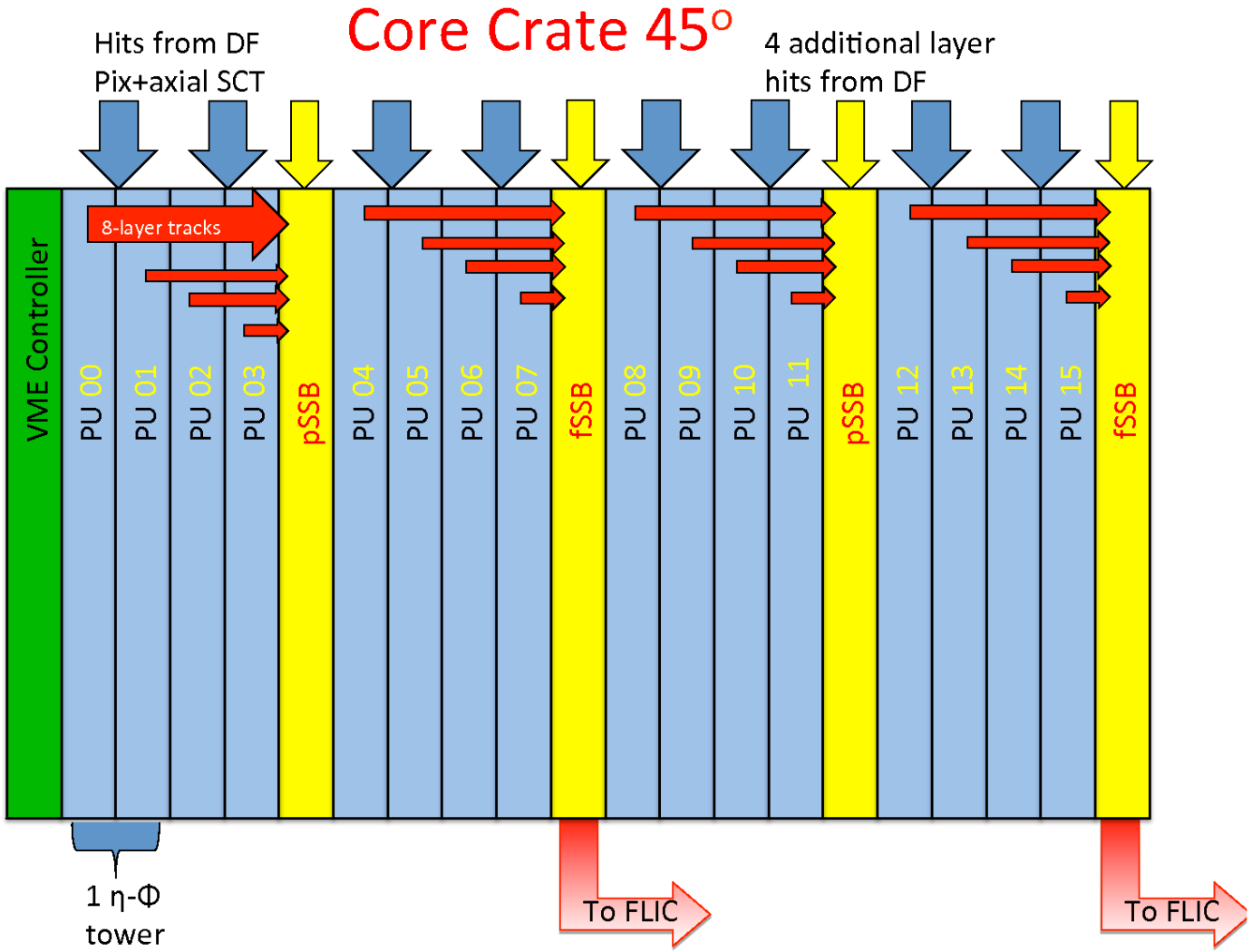


FTK Input Mezzanines (IM) and Data Formatters (DF)





FTK Input Mezzanines (IM) and Data Formatters (DF)



FTK Run-3 Configuration

~8000 ASICS

~2000 FPGAs

Thousands of I/O links

@ up to 10 Gbps