RD53 status and plans.

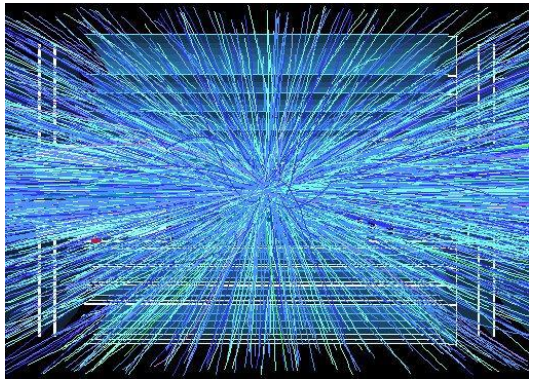
Pixel readout integrated circuits for extreme rate and radiation

4th LHCC status report

Jorgen Christiansen and Maurice Garcia-Sciveres on behalf of RD53

RD53 Introduction and history

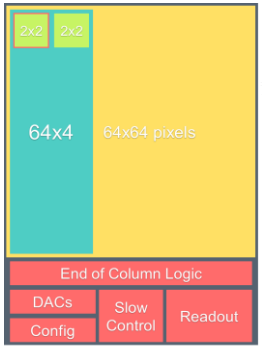
- Focussed R&D developing pixel chips for ATLAS/CMS upgrades
  - Baseline technology: 65nm CMOS
- Extremely challenging requirements for HL-LHC:
  - Small pixels: 50x50um^2 (25x100um^2) and larger pixels
  - Large chips: ~2cm x 2cm (~1 billion transistors)
  - Hit rates: 3 GHz/cm^2
  - Radiation: 1Grad, 2 10^{16} neu/cm^2 over 10 years (unprecedented)
  - Trigger: 1MHz, 10us (~100x buffering and readout)
  - Powering: Serial Powering

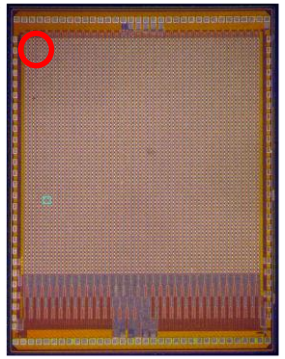


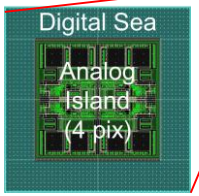
- Developed and tested many test structures, building blocks and small pixel arrays
  - Extensive radiation testing to determine how best to obtain sufficient radiation hardness
- Developed design, simulation and verification framework
  - Architecture development and optimization, Extensive verification of complicated and expensive chip
- **Last year**: Full scale demonstrator pixel chip: RD53A. Major milestone
- **Future**: Propose development of ATLAs and CMS pixel chips in RD53
- 18 collaborating institutes and many Guests
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, RAL, Seville, Torino,
  - 162 on collaboration Email list,
    103 on RD53 guests list (ATLAS/CMS people involved in phase 2 pixel but not on chip design)
    89 on RD53 NDA list (65nm TSMC technology access),
    81 on serial power list (ATLAS/CMS people interested/working on serial powering)
    34 on RD53A core design team
    108 on RD53A testing mailing list
  - ~12 PHDs, ~80 conference/workshop/ publications presentations

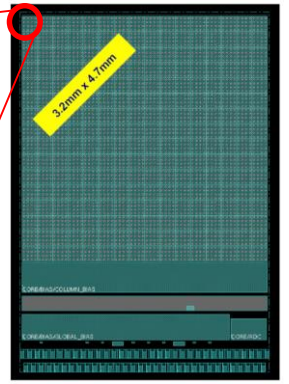
Submitted test chips

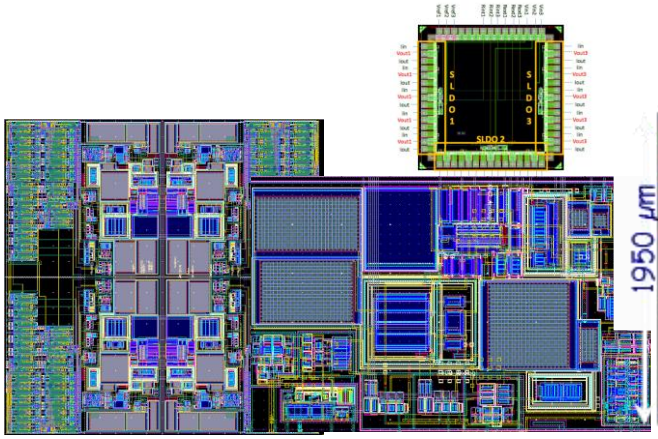
- Design, submission, functional/performance test, radiation test of many different circuits
  - Building blocks (optimized for radiation)
    - 4 different analog front-ends, DACs, ADCs, Analog buffer, PLL, Biasing, Shunt-LDO, Differential IO, Serializer, Cable driver, Power-on reset,
  - Radiation test structures:
    - Transistor arrays, Analog Circuits, Digital libraries (small transistors)
  - Two small scale (64x64) pixel arrays: FE65-P2, CHIPIX65
    - 3 different FEs
    - Analog islands (4 channel quad) in digital sea with shielding
    - Two different latency buffering architectures: Fully functional
    - Demonstrated good analog performance and radiation tolerance
- Given extensive experience to our community on 65nm technology, design tools, design repositories, testing, radiation tolerance, etc.
- Foundation for building large complex rad hard ICs

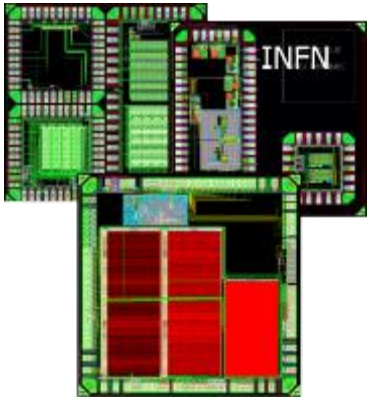


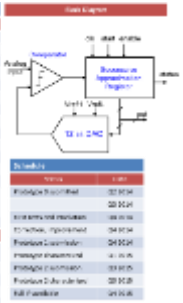








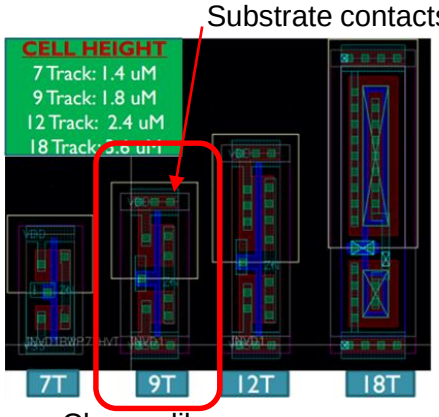




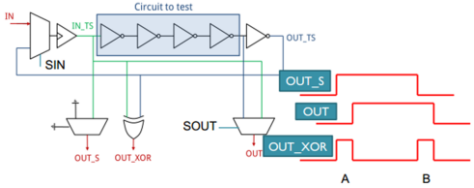
Radiation tolerance

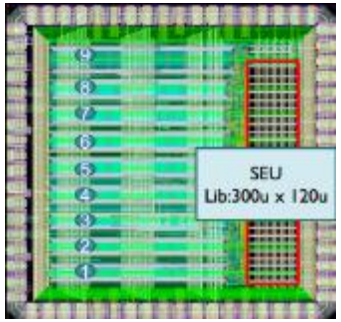
- Radiation test and qualification of 65nm technology: 1Grad and 2 10^{16} neu/cm^2
  - Radiation tests with X-rays, Cobalt source and 3Mev protons
- Significant radiation damage above ~100Mrad (only critical for pixels)
  - New radiation effects made it difficult to reach clear conclusions
- Two major “effects”
  - Radiation damage (transconductance) during radiation depends on: Device type, L, W, Bias, Temperature
  - Annealing effects depends on: Temperature, Time, Bias, Device type, L, W, Received dose
    Partial recovery (transconductance) or getting worse (V_t shift)
  - (Low dose rate effect seen. Requires long term low dose rate radiation tests)
- Realistic to stand 500Mrad with conservative design approach
  - Cold detector: -20 ^oC, Not getting hotter than room temperature while powered for limited periods
  - Analog: Appropriately designed (large transistors) will only have small radiation degradation
    - Confirmed with multiple RD53 prototypes
  - **Digital: Speed degradation when using small transistors**
    - High density logic in pixel array could have significant speed degradation.
      Only needs 40MHz operation frequency.
      High/moderate density digital library for pixel array (small modifications of TSMC lib)
    - High speed circuits designed with large transistors (high speed serializer)
    - Leakage NOT a problem in 65nm (is the case for 130nm).
    - Verified with dedicated digital radiation test chip (DRAD)
  - Inner barrel layer can be replaced after 5 years
- Conservative 200/500Mrad simulation models for circuit simulations and optimizations
- RD53A demonstrator will determine if 1Grad can be accomplished

Digital speed degradation

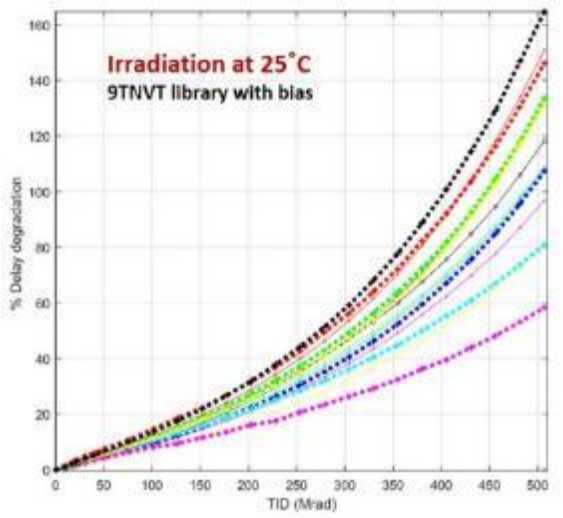


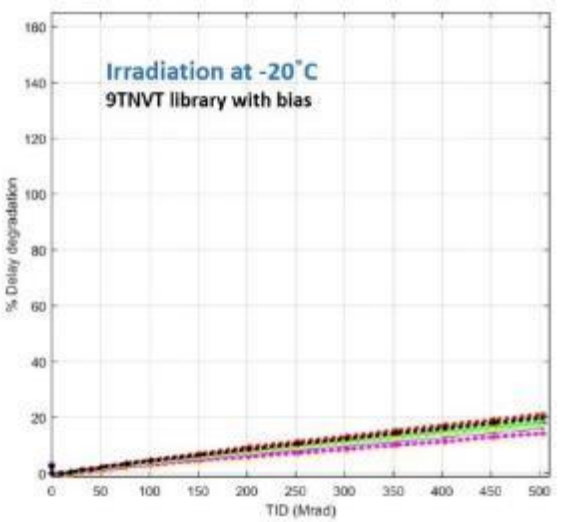
Chosen library

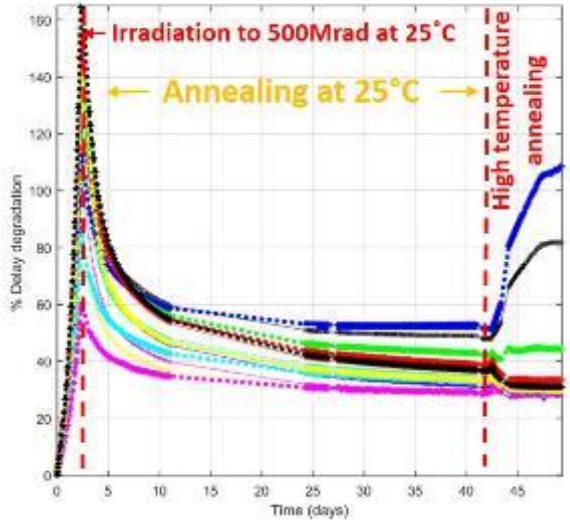


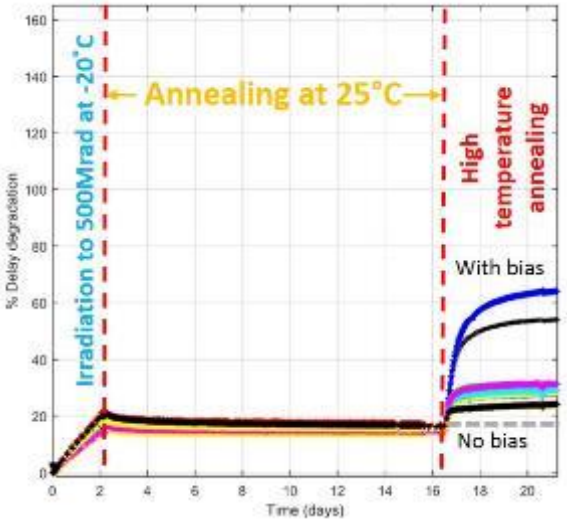


1. 7T-HVt
2. 9T
3. 9T-HVt
4. 9T-incr
5. 12T
6. 12T-LVt
7. 12T-HVt
8. 12T incr
9. 18T-ELT

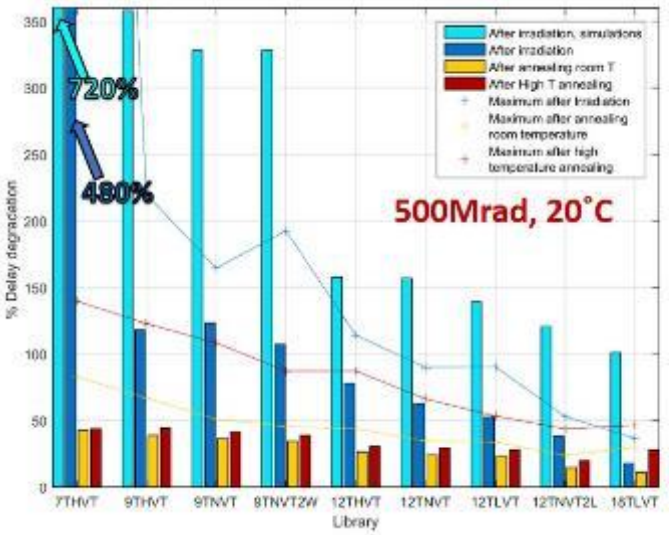


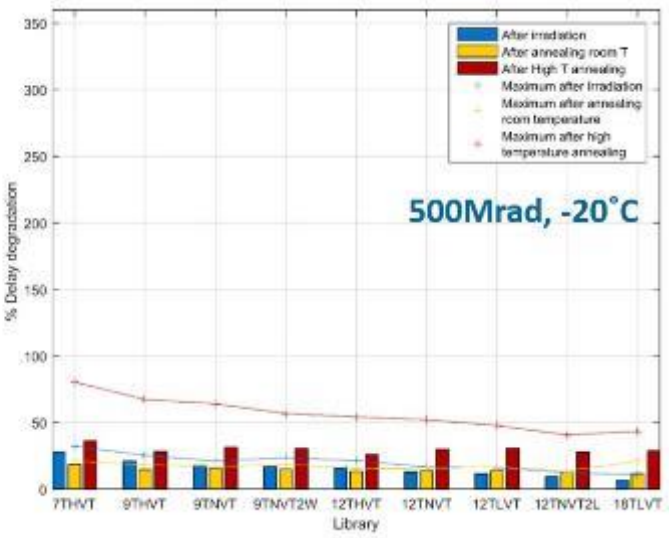


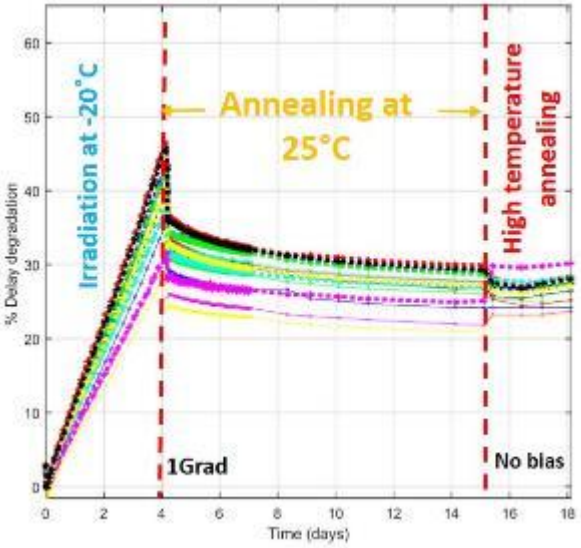


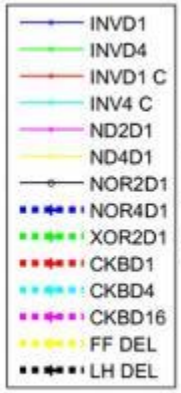


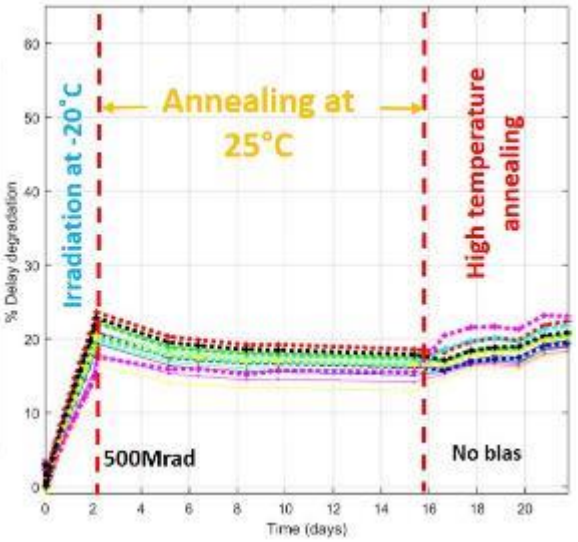
Digital lib and 1Grad ?











Extensive DRAD test results: *https://cds.cern.ch/record/2242708*

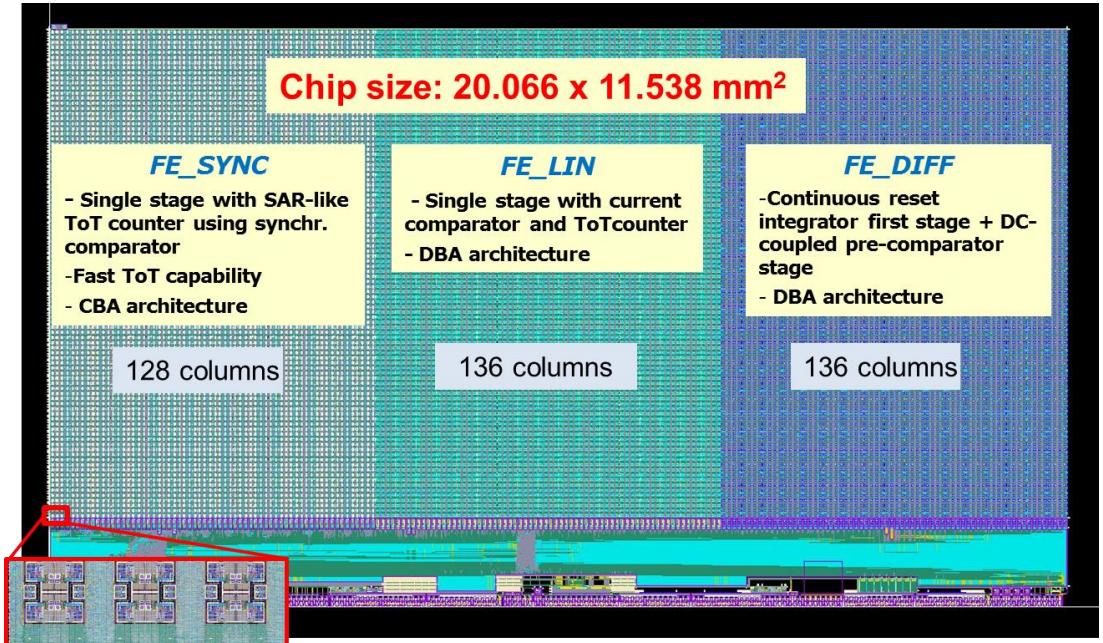
RD53A large scale demonstrator

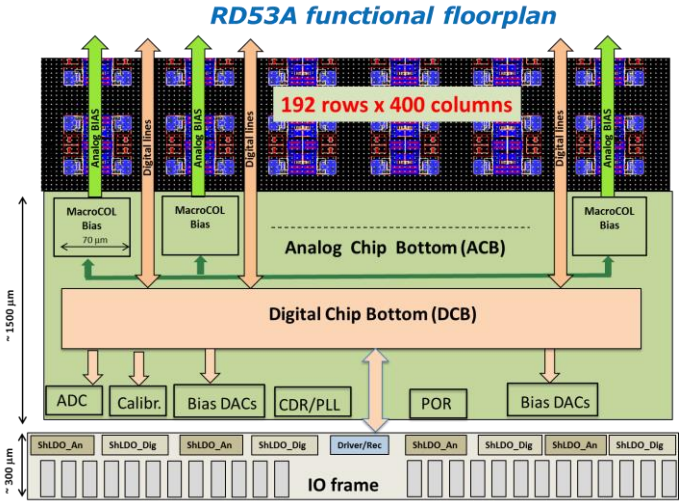
- Large complicated chip:
  - Chip size: 20mm x 12(20)mm, small pixels (50x50um^2), 3 alternative analog FEs.
    Two alternative buffering scheme. Very high hit and trigger rates, Radiation and SEU tolerance,
    600e- threshold, 1200e- in-time threshold, “Low” power, Serial powering,
    Extensive analog and digital monitoring, Calibration features, Fully functional in test beams, etc.
- Specification document agreed with CMS and ATLAS phase 2 pixel communities:
  https://cds.cern.ch/record/2113263
- Core design team of ~10 designers for ~1year
  - 9 months remote collaboration with weekly meetings, common repository, Gitlab, blog, Emails, etc.
  - 3 months together at CERN with daily coffees and weekly meetings
  - 3 months for extensive verification: multiple problems and bugs resolved
  - Not forgetting major work before on radiation, IPs, simulation framework, prototypes with testing, ,
- Engineering run ~1M$ (last minute 25% reduction):
  - Shared run with other projects: CMS MPA/SSA,
    Clicpix, Pixfel, RD53 small pixel arrays,
    Radiation test structures
- Implementation document of ~80pages
- **Submitted last week, chips back in November**

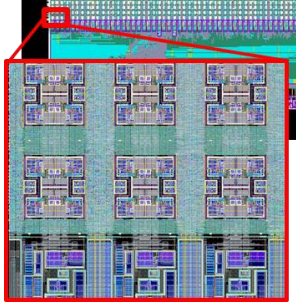
Basic specs

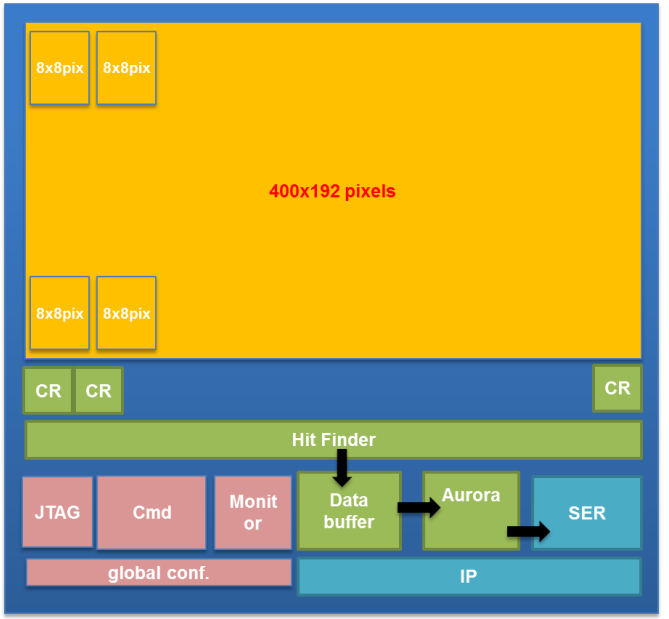
Technology	65nm CMOS
Pixel size	50x50 um^2
Pixels	192x400 = 76800 (50% of production chip)
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	<600e-
In -time threshold	<1200e-
Noise hits	< 10^{-6}
Hit rate	< 3GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	Max 1MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	500Mrad, 1 10^{16} 1Mev eq. n/cm^2 at -15°C
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1W/cm^2 including SLDO losses
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

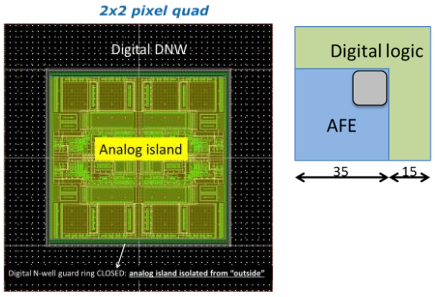
Implementation

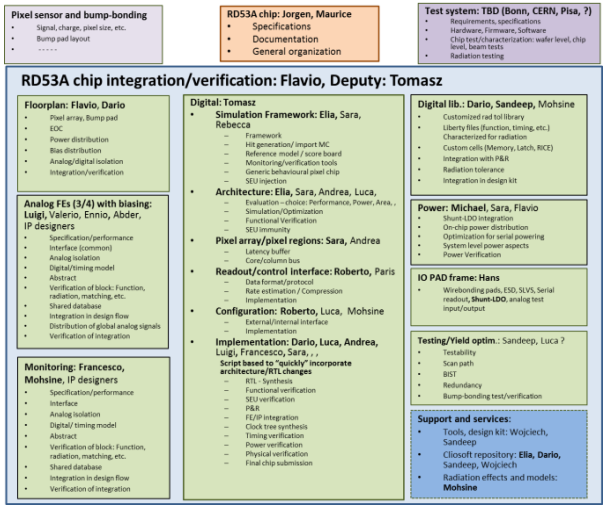






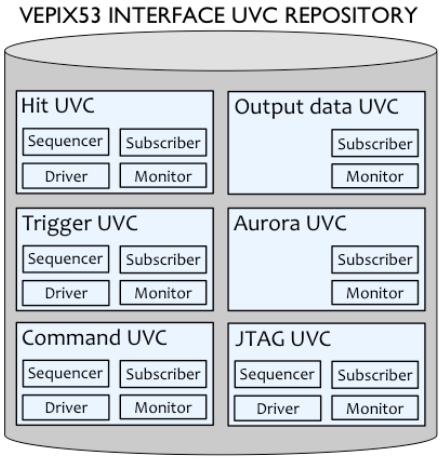


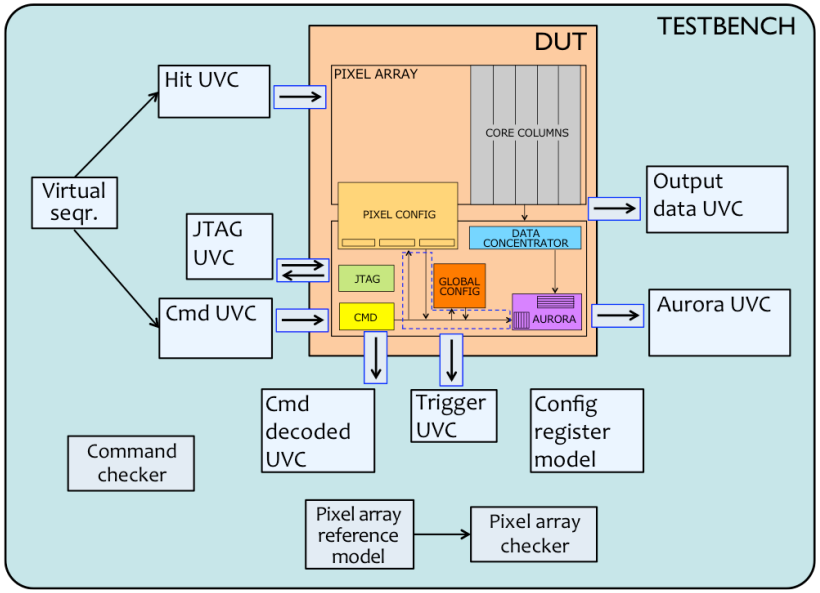




Verification

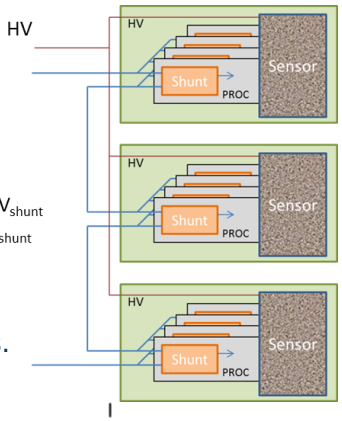
- Analog simulations
  - Analog blocks
  - Multiple analog blocks
  - Pixel core with both analog and digital
  - Availability of conservative radiation models
- Timing verification of digital
  - Challenging for large chip when taking into account radiation damage
- Formal equivalence checking (after synthesis)
- VEPIX53 simulation and verification framework: System Verilog & UVM
  - Developed/used in RD53 during last 3 years
  - Architecture optimization and verification
  - Debugging during design
  - Final design verification
    - Behavioral level, RTL level and Gate level
    - Driving mixed signal simulations for analog blocks (FE, biasing, monitoring, etc.)
    - Driving power simulations/verifications
    - Global tests with hits and triggers at different rates
      A. Internally generated hits
      B. Monte Carlo hits from detector simulations
    - Directed tests for specific functions
    - (SEU simulation: to come)
- Critical for design verification
  - Many major and small bugs found and corrected during whole design process and in particular during last 3 months for final verification
  - Even more effort must be put on this for verification of final chips



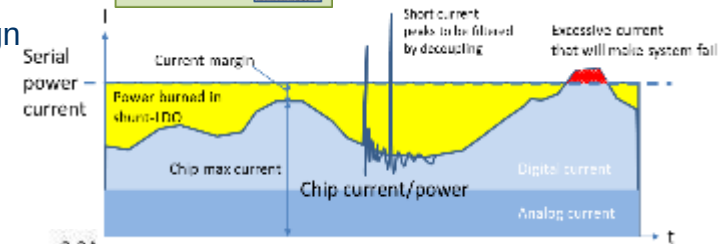


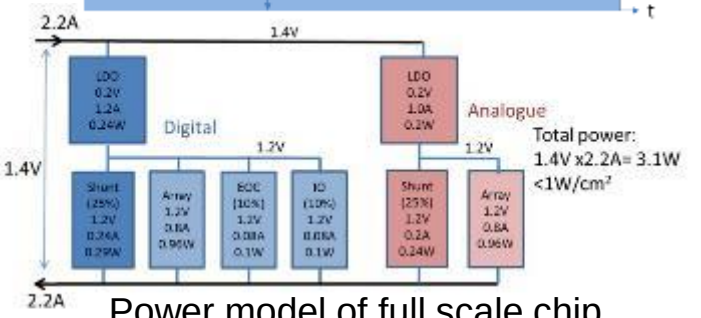
RD53A serial powering

- Serial powering critical for low mass power distribution:
  - ~10k chips of 3W = ~30kW in ~1m^3 ,
    ~10K chips of ~3A = ~30kA over 50-100m cables
- Integration of Shunt-LDO in pixel chip critical
  - SLDO prototypes (0.5A and 2A): Works as simulated
    - Radiation, Noise coupling, Failure modes
  - Improvements made of SLDO for RD53A:
    - Improved control loop to assure stability with capacitive loads.
    - Configurable voltage offset of SLDO impedance
  - Extensive system simulations made with detailed SLDO design and detailed power profiles from detailed chip design: Analog and Digital power
  - Verification of local thermal hot spots (to be extended)
- Power "model" of full sized pixel chip available

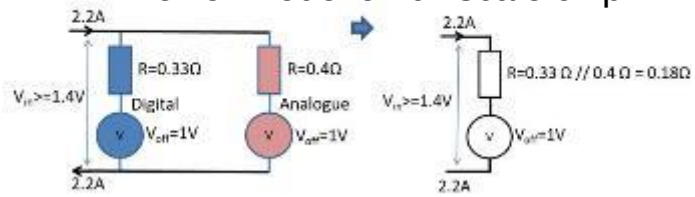


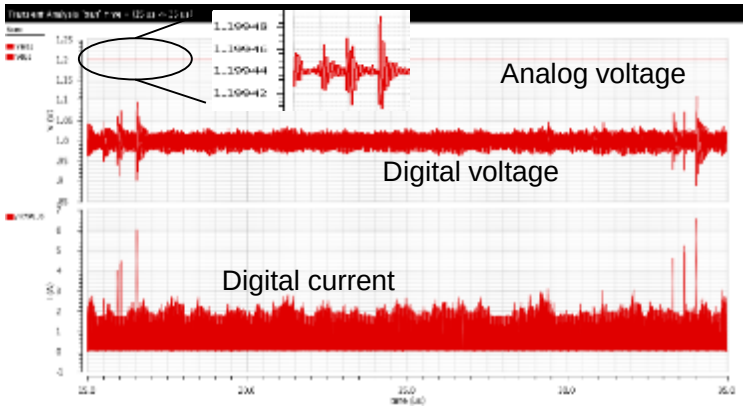
SLDO testing





Power model of full scale chip

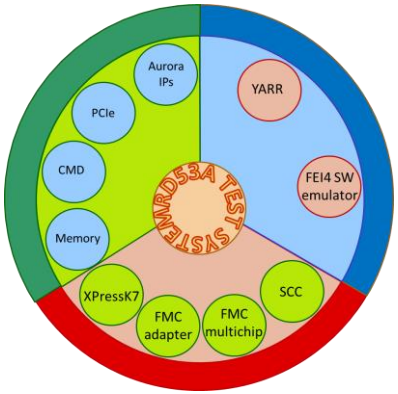


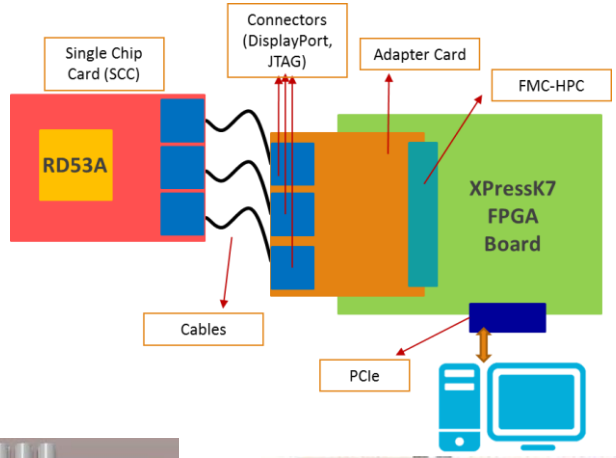


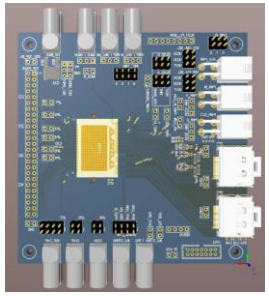
Serial power simulation: System, shunt-LDO, chip

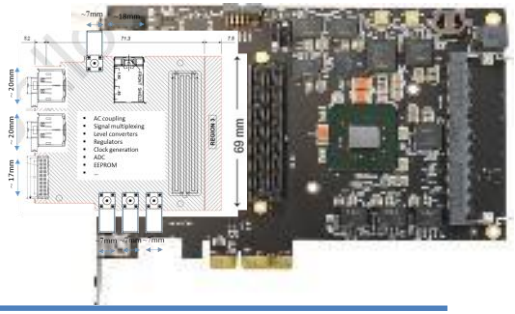
RD53A test preparation

- RD53A test working group preparing testing
  - Chips will come in November
  - Also ATLAS/CMS groups in formally in RD53
- Test systems being prepared:
  A. PC plug-in Hardware:
    - Commercial PCI-E FPGA card
    - Custom FMC adapter card
  B. Standalone custom card: Ethernet
  - Single chip card with standardized interface:
    - Command/clock line and Readout link(s) on standard display port cable
    - Power prepared for serial powering
  - Multi-chip hybrids: In the pipeline for later tests
  - Firmware,
  - Software
  - Based on previous experience with FEI4 test systems
- Pixel sensors being produced in both ATLAS and CMS.
- Bump-bonding being prepared
  - RD53A dummy wafers and sensors for initial trials
  - 300mm wafer handling in HEP community and BB companies
    - Community getting equipped with 300mm wafer probers
- Radiation testing
- Many systems will be used in ATLAS/CMS pixel community









Final CMS and ATLAS chips

- Final CMS and ATLAS chips
  - Differences:
    - Chip size (can unfortunately not fit both on common reticle)
      - CMS: ~22 x 16.4 + 2 mm^2
      - ATLAS: ~20 x 20 mm^2
    - Hit rates: 3GHz/cm^2
      - CMS (r=3cm), ATLAS (r=4cm)
    - Readout interface:
      - CMS: 4 x 1.28Gbits/s to LPGBT module with opto conversion(~0.5m).
        Number of links according to location 1, 2, 3, 4
        Data merging on pixel chip between up to 4 pixel chips to shared link (outer layers)
      - ATLAS: Single 5Gbits/s to patch panel (6-8m)
        Opto conversion on patch panel
    - Latency buffering
      - CMS: 1 level trigger: 12.8us , 750KHz
      - ATLAS: 2 level trigger for possible future upgrades
    - Analog Front-end: Each experiment will choose most appropriate analog FE

  Common chip seems impossible/difficult
- Many common issues
  - Building blocks: Support, integration and verification must be assured for both designs
  - Radiation effects: TID and SEU
  - Serial powering and power optimization.
  - General architecture, configuration, Monitoring, Data merging, Data compression
  - Design approach, Global floorplan, Synthesis & P&R scripts, Verification framework, , ,

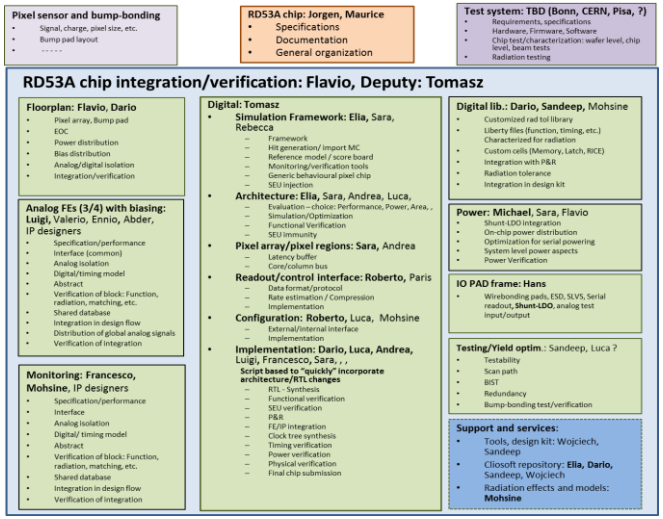
Proposal

- Design ATLAS & CMS chips within RD53
  - Common design framework
  - RD53A was a common design framework mapped into one physical chip
  - Updated common design framework can be mapped into two different physical chips
  - Common design framework with dual responsibles for major parts.
  - Dedicated teams for final implementation and verification
  - Schedule sketch
    - 2017: Finalize specifications of both chips
Extended architectural simulations
Incorporate experience and test results from RD53A
    - 2018: Design and finalization of common design framework
Extended optimization and Verification framework
Extended SEU protection and verification
Mapping into generic implementation (like RD53A)
    - 2019: Mapping into CMS and ATLAS specific implementations
Exhaustive verification and submission
- We will profit a lot from common IP blocks, architecture, design expertise, verification, testing and qualification, etc.
- RD53A team worked very well across CMS – ATLAS boundaries.
  - Helped a lot bringing team physically together for extended period (4 months at CERN)

Experiments represented by RD53 co-spokes persons	CMS	ATLAS
Integration		
Digital design		
Analog integration and verification		
Control, readout and IO interface		
Analog front-end		
Chip verification		
Serial powering		
Radiation hardness		
Common IP blocks	One per IP block	

In the process of assigning names
(most names known from RD53A)

We had similar structure for RD53A



Summary and outlook

- RD53A has been successfully submitted
  - Huge design, verification and testing efforts
  - Team worked very well across ATLAS – CMS boundaries
  - This was the principal milestone of the RD53 collaboration
- RD53A testing is being prepared
  - Many ATLAS and CMS pixel groups will do chip, sensor, pixel module, serial power and system tests with this chip in the coming months - years
- Better understanding of radiation issues
  - Radiation when cold and no bias when at high temperature assures 0.5Grad (possibly 1Grad) radiation tolerance
- Propose to develop final ATLAS and CMS pixel chips within RD53
  - Common design framework (as for RD53A)
  - Final mapping into two dedicated chips
  - Project structure and responsible will be finalized in coming RD53 collaboration meeting (November)
- We formally request the RD53 collaboration to be continued for the final CMS and ATLAS chips
  - Supported by both ATLAS and CMS experiments
  - Supported by RD53 collaboration members (18)

    Additional institutes (2-4) want to join for development of the final ATLAS and CMS pixel chips