Interstrip resistance in silicon position-sensitive detectors

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Outline

- **Motivation**
- **Physical model of interstrip resistance**
- **Experimental results on interstrip resistance in as-processed Si detectors**
- **Influence of nonequilibrium carrier generation**
- R_{IS} **in n-type FZ and CZ Si samples**

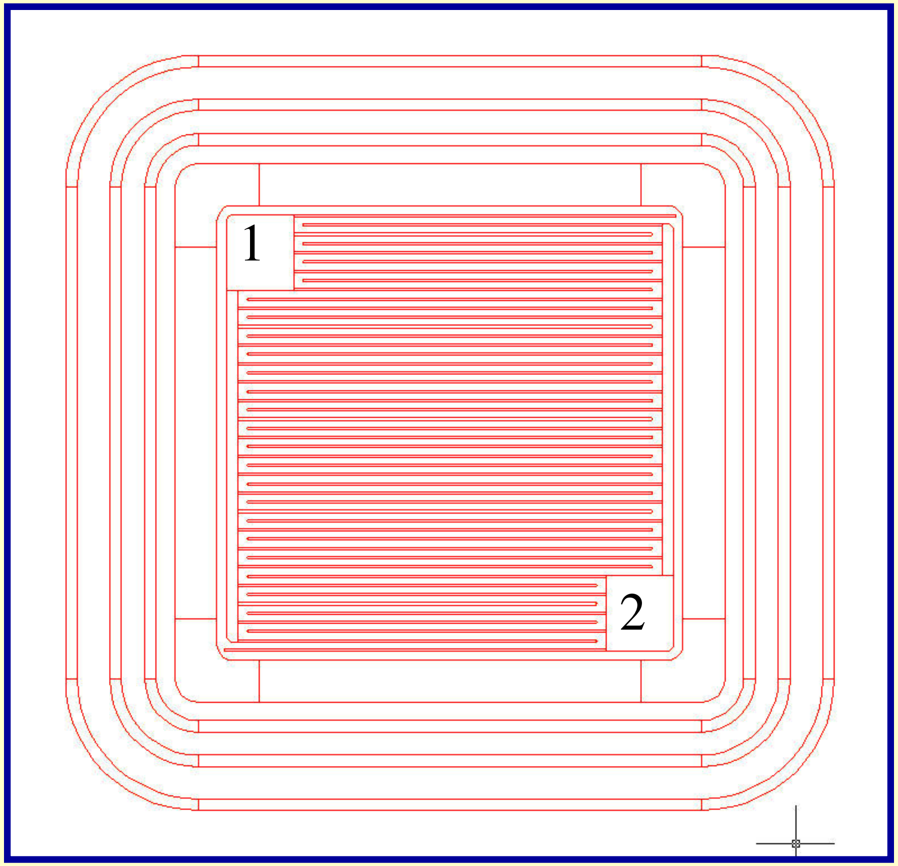
Conclusions

Motivation

Current subjects:

- Development of operational model for voltage terminating structure (VTS) and current terminating structure (CTS, edgeless detectors)
- Strip detector performance at SLHC: very high fluences and enhanced bulk generated current
- Noise performance of spectroscopic strip detectors (GSI, Darmstadt)

Special design of test structures



p^+-n-n^+ structure
- area 1x1 mm^2

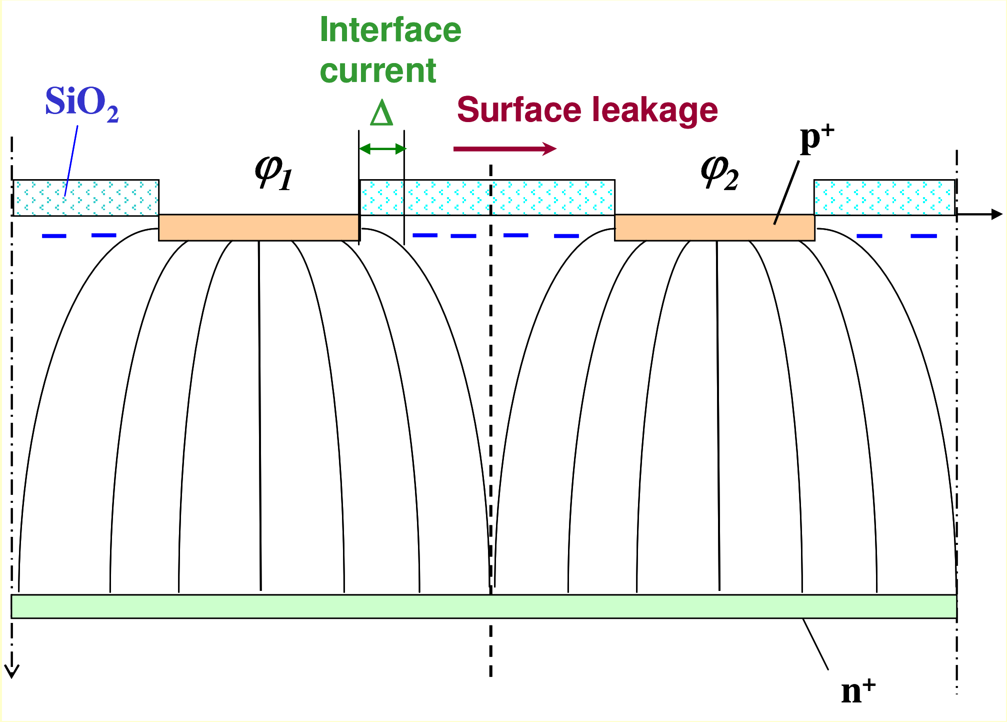
Strips:
two interpenetrating "combs":
- pitch 25 μm

➔ increased length of interstrip gap

➔ equivalent to 4 cm strips

FZ n-Si, ρ>5 kΩ
d = 300 μm $V_{fd} \approx 20$ V

Physical model



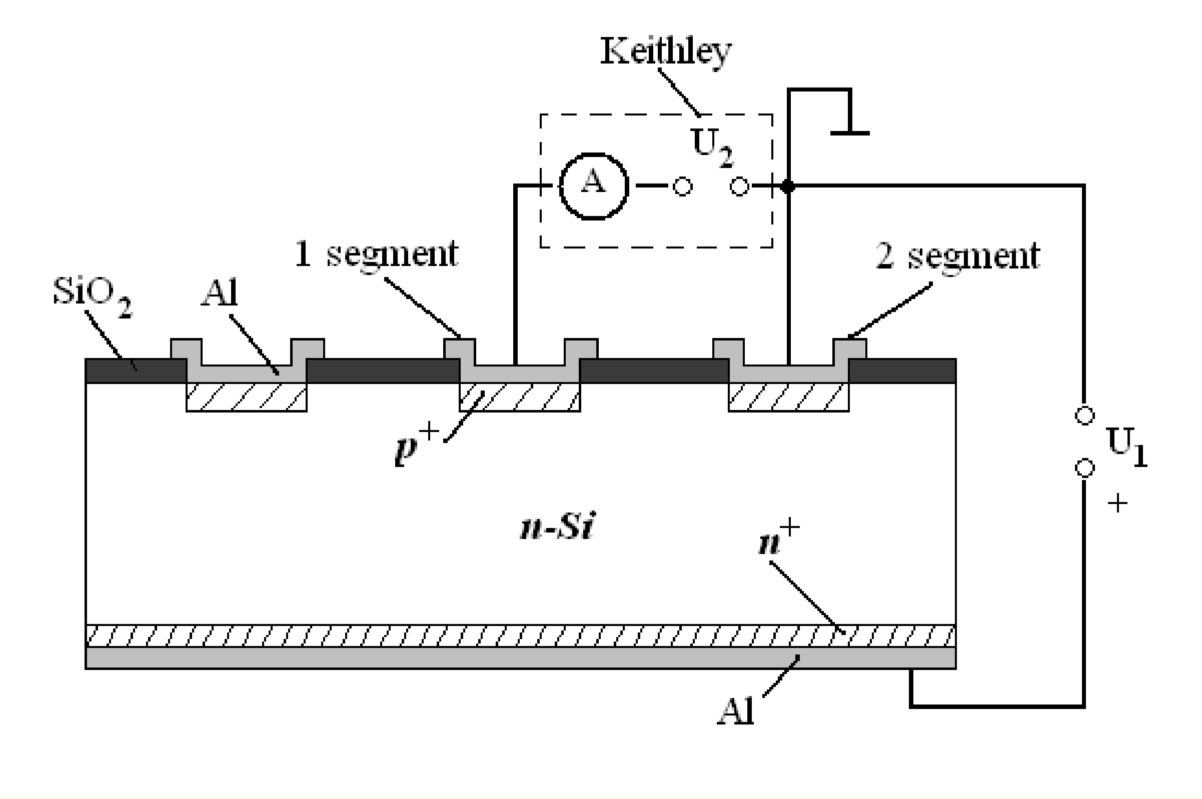
$\varphi_1 = \varphi_2$
- potentials at the strips

Components that control interstrip resistance R_{IS}:

- **surface leakage**
- **interface current**

Distortion of symmetric distributions of potential and electric field may stimulate excess current flow between strips

Measurements of interstrip gap characteristics

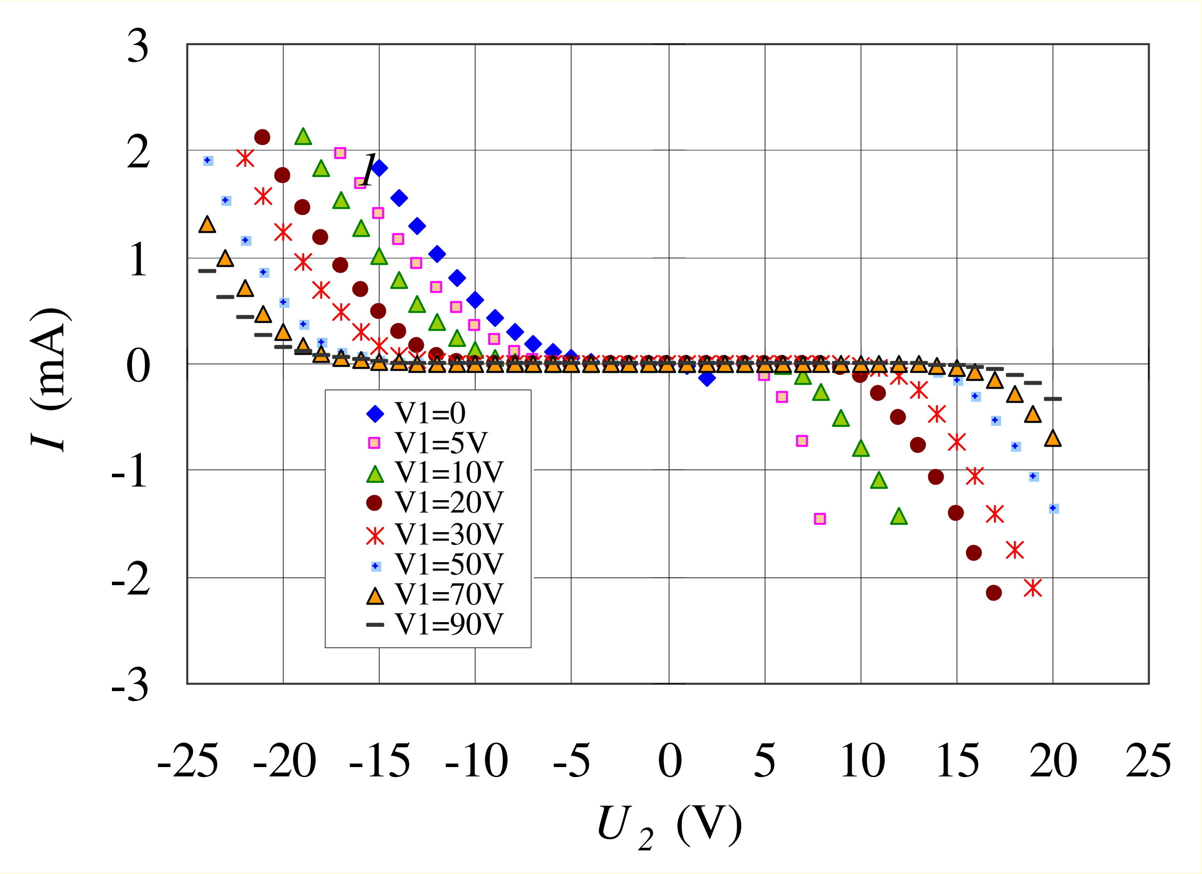


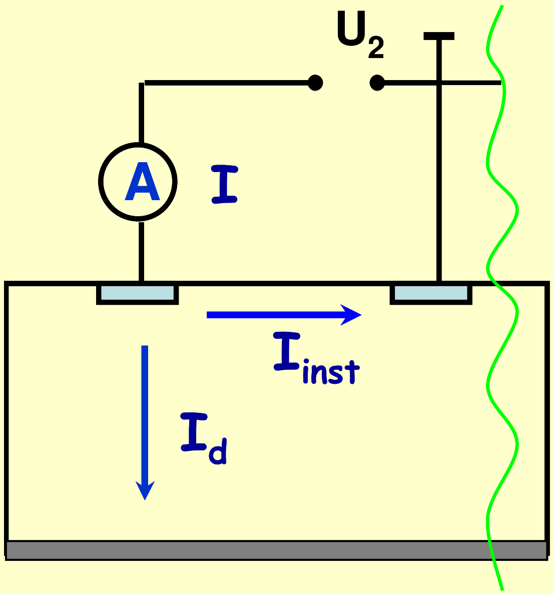
U_1 – bias voltage applied to p-n junction

U_2 – bias voltage between the strips

I-V characteristics of interstrip gap

FZ n-Si, # WP 3-6-2

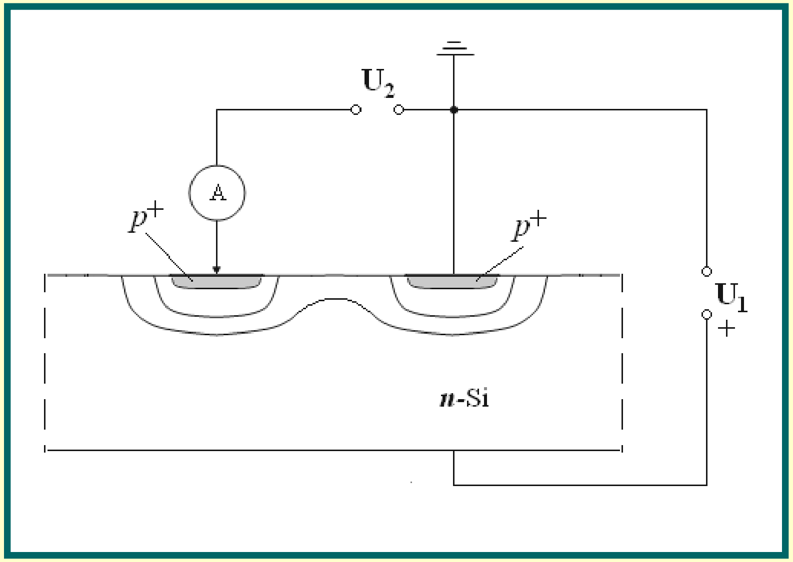


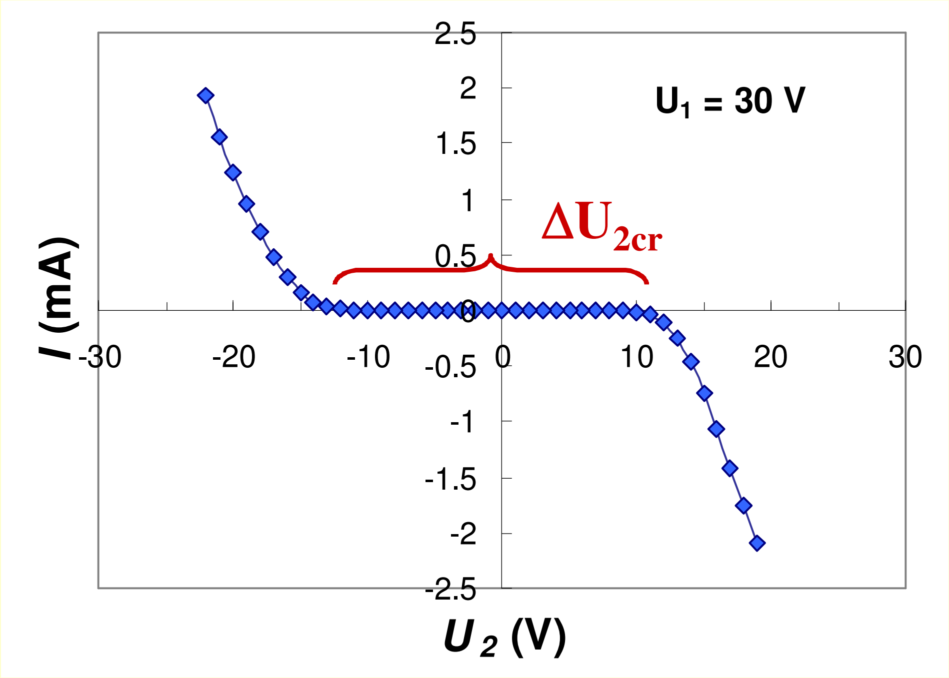


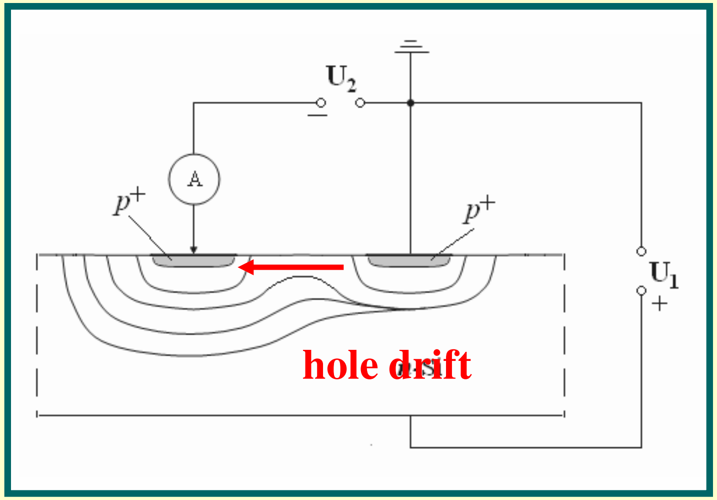
$$I = I_d + I_{inst}$$

I_d – strip dark current
I_{inst} – interstrip current

Current flow in interstrip gap





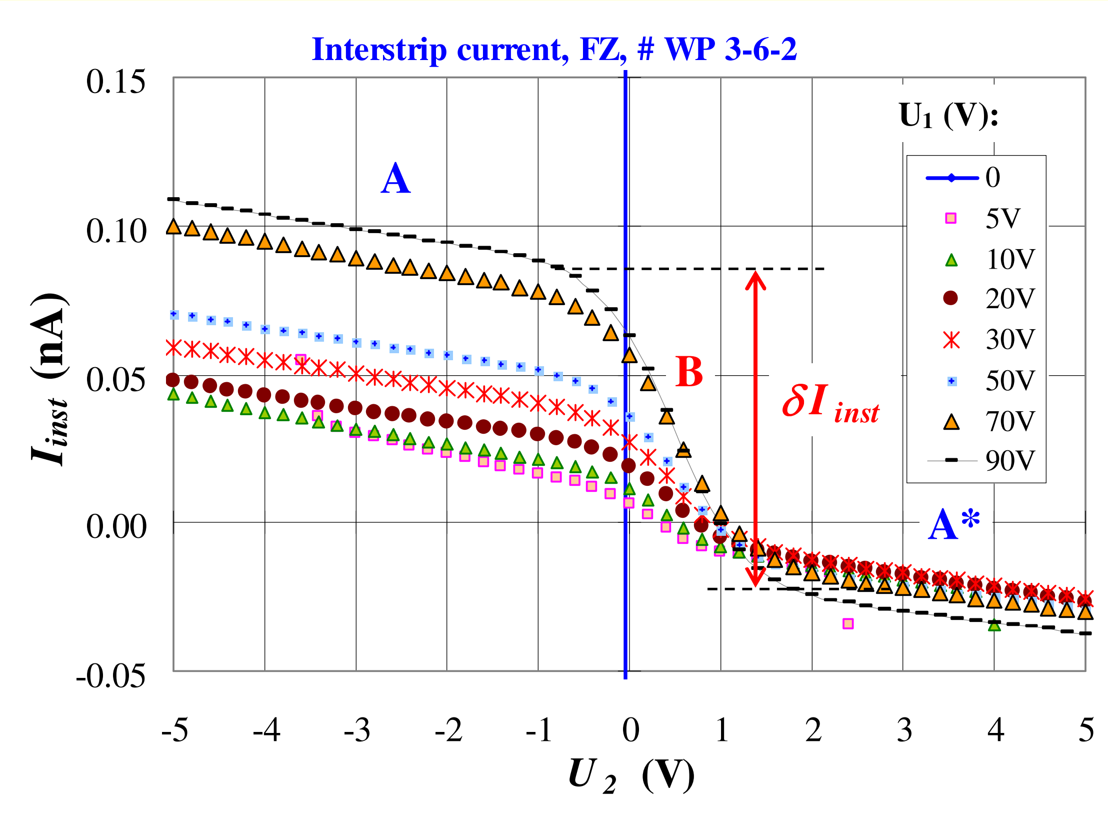


ΔU_{2cr} - range of bias voltage in which I_{inst} is small

- **ΔU_{2cr} ↑ with U_1 ↑**

Interstrip current I_{inst}

$I_{inst}(U_2)$: dark current is subtracted



Interstrip resistance:

$R_{IS} = dU_2/dI_{inst}$

- Regions with different slopes:
  - **A and A*:** $R_\Omega = (dI_{inst}/dU_2)^{-1}$ - ohmic isolation resistance, independent on U_1, related mainly with surface leakage
  - **B:** current step δI_{inst}
- δI_{inst} and dI_{inst}/dU_2 ↑ as U_1 ↑

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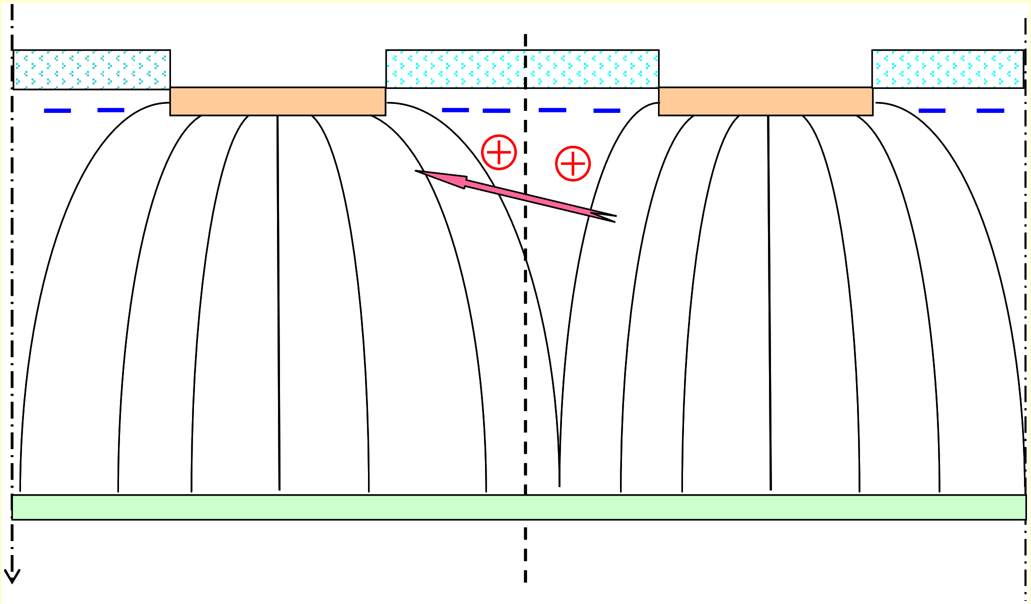
Origin of interstrip current step δI_{inst}

$\varphi 1 \neq \varphi 2$



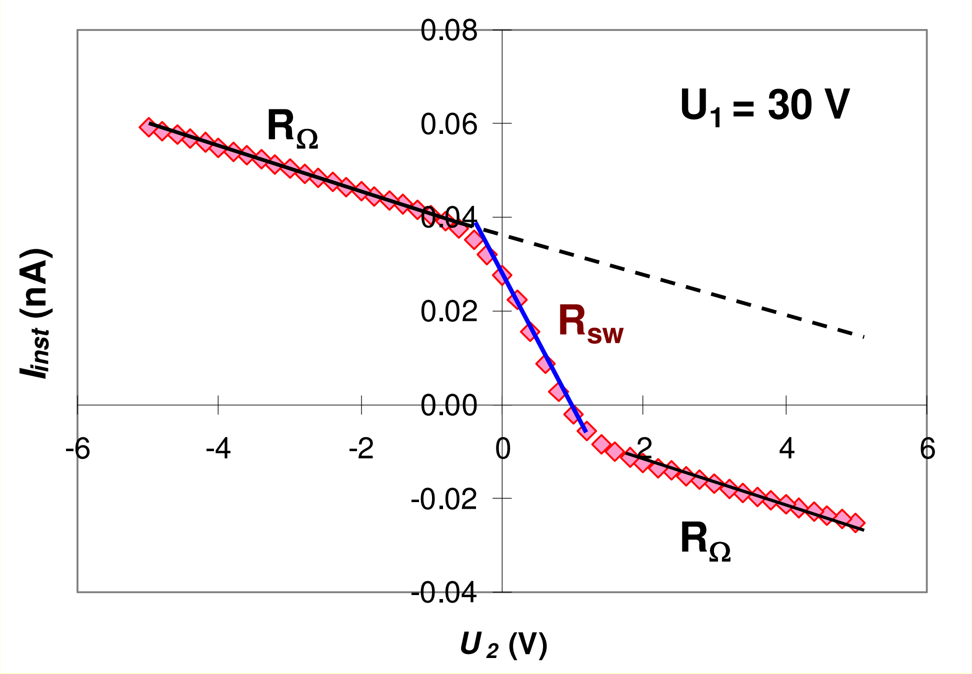
Current switching – redistribution of strip hole currents

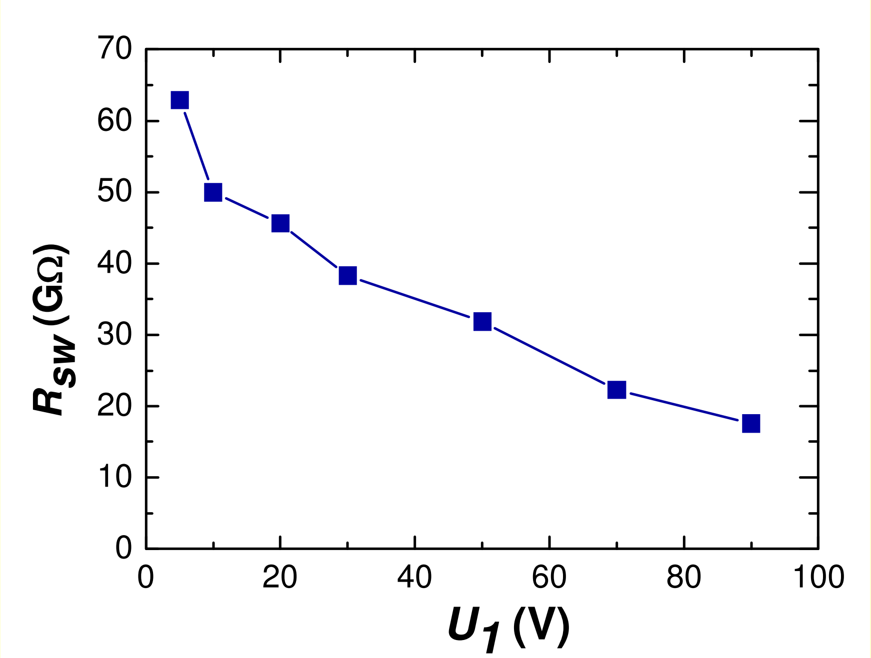
In detector:
Switching acts as negative feedback
➔ recovery of potential balance

$$R_{sw} = (dI_{inst}/dU_2)^{-1}$$

in δI_{inst} region

Interstrip resistance vs bias voltage





$R_\Omega \approx 200$ GΩ

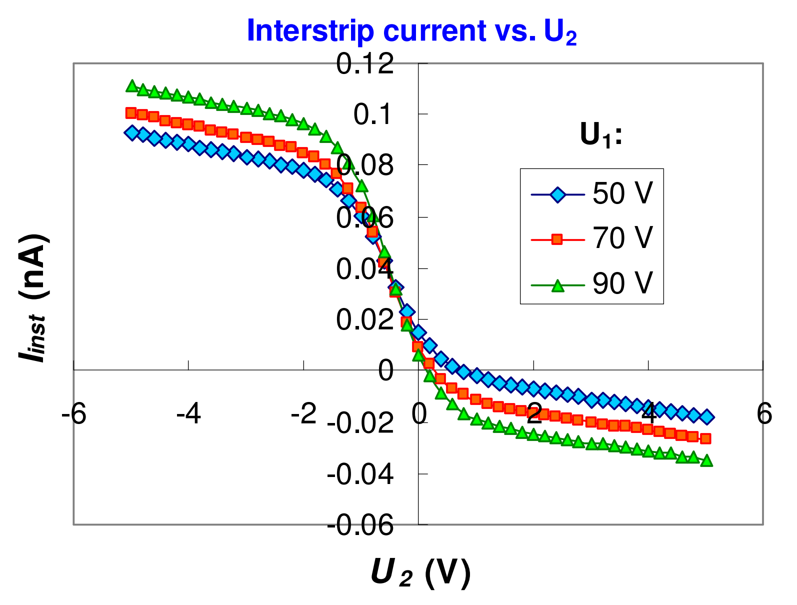
irrespective to U_1 and at $\pm U_2$

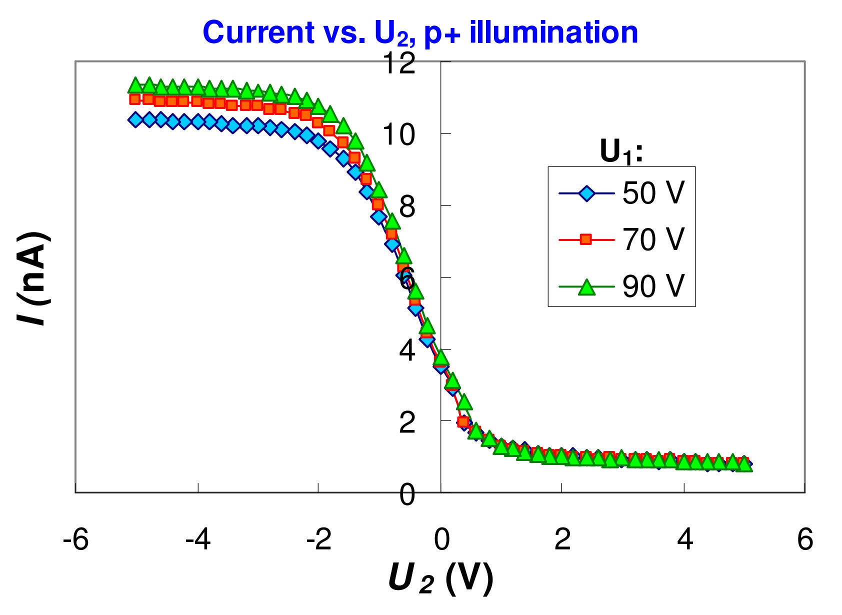
$R_{sw} = dU_2/dI_{is}$ at $U_2 \approx 0$

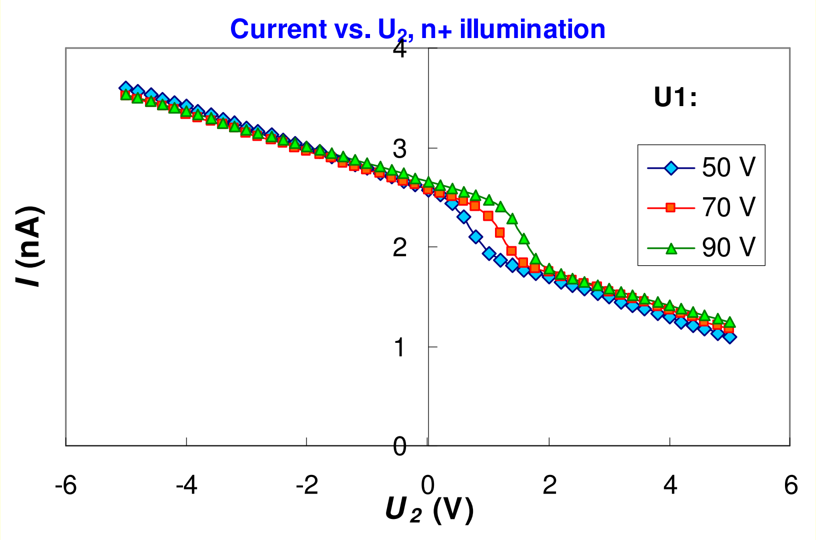
R_{sw} ↓ with U_1 ↑

$R_\Omega > R_{sw}$

Influence of nonequilibrium carrier generation







Carrier generation:

- by LED illuminating p^+ side
- white light on n^+ side

$$I = I_{ph} + I_{inst}$$

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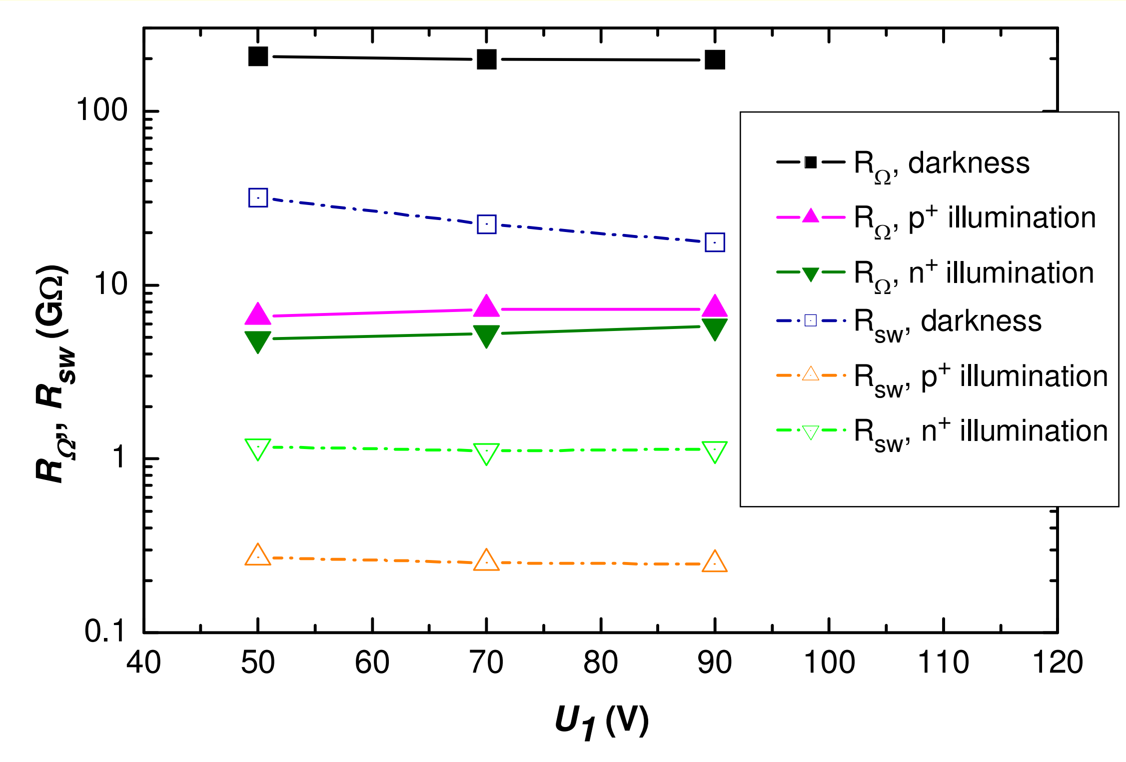
Influence of nonequilibrium carrier generation on R_{IS}



- R_Ω and R_{sw} ↓ with carrier generation
- R_Ω↓ : p$^+$ illumination
  – high n and p under SiO_2
- R_{sw} at carrier generation: no dependence on U_1
  – switching is controlled by photocurrent rather than dark current
- Ratio of R_{sw} is about one half of current ratio since ½ of a total structure current is switched

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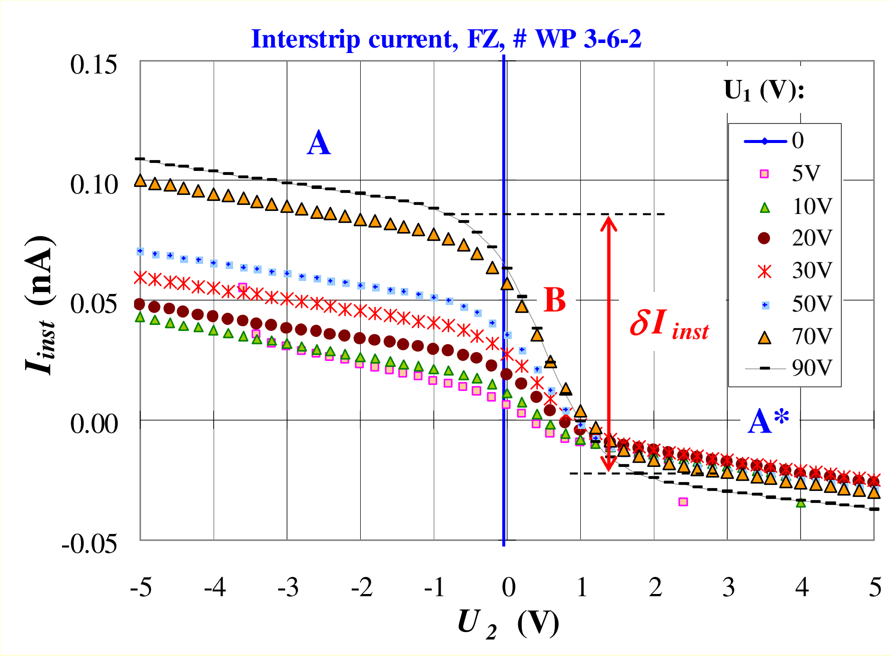
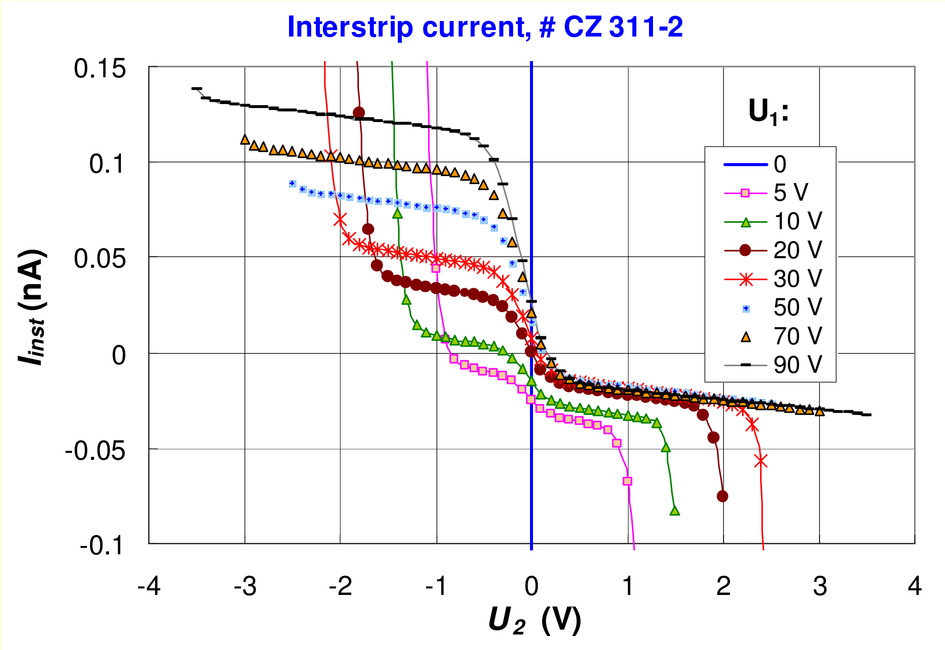
Influence of Si type

FZ n-Si

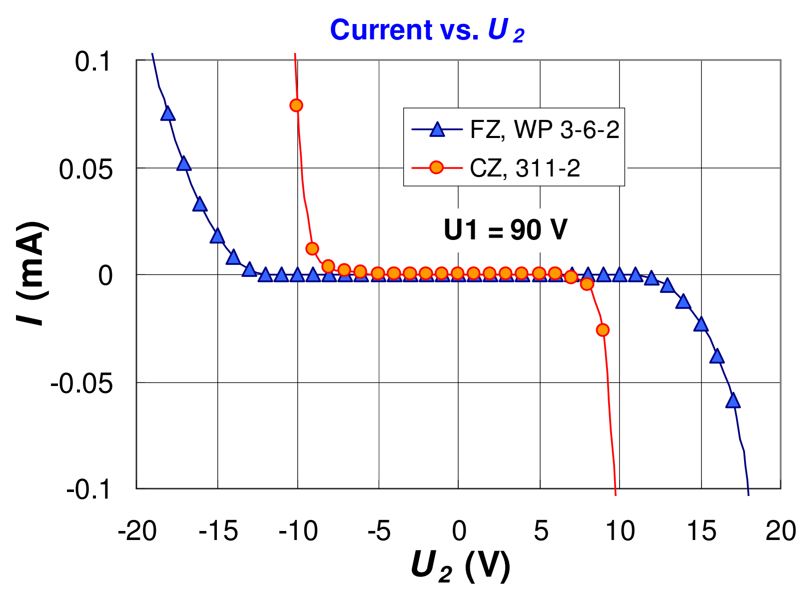


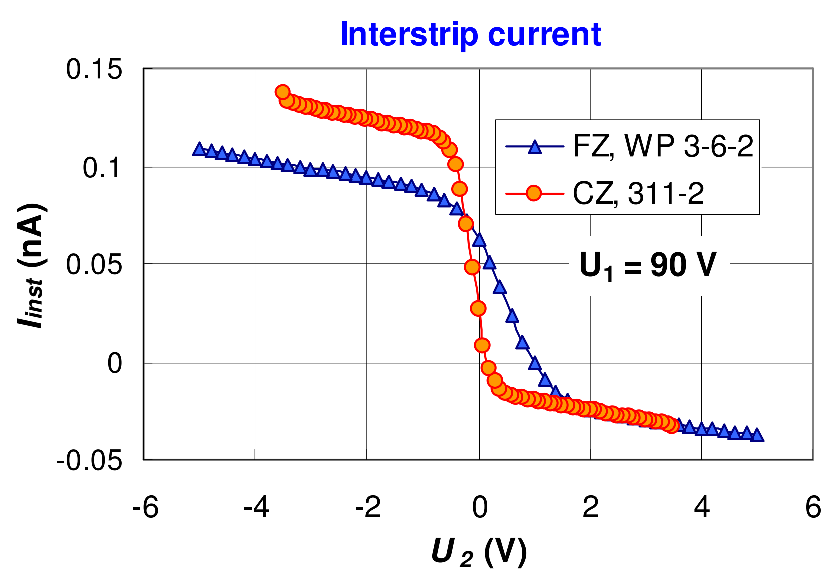
CZ n-Si



Similar behavior of I_{inst} vs. U_1 and U_2

Comparison of I_{inst} for different Si types





- ΔU_{2cr} is smaller in CZ Si
- δU_2 corresponding to δI_{inst} is smaller in CZ Si
- R_Ω is similar

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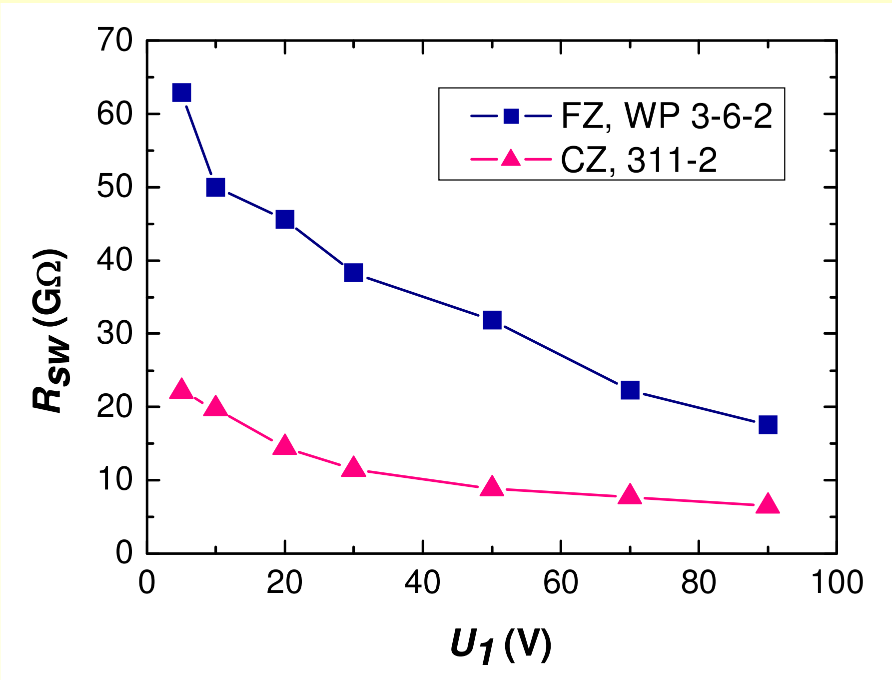
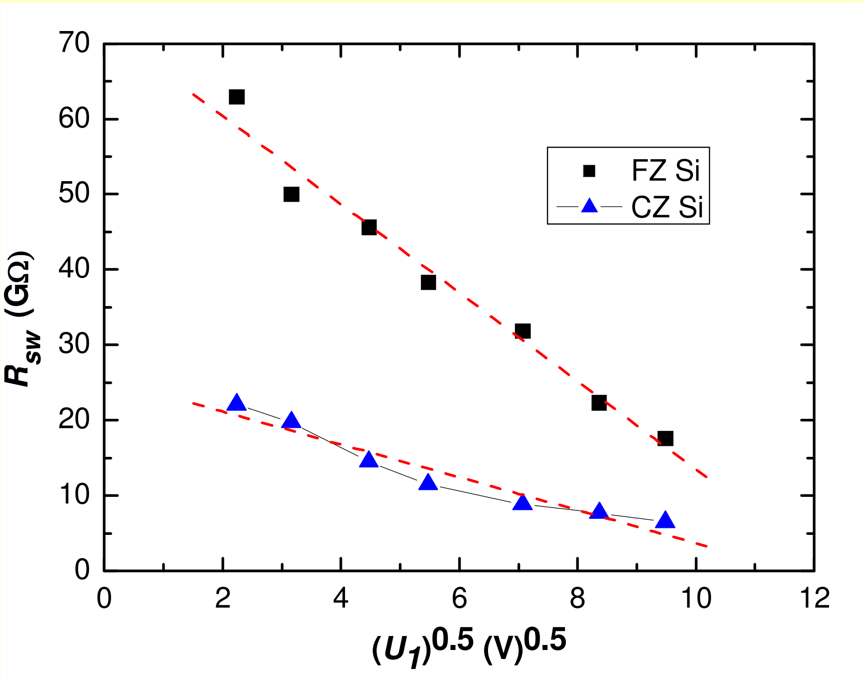
Comparison of R_{sw} for different Si types





R_{sw} is smaller in CZ Si

Parameterization: $R_{sw} = A - B(U_1)^{0.5}$

FZ: $R_{sw} = 7.2 \cdot 10^{10} - 5.9 \cdot 10^{9}(U_1)^{0.5}$
CZ: $R_{sw} = 2.5 \cdot 10^{10} - 2.2 \cdot 10^{9}(U_1)^{0.5}$

➔ R_{sw} depends on bulk generation current

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Future studies

- Different wafer orientation
- Detectors with different configuration
- Study of irradiated Si detectors

Conclusions

- The factors that define interstrip isolation resistance are:
  - surface leakage,
  - interface current,
  - new mechanism - distortion of symmetric potential distribution at the strips and switching of strip currents.

- Switching of strip currents is a negative effect since it decreases interstrip isolation. This effect may control interstrip resistance rather than ohmic conductance between the strips.

- R_{Ω} is about 200 GΩ irrespective to the bias voltage while R_{sw} is bias dependent and decreases with bias voltage rise down to few GΩ.

Results are partially published in:
V. Eremin et al., Semiconductors 43 (2009) 796.

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Thank you for attention!