Simulations of Guard Ring Designs for n-on-p Sensors and of 3D CMS Detectors

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Planar Silicon Detectors–Different Technologies

p-on-n :

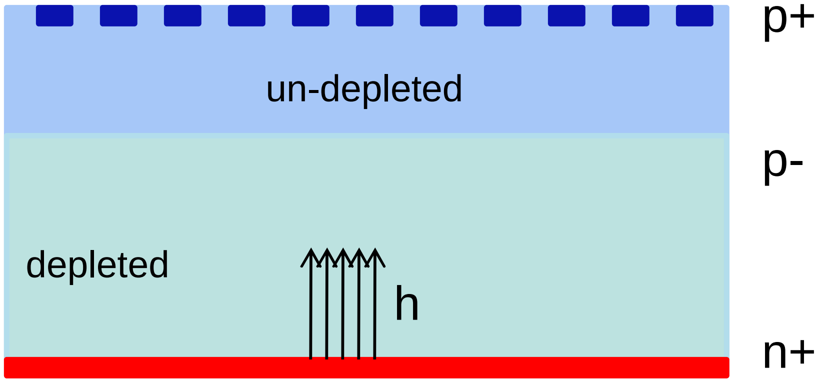
- Collects holes
- Single-side processing
- Lowest cost
- Most production experience (All strip detectors at ATLAS/CMS/ALICE, Tevatron, etc.)
- Available from all foundries

n-on-n :

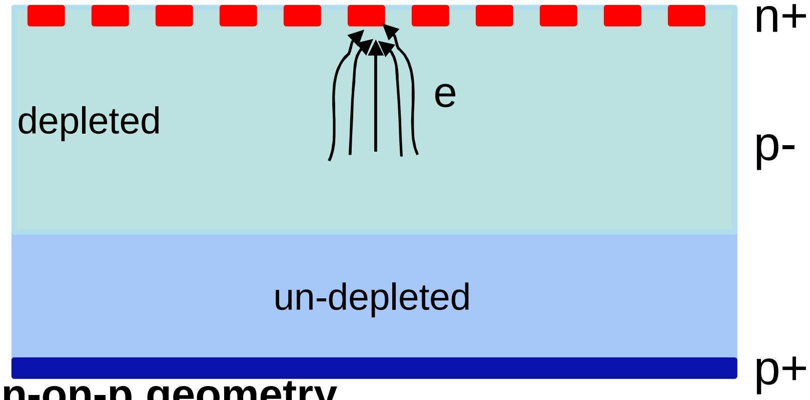
- Collects electrons
- More radiation-hard than p-on-n
- Double-side processing
- More expensive
- Some large scale production experience (Pixel detectors at ATLAS/CMS, LHCb VELO)
- Limited suppliers

n-on-p :

- Collects electrons
- Might be as radiation-hard as n-on-n
- No substrate type inversion
- Single-side processing
- ~50% less expensive than n-on-n
- Limited production experience
- More suppliers ?



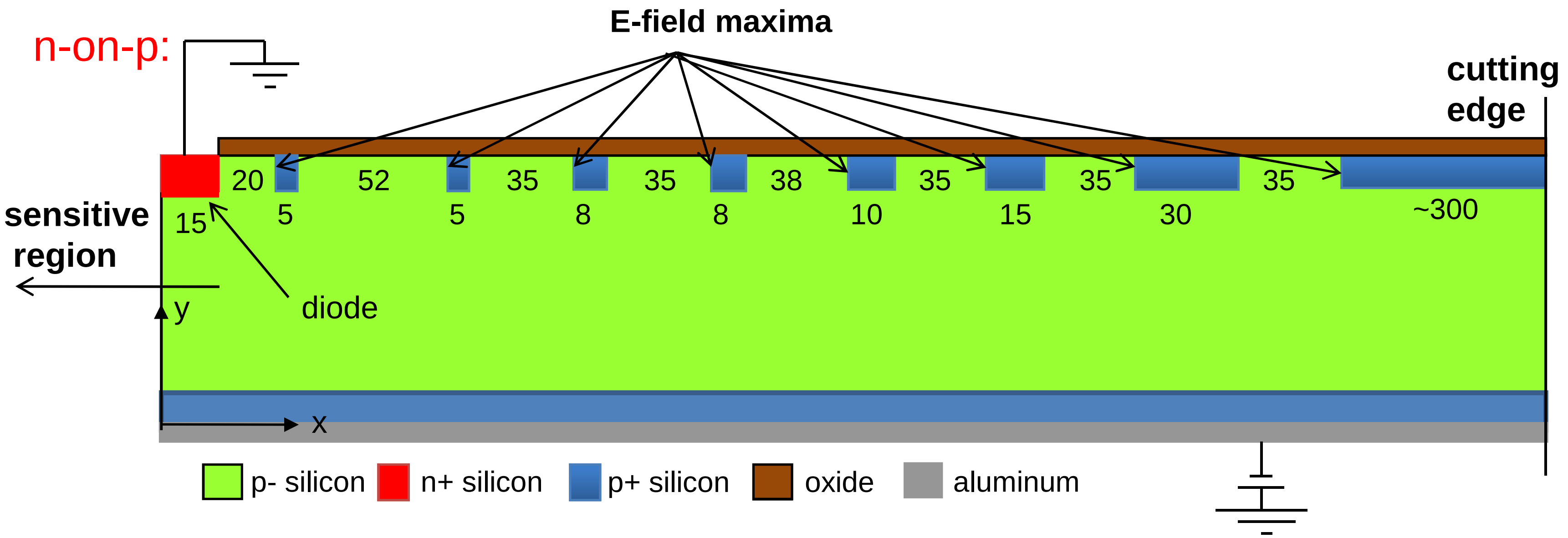
p-on-n geometry (after type inversion)



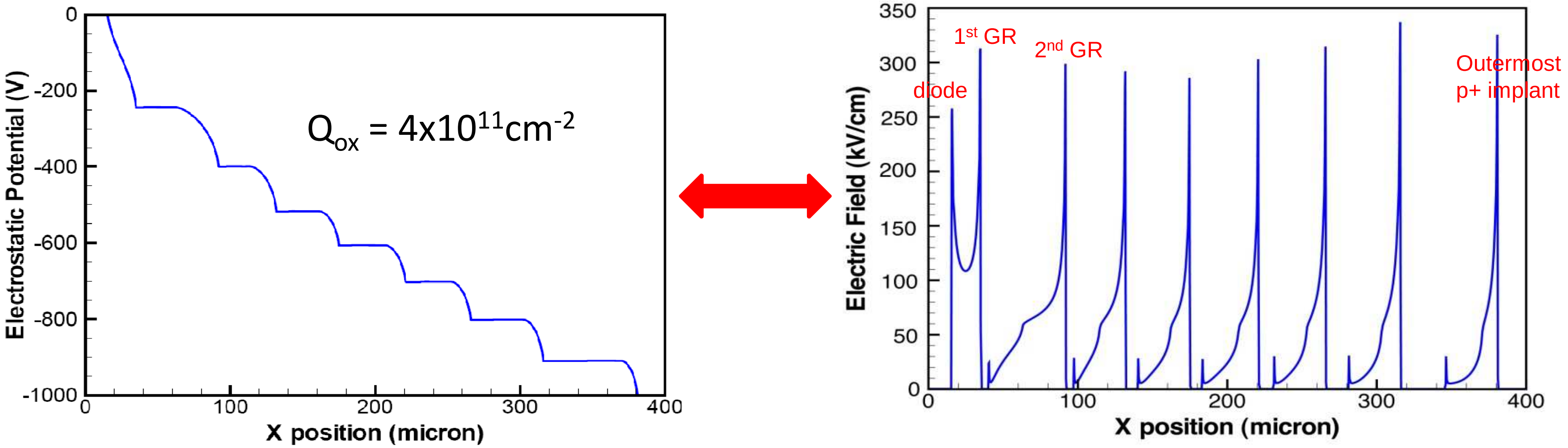
n-on-p geometry
n-on-n geometry (after type inversion)

Guard Rings for n-on-p Technology

- Damaged cutting edge is a very effective generation center
- Edge termination to shield the sensitive region from dice line leakage current
- Guard rings allow uniform potential drop along silicon surface and prevent localized breakdowns
- Outermost wide p+ implant to prevent depletion region from reaching out the edge
- Simulations were performed with Synopsys Sentaurus to optimize the design. A fixed oxide charge of of 4x10^{11} cm^{-2} was assumed



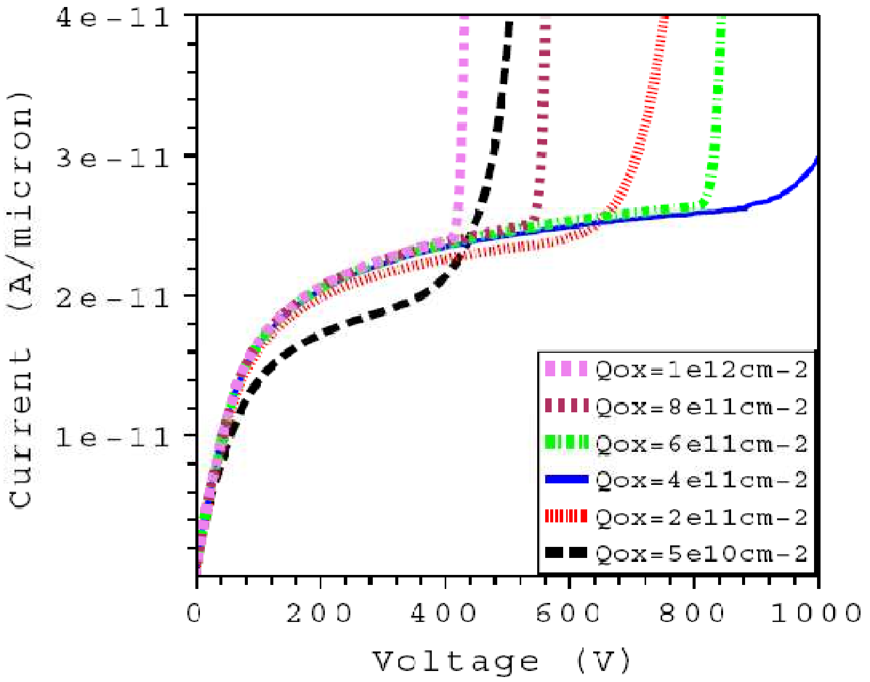
Guard Rings for n-on-p Technology



Plots taken at a depth of 100nm from the silicon/oxide interface

- For $Q_{ox} < 4x10^{11}$ cm^{-2}, decrease in breakdown voltage is mainly due to non-uniform distribution of potential along guard rings

- For $Q_{ox} > 4x10^{11}$ cm^{-2}, decrease in breakdown voltage is mainly due to steeper potential drop at each guard ring

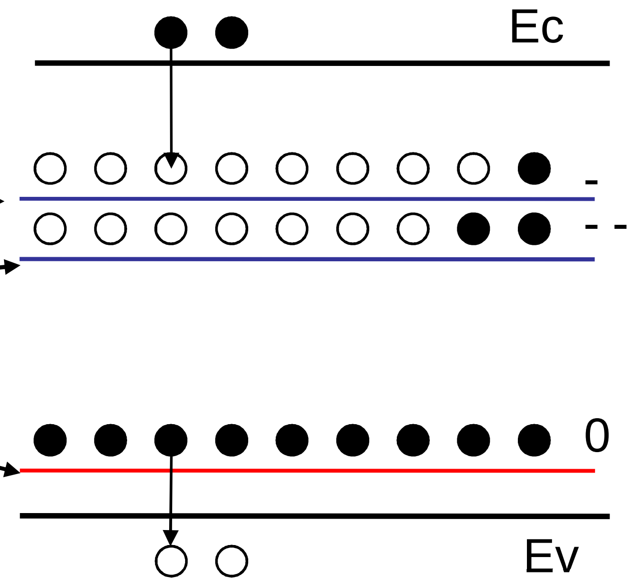


Modeling of Radiation Damage

University of Perugia Model (Petasecca et al.)

Type	Energy (eV)	Trap	σ_e (cm^2)	σ_h (cm^2)	η (cm^{-1})
Acceptor	E_C-0.42	VV	**$2.0*10^{-15}$**	**$2.0*10^{-14}$**	1.613
Acceptor	E_C-0.46	VVV	$5.0*10^{-15}$	$5.0*10^{-14}$	0.9
Donor	E_C+0.36	CiOi	**$2.5*10^{-14}$**	**$2.5*10^{-15}$**	0.9

$$Conc(cm^{-3}) = \Phi_{eq}\eta$$



Donor level: Trapping of free holes

Acceptor levels: Leakage current, negative charge (N_{eff}), trapping of free electrons

Predicts increase in leakage current and depletion voltage accurately but not carrier trapping

Carrier Trapping:

$$\frac{1}{\tau_{e,h}} = \beta_{e,h}\Phi_{eq} \qquad \beta_{e,h} = v_{th}^{e,h}\sigma_{e,h}\eta$$

Space Charge:

$$n_{e,trap} = N_{trap} f_n \approx N_{trap} \exp\left(-E_t/kT\right)\left(\frac{n}{n_i} + \frac{\sigma_h v_{th}^{h}}{\sigma_e v_{th}^{e}} \exp\left[-E_t/kT\right]\right)$$

Perugia Model Modified by D. Pennicard

Type	Energy (eV)	Trap	σ_e (cm^2)	σ_h (cm^2)	η (cm^{-1})
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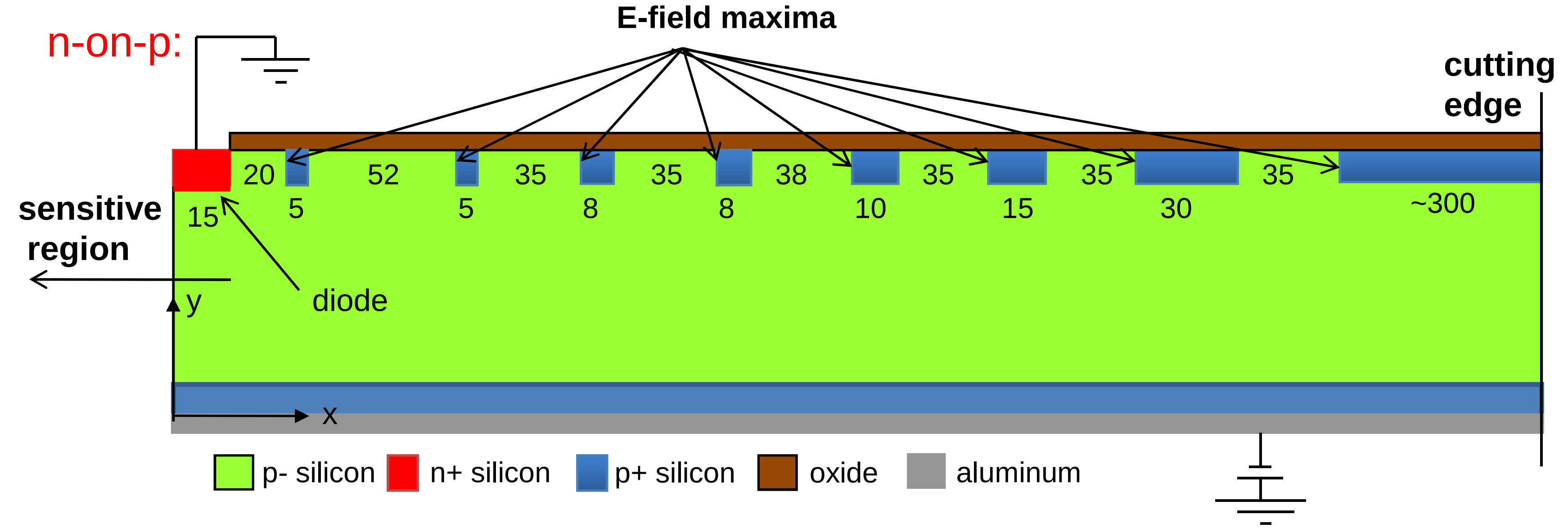
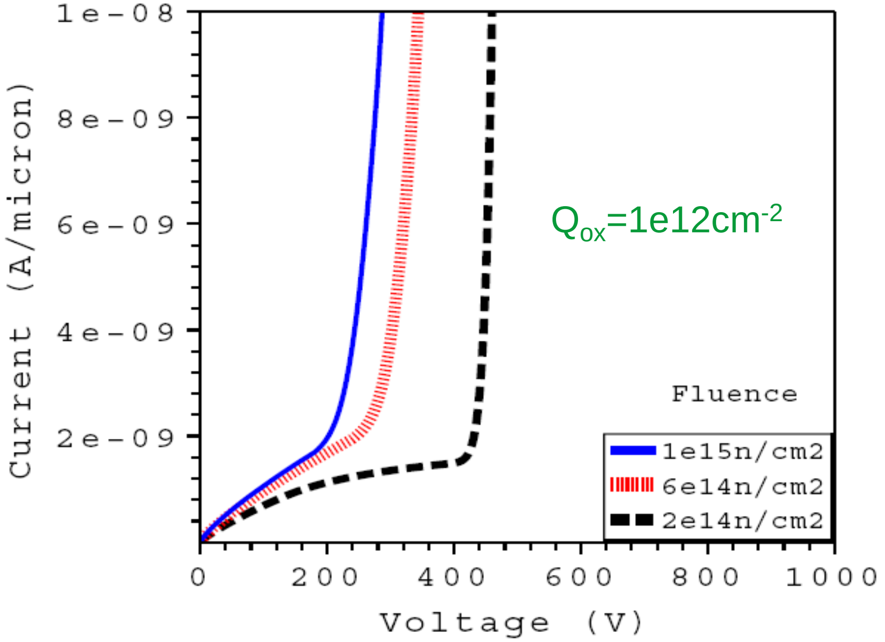
Post-Irradiation Performance

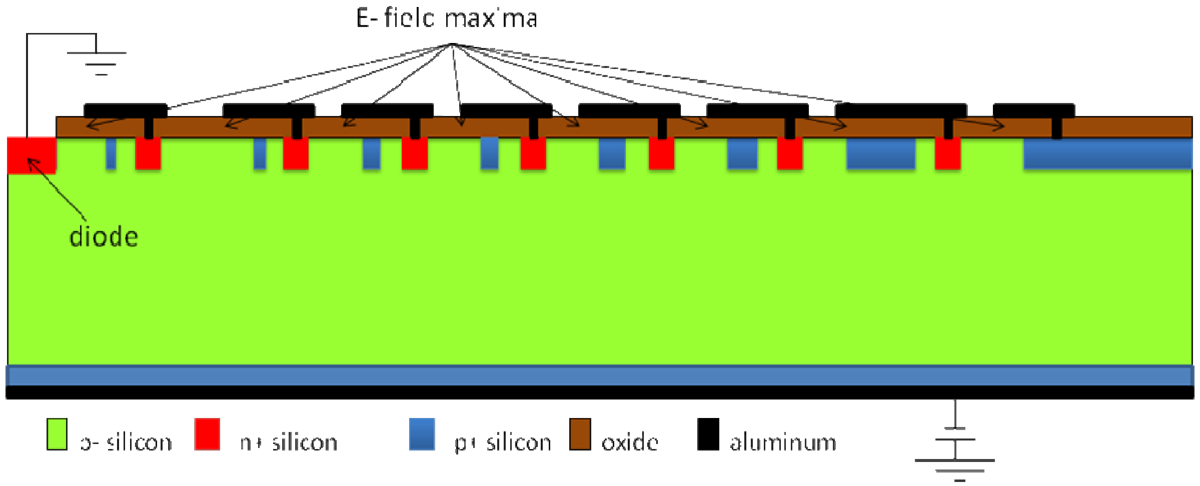


- Simple design with no metal over the rings
  - Easier to have passivation to protect readout chip
- Results in too low breakdown voltage
  - Increasing surface conductivity from increasing oxide charge ⇒ the potential drop at each p+ guard ring becomes steeper ⇒ higher electric fields.
  - The depletion region might not reach the outer guard rings. Potential is shared between less guard rings ⇒ higher electric field

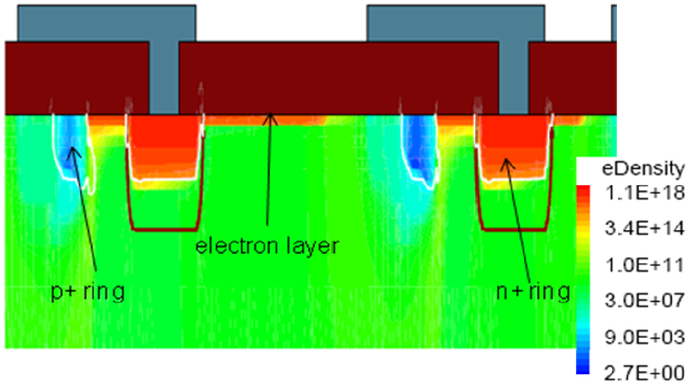
No Field Plates



Post-Irradiation Performance & Field Plates

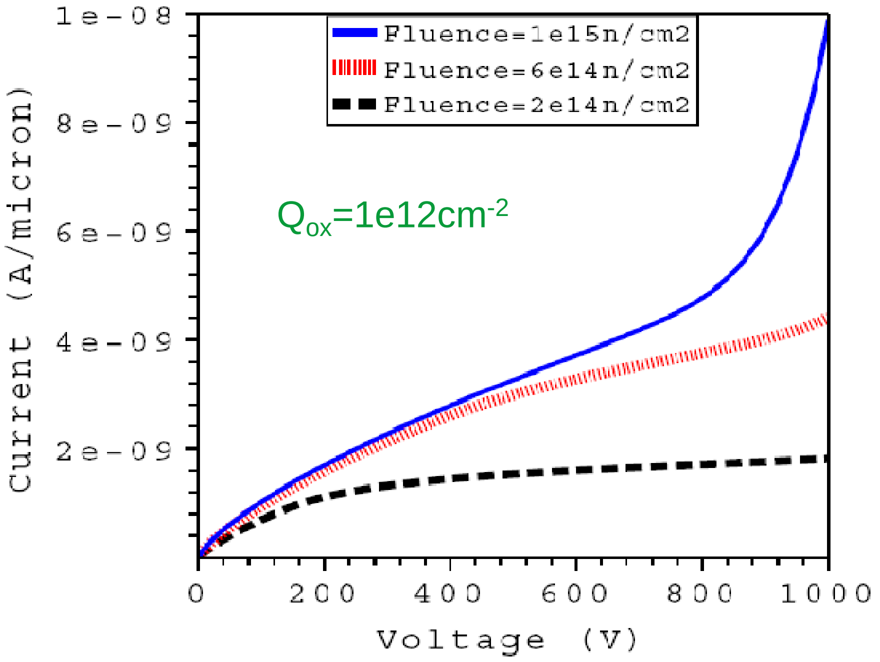


1000 V, @1E15 n/cm^2



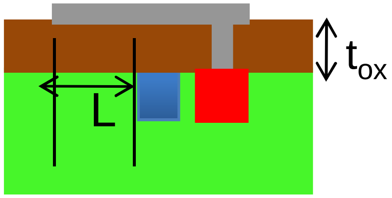
- Reduce the electric field after irradiation with field plates pointing towards the sensitive region
  - The field plates are at lower potential than the underlying silicon as the potential drops from the active region towards the edge ⇒MOS
  - The electron layer disappears at the silicon/oxide interface on the left of the p+ rings
  - Larger E field in the oxide ⇒ larger breakdown voltage

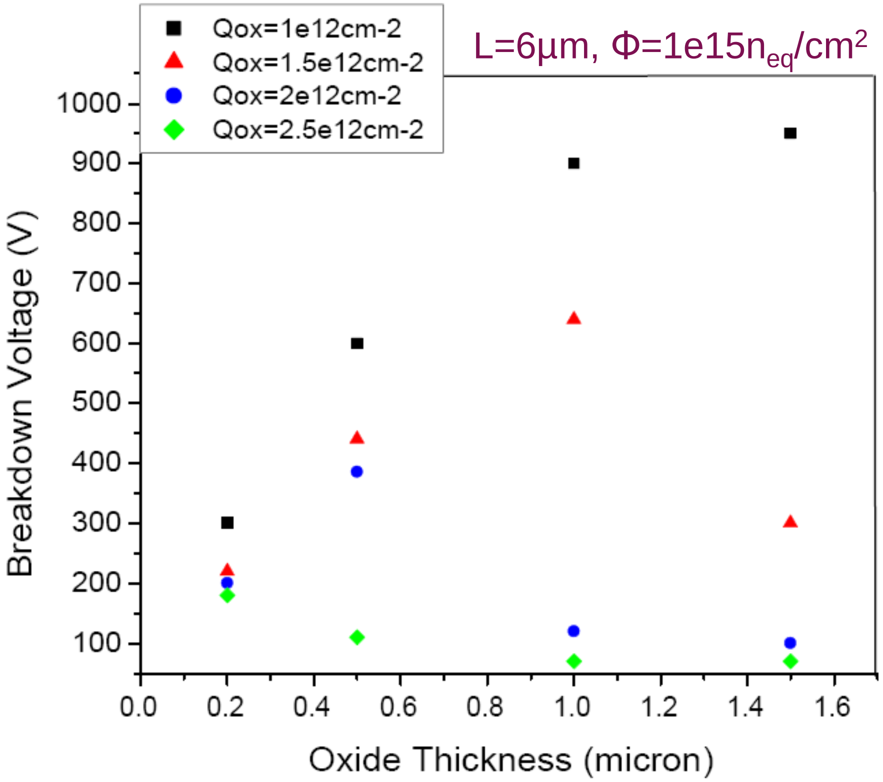
With Field Plates

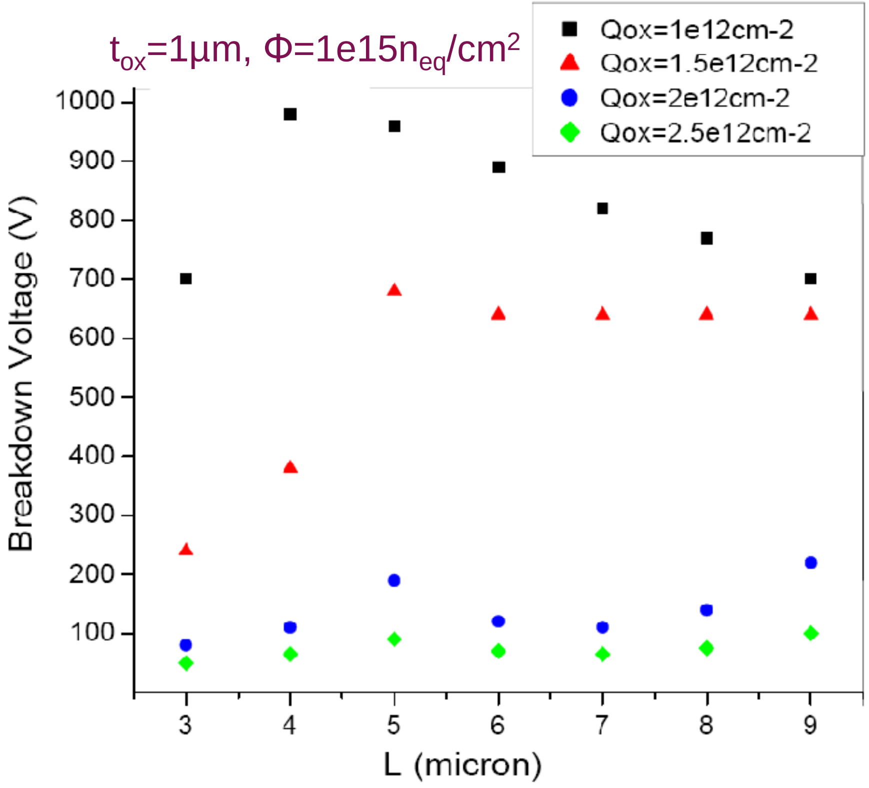


Field Plate Length & Oxide Thickness

$$\Delta V_{FB} = q\boxed{t_{ox}Q_{ox}} / \varepsilon_0\varepsilon_{ox}$$



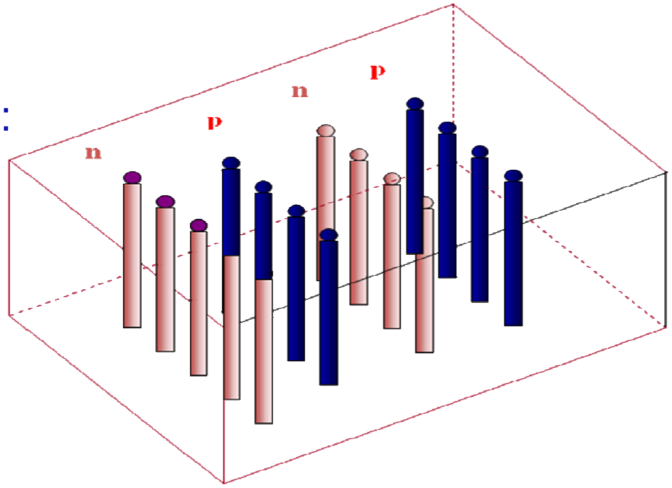

L=6μm, Φ=1e15n_{eq}/cm^2


t_{ox}=1μm, Φ=1e15n_{eq}/cm^2

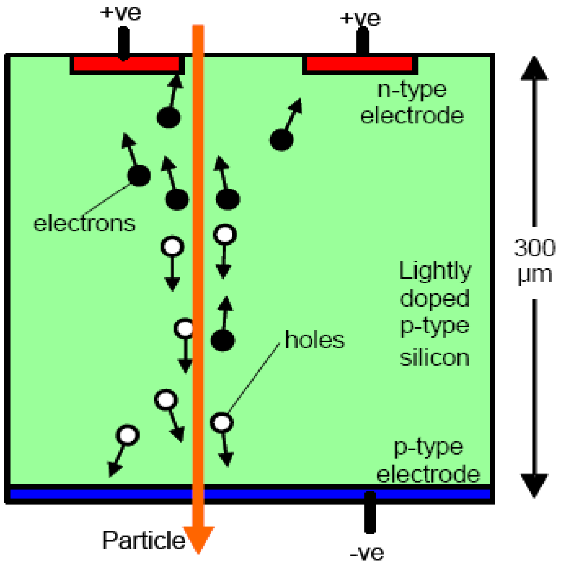
- Low breakdown at $Q_{ox} \geq 2\times10^{12}$cm^{-2} regardless of field plate length
- 2μm thick polyimide passivation on the top of oxide?

3D Detectors

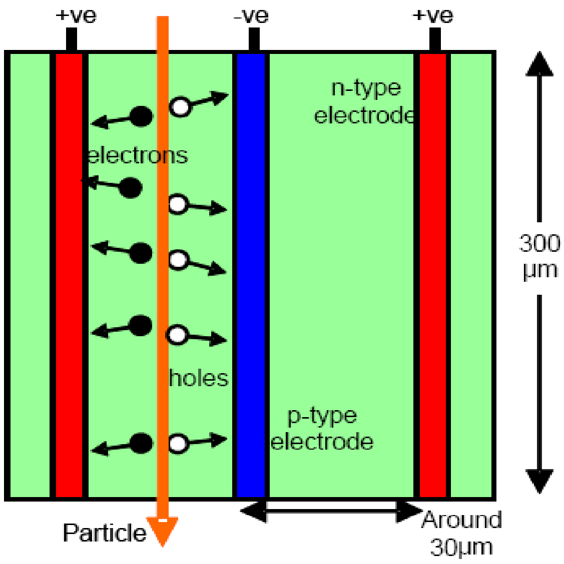
- Proposed by Parker et al. (1995)
- p+ and n+ electrodes are arrays of columns that penetrate into the bulk
- Lateral depletion
- Charge collection is sideways
- Superior radiation hardness due to smaller electrode spacing:
  - smaller carrier drift distance
  - faster charge collection
  - less trapping
  - lower depletion voltage
- No edge termination is required
- Complex, non-standard processing



Planar



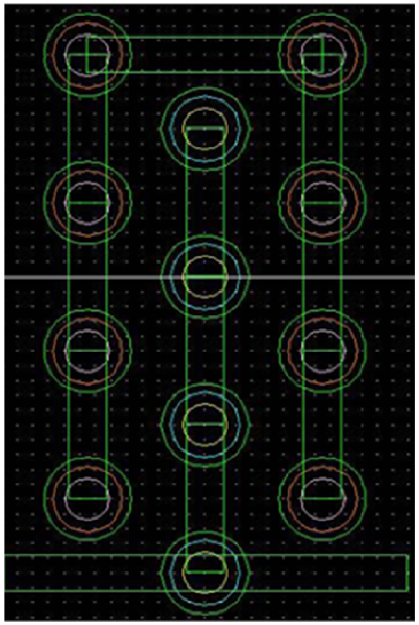
3D



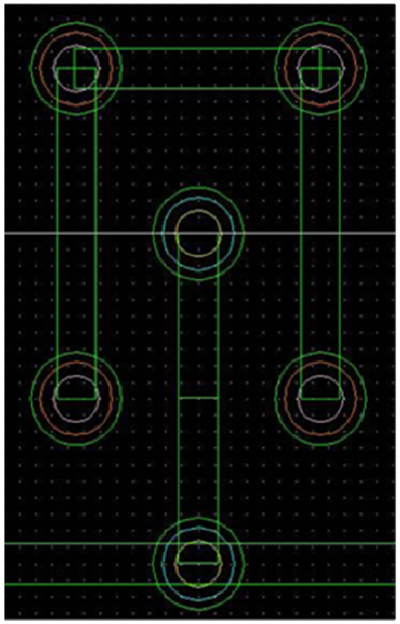
3D CMS Detectors

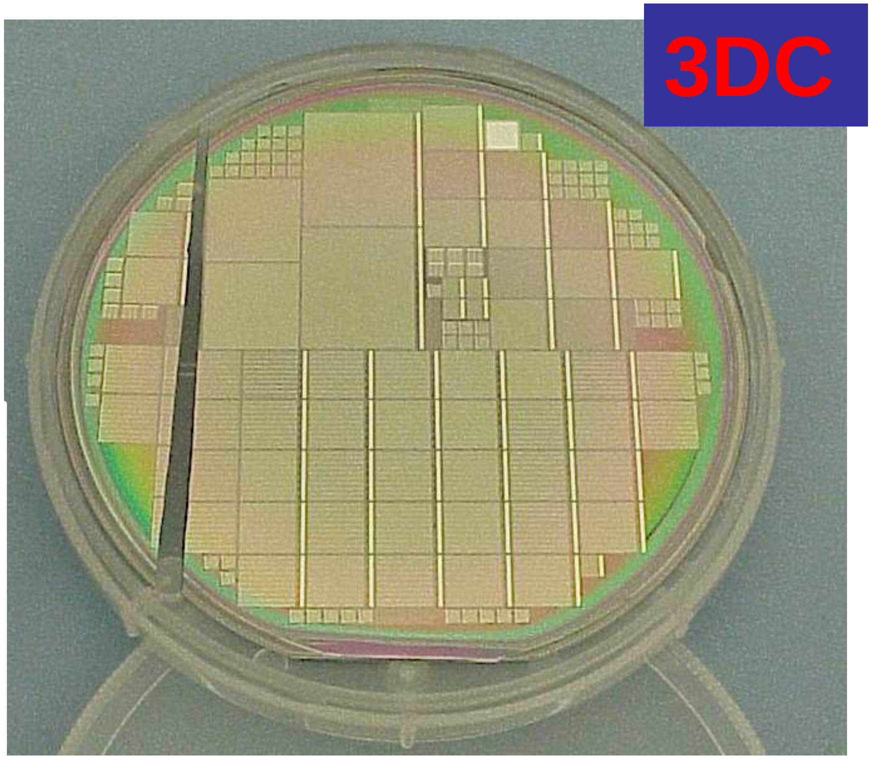
- First 3D detectors fabricated at Stanford Nanofabrication Facility
- Recently processing has been transferred to SINTEF as part of the 3DC collaboration (Stanford is still contributing the polysilicon filling and consulting)
- 3D CMS detectors
  - 2 different layouts
  - fabrication of wafers completed at SINTEF
  - currently 4 wafers have been bump bonded at IZM
  - final removal of support wafer is an issue
  - CMS sensors will be characterized first at Purdue and then with a beam test at FNAL

4 electrodes / pixel



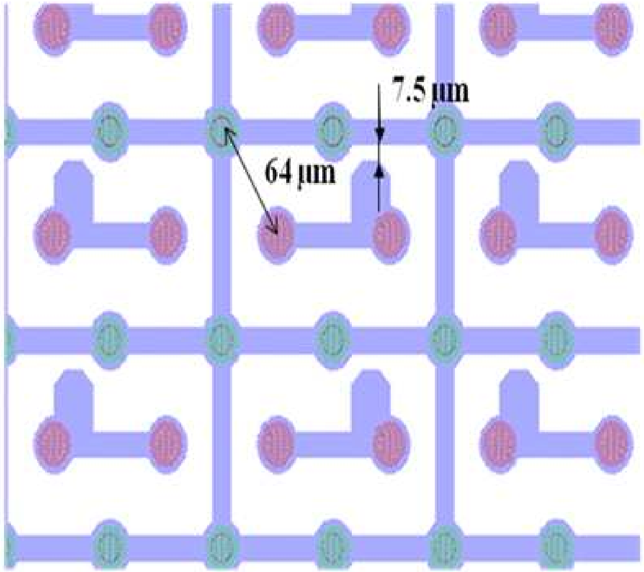
2 electrodes / pixel



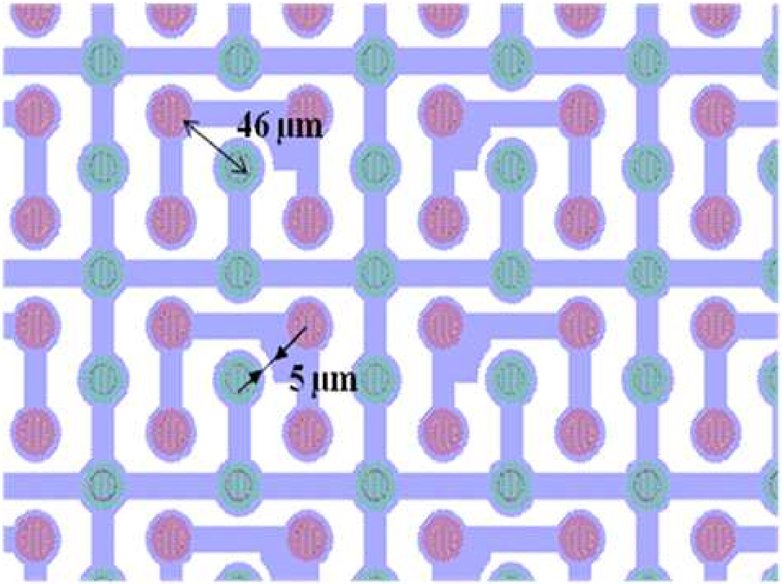


- Substrate thickness = 200, 280µm
- Substrate resistivity > 10000Ω.cm, p-type
- p-spray isolation: 6×10^{12}cm^{-2}, 60keV, through a 60nm oxide. Annealed at 900°C for 30 minutes.

3D Sensors: pixel details



2E configuration



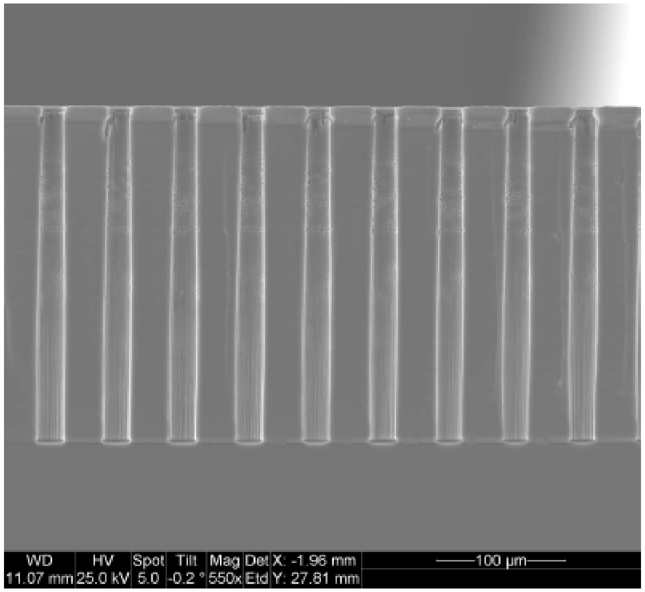
4E configuration

1. **2 and 4 column pixels**
    - **Different distance between n+ and p+ electrode**
2. **Not possible to implement a bias GRID**
    - **Need for a temporary metallization to short all the pixel together**
        - **To be replaced before bumping.**
3. **Devices were simulated with Sentaurus**

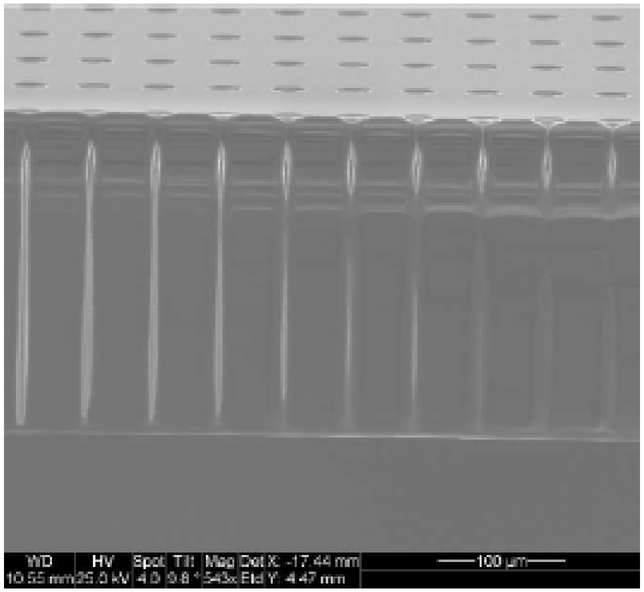
Processing of 3D Detectors at SINTEF

3DC

- p-spray implant
- Wafer bonding by direct fusion bonding
- Deep Reactive ion etching (DRIE) & polysilicon filling and doping of electrodes
  - n-type electrode etching & filling
  - 300nm thermal oxide barrier protection
  - p-type electrode etching & filling
- Metal layer deposition & patterning
- Passivation layer of 0.5µm oxide and 0.25µm nitride deposition by PECVD & patterning

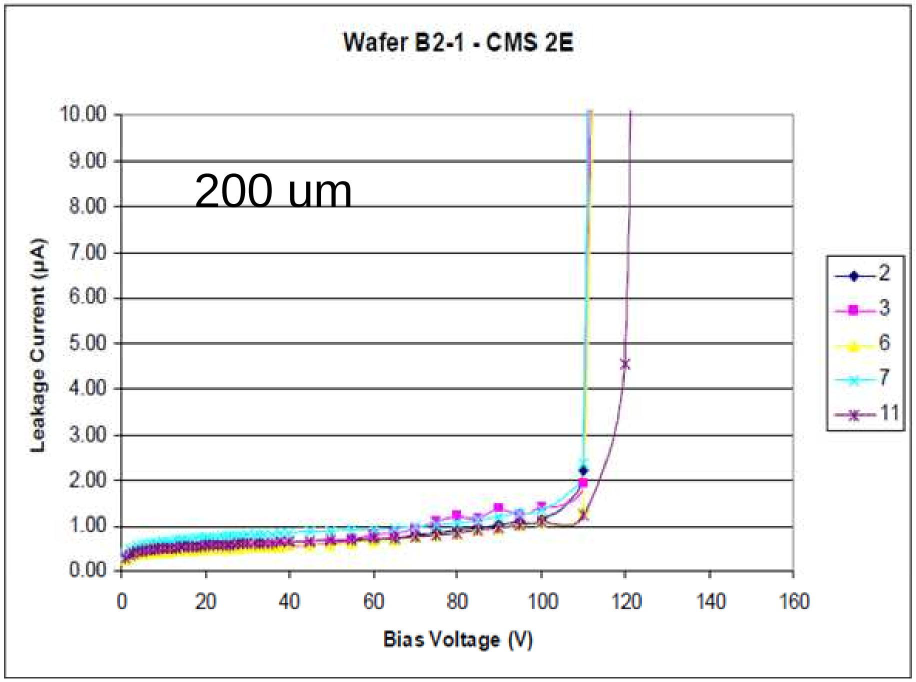


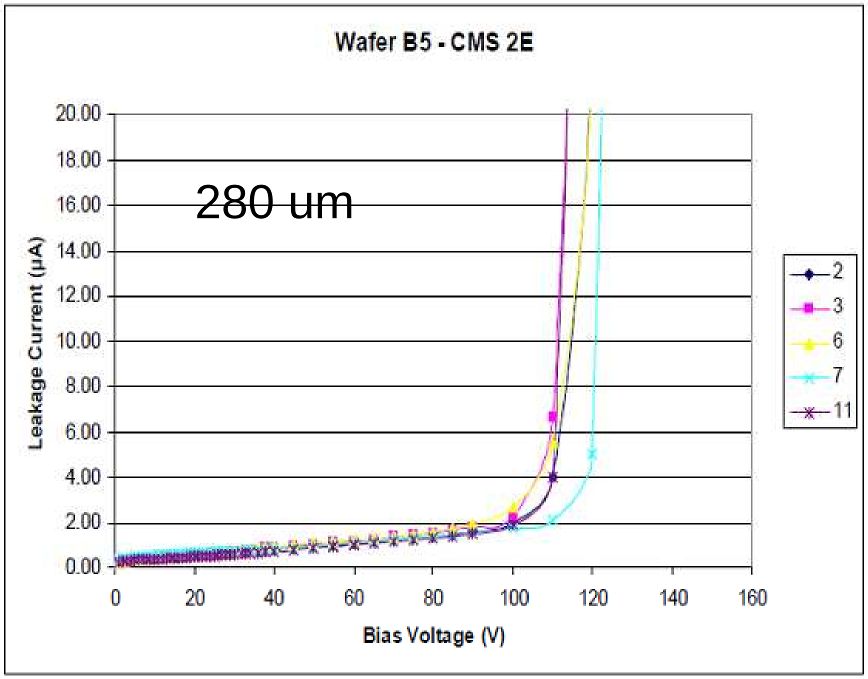
After trench etching



After filling holes with polysilicon

3D Sensors: IV characteristics



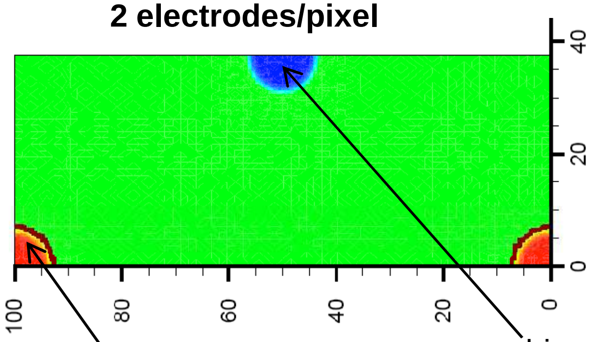


IV measurement made at SINTEF

1. **Leakage current in the order of 1 uA/cm^2 before breakdown (100 nA/cm^2 at V_{dep})**
   - **There is a theory that some of this current might be due to the temporary metal layer**
     - **To be verified after bumping**
2. **Depletion voltage around 15-20 V**

4 electrodes/pixel vs. 2 electrodes/pixel

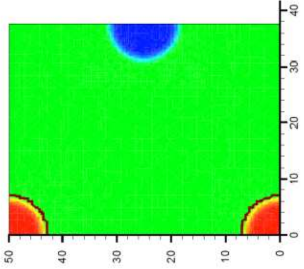
2 electrodes/pixel

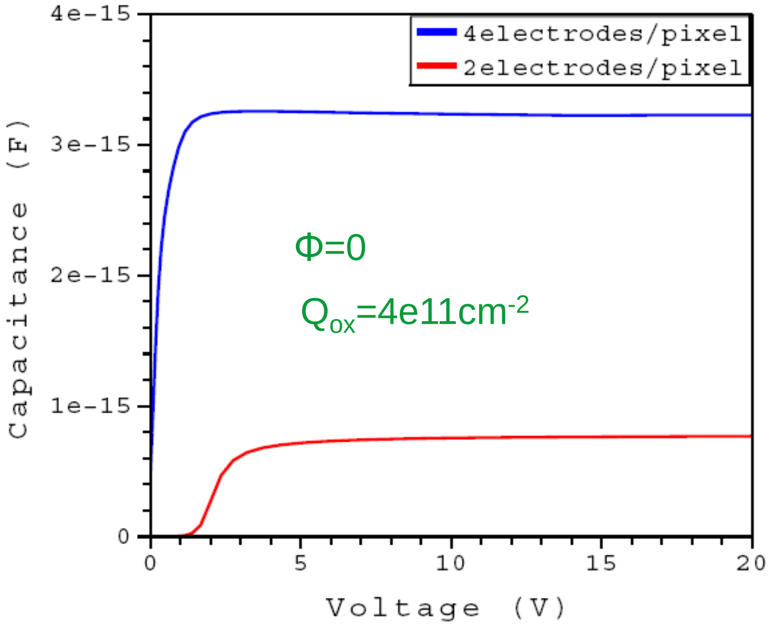


readout (n+)
electrode

bias (p+)
electrode

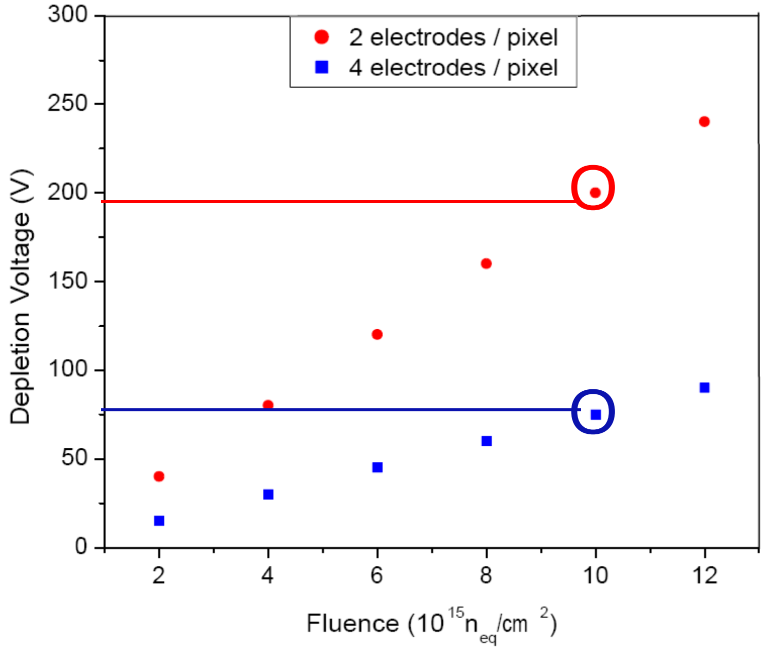
4 electrodes/ pixel

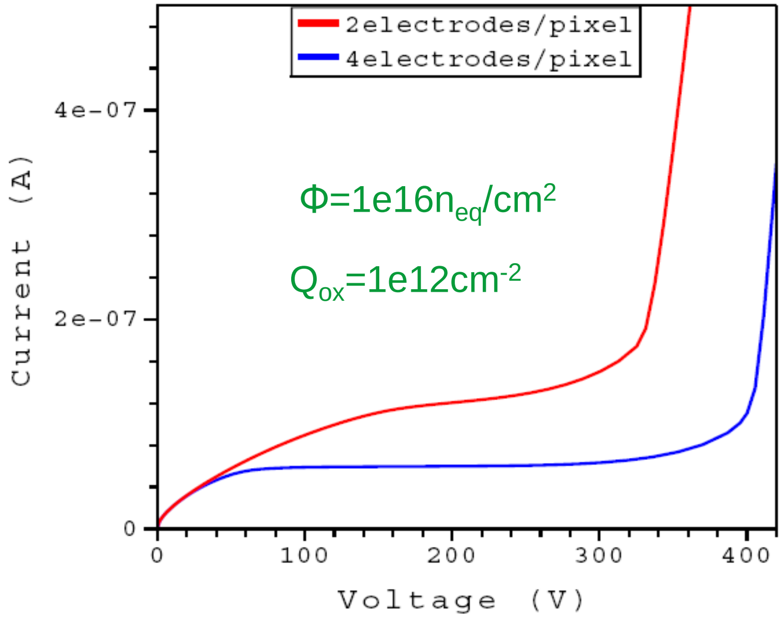




$\Phi=0$

$Q_{ox}=4e11cm^{-2}$





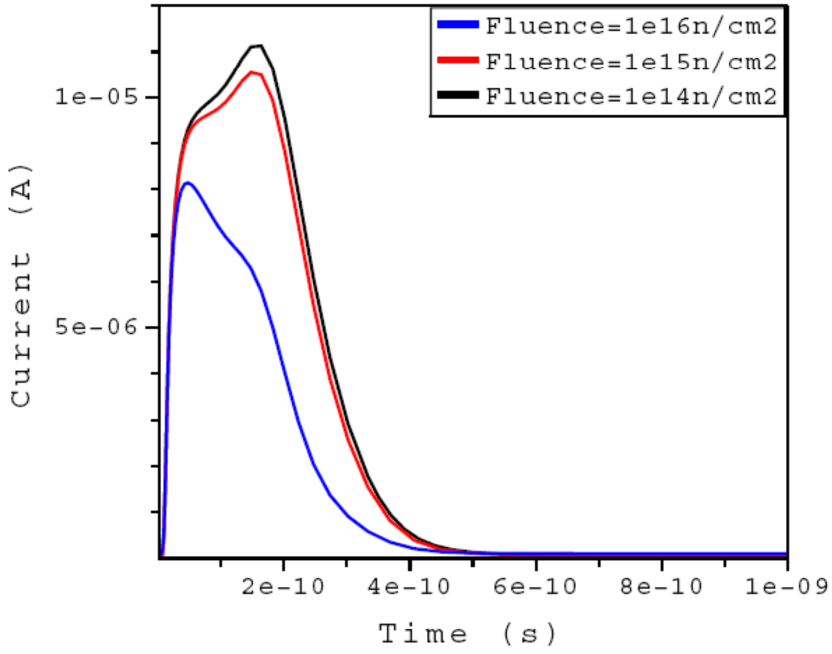
$\Phi=1e16n_{eq}/cm^2$

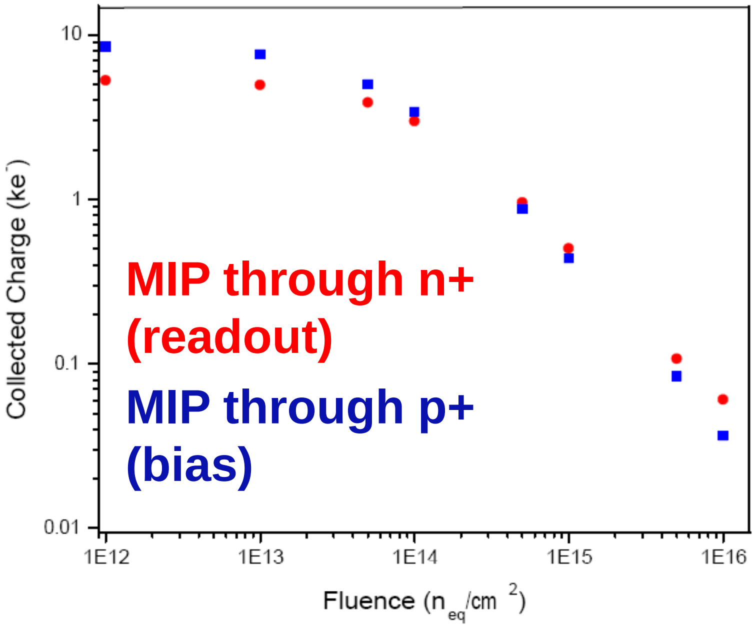
$Q_{ox}=1e12cm^{-2}$

Charge Collection

- Layout: 4 electrodes per pixel
- 200µm substrate thickness
- V_{bias} = -150V
- Minimum Ionizing Particle (MIP):
  - travels vertically through the substrate thickness
  - track generates 80 electron hole pairs per micron
  - Gaussian lateral profile with 1µm standard deviation
  - > 99% of charge generated within a radius of ~2.1µm

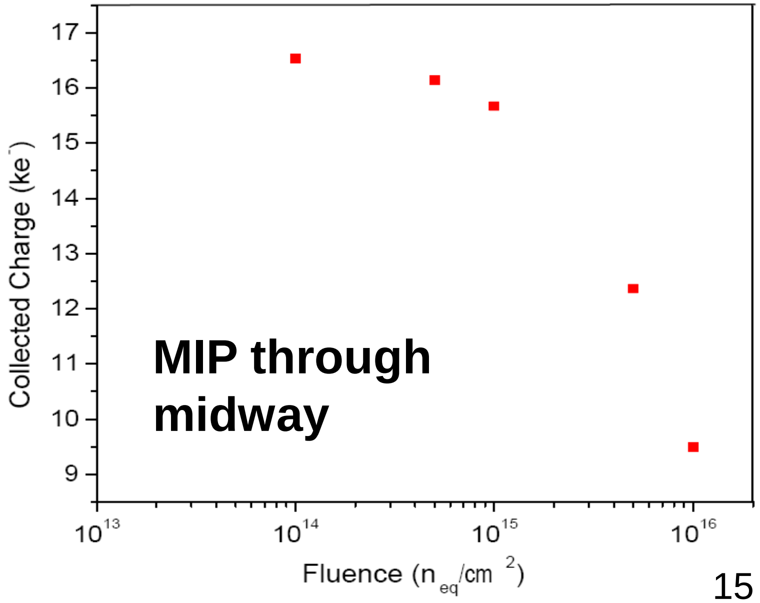
MIP through midway between n+ and p+ electrodes





MIP through n+ (readout)

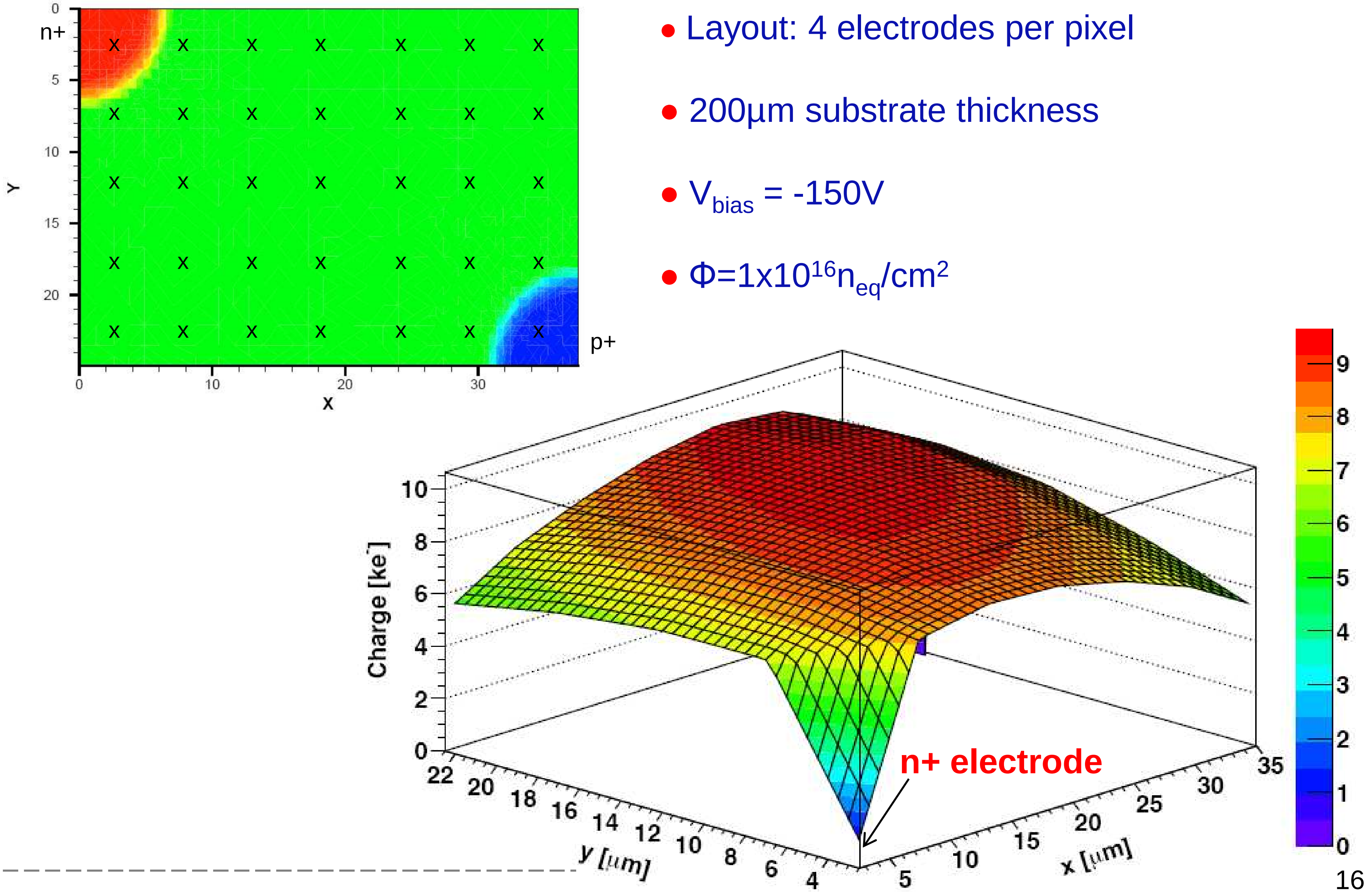
MIP through p+ (bias)



MIP through midway

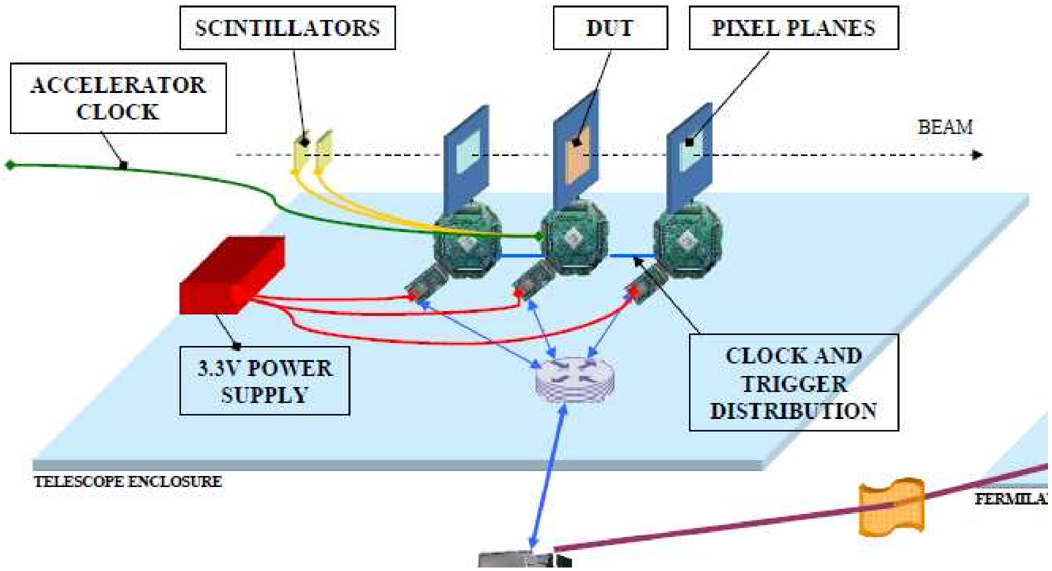
Charge Collection as a Function of MIP Position

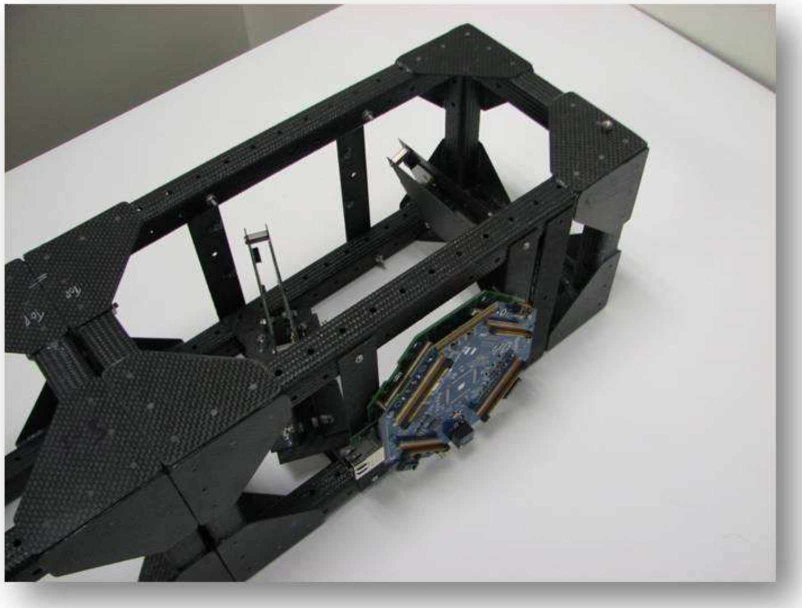
- Layout: 4 electrodes per pixel
- 200µm substrate thickness
- V_{bias} = -150V
- $\Phi = 1\text{x}10^{16} n_{eq}/cm^2$

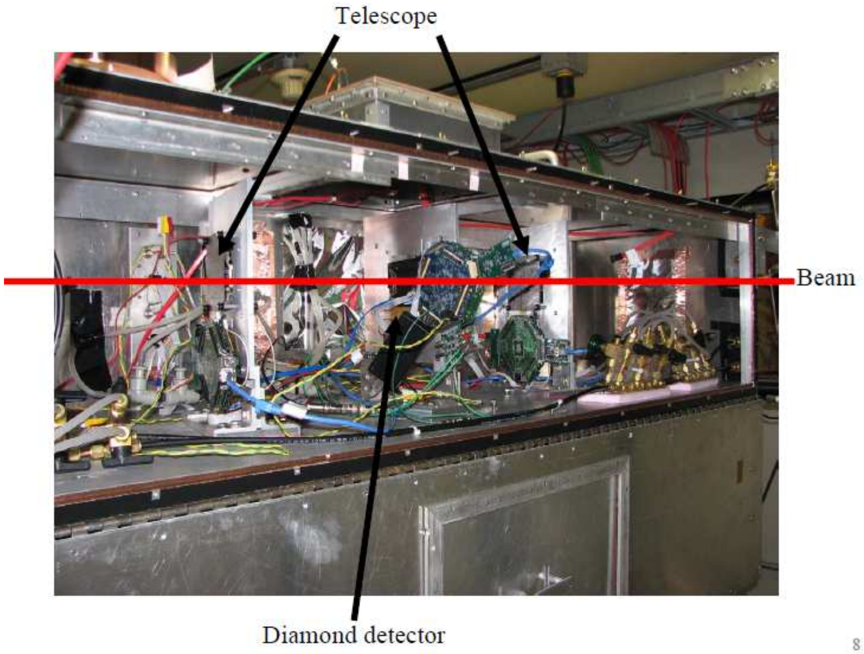


n+ electrode

Beam test at Fermilab







Conclusions

Guard rings for n-on-p sensors :

- Proposed guard ring design with field plates can sustain reverse biases up to ~900V at $\Phi=1e15n_{eq}/cm^2$ and saturated $Q_{ox}=1e12cm^{-2}$.
- Too low breakdown voltages for saturated $Q_{ox} \geq 2x10^{12}cm^{-2}$
- Optimize guard ring structure to give best performance for high oxide charges within the limits of design rules (current structure optimized for $Q_{ox}=4e11cm^{-2}$)
- Polyimide passivation on the top of oxide

3D CMS detectors :

- Columns become dead regions at $\Phi>1e14n_{eq}/cm^2$
- CCE highest in regions between electrodes (~ 9 ke^- at $\Phi=1e16n_{eq}/cm^2$) and lowest near cell edges (~ 5.5 ke^- at $\Phi=1e16n_{eq}/cm^2$)
- 2 columns / pixel geometry:
  - **lower capacitance between readout electrodes (~0.7fF at $\Phi=0$, $Q_{ox}=4e11cm^{-2}$)**
  - **less dead volume (~ 4% of total volume)**
- 4 columns / pixel geometry:
  - **faster charge collection**
  - **less trapping at high fluences**
  - **lower depletion voltage**
  - **higher breakdown voltage**
  - **larger capacitance between readout electrodes (~3.2fF at $\Phi=0$, $Q_{ox}=4e11cm^{-2}$)**
  - **larger dead volume (~ 8% of total volume)**