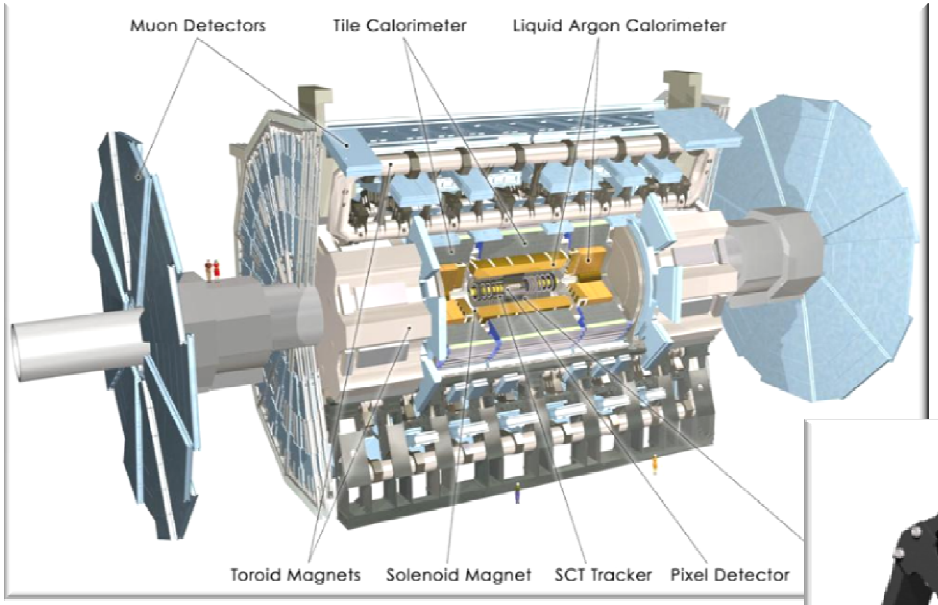
# ATLAS Insertable B-Layer (IBL)

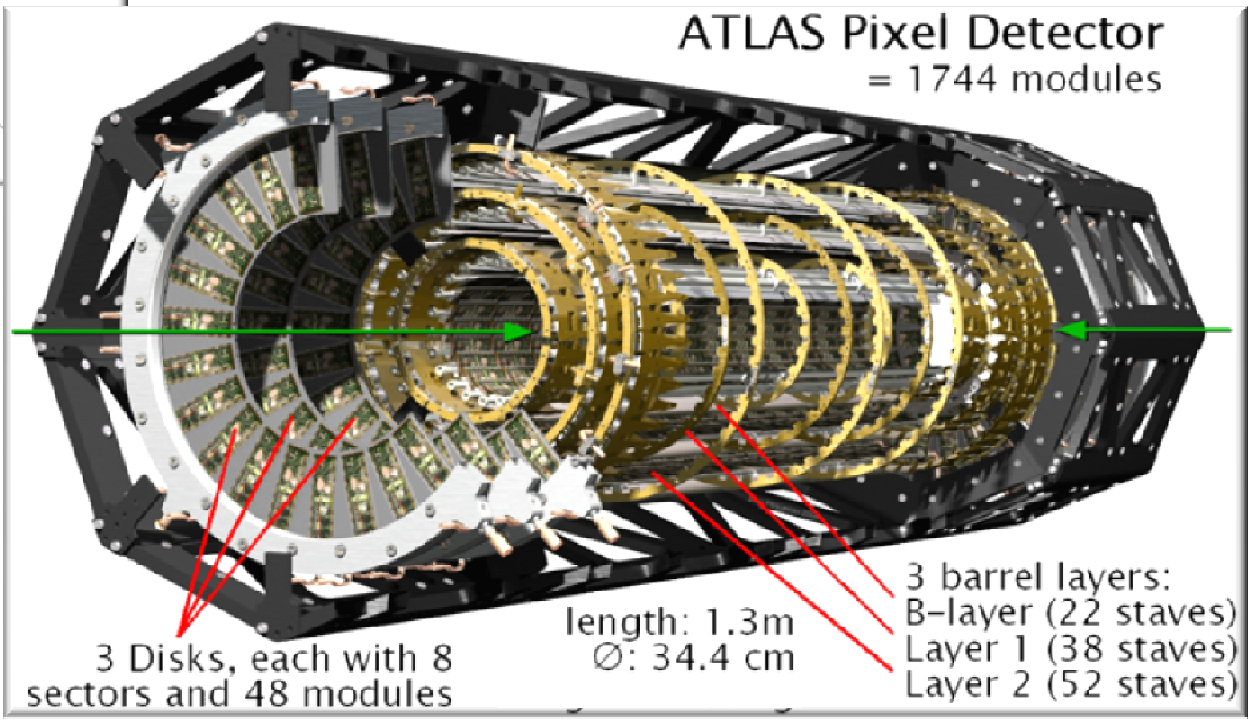
H. Pernegger / CERN

# The present ATLAS Pixel Detector




- 1744 separate pixel modules
- 80 mio. readout channels
- 3 track points down to $|\eta|=2.5$

- 50x400 $um^2$ pixels
- spatial resolution:
  10 um in R-f, 115 um in z
- radiation hardness
  Specs 500kGy ; tested to >1000kGy and 2e15 $n_{eq}$

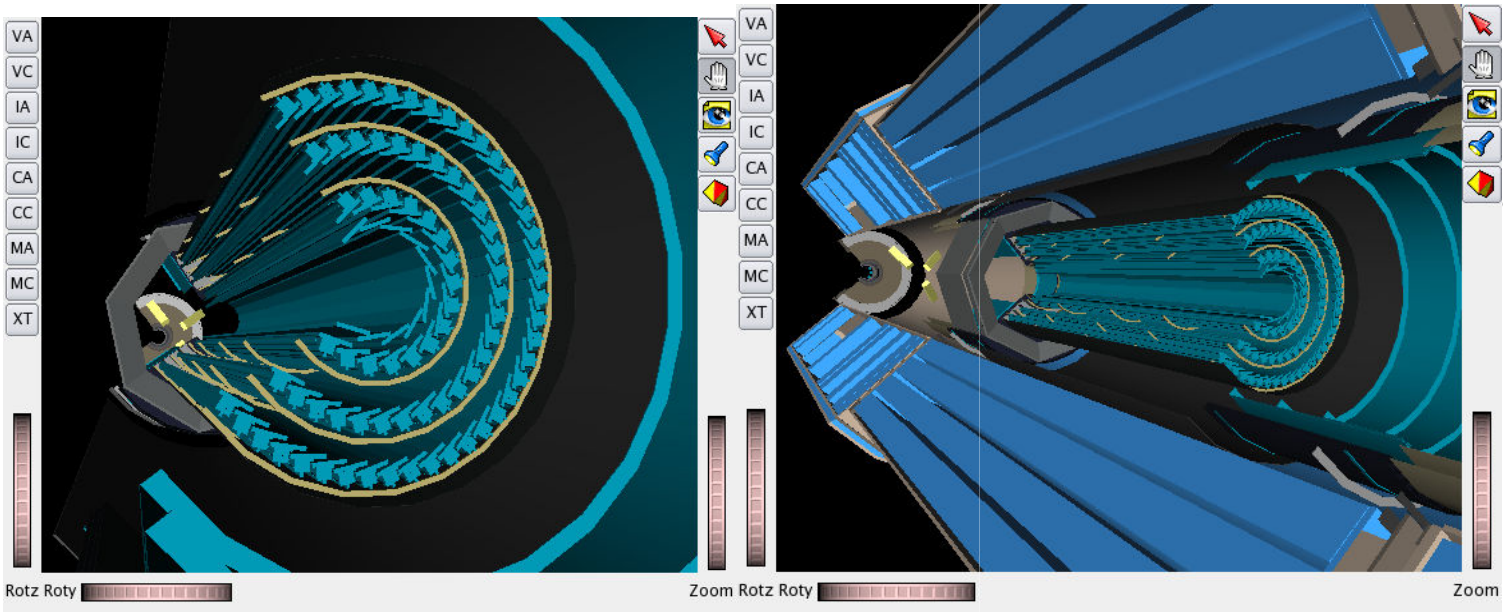


# The 4th Pixel Layer: Insertable B-Layer

- Add a 4th low-mass pixel Layer inside the present B-Layer: **The Insertable B-Layer**
  - Improve performance of existing system + maintain performance when present B-Layer degrades.
  - Existing Pixel detector stays installed and a 4th layer is inserted inside the existing pixel detector together with new beam pipe . (Requires new, smaller radius beam pipe to make space)
  - It needs to be replaced in a 8-months shutdown (~2014/15)
- It serves also as a "**technology step**" from now to sLHC
  - The IBL project will be the first to use much of the **new technologies** currently under development **for sLHC**
  - Radiation hardness ~5 x $10^{15}$ $n_{eq}/cm^2$
  - **Frontend IC4**: go to IBM 130nm process and improve readout architecture
  - **Sensors**: investigate 3D silicon sensors, new planar sensors and CVD diamond
  - **Readout system & optolink:** 160MB/s for data
  - **Cooling system & Mechanics**: develop light-weight support

# IBL Simulation

- Simulation for IBL implemented in present ID
  - Simulated different layouts (sensors facing beam pipe, sensors facing present B-layer,…)
  - Simulation includes standard digitization, PR and track reconstruction
  - Added in simulation Layout description, material map



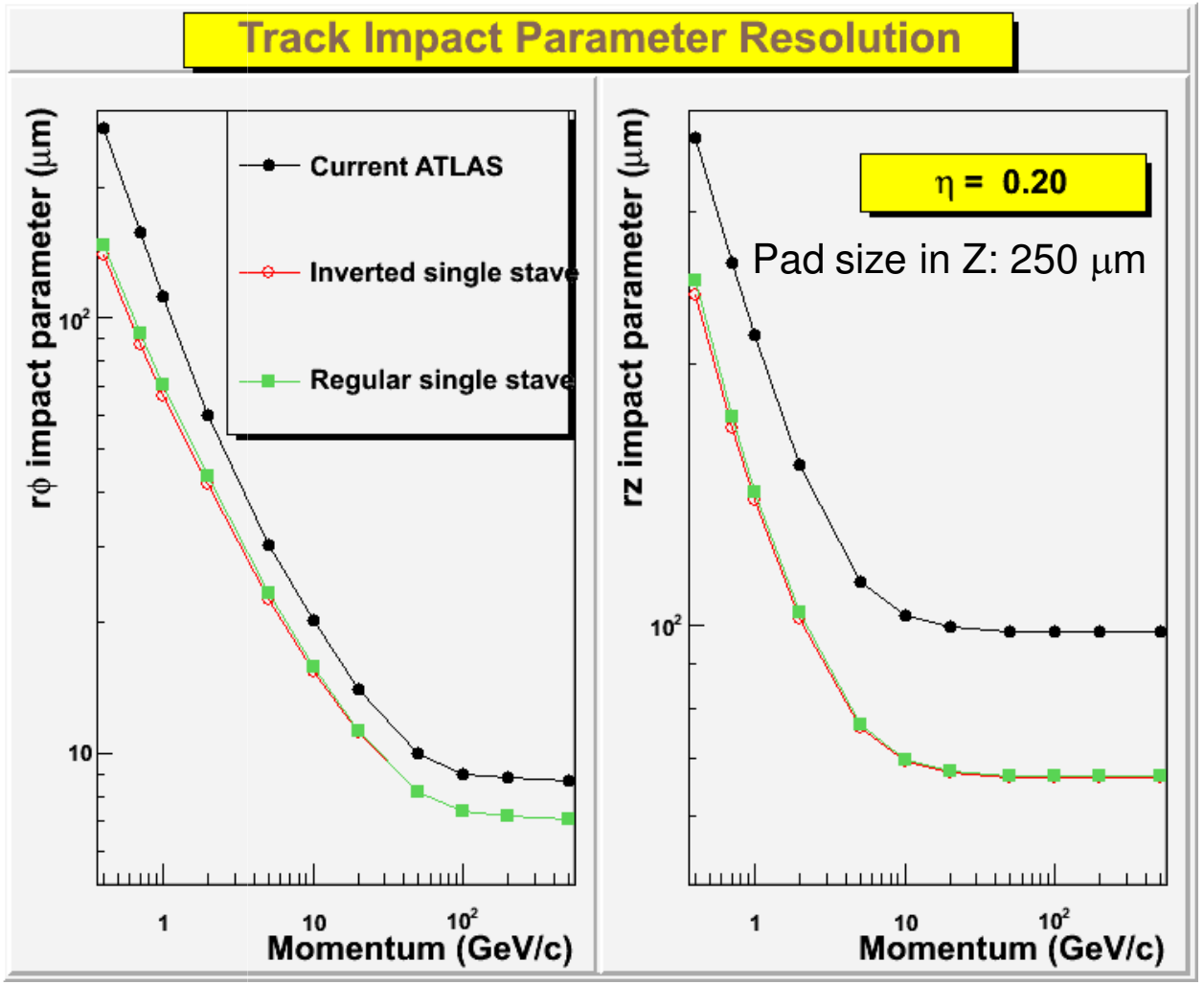

IBL implementation in 15.4.0 release

Pixel disks and beam pipe are removed to show IBL

# IBL Performance

- IP res Z: 100μm->~60μm
- IP res RΦ : 10μm -> 7μm
- B-tagging: Light Jet rejection factor improves by factor ~2
- To maintain Pixel Detector performance with inserted layer, material budget is critical.

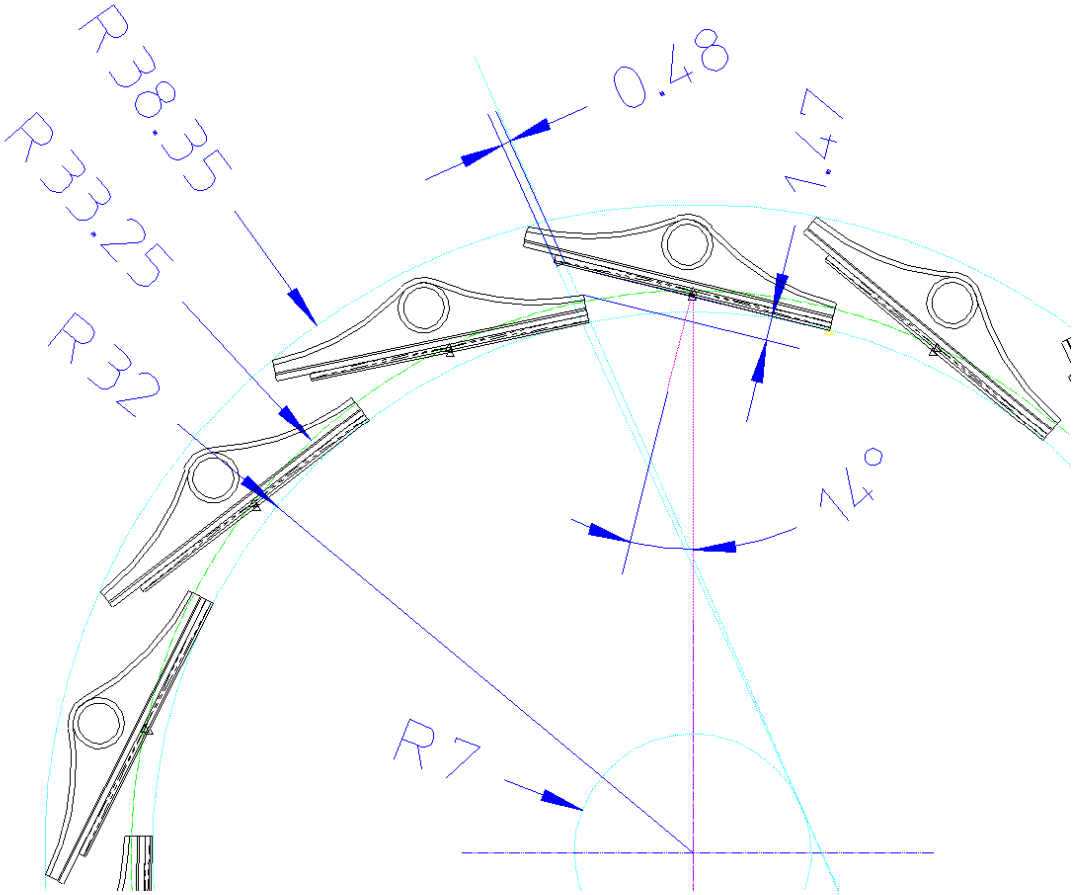
| Component | % $X_0$ |
|---|---|
| beam-pipe | 0.6 |
| **IBL @ R=3.2 cm** | **~1.5** |
| Old BL @ R=5 cm | 2.7 |
| L1 @ R=8 cm | 2.7 |
| L2 + Serv. @ R=12 cm | 3.5 |
| *Total* | *11.0* |



# IBL Layout

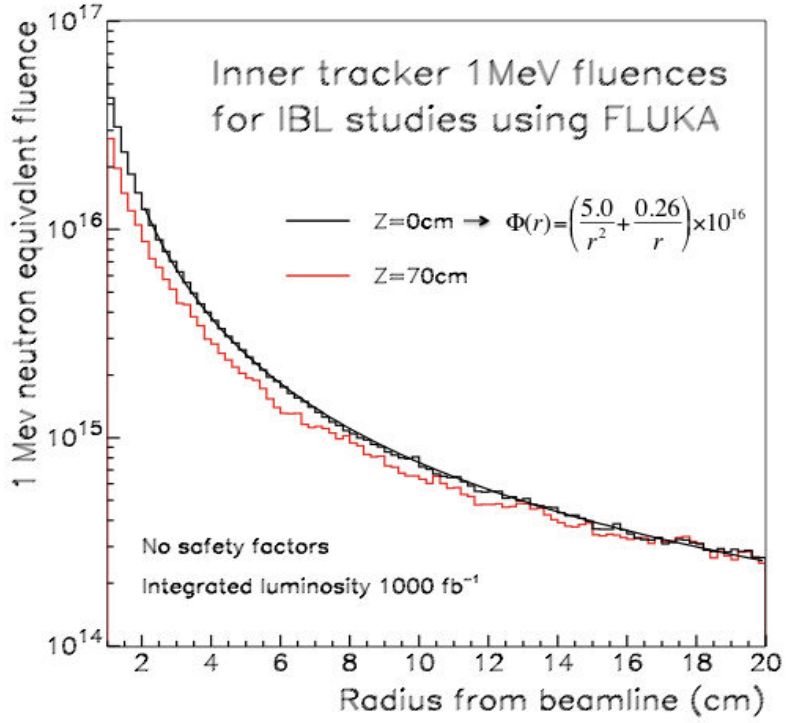
- Converging towards “reverse turbine” layout with 14 staves as baseline layout for engineering studies and TDR:
- Work on others continues at slower pace

- 14 staves – layout parameters
  - IR 32mm
  - OR (structure) 38.35mm
  - Sensor Radius 33.25mm
  - Sensor Tilt Angle 14 degrees
  - Nominal Internal Clearance ~1.47mm
- Proposed tolerances for the stave assembly
  - Geometry tolerance (+/- 0.1mm)
  - Assembly tolerance (+/- 0.15mm)
  - Total tolerance range ½ mm

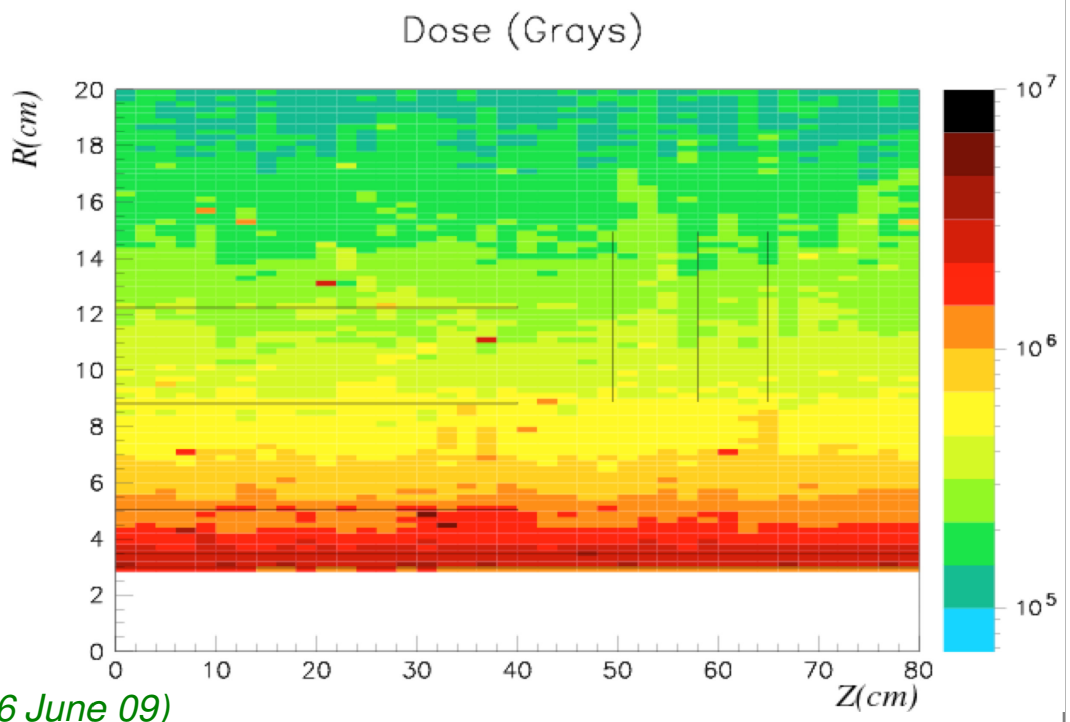


# Requirements for Sensors/Electronics

- Requirements for IBL (sensors/electronics)
  - IBL design Peak Luminosity = $3 \times 10^{34}$ cm$^{-2}$s$^{-1}$ → New FE-I4, higher hit rate
  - Integrated Luminosity seen by IBL = 550 fb$^{-1}$
  - Total NIEL dose ($r_{min}$=3.1cm): $\Phi_{1MeV} = 3.1 \times 10^{15} \pm 30\%$ ($\sigma_{pp}$) ± 50% (sensor damage factor)
- Safety factor for IBL (60%) → design for 5 x $10^{15}$ $n_{eq}$/cm$^2$ → more rad-hard sensors
  - Total ionization dose (TID) > 200 Mrad
- ATLAS Pixel Sensor/FE-I3 designed for $10^{15}$ $n_{eq}$/cm$^2$ / 50 Mrad



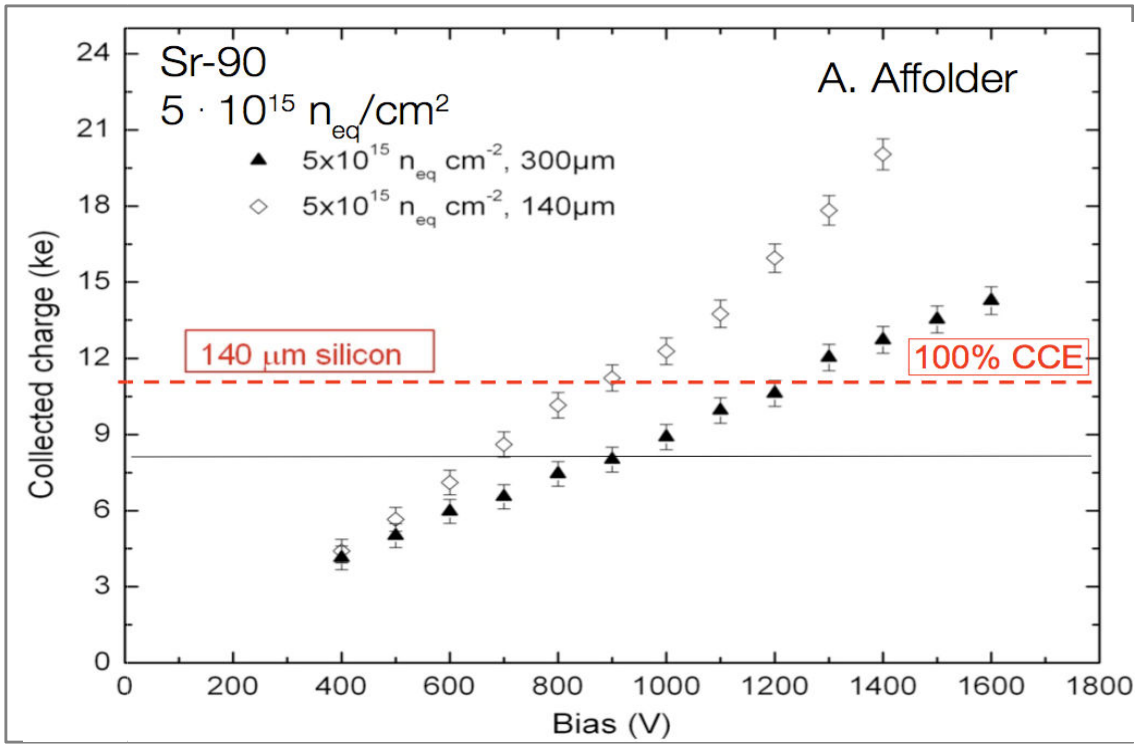

1MeV and TID for integrated luminosity of 1000 fb$^{-1}$




*Ref. Ian Dawson – ATLAS IBL General Meeting (25-26 June 09)*

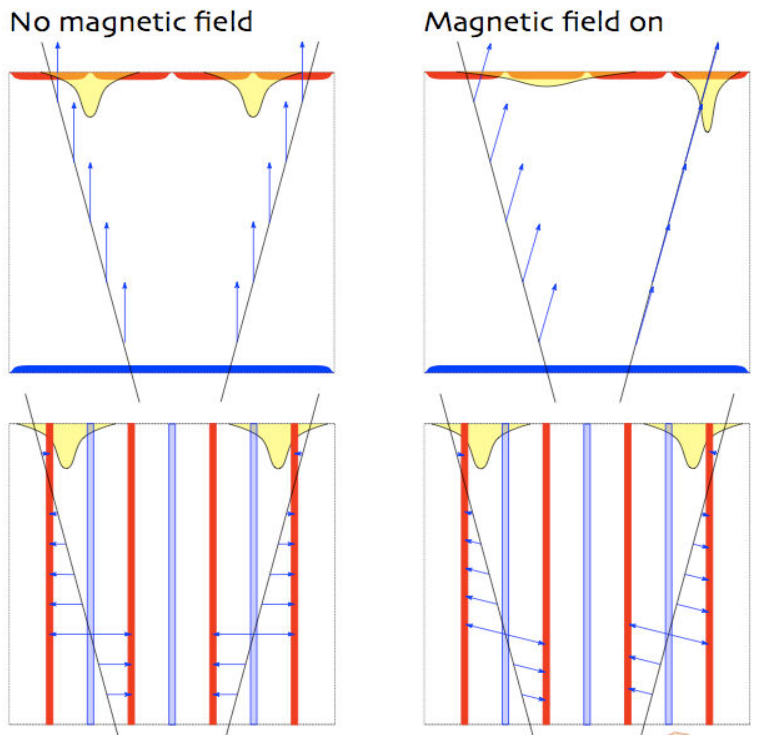
# Planar Sensors – Slim Edge

- Planar sensor prototyping for IBL
  - Large numbers of new results with strips and diodes (RD50) promise enough CCE for IBL
- Parameter optimization under study – what the best trade-off for IBL parameters?
  - Detector bias
    - Present pixel $V_{bias}$=600V, looking at implication of higher $V_{bias}$ (1000÷1500V)
  - Optimize guard ring (geometrical inefficiency in Z) for slim edge
    - 300÷500 µm look feasible
  - Reduce thickness: more charge collected for given $V_{bias}$, lower bulk current
    - 250 is the standard, 200÷220 µm looks feasible, 140µm would be attractive



# 3D Sensors - Test Beam

- Jun.09 test beam: 1 ATLAS Pixel planar, 1 3D SINTEF/Stanford (full column), 2 FBK partial double columns (FBK 3EM5 has low breakdown @ 10V)
  - For inclined tracks 3D sensors have similar efficiency and spatial resolution as planar – No Lorentz angle effect in 3D sensor
  - Active edge (STA) show efficiency up to 5÷10μm from edge
- Very good collaboration between 3D sensor producers:
  - Two meetings (Jun'09, Sep'09)

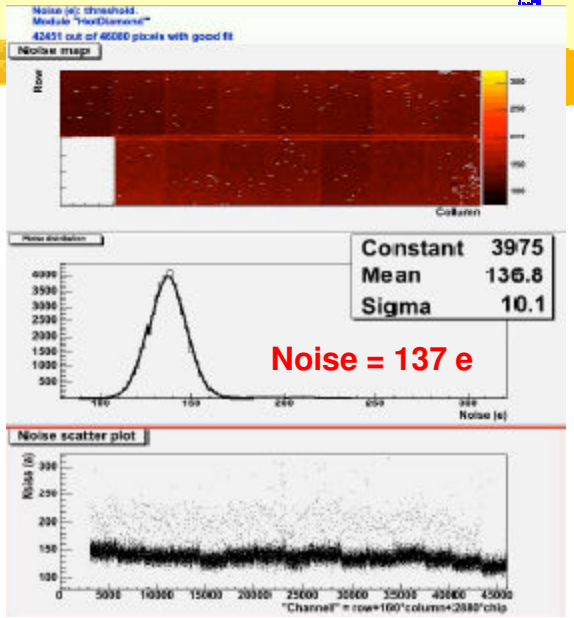


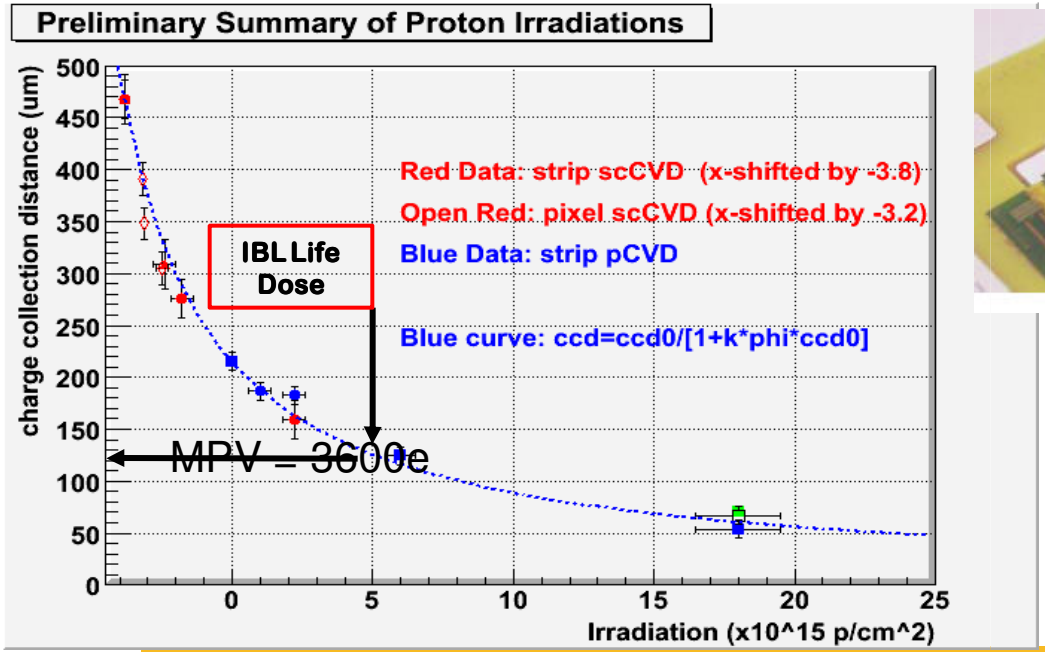

*Ref.: O. Rohne – Vertex 2009*

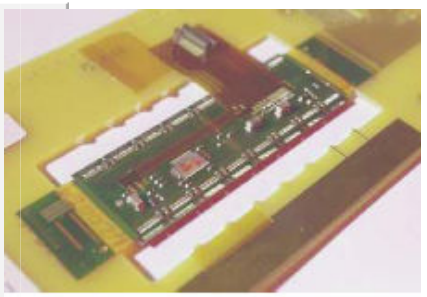
| | Hit efficiency (%) | | RMS (μm) | | | |
|---|---|---|---|---|---|---|
| | B = 0.0 T | | B = 0.0 T | | B = 1.4 T | |
| | $\phi = 0°$ | $\phi = 15°$ | $\phi = 0°$ | $\phi = 15°$ | $\phi = 0°$ | $\phi = 15°$ |
| Planar | 99.9 | 99.9 | 13.8 | 9.7 | 10.2 | 10.4 |
| STA 3E | 96.7 | 99.8 | 14.3 | 10.8 | 13.9 | 9.8 |
| FBK 3E7 | 99.0 | 99.8 | 14.0 | 10.4 | 13.5 | 9.7 |
| FBK 3EM5 | 90.2 | 97.7 | 15.4 | 11.9 | 14.8 | 11.3 |

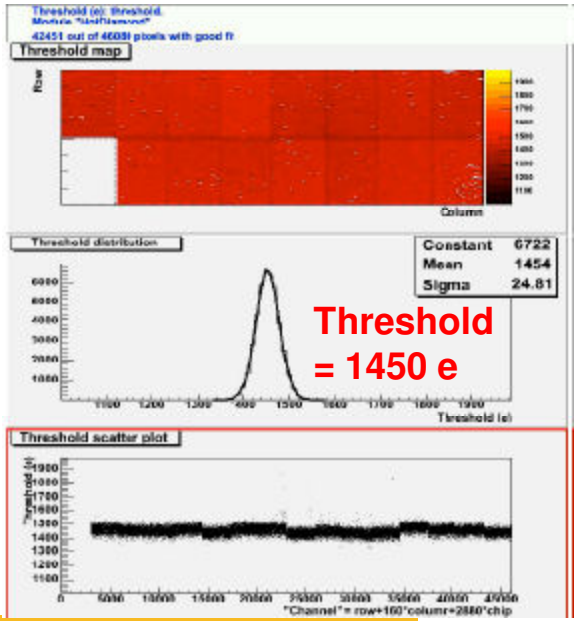
# Diamond

- Diamond advantages:
  - Small capacitance → low noise (140e vs 180e of planar); possible lower threshold operation (1500e)
  - Operation with no cooling: no leakage current
- Three full-size modules built, more prototypes in 2010, >14 FEI4 modules planned for next year



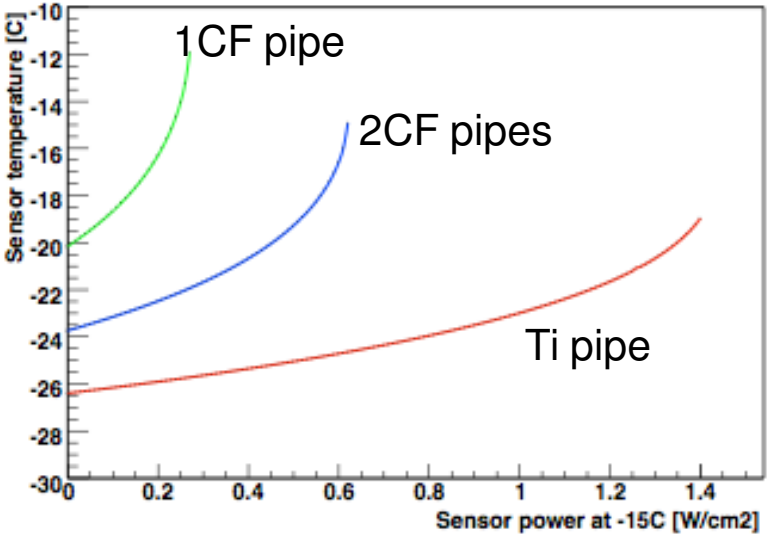





# IBL Sensor & Module

- Bring the 3 detector technologies together for 2010 IBL module qualification program: Planar, 3D, CVD diamonds
  - Proposal is to construct 40 IBL qualification modules with each sensor technology to test FEI4 and sensor (lab, testbeam, irradiation)

Thermal run-away with different staves




| |
|---|
| **Sensor maximum operation voltage: 1000V** |
| **Sensor maximum power dissipation: 200mW/cm$^2$** |
| **Sensor thickness: 225 +/- 25 μm** |
| **Sensor target temperature: ~ -15C** |
| **Coolant temperature: ~ -30C or less** |

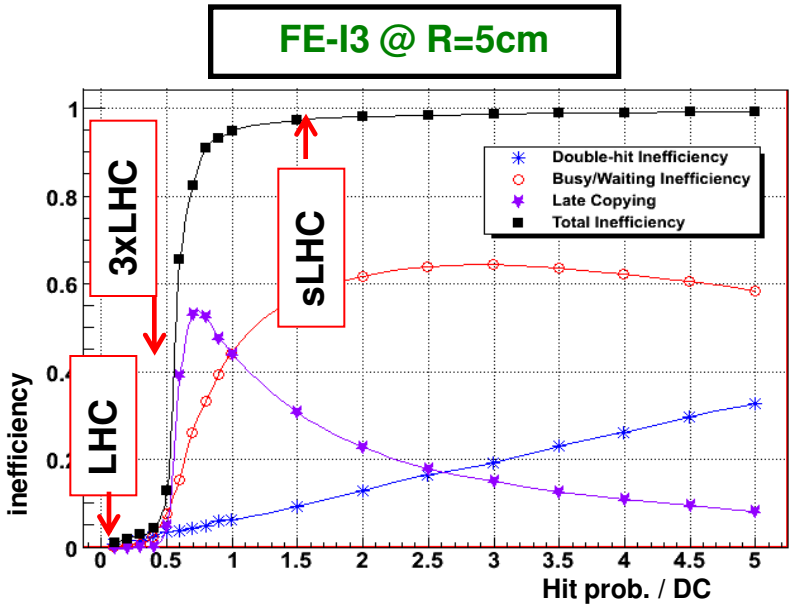
# Sensors

- **Planar sensors**
  - Sensor parameters (previous slide) considered ok for planar sensors (annealed) up to 5 x $10^{15}$ neq/$cm^2$
  - Currently look at different layouts for IBL (final 2-chip module)
    - "conservative" n-in-n with ~ 500μm guard ring area
    - More "advanced" n-in-n with slim edge (~100μm) or thin (~150μm) sensors (n-in-n and n-in-p)
  - FEI4-compatible sensors in production at different vendors (CIS, Micron)
- **3D sensors**
  - Prefer full 3D active edge sensors for IBL (as single chip modules) (2E on 50x250μm)
  - 2010 prototyping runs of full 3D active edge at Sintef/Stanford, CNM, FBK
  - Additional double sided 3D with slim edge at CNM and FBK
  - Study "charge multiplication" at higher voltages (~250V)
- **Diamonds**
  - Have assembled 3 full size (16chip FEI3) modules and study in testbeam
  - Plan to prototype 11 FEI4-single chip and 3 FEI4-double modules next year
    - Sensors for that available and/or on order
  - Present vendor DDL and investigate new vendor "II-VI" (US)

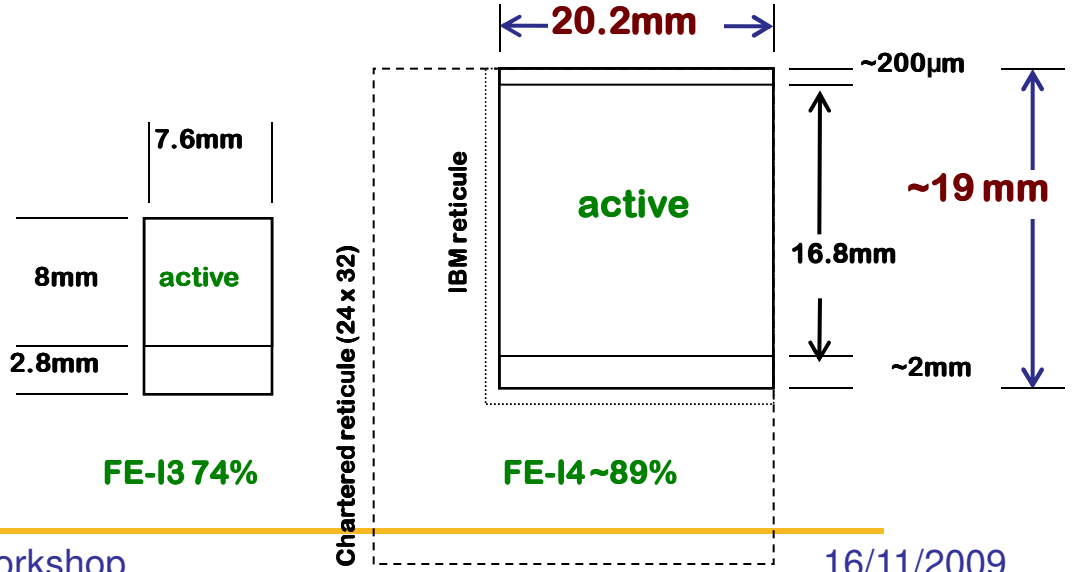
# New Pixel Front-End Chip: FEI4

- Reasons for a new FE design:
  - Increased radiation hardness
  - New architecture to reduce inefficiencies ($\mathcal{L}$=3xLHC)
- New FE-I4
  - Pixel size = 250 x 50 μm²
  - Pixels = 80 x 336
  - Technology = 0.13μm
  - Power = 0.5 W/cm² (max) , 0.25 W/cm² (nominal)
- FE-I4 Design
  - Contribution from 5 laboratories: Bonn, CPPM, INFN Genova, LBNL, Nikhef

"Busy" inefficiency: with FEI3 at LHC = 0.08% but with IBL 3%!

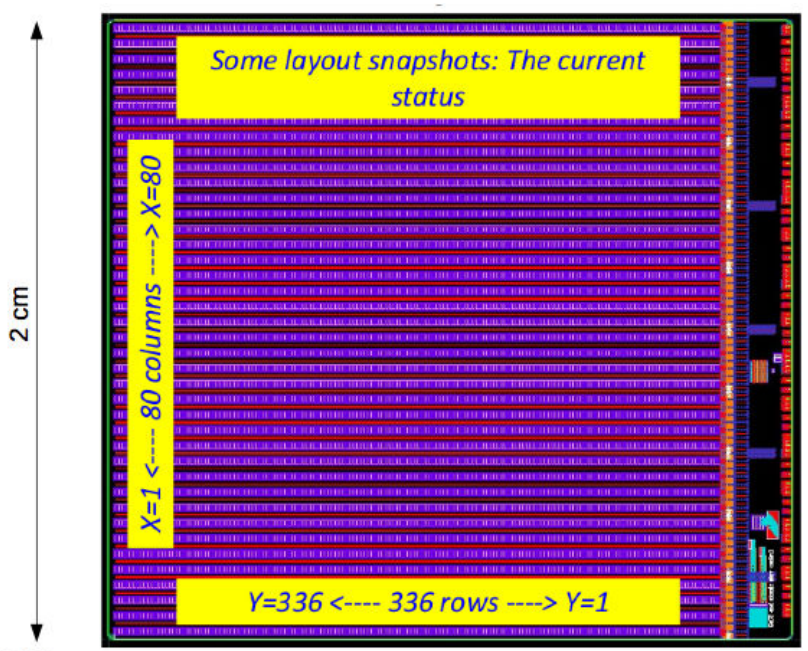



| | FE-I3 | FE-I4 |
|---|---|---|
| Pixel Size [μm²] | 50×400 | 50×250 |
| Pixel Array | 18×160 | 80×336 |
| Chip Size [mm²] | 7.6×10.8 | 20.2×19.0 |
| Active Fraction | 74% | 89% |
| Analog Current [μA/pix] | 26 | 10 |
| Digital Current [μA/pix] | 17 | 10 |
| Analog Voltage [V] | 1.6 | 1.5 |
| Digital Voltage [V] | 2 | 1.2 |
| pseudo-LVDS out [Mb/s] | 40 | 160 |



# FEI4 Chip Status

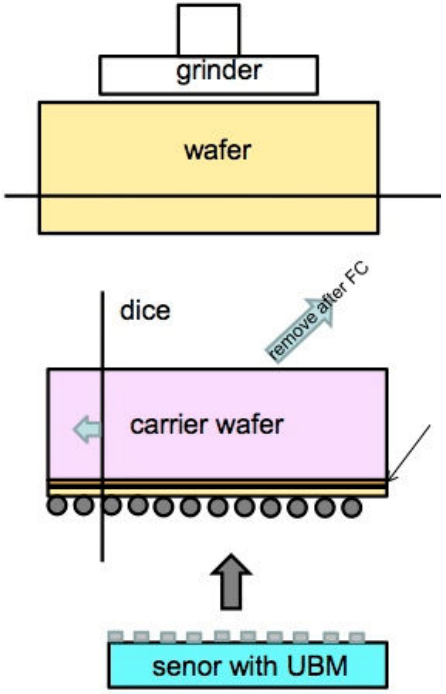
- Review Nov 3-4
  - http://indico.cern.ch/conferenceDisplay.py?confId=72160
- Status of internal blocks
  - All are designed and most have final or near final layouts
  - Total of 24 circuit blocks produced by 14 designers
  - Approximately 100M transistors
- Status of integration
  - Complete pixel array done and partially verified + Schematics for full chip advanced but not yet complete
  - Simulation from full chip schematics started
  - test setup development for wafers and single chip modules progressing, incl. FEI4 emulator
  - Dec:new design kit include “T3” substrate isolation (analog & digital ground separation) - Re-verify entire chip with new design kit

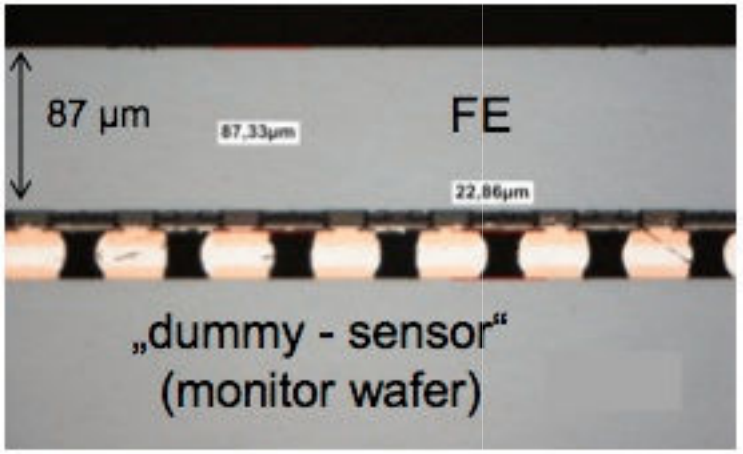



- Present timeline:
- Submission ~ Feb
- Wafers back May

# Bump bonding of thin large chips

- "old style" bump bonding would require chip thickness of 300-350 μm for FEI4-size (chips bow under bonding process)
- Started bump-bonding tests with IZM using a carrier wafer:
  - Tested with 2x2 FEI3: 14x23mm (~88% physical size of FEI4) thinned to 90μm




ATLAS FE (thickness 90μm) after flip chip assembly and carrier chip release

- Results
  - Chip bow appears acceptable
  - Bonds good also on edge
- Encouraging results for bump-bonding of large area thin chips
- Gain up to 0.3% X0

# FEI4 - Module qualification program

- Plan to construct qualification modules with each technology during 2010
  - Goal is to qualify the prototype modules in lab, beamtests and irradiations to IBL specs and gain production experience (yields,…)
  - Orignal plan is ~40 modules/technology with sensors provided by sensor RD groups from recent submissions
  - This program is of common interest to sensor RD groups and IBL
    - Cost of those modules is substantial (i.e. also bump bonding) and need to be shared in a reasonable way between communities.
- Common sensor “foot print”
  - To unify (and simplify) module construction and bump bonding, we have to make sure we have a common foot print of sensors (at least with technology)
- **Submission: Feb 2010**
  - Receive wafers: early May
- Send wafer and sensor to bump-bonding: mid June
  - need sensors by beg. June
- **Receive first qualification modules mid Aug. 2010**
- Proceed in parallel with lab tests, testbeam and irradiation.

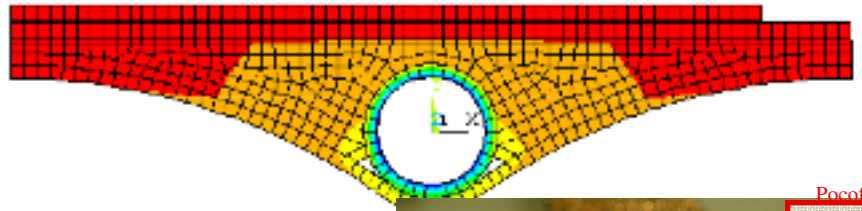
# Off-detector

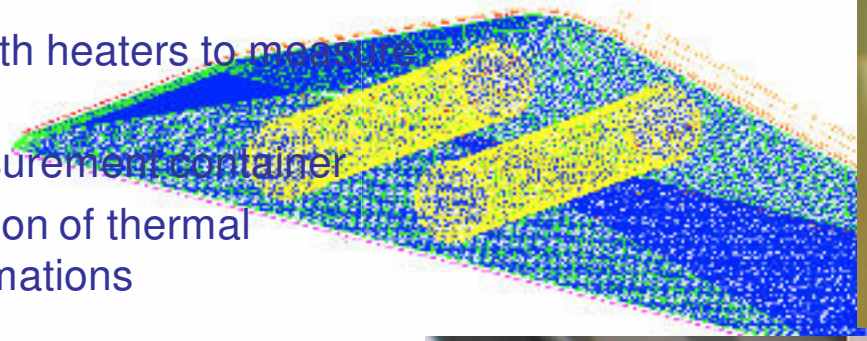
- Opto signal transmission
  - Testing available DORIC and VDC chips for signal transmission with IBL specs (160Mb/s)
  - Dedicated test bench available and running to test signal integrity with internal cable prototypes and opto chips
  - Testing data transmission over ~ 6m electrical at 160Mb/s before conversion to optical (old system ~1m electrical)

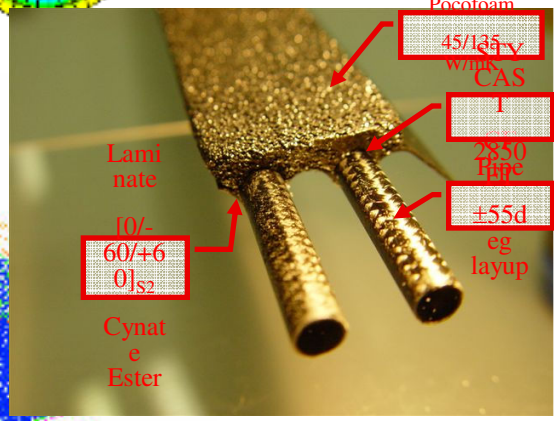

- BOC/ROD readout:
  - See http://indico.cern.ch/conferenceDisplay.py?confId=68905
  - Baseline with VME-based system with BOC/ROD redesigned but with “pixel infrastructure” (ATLAS LTP, TIM, VME system)
  - Need to keep an eye on the required SW developments and integration to pixel system

# IBL Stave

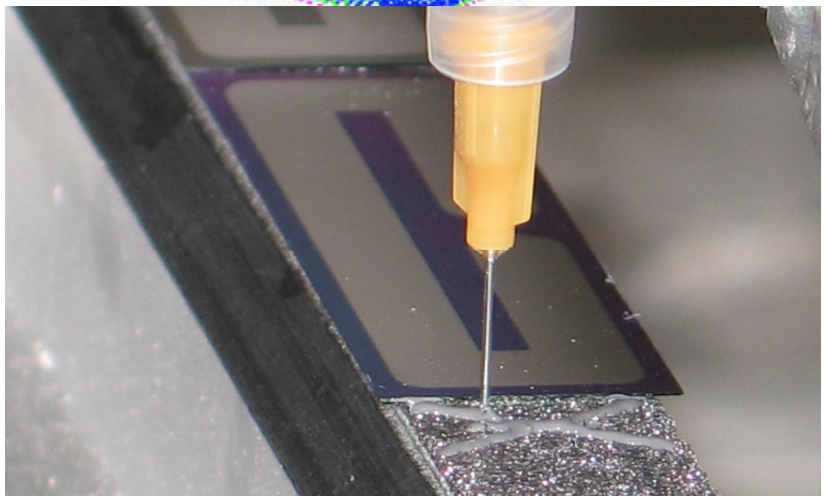
- Minimize X0 !!!
- Stave Construction:
  - CF shell + Carbon foam
  - Pipe diameter 2 to 3mm (OD)
- Stave thermal performance
  - Constructed first staves with heaters to measure thermal figure of merit
  - Constructed thermal measurement container
  - Very detailed FEA simulation of thermal gradients and stave deformations
- Pipe : CF & Ti
  - Constructed samples of pipe+heater to measure coolant to pipe heat transfer coefficient with C3F8 and CO2
  - Started with tests on Ti pipe welding and bending and made first CF-Ti transitions
  - Starting off on pipe irradiation to qualify CF pipe against micro-cracks








Picture 2: Mesh



# 2010 Stave qualification program

- Defined draft stave qualification program for 2010
  - Cooling pipe: qualification of CF and Ti pipe
    - Micro-cracks
    - Welds
  - Connections: pipe-pipe transitions and connectors at PP1
  - Stave CF and foam: measurement of thermal figure of merit and deformation under cooling
  - Flex circuit: design and prototypes of flex circuit (Kapton Cu/Al?)
    - Layout , X0 and connectivity to mini-flex on FEI4
    - Connectors on EoS

| | Item description | Flavor | | |
|---|---|---|---|---|
| | | Pipe Material | Pipes diameter (and number) | Samples Number |
| 2.1 | Stave | 1.1 (CF) | Φ=4mm OD N=2 | 1 |
| 2.2 | | 1.2 (Ti) | Φ=4mm OD N=1 | 2 of (4) |
| 2.3 | | 1.1 (CF) | Φ=4mm OD N=1 | 4 [on hold] |
| 2.4 | | 1.4 (Ti) | Φ=3mm OD N=1 | 2 |
| 2.5 | | 1.3 (CF) | Φ=3mm OD N=1 | 2 |
| 2.6 | | 1.3 (CF) | Φ=3mm OD N=2 | 2 |
| 2.7 | | 1.6 (Ti) | Φ=2mm OD N=1 | 2 |
| 2.8 | | 1.6 (Ti) | Φ=2mm OD N=2 | 2 [on hold] |
| 2.9 | | 1.7 (CF) | Φ=2mm OD N=2 | 2 [on hold] |
| 2.01 | Bi-stave | 1.3 (CF) | Φ=3mm OD N=2 | 2 |
| 2.02 | | 1.6 (Ti) | Φ=2mm OD N=2 | 2 |
| 2.9 | Pipe + foam+heaters | 1.1 (CF) | Φ=4mm OD | 1 of (2) |
| 2.10 | Pipe + foam+heaters | 1.2 (Ti) | Φ=4mm OD | 1 |
| 2.11 | Pipe + foam+heaters | 1.3 (CF) | Φ=3mm OD | 1 |
| 2.12 | Bare Pipe | 1.4 (Ti) | Φ=3mm OD | 1 |
| 2.13 | Bare pipe | 1.6 (Ti) | Φ=2mm OD | 2 |
| 3.01 | Short stave [L=80mm] | 1.3 (CF) | Φ=3mm OD N=1 | 8 |
| 3.02 | | 1.4 (Ti) | Φ=3mm ID N=1 | 8 |
| 3.03 | | 1.6 (Ti) | Φ=2mm ID N=1 | 8 |

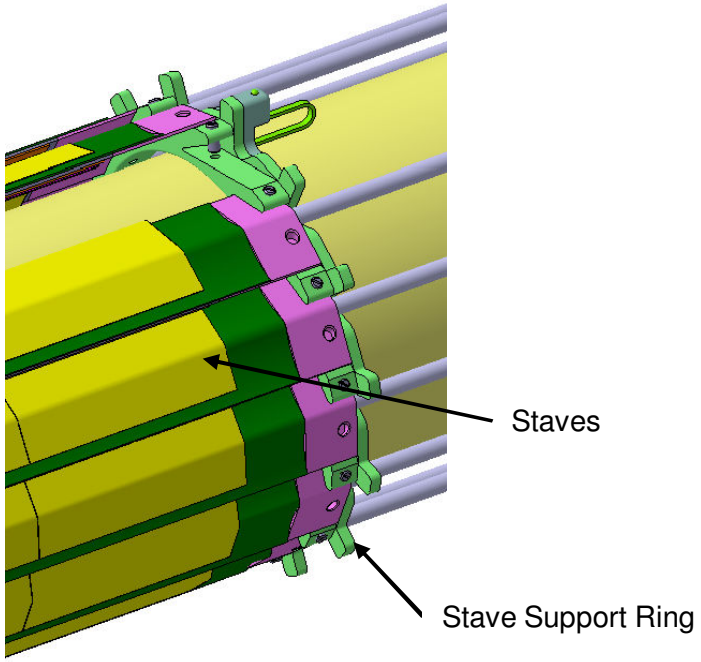
- Plan to review in December of the Stave Prototyping program in 2010

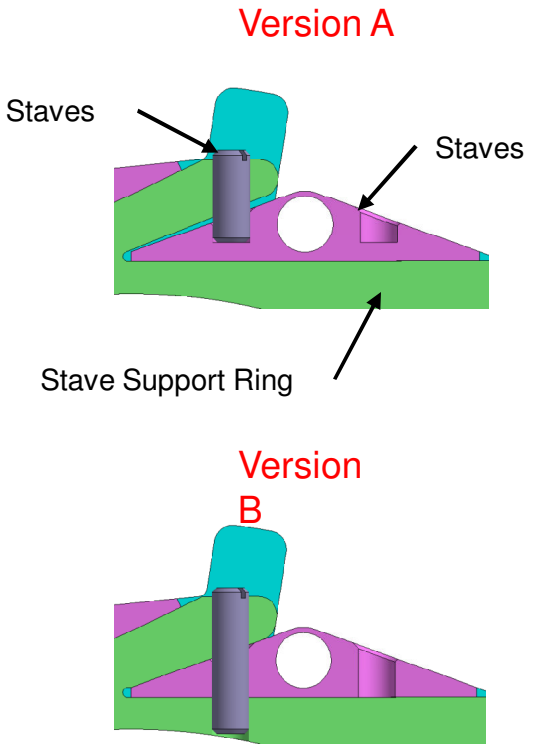
| | Omega [um] | Foam [g/cm$^3$] | Pipe [Mat + ID] | Coolant | X/X0 [%] | | Γ [°C.cm$^2$/W] | Grav sag [μm] | ThermalDef [μm] |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Structure +Coolant | TOTAL | | | |
| Option 1 | 150 | 0.5 | CF 2.5ID | $C_3F_8$ | 0.48 | 0.88 | 17.25 | 97 | 63 |
| Option 2 | 150 | 0.25 | CF 2.5ID | $CO_2$ | 0.36 | 0.78 | 18.56 | 75 | 50 |
| Option 3 | 300 | 0.25 | Ti 3ID | $C_3F_8$ | 0.66 | 1.1 | 2.79 | 44 | 58 |
| Option 4 | 300 | 0.25 | Ti 2ID | $CO_2$ | 0.57 | 0.99 | 3.22 | - | - |

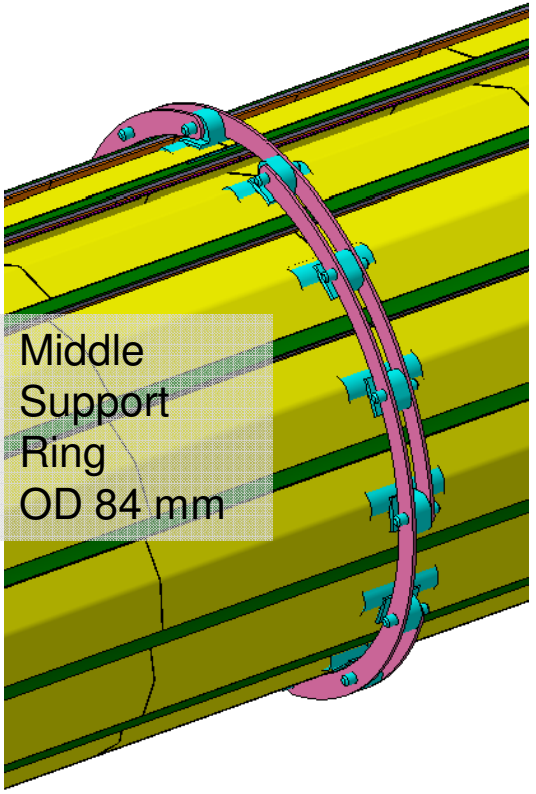
| Component | X/X0 |
|---|---|
| Stave (incl. FE+sens ~340μm) | Range 0.8 to 1.1 % |
| Flex (under evaluation) | Range 0.1 to 0.2 % |
| IST | 0.3% |
| **Total** | **~1.2% (lightest) to 1.6% (heaviest)** |

# Stave mounting

- Currently developing concepts for stave mounting based on a full 3D model of the IBL
  - FEA simulations for vibration and deflection and positioning
  - Next step is to implement 3D model of internal services and EoS cards

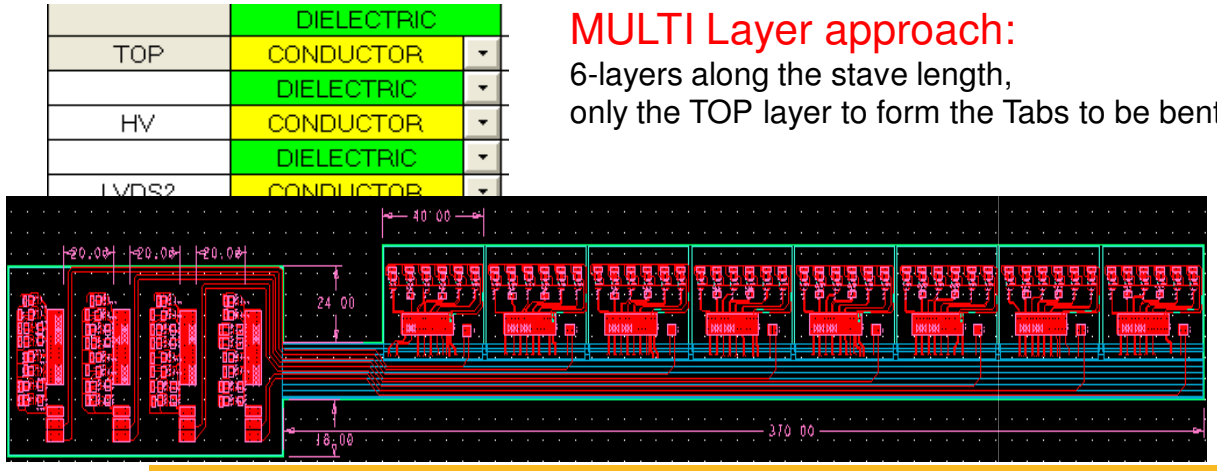


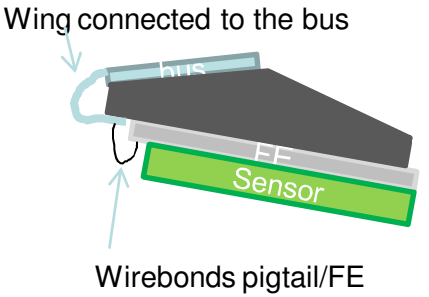



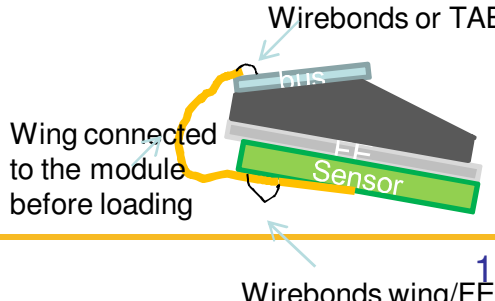
# Flex circuit

- One of highest priorities now is to define concept for flex circuit and connection to modules
  - Drives layout to some extend (envelops)
  - Need to achieve and **optimal layout for stave mechanics AND flex circuit**
- Proposed baseline is to have multilayer bus with tabs to connect to modules
  - Prototype in production
  - Single layer approach is still developed further in case its needed
  - Connection to FEI4/miniflex not yet clear (several options)



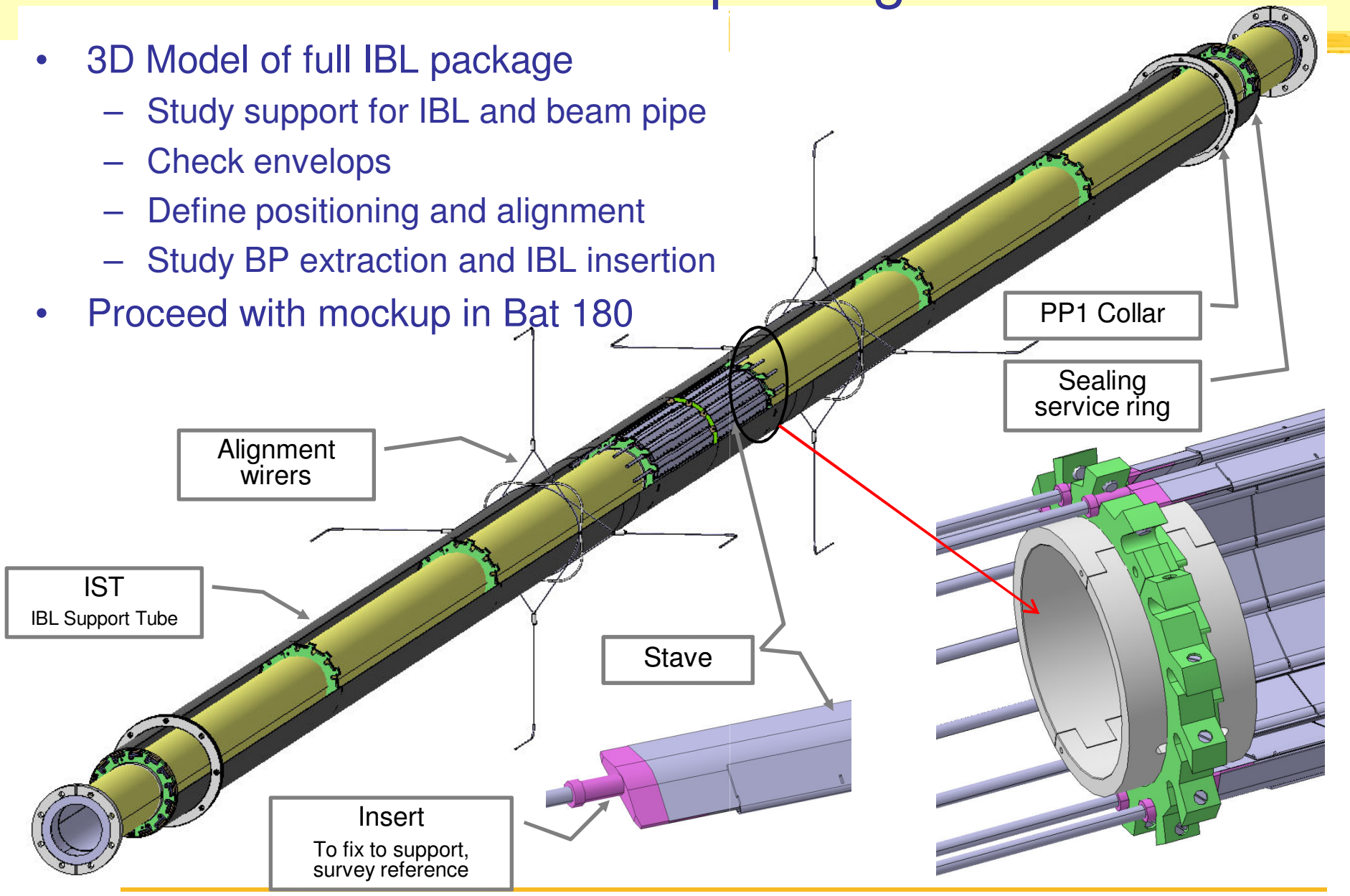

MULTI Layer approach:
6-layers along the stave length,
only the TOP layer to form the Tabs to be bent.



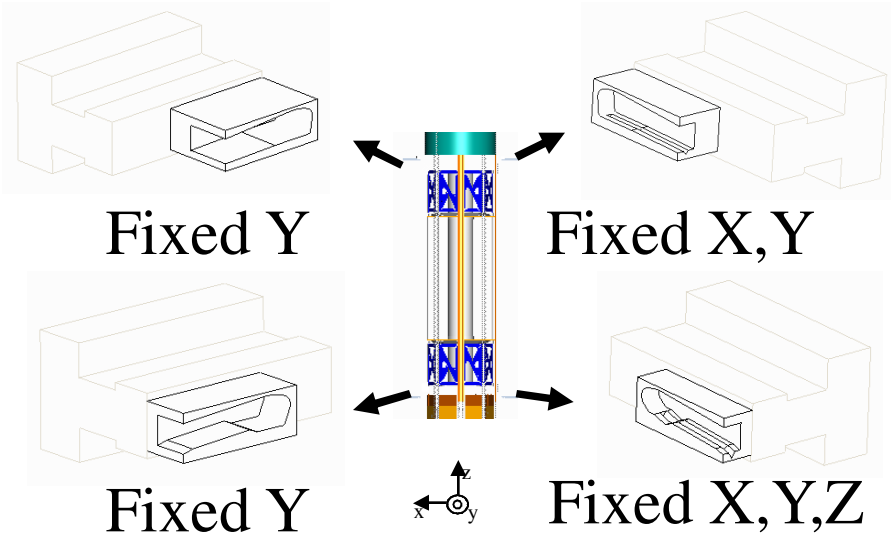
# IBL full package

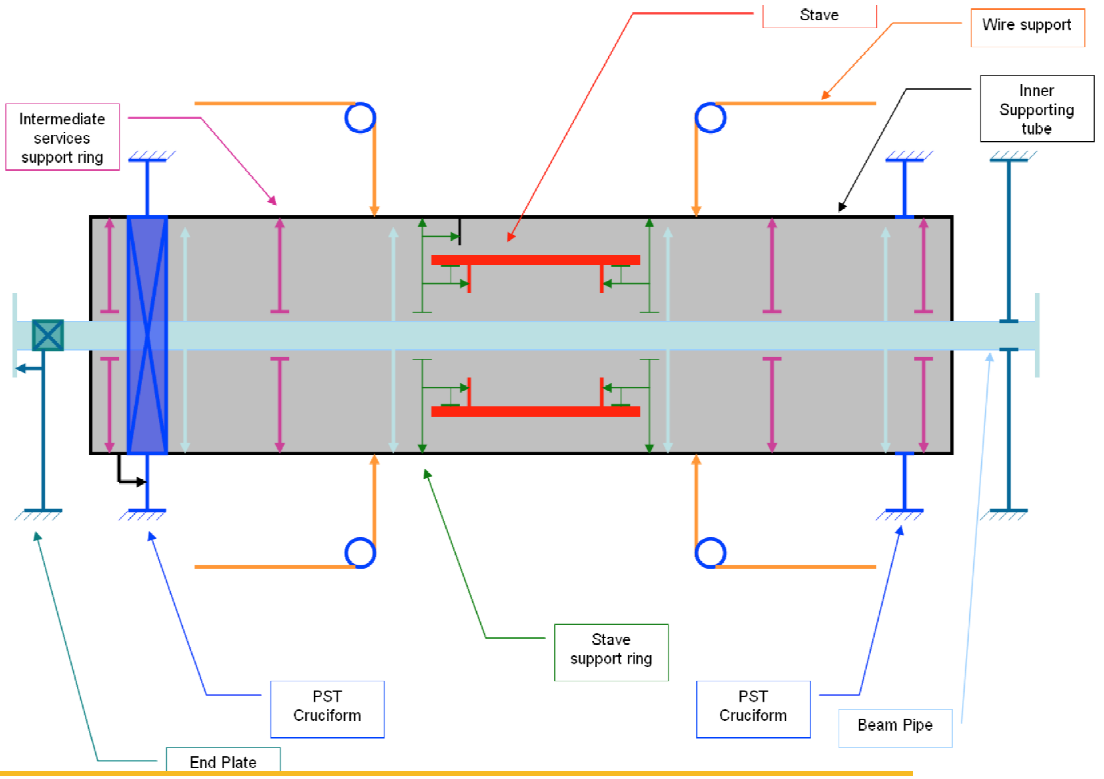
- 3D Model of full IBL package
  - Study support for IBL and beam pipe
  - Check envelops
  - Define positioning and alignment
  - Study BP extraction and IBL insertion
- Proceed with mockup in Bat 180



# Referencing IBL to Pixel

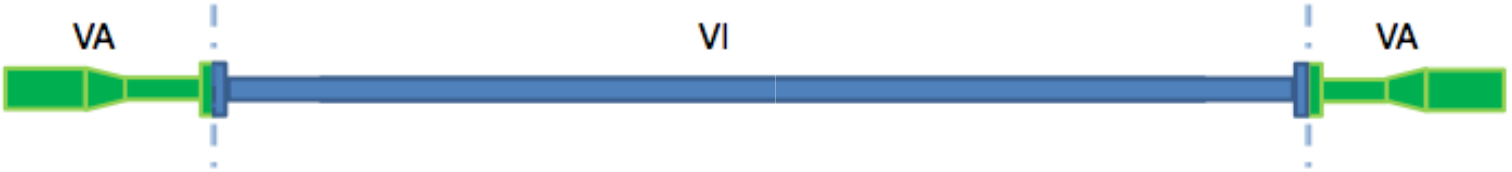
- Study the kinematics of IBL staves to IST and beam pipe
- Decided to decouple IBL from beam pipe to have best possible positional stability of IBL staves to pixel detector
  - Develop details for stave, BP and services support and feed-through
- Plan to use adapted version of present Pixel (quasi-)isostatic supports



# New Beam Pipe

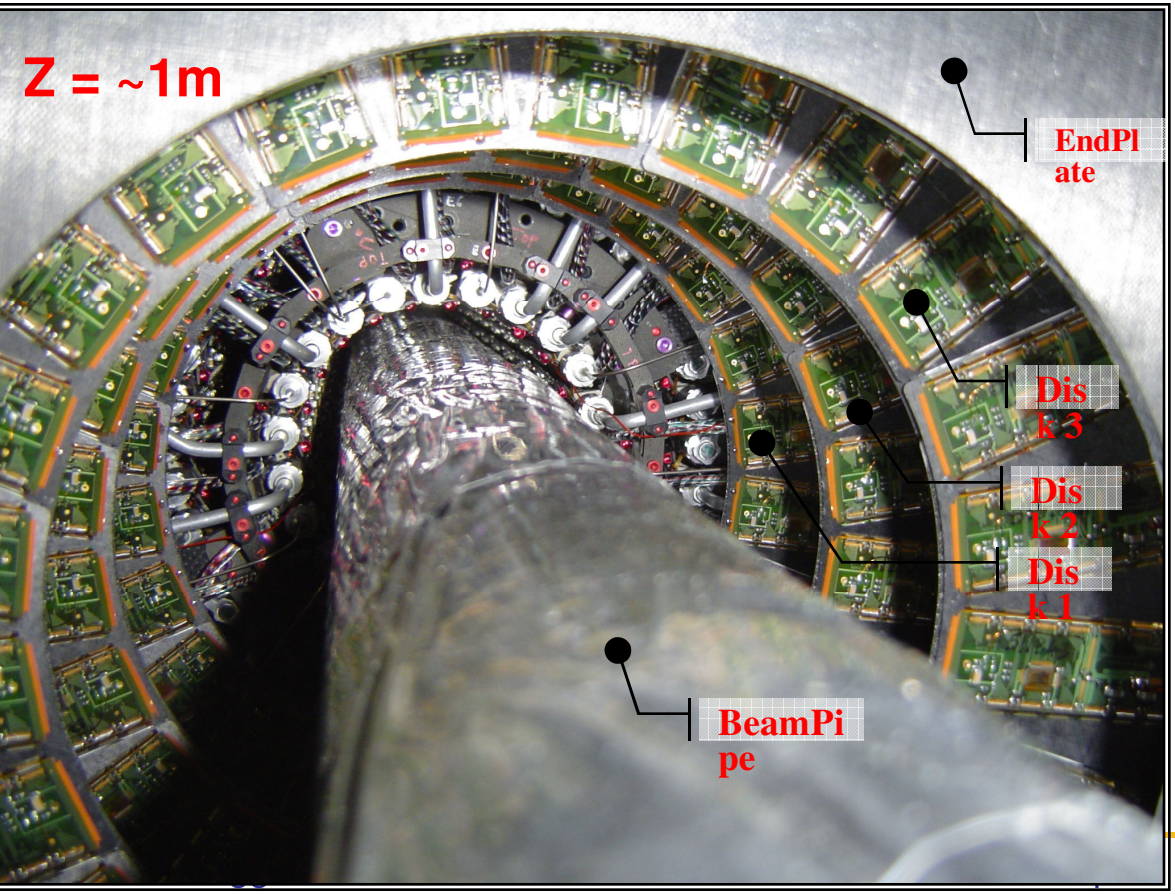
- Several options for transitions from larger to smaller radius currently under discussion with beam pipe group
  - Links to reproduction of VA beam pipe in aluminium and needs definition soon
- IBL strongly prefers to do the transition from 29->25mm IR on VA (~Z 4m to 5m?)
  - Under discussion with ATLAS TC and Beam Pipe Group
- Necessary to minimize flange diameter and serivces to fit through pixel package

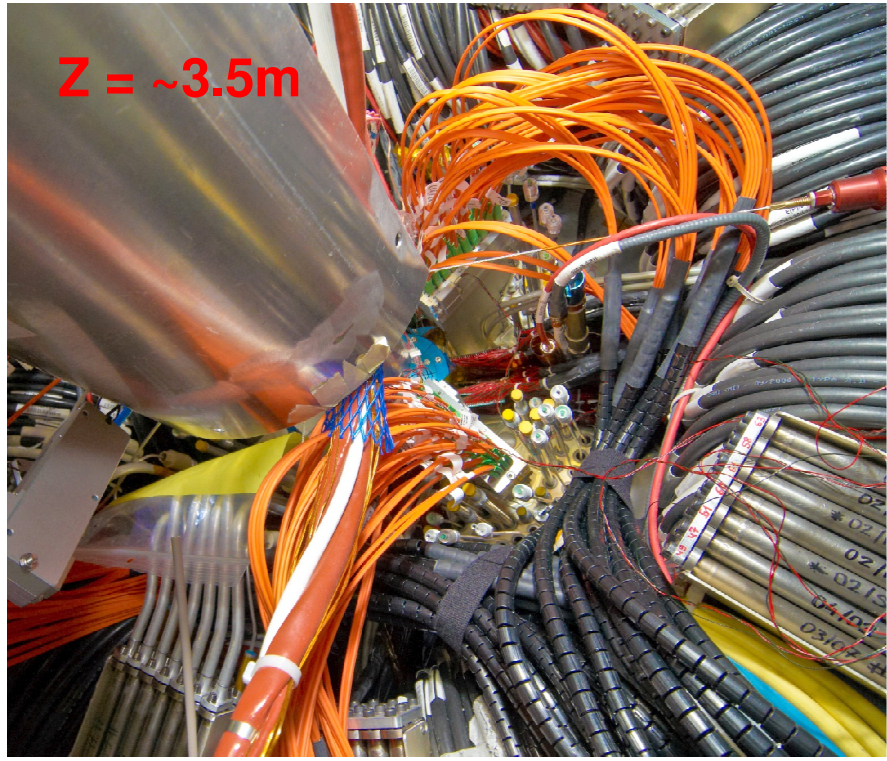



- Details
  - VI is all Be, constant section, 50mm ID
  - VA is Al, tapered section, 50mm/58mm ID
- Pros
  - All Be inner pipe, Be flanges more likely to work with Split flange concept
  - *Smallest passable flange diameter for B-layer clearance*
  - No RF fingers
- Cons
  - Must change VA
  - Worst beam clearance

# IBL Installation and access to present Pixel

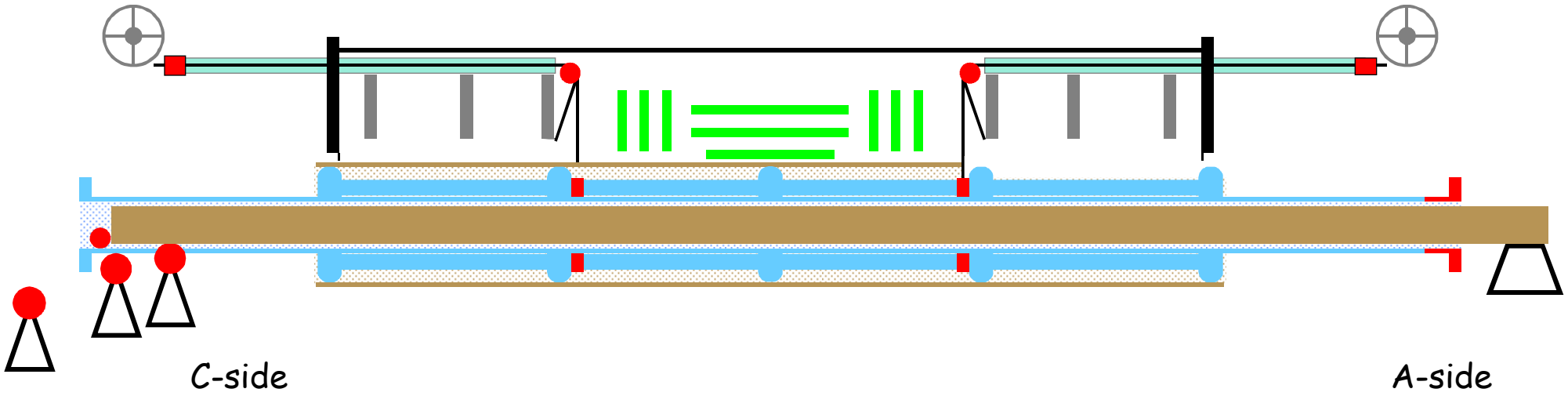
- Beam Pipe extraction & Installation complicated by
  - Activation of surrounding area
  - Very little access to beam pipe and long lever arm (access is at z~3.5m)
  - Minimize any risk to present Pixel Detector



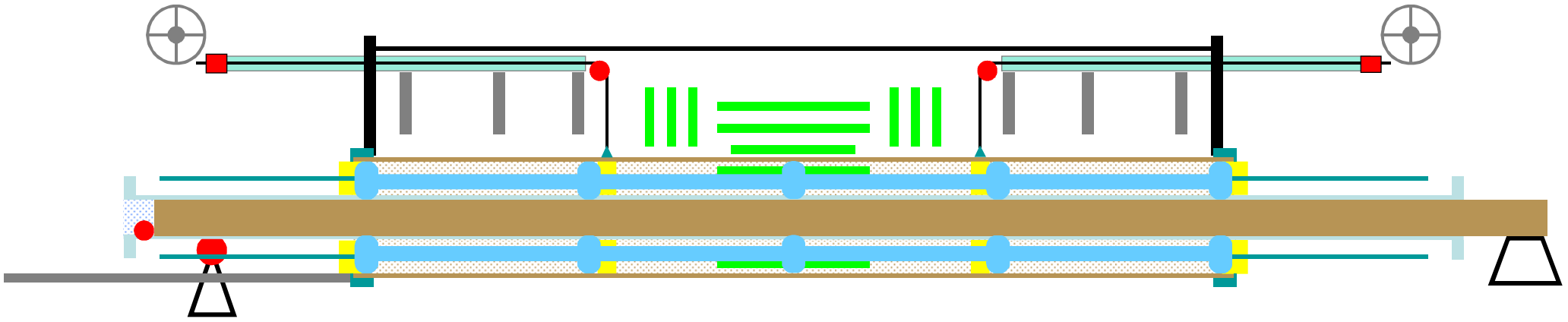
# Extraction sequence

- **The beam pipe flange on A-side is to close to the B-layer envelope . Need to be cut on the aluminum section**
- A structural pipe is inserted inside the Beam Pipe and supported at both sides.
- The support collar at PP0 A-side is disassembled and extracted with wires at PP1.
- Beam pipe is extracted from the C-side and it pulls the wire at PP1
- New cable supports are inserted inside PST at PP0.
- A support carbon tube is pushed inside the PST along the structural pipe.



# IBL installation scenario I

- Different scenarios under study now
- The support carbon tube is fixed in 2 point of PP0 and on PP1 walls on side C and A.
- The structural pipe with a support system is moved out from the support carbon tube.
- The new beam pipe (in any configuration with OD up to 82,5 mm) is inserted from C-side. It has 2 supports at PP0 area and 2 floating wall at PP1 on side A and C.



# IBL timeline

- Overall
  - Installation date end 2014
  - Decision was made by ATLAS management that IBL is decoupled from phase 1 upgrade
  - We assume an 8 months shutdown for IBL installation
    - Start opening to finish closing, time with access to pixel package ~ < ½ that time.
- 2010 Schedule for modules largely driven by FEI4 availability:
  - Expect submission ~ Feb 2010
  - First modules available during mid/end summer next year
  - Will request irradiation and testbeam time as late as possible for module qualification
  - Proceed in parallel with stave prototyping, integration and off-detector work

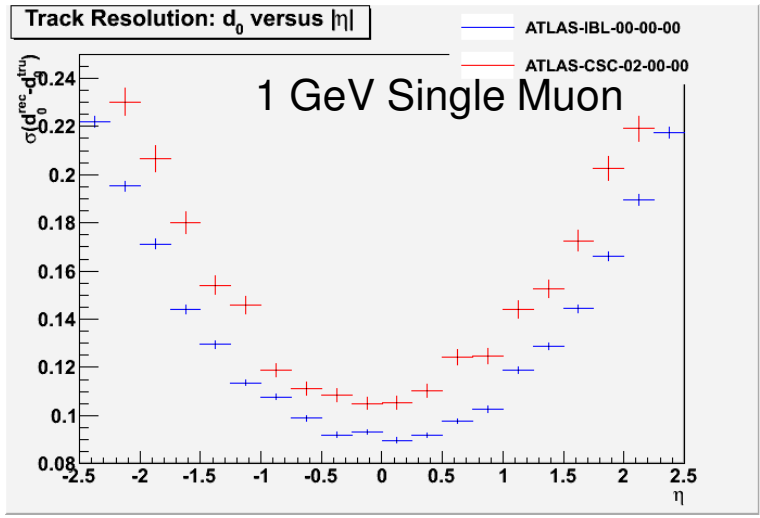
# Summary

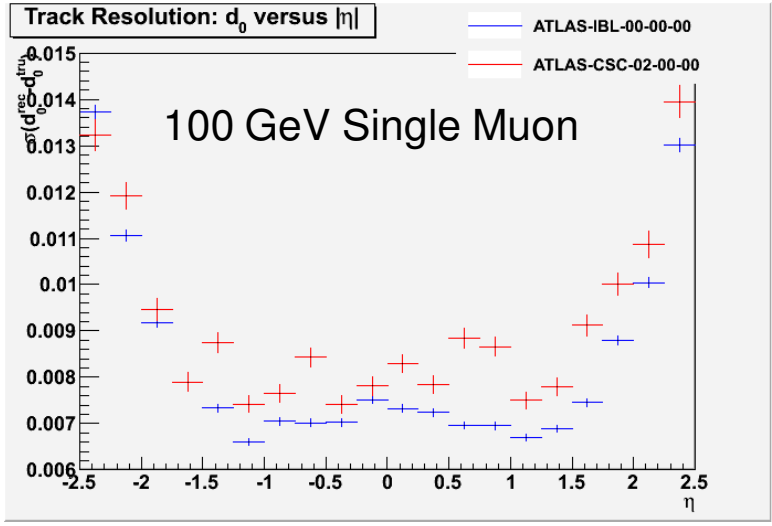
- The Insertable B-Layer will be a new, **4th pixel layer** to be added for the high-luminosity in the present ATLAS Pixel system
  - Smaller radius and lighter to further improve pixel performance
  - Compensate for gradual inefficiency of existing B-Layer
- The IBL is the **"technology" bridge to sLHC**
  - Its specification requires us to develop and use new technologies, which are directly relevant for sLHC
  - Construct a full detector system with those technologies on the time scale of 4-5 years
  - Development of Radiation hard **sensors**
  - New architecture and process for **Pixel Front-End** Chip
  - **Lighter Support** structures to minimize X0

# Backup slides

# IBL simulation

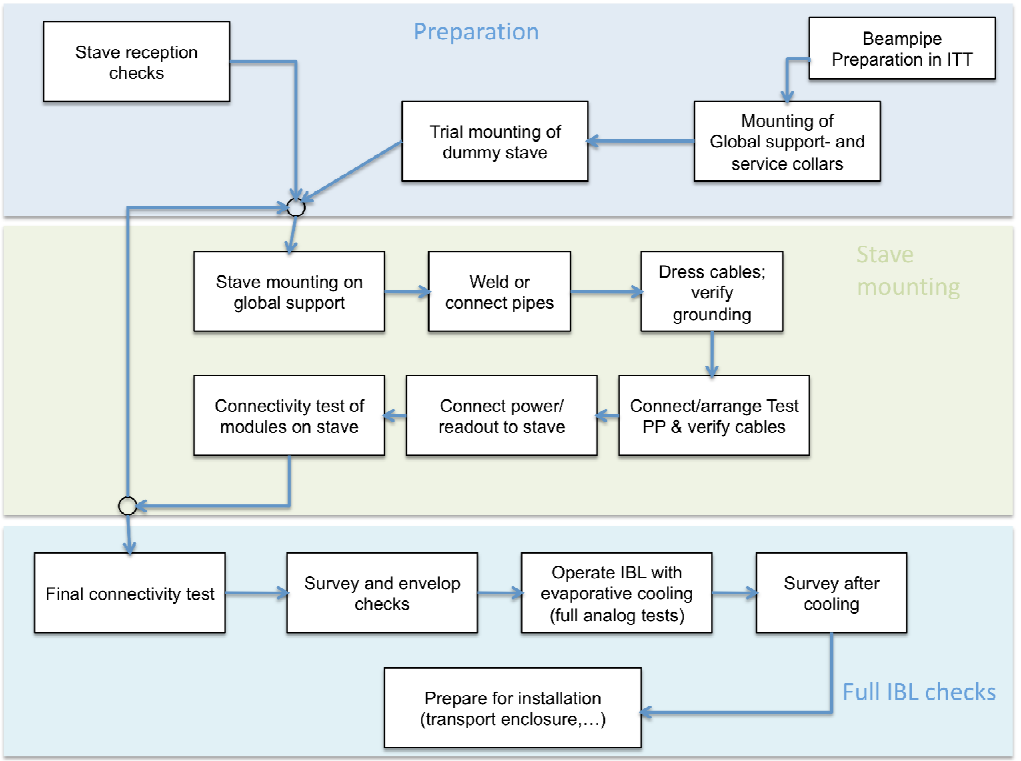
- Run simulation, digitization, tracking
  - Generated single muons with pt=1,100 GeV/c
- Looked at resolution
- Digitization & radiation damage
  - In addition to planar pixel sensors considering different sensor technologies
  - 3d pixel sensors
  - Diamond
- Radiation damage to the existing pixel layers
- Next steps
  - Work started on more realistic IBL layout
  - Actual chip/sensor dimensions
  - Radiation damage in Layer 0 and beyond
- Run through a physics process
  - Evaluate performance



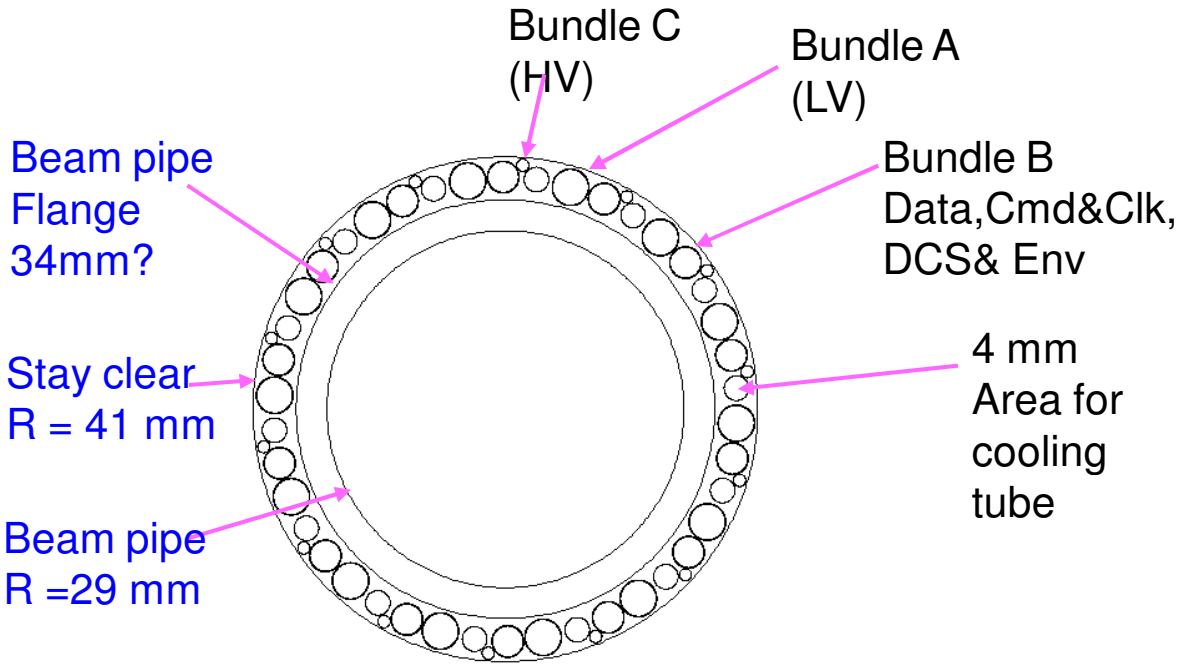
# Integration concept

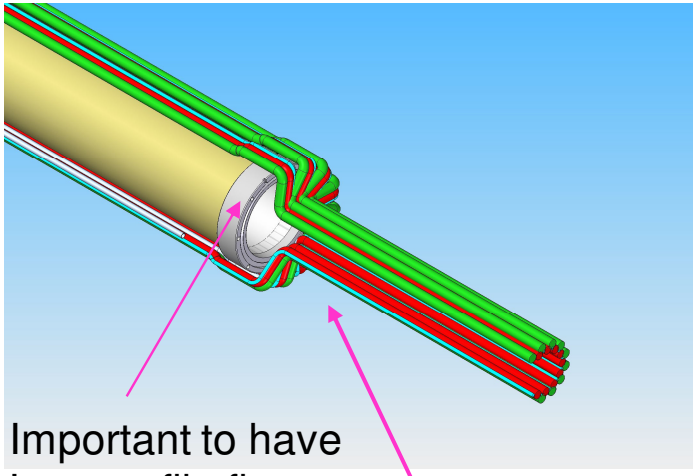
- Integration process studied already now as this influences support designs
  - will request space in SR1 (similar to pixel integration)
- Integration = stave mounting to global support + final tests of IBL package on surface
- Strongly influence by EoS connection
  - assume that pipes are permanent connected and electrical services added during integration of staves to BP



# Services from stave to PP1

- Services between EoS and PP1: very tight around flange -> need to minimize flange diameter and service cross section to fit through IST



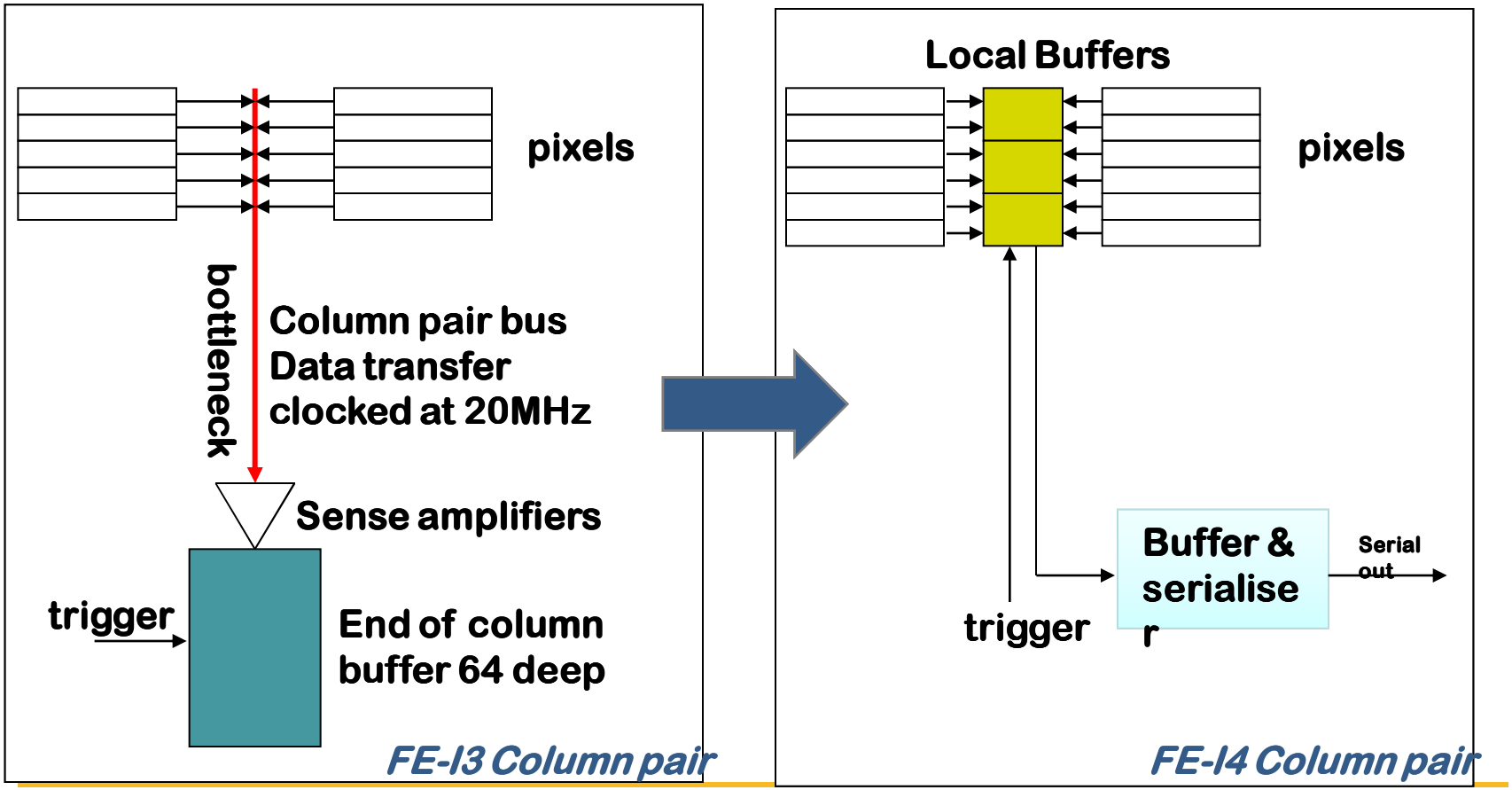




**Dominated by LV services: DC-DC converter would help**

… not yet included: beam pipe services, N2 pipes

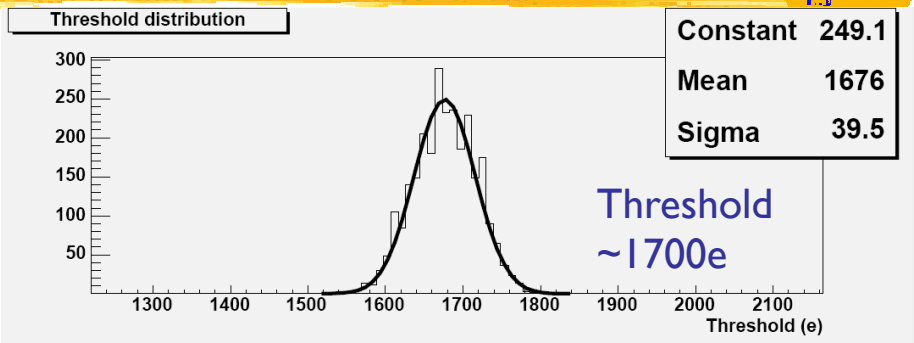
# FE-I4 Architecture: Obvious Solution to Bottleneck

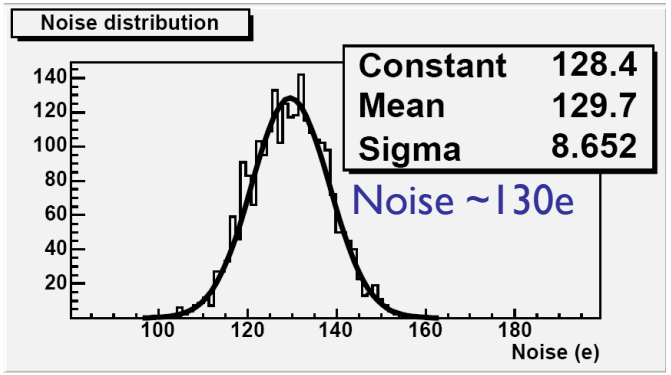
- >99% of hits will not leave the chip (not triggered)
  - So don't move them around inside the chip! (this will also save digital power!)
- This requires local storage and processing in the pixel array
  - Possible with smaller feature size technology (130nm)

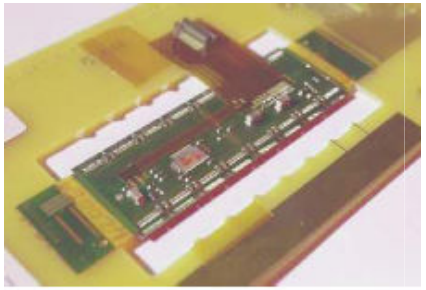


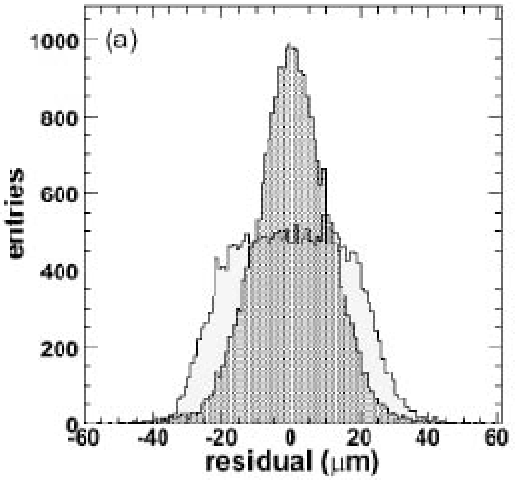
# Sensors: CVD diamond

- Approved ATLAS upgrade R&D
- pro's:
  - No leakage current increase with radiation
  - Lower capacitance, therefore less threshold required for in-time efficiency
  - Can operate at any temperature, no cooling issues
- Con's:
  - Smaller signal (with poly-crystal CVD)
  - Need to establish yield in "scale" production
  - Higher cost & number of vendors (?)






Spatial resolution with TOT informatio:

8.9μm