A low mass pixel detector upgrade for CMS

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CERN

Outline

- Scope of upgrade
- New End Disk Design
- New Barrel Design
- Detector Module Changes
- Changes to the readout chip
  - Design
  - Tests

LHC upgrade plans

By 2014:

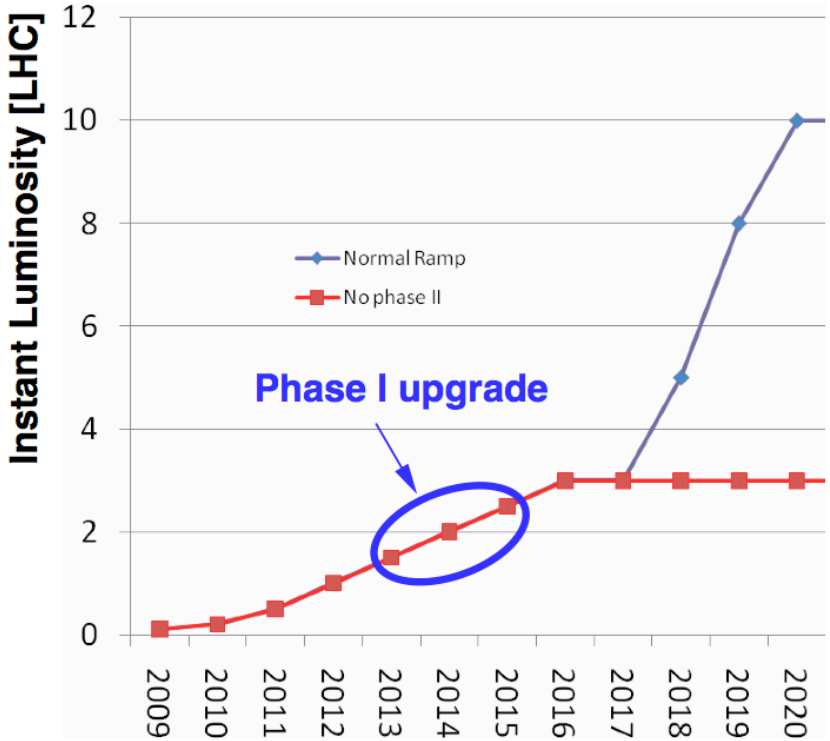
- ~2xLHC luminosity
- Upgrades in (longer) shutdown

Consequences for CMS:

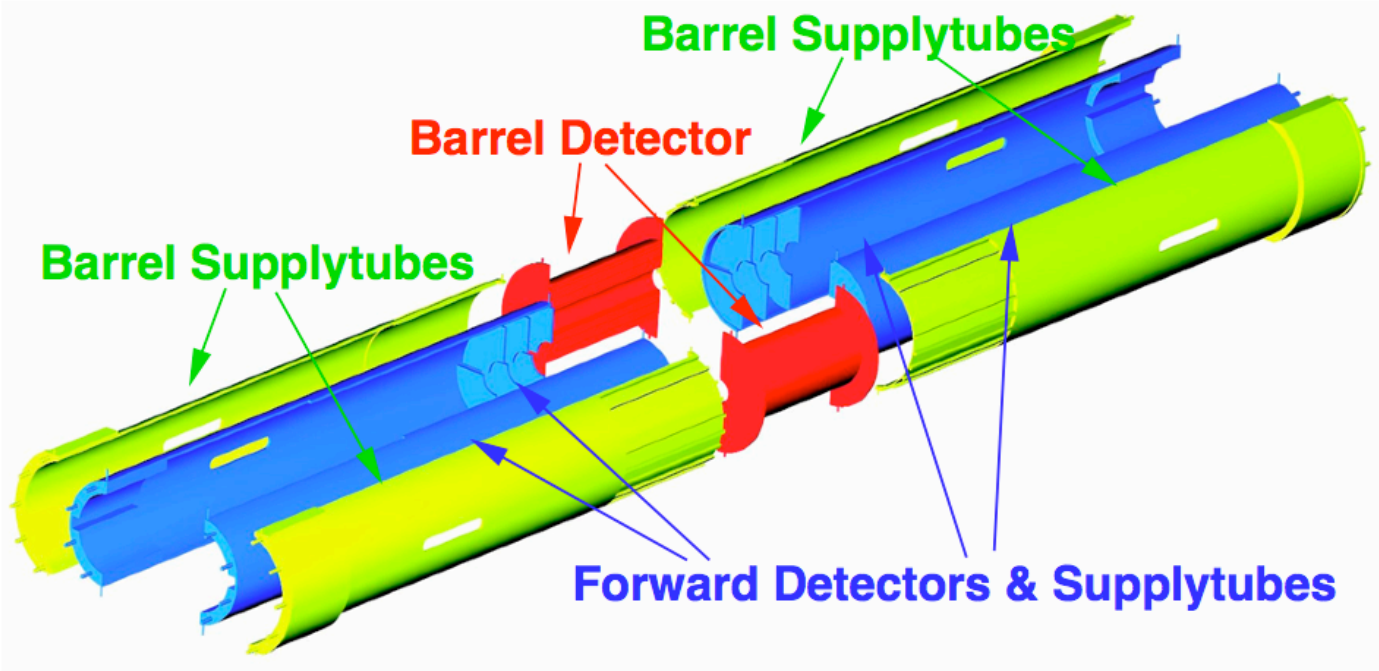
- Most subdetectors min. changes
- Replace pixel system (rad damage)

By 2018:

- ~10xLHC luminosity
- very long shutdown
- replacement of complete (CMS) Tracker



CMS Pixel System



- Designed for fast insertion (beam pipe bake out)
- Will be done in regular shutdown
- Can be replaced by improved system

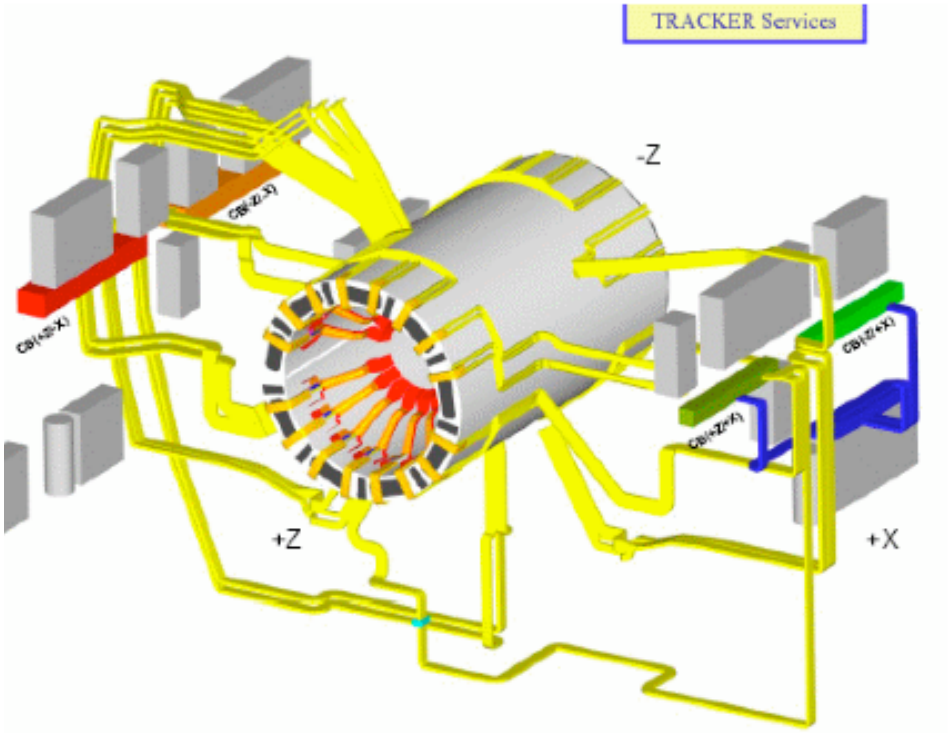
Constraints and Requirements

Same/better performance:

- less inefficiency at high rates
- reduce material effects

Have to use existing services:

- Cooling pipes, cabling, fibers
- power supplies, readout hardware



Stay in old envelope

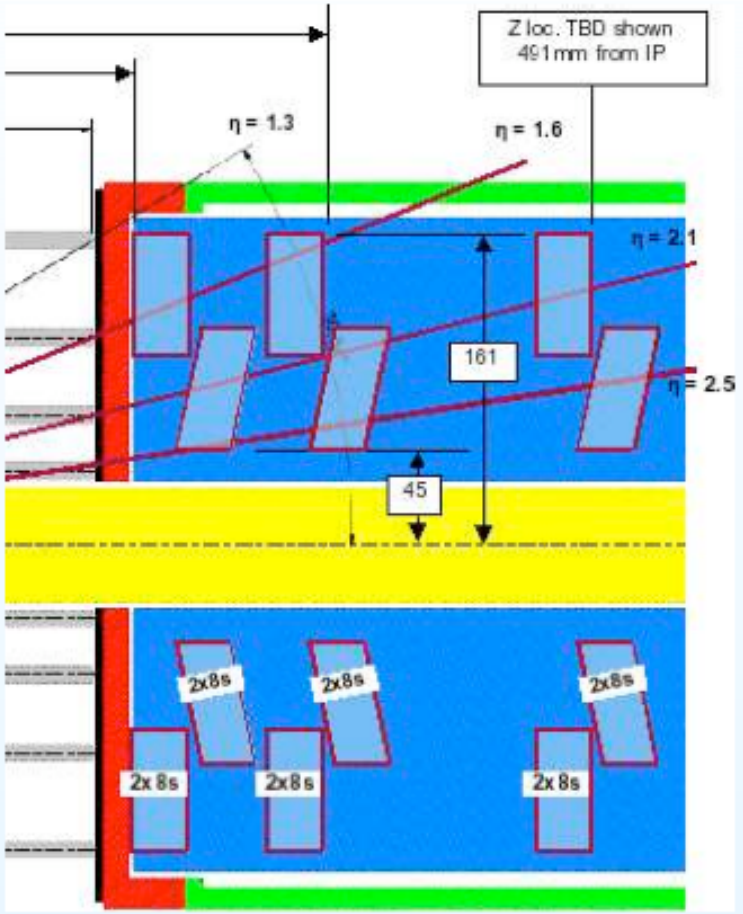
Leave system unchange as much as possible:

•keep ROC core untouched

→ minimise recovery time in competetive physics situation

Mechanics of Disks

- 3 + 3 discs @ barrel ends
- Each disc consists of:
  - 2 half discs
  - inner & outer ring of modules
  - inner ring tilted by 12°
- 4 point coverage up to η= 2.5
  - very small gap ~ η= 1.3



Mechanics of Disks

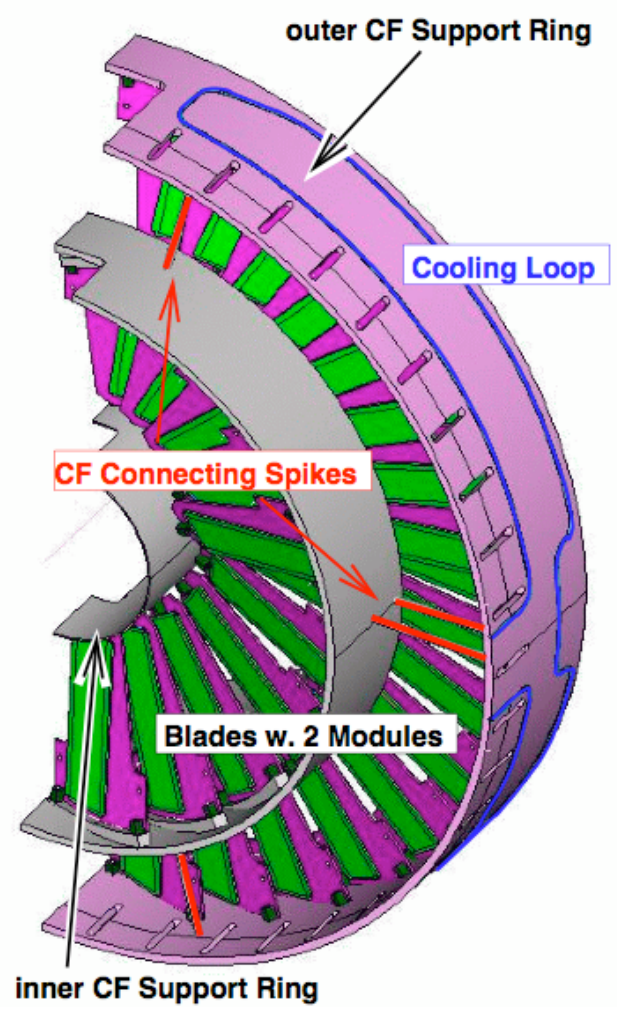
Inner & outer ring of blades

CO_2 tubes embedded in half disk support:

- support cylinder:
  - Carbon carbon
  - Grooves for cooling tube
  - Stainless steel tube:
  - 1.8mm OD, 100μm wall

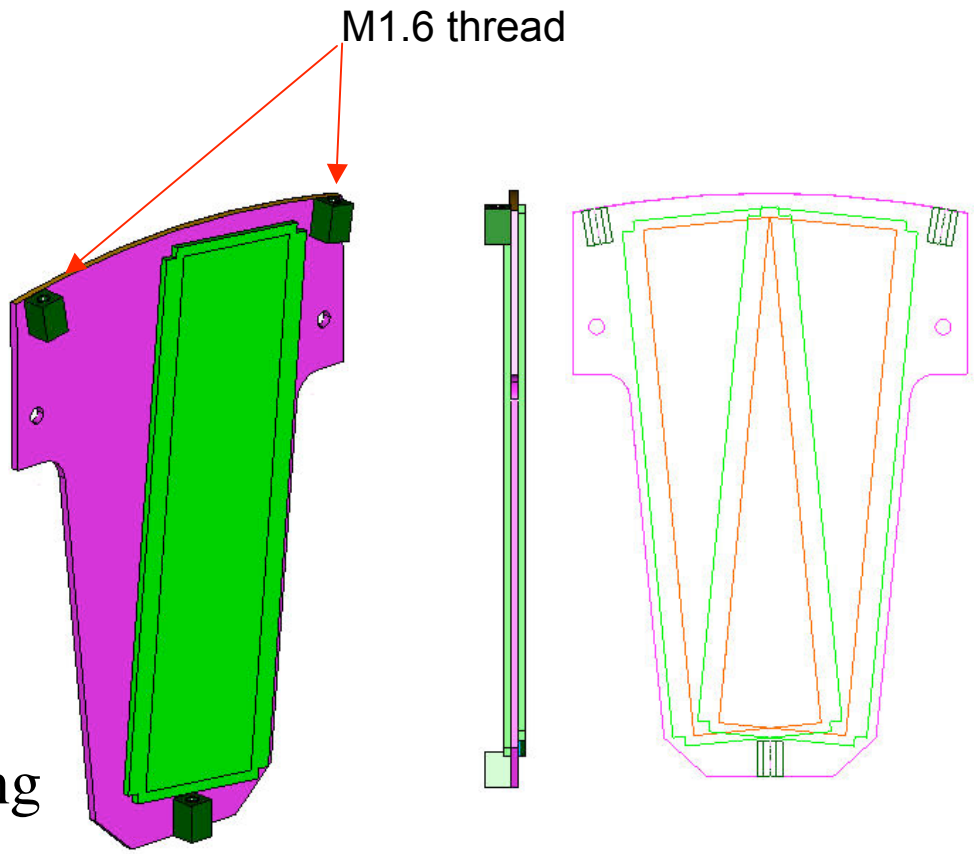
Blades:

- all identical
- Rotated by 20^o radial
- Tilted by 12^o (inner ring)
- 2 modules per blade (ϕ overlap)
- individually replaceable



Blades

- Solid TPG (0.88 mm thick) encapsulated with carbon fibre (0.06mm)
- All blades are identical
- Cooling through the rings
- Easy attaching/removing of blades with screws



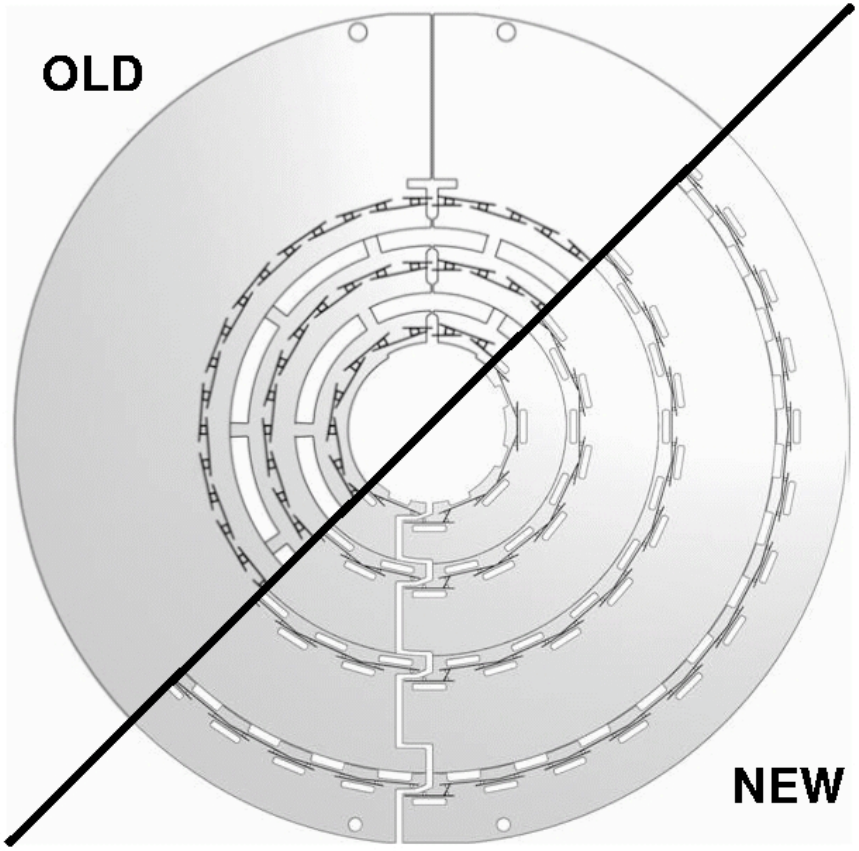
Mechanics of Barrel

Add 4th layer :

- layers @ 39,68,109 & 160 mm
- beam pipe clearance 4 mm
- 8 modules along z (1216 total)
- ‘ultra‘ light support structure

CO_2 based cooling system

→ more robust (standalone) tracking
→ better connection to strip tracker



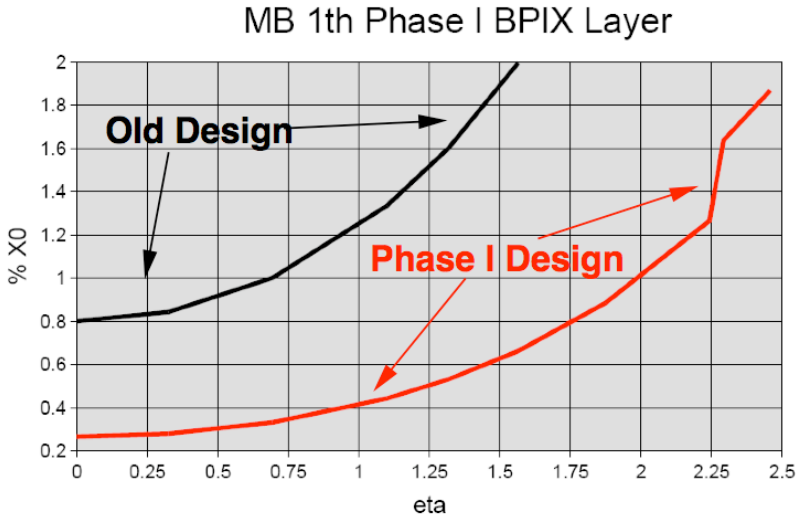
Prototype

Layer 1 prototype:

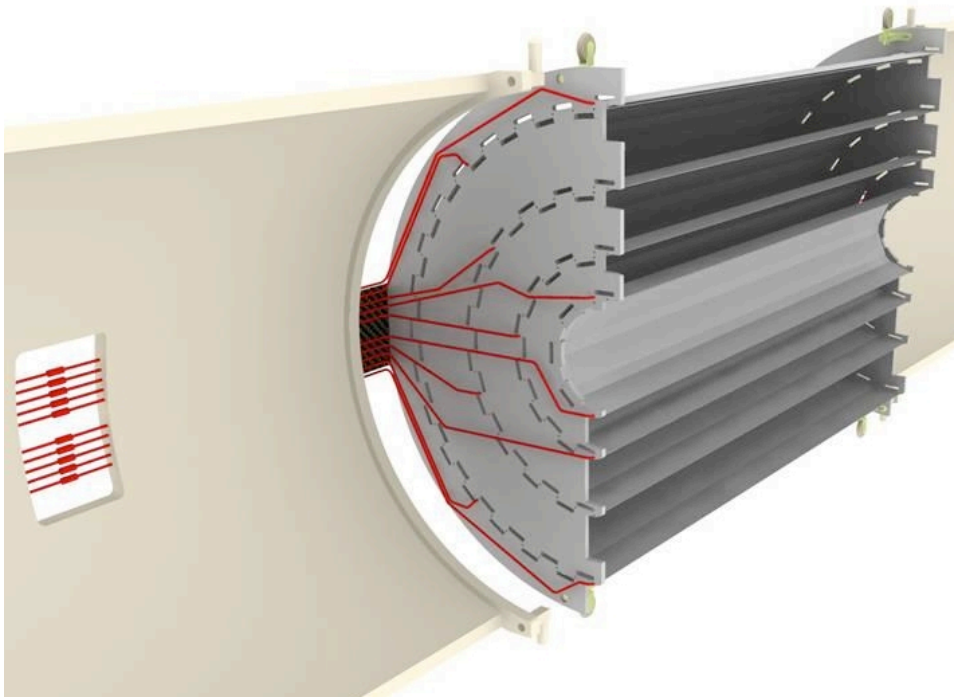
- 200 μm carbon fiber
- 4mm Airex foam
- Stainless steel tubes:
  - 1.5 mm OD, 50μm wall
  - Tube bends: 1.8mm OD, 100μm wall
- tested: ~100 bar & -10°C..10°C

- Factor >3 gain in material budget

  →4 layer system will have half of MB of old 3 layer system



CO_2 cooling



Advantages:

- long cooling lines ~ 5m
- no manyfolding needed
- very small tubes

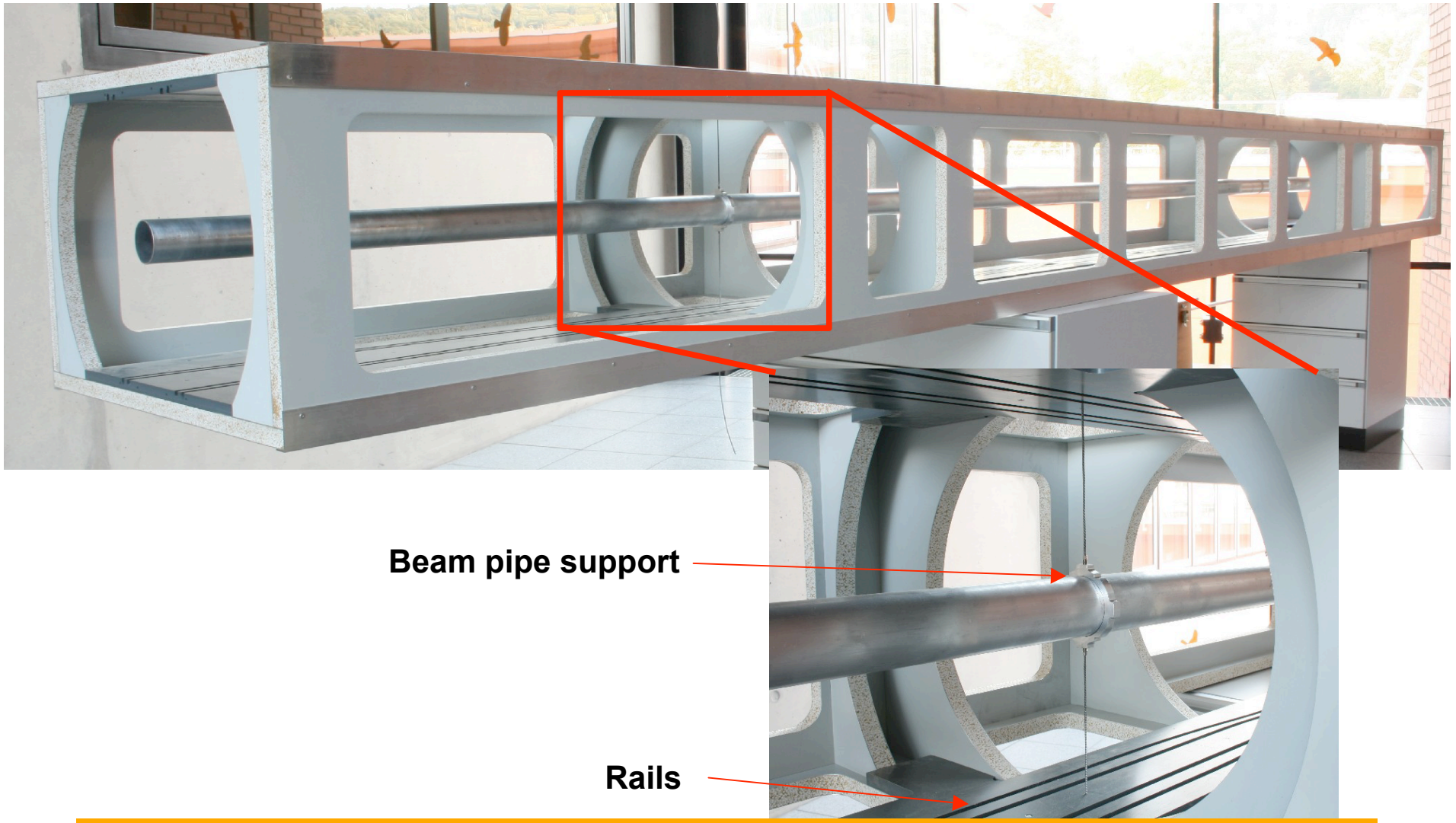
  →big MB reduction

BUT:

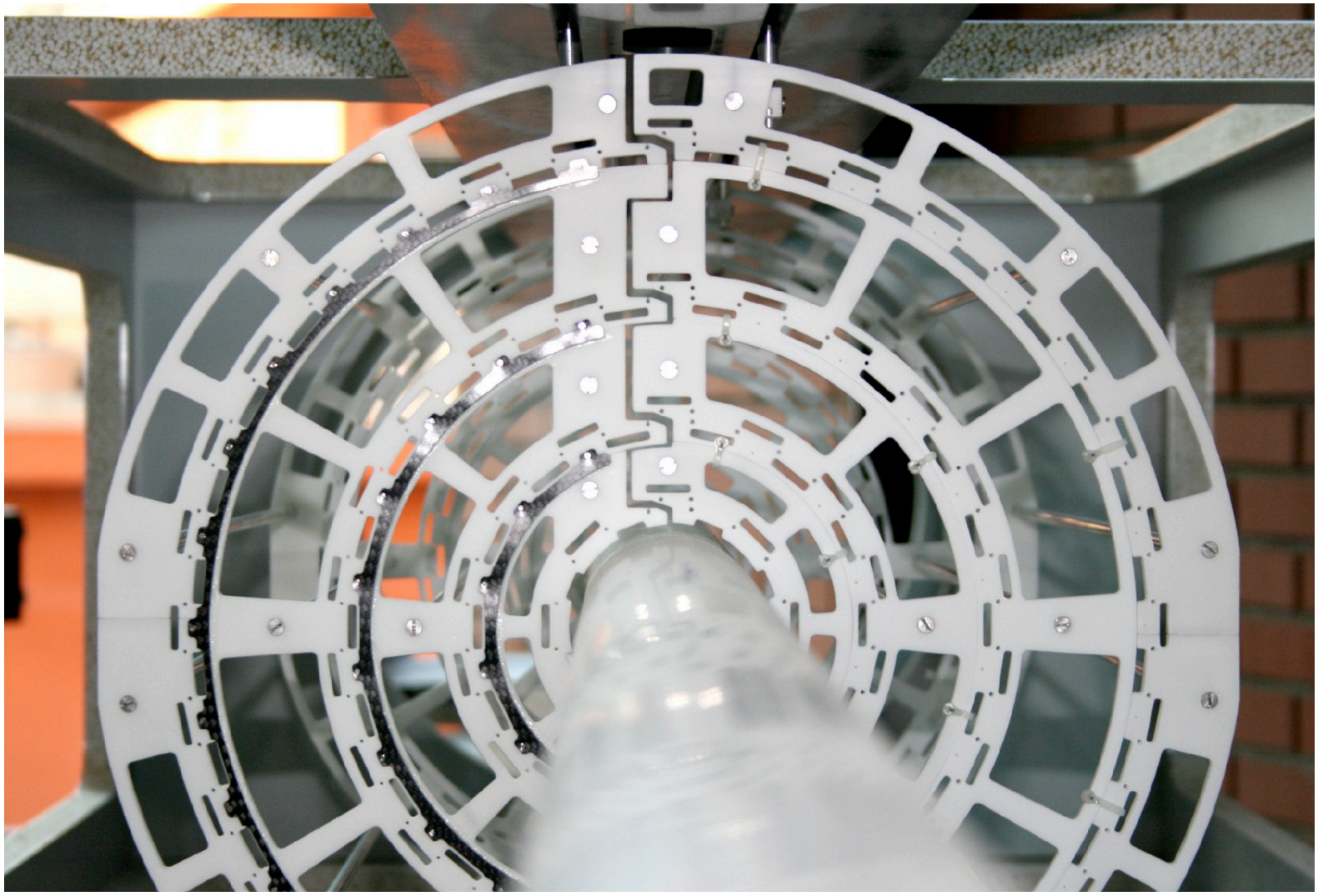
- system with relatively high pressures (~60 bar @ room temperature)
- CMS cooling tubes ok up to 40 bar

  → special star tup/safety

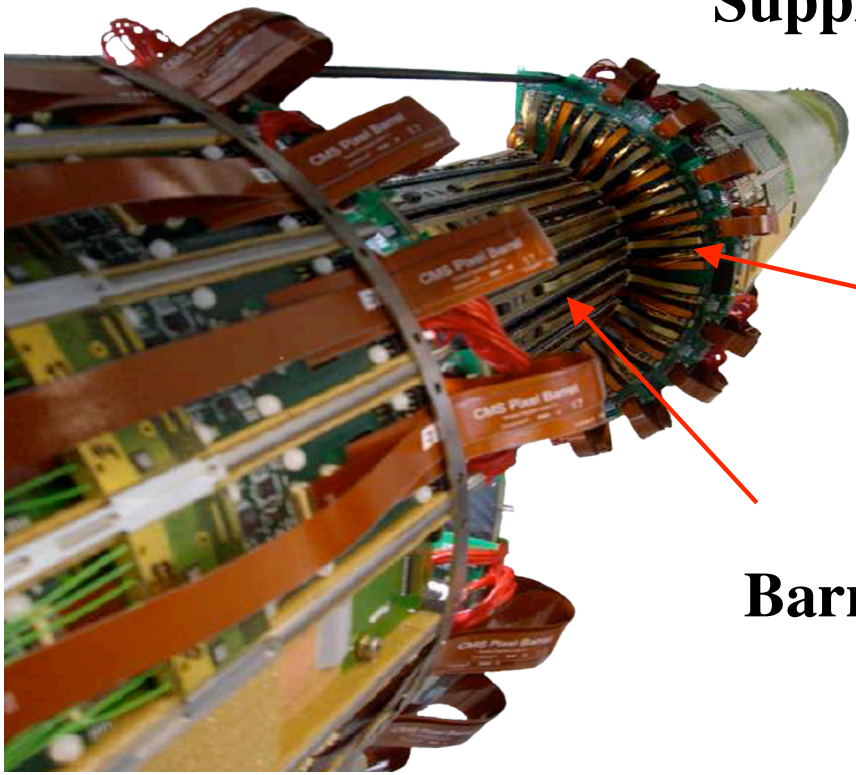
CMS pixel installtion mock-up



Final Position



Reduction in Services



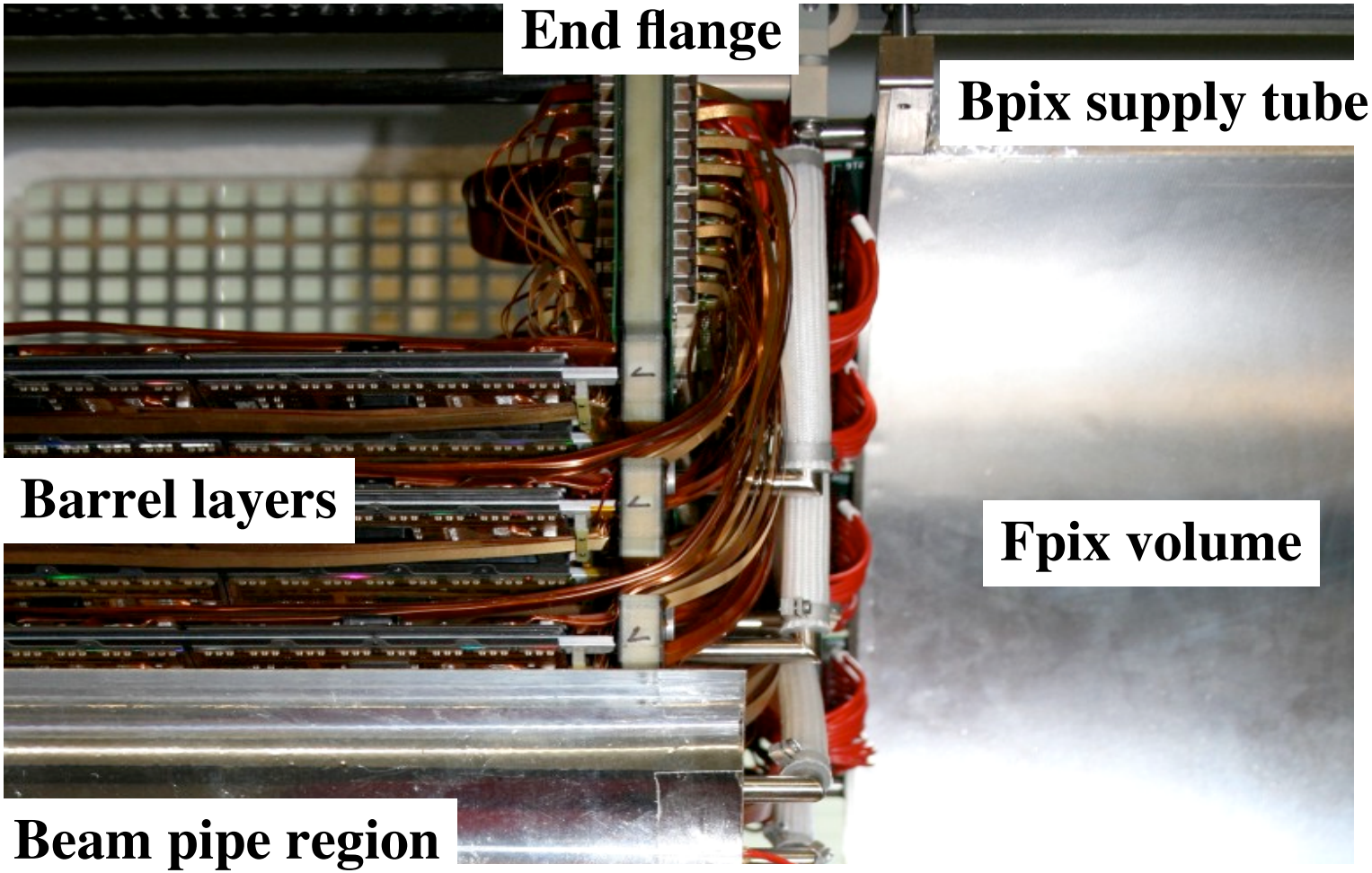
Supply Tube (-Z)

End flange with Prints, plugs and cables

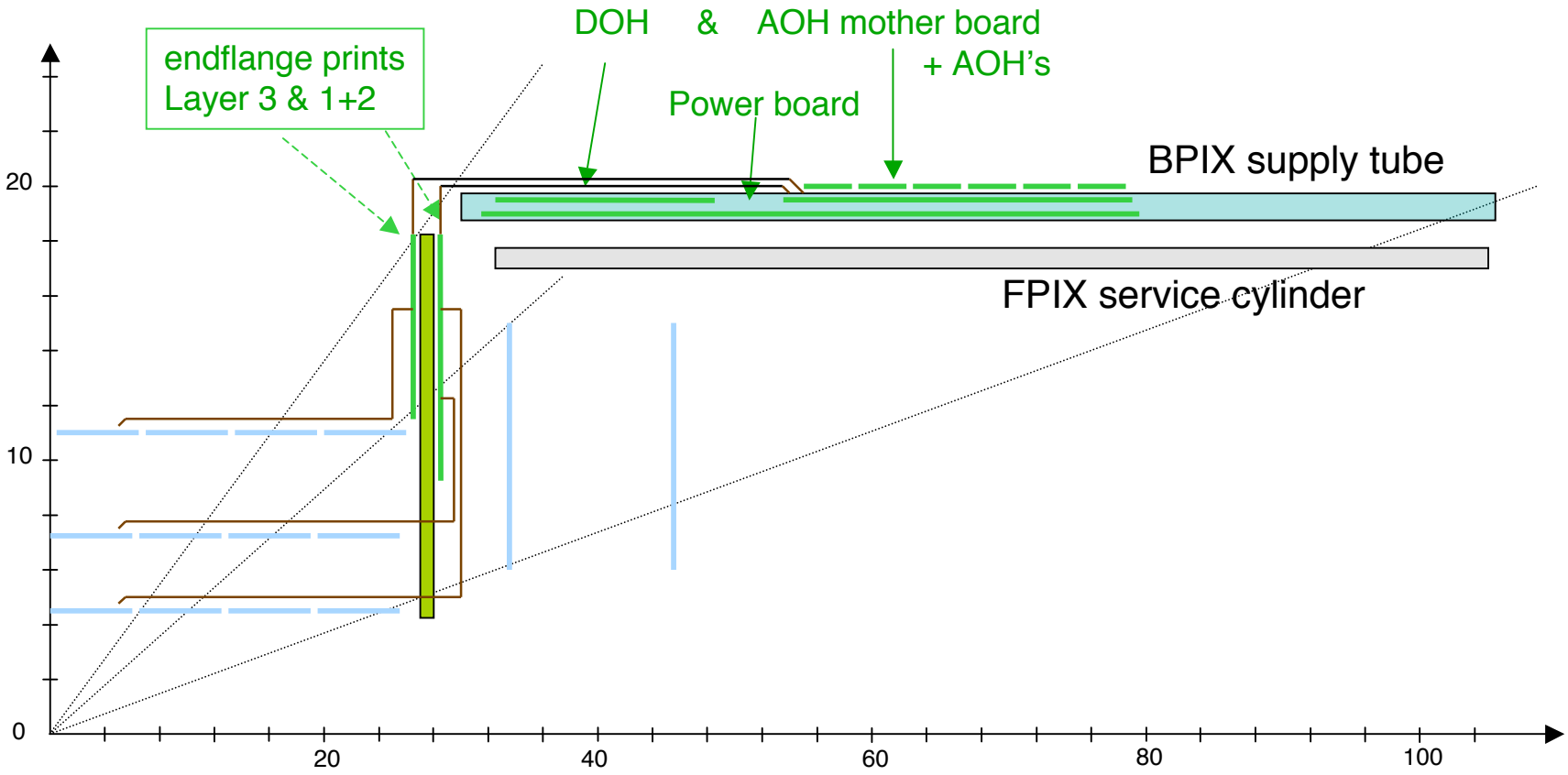
Barrel detector

Supply Tube (+Z)

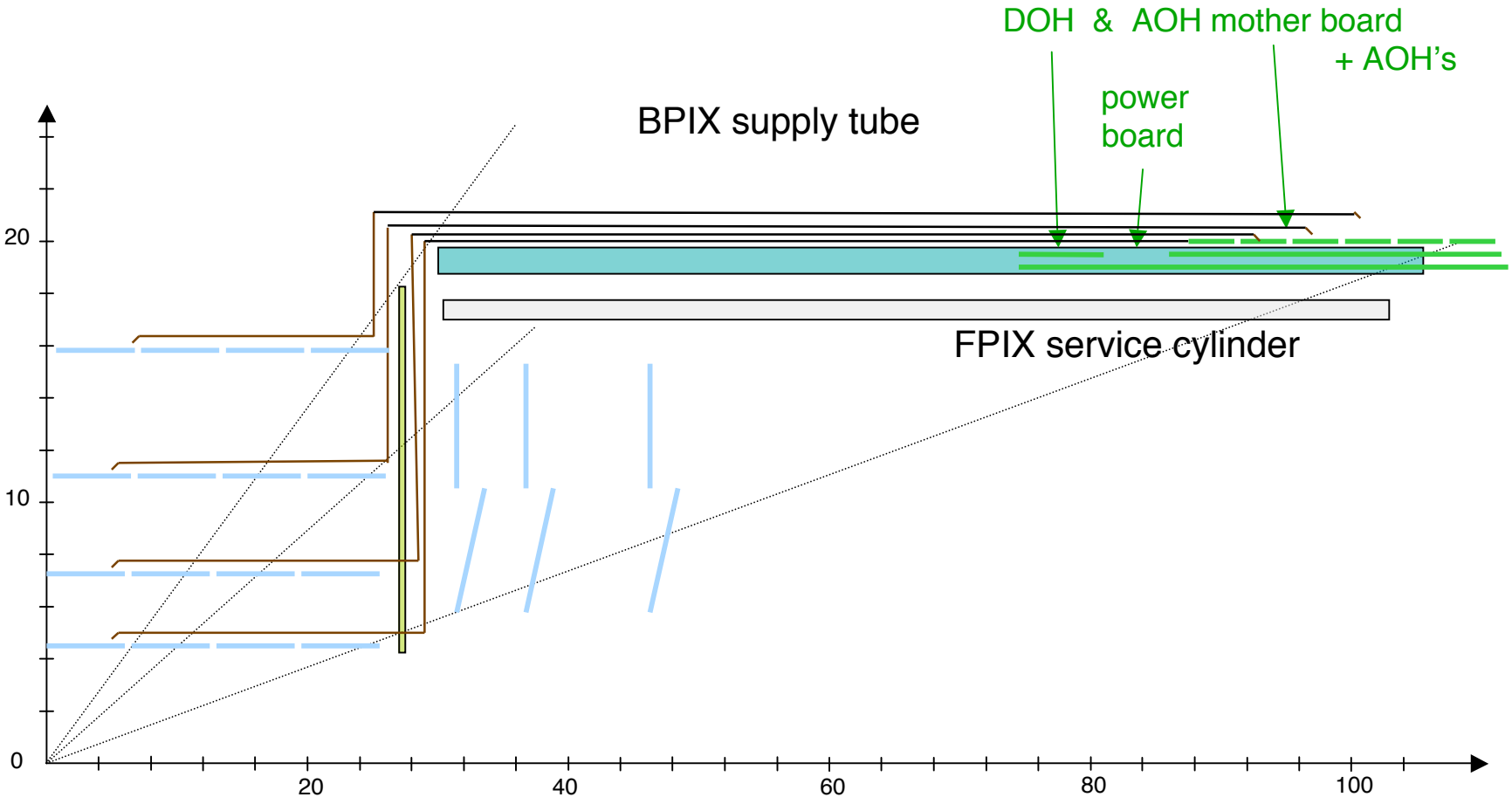
Reduction in Services



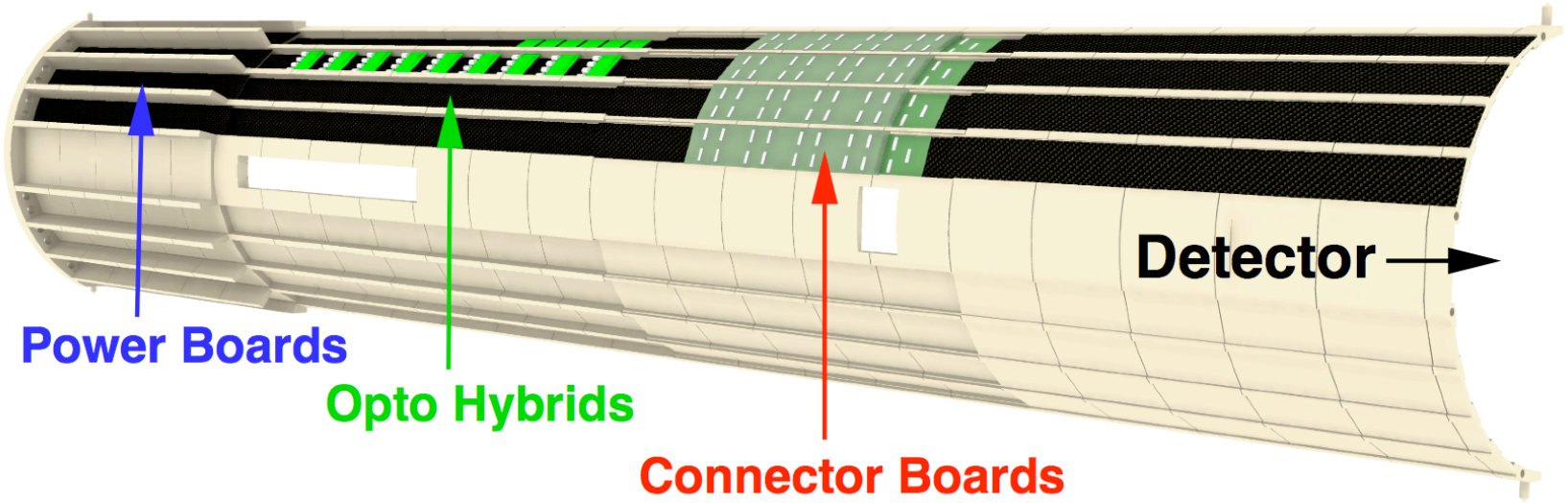
Present Services



Future Services



New Supply Tube



- Very low mass cable trenches
- Module connectors:
  - Layer 3+4 outside
  - Layer 1+2 inside
- New opto hybrids
- 2:1 DC/DC converters

Parts for the support tube

Airex foam parts for one supply tube

Carbon fibre parts for one supply tube

Airex carbon fibre stack (storage)

Module Design Changes

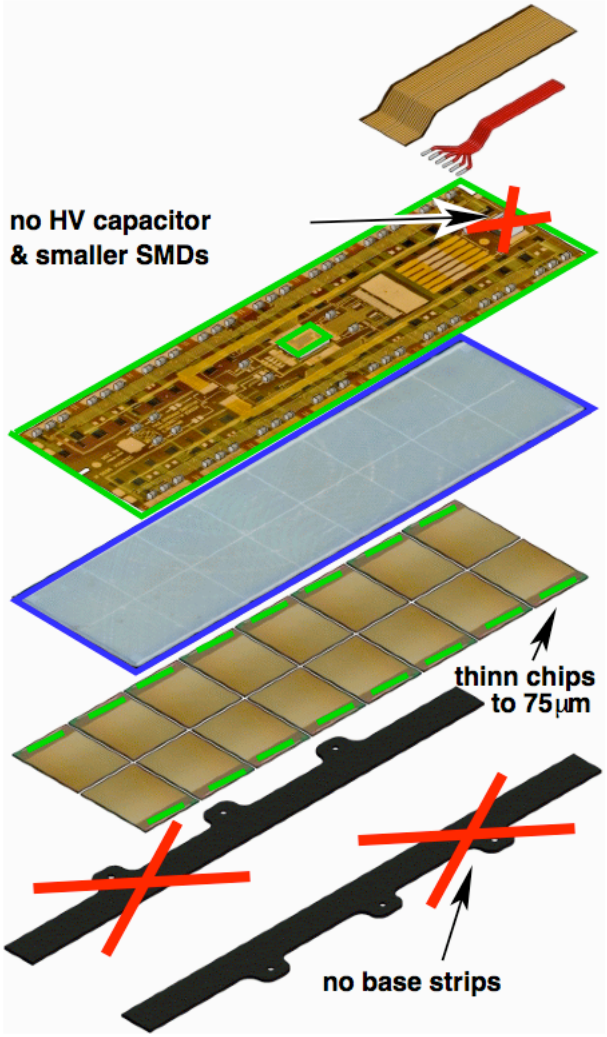
One design(barrel +endcap)

Based on present barrel module

Changes:

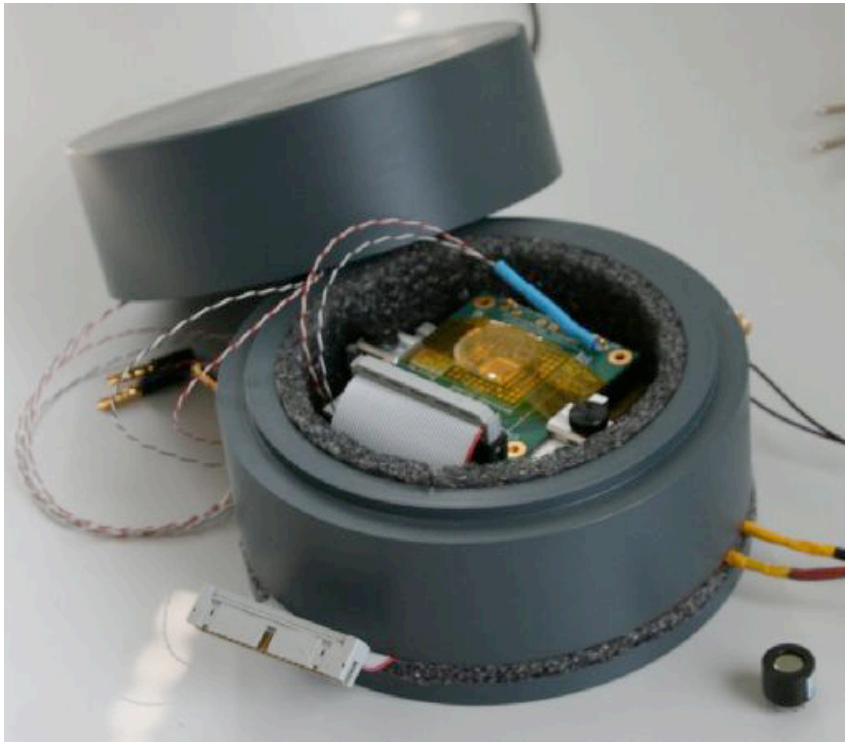
- No basestrips
  →Better cooling contact

- ROC:
  - thickness 175μm ⇨ 75μm
- HDI:
  - No HV-capacitor
  - Miniaturize SMD-components



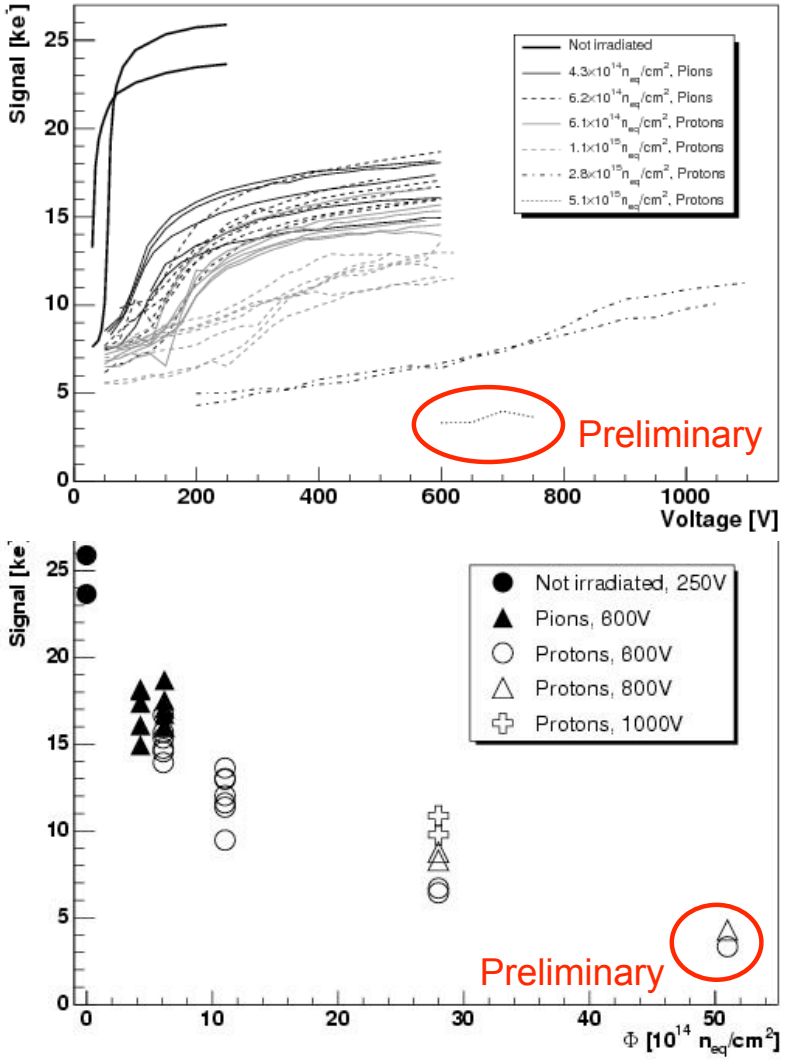
Radiation hardness of Sensors

- Irradiated numerous samples consisting of a small sensor and 1 ROC
  - PSI Pi-E1 up to ~ $6\times10^{14} n_{eq}/cm^2$
  - CERN-PS up to ~ $5\times10^{15} n_{eq}/cm^2$
- Measured charge value obtained from a Sr-90 beta particle
- Leakage current stayed within “limits”
- Spatial resolution decreases to “binary” value (not measured)
- Presently no independent trigger (no efficiency measurement possible)



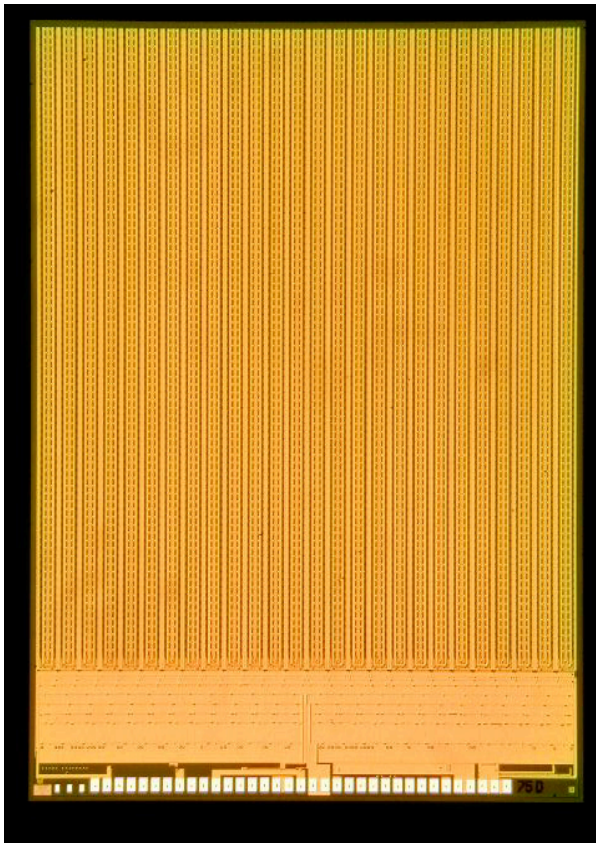
Results

- Highly irradiated sensors operative up to 1kV
  - Presently problems with high voltage capability of the setup (connectors, PCBs etc.)
- No signal saturation with bias for $\Phi > 2\times10^{15} n_{eq}/cm^2$
- Sensor with $\Phi = 2.8\times10^{15} n_{eq}/cm^2$ deliver > 5ke (at 800V)
  - No sign for charge multiplication
- Sensors seems suitable for upgraded LHC



Radiation effects on the ROC

- **ROC stays fully operational within the full fluence range tested (up to $\Phi=5\times10^{15}N_{eq}/cm^2$).** All sensor data were taken with irradiated ROCs
- Apart from few settings (preamplifier and shaper feedback, source follower) the standard calibration procedure was followed
- Try to characterize the degradation
  - voltage of band gap reference (done)
  - peaking time of preamplifier as function of I_a (in progress)
  - Skipping speed of column drain (to be done)
  - High frequency limit of the ROC (to be done)



Readout Chip for Phase I

- Based on present readout chip (0.25μm)
- Limitations of present ROC at Phase1:

1. Buffers sizes for L1 latency (dominating)

   → **Increase number of buffers by factor ≈2.5 (trivial, more compact layout achieved in order to limit increase in chip size)**

2. Readout related dead-time at higher data volumes

   → **Additional readout buffer stage**

3. Higher module count / same number of fibres

   → **Digital readout**

   – On chip ADC
   – New fast digital readout links
   – PLL to provide higher frequencies
   – Modification to control logic

New Readout Buffer Stage

- With larger buffers leading inefficiency is waiting time for readout token
  - After L1A, double column stops until read out.
  - The waiting time for the r/o token can become long since the whole/half module (416/208 double columns) is daisy chained
- Solution: add ROC internal readout buffer.
  - ROC generates internal r/o token from trigger
  - Immediate digitization and transfer into r/o buffer
  - Double column resumes data taking
  - Hits wait in r/o buffer for module r/o token
- Further benefit: equalizes data fluctuations, can make better use of bandwidth
- Would leave double column logic exactly as today
  - Modification on ROC level only
  - Purely digital, 40MHz synchronous logic
- Need 23 bits x 80-100 words (size not critical, depends on space constraints)
- Design not yet started

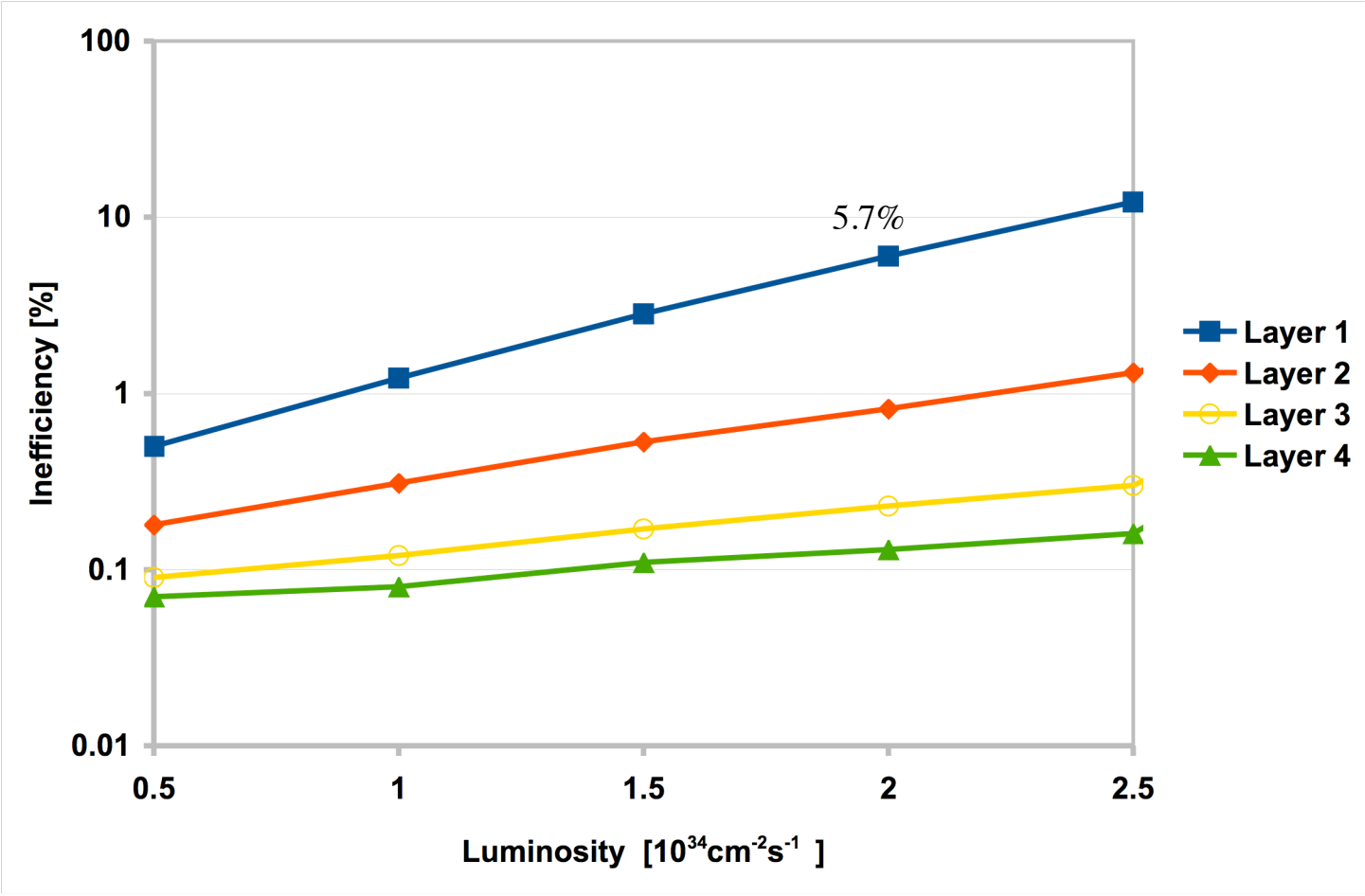
Digital Readout

- In 4 layer barrel pixel system we will have 1216 modules (128 / 224 / 352 / 512). Now 720
- We will have to re-use existing fibres from PP1 out.
- → can only use one fibre per module everywhere Now 2 fibres per module for layer 1 and 2
- Present analog links too slow. Hard to make faster.
- Only reasonable solution with digital links

Data loss simulations

- New C++ program written for time domain simulations of data flow
- Closer to actual hardware than old, historically grown FORTRAN code. 1:1 map from hardware onto software objects
- Flexible to simulate different readout schemes (speed, number of links, data format, parallel vs. daisy chained...)
- Validated against old code
- Hits from full GEANT simulation. Mix of MinBias events plus b-jets, Z->jj, ttbar
- **All here presented changes included**

Inefficiency vs luminosity



→Inefficiency depends exponentially on luminosity

Mean inefficiency

τ_{lumi} = 10h

$T_{turnaround}$	T_{run}	Layer 1 Min	Layer 1 Mean	Layer 1 Max	Layer 2 Min	Layer 2 Mean	Layer 2 Max	Layer 3	Layer 4
10	11.5	1.3	1.7	2	0.26	0.34	0.41	<0.2%	<0.1%
5	8.6	1.6	2.1	2.5	0.3	0.38	0.46	<0.2%	<0.1%
2.5	6.3	2	2.5	2.9	0.35	0.44	0.53	<0.2%	<0.1%

τ_{lumi} = 5h

$T_{turnaround}$	T_{run}	Layer 1 Min	Layer 1 Mean	Layer 1 Max	Layer 2 Min	Layer 2 Mean	Layer 2 Max	Layer 3	Layer 4
10	7.5	1.1	1.4	1.7	0.13	0.22	0.36	<0.2%	<0.1%
5	5.7	1.3	1.7	2.1	0.14	0.26	0.41	<0.2%	<0.1%
2.5	4.3	1.6	2.1	2.5	0.16	0.3	0.46	<0.2%	<0.1%

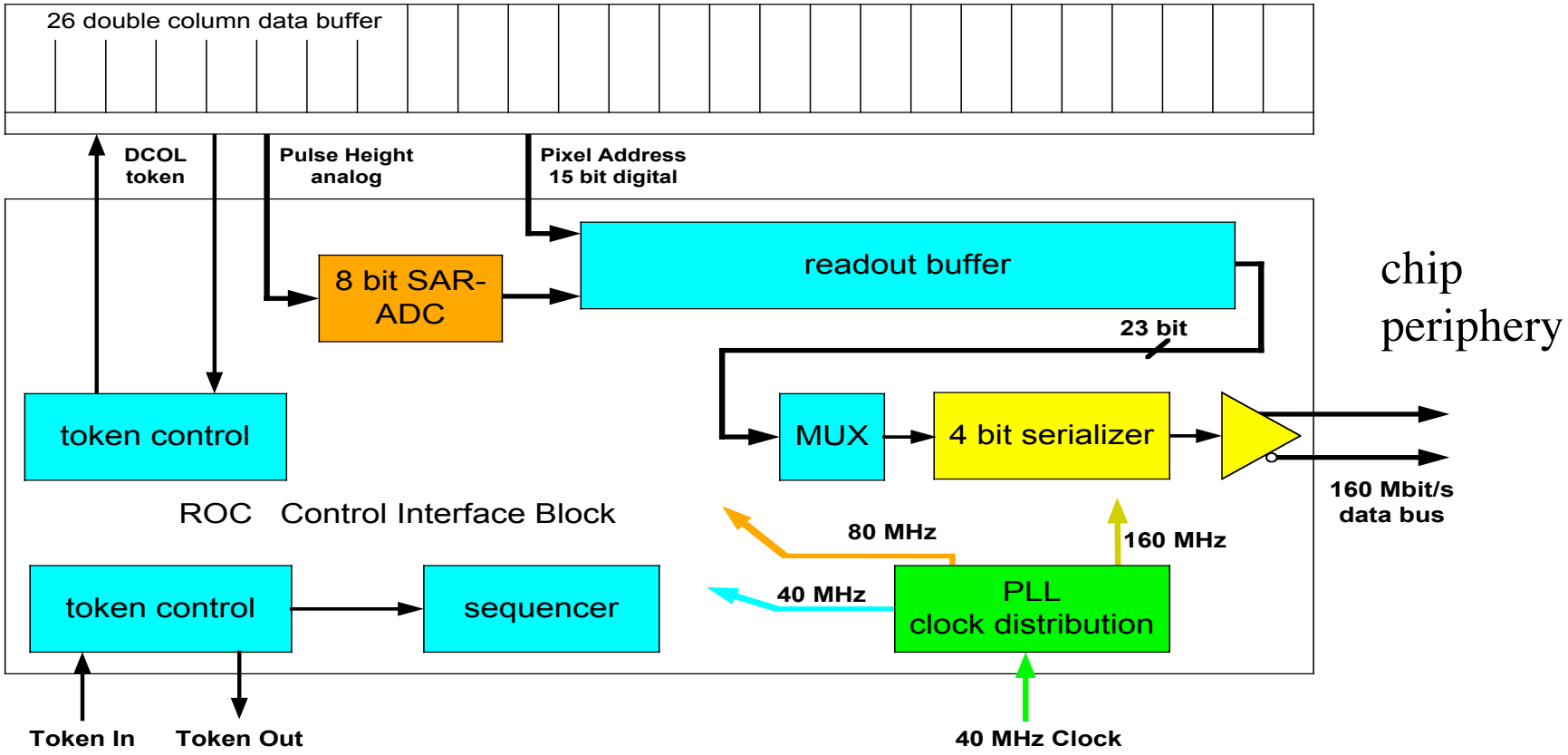
Inefficiencies averaged over a run in % for peak lumi $L=2\cdot10^{34}$, times in hours
→Depending on LHC operation (turnaround time, lumi lifetime τ_{lumi}), mean efficiency in **layer 1 between 1.4 and 2.5%**

•Min/Max corresponds to low/high eta modules

Changes in the ROC

- **Larger data buffers to cope with higher rates**
- **Digital readout links at 160 Mb/s**
  - **Now 2x analog link at 40 MHz in layer 1&2**
- **Very low power electrical link of O(1m)**
- **ADC on chip operating at 80 MHz**
  - **Now analog transmission of pulse height information**
- **New readout buffer stage to reduce dead time**
- **PLL to provide 80/160 MHz**

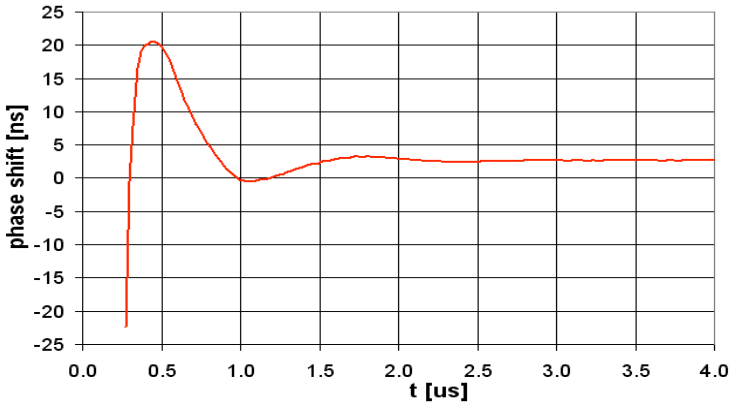
Changes in the ROC



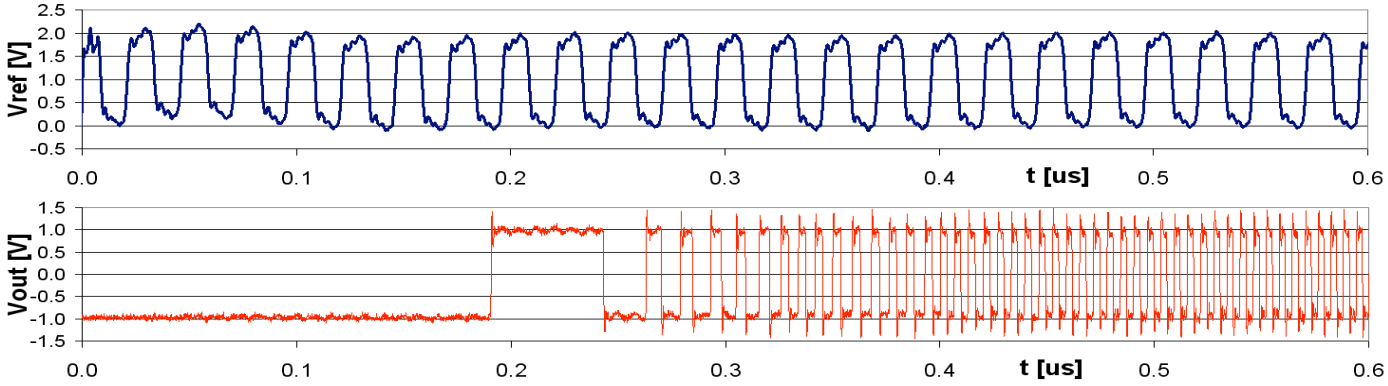
PLL Prototype

- Cell designed and produced in 0.25µm
- PLL locks for 10 … 75 MHz reference frequency
- Supply current: 720 µA
- Lock time: 3 µs
- Jitter < 30 ps

start up phase vs time

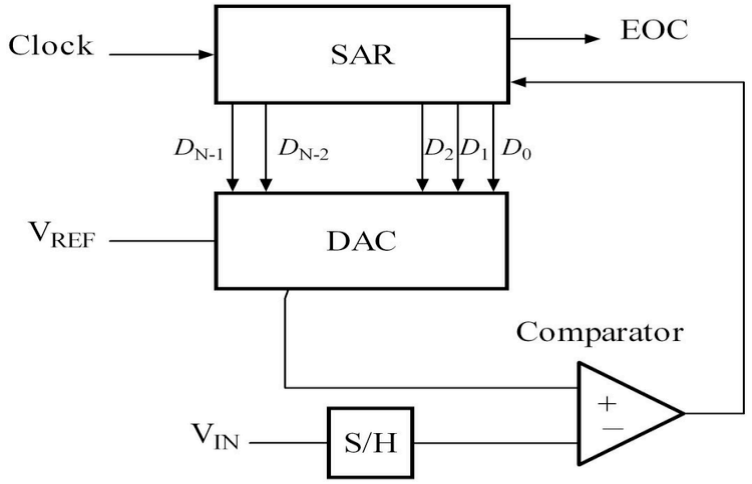


reference and output signal at start up



8-bit ADC

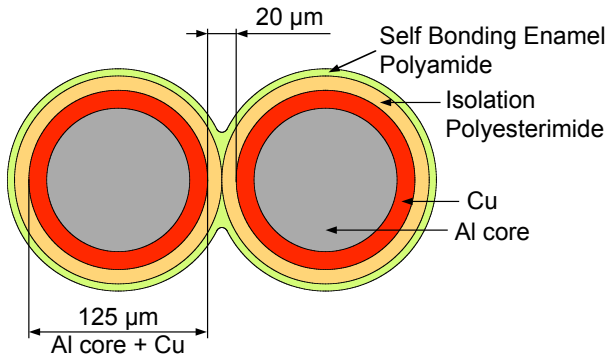
- Successive approximation 8 bit ADC with S&H
- Clock frequency: 80 MHz
- Conversions time: 8 clock cycles



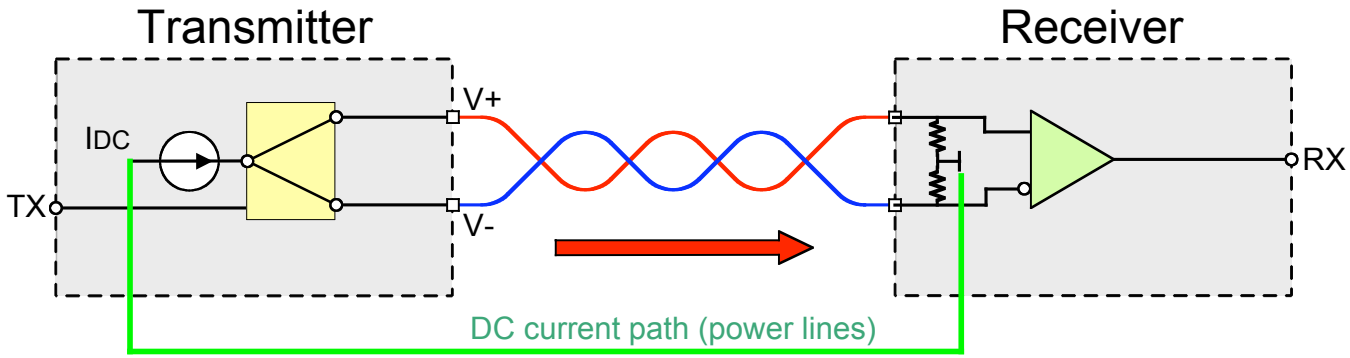
- Prototype designed and under test
- Results:
  - Works well up to 40 MHz
  - Very good linearity
  - But: is unstable at 80 MHz
    - → good diagnostic possibilities
    - → could reproduce in simulation by adding parasitics
    - → problem likely understood (need more confirmation). Solution in hand

Electrical Low Power Data Link

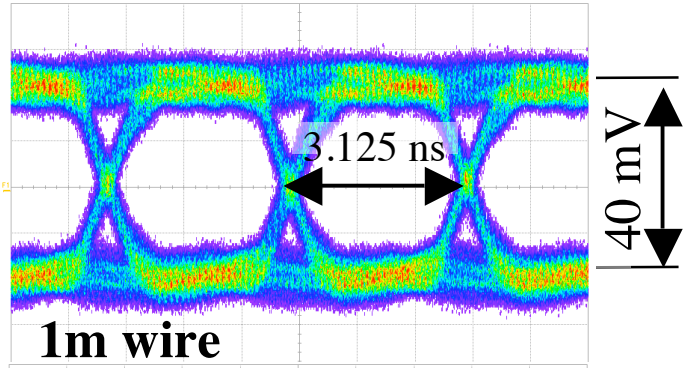
- 1216 Up links from module to outside the tracking area
- 320 MBit/s over 1 m
- Unshielded micro twisted pair cable (125 µm wire diameter, low mass)

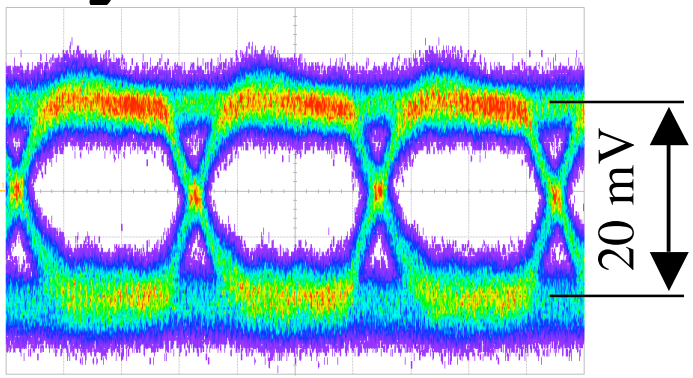


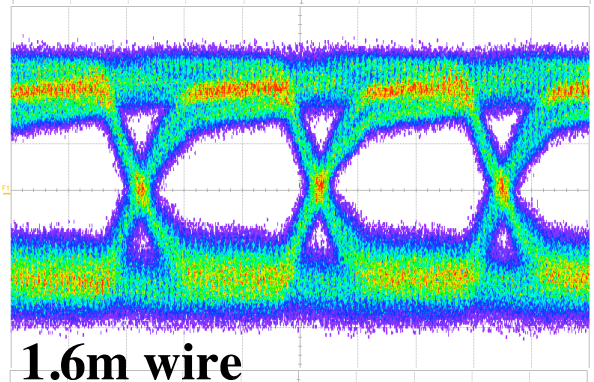
- Low power differential driver and receiver (LCDS)
- Bundled with power and control wires to one module cable

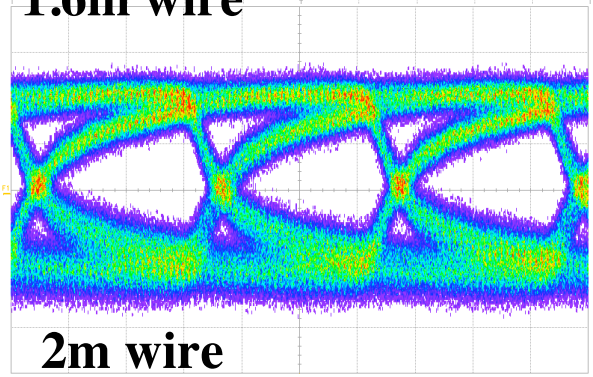


Results: Eye Pattern









- Wire length: 1 m
- 320 Mbit/s
- Minimal amplitude: 20 mV (+/- 10mV)
- +/- 500 mV DC offset between driver and receiver
- Bit error rate < 10e-12 (different condition)
- Crosstalk: -27 dB
- Power consumption / link: 4mW (12 pJ/bit)

Conclusion

New improved design for CMS pixel detector shown

- **4 barrel layers and 3+3 disks**

Large reduction in material budget

- **Mainly due to change in cooling system to CO_2 cooling**
- **Extra savings by moving material out of tracking volume**

Mechanical design finished (barrel) or quite advanced (disks)

Barrel: Prototype for layer 1 mechanics built

Prototype for supply tube in production

Electronics based on present front end:

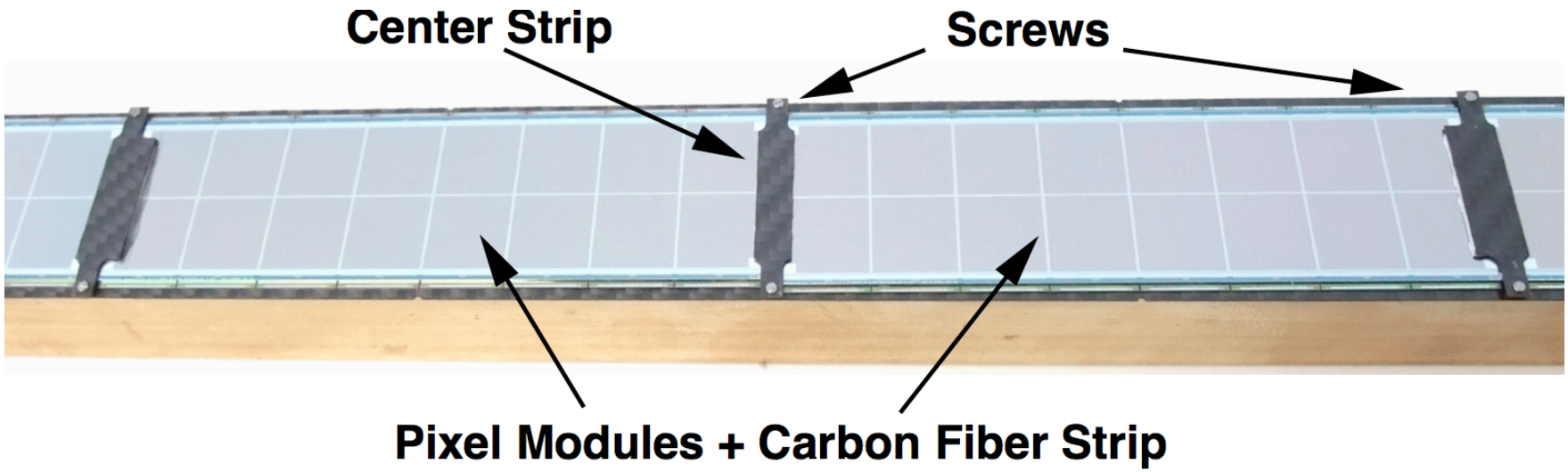
- **ROC sufficient radiation tolerant.**
- **Improvements to reduce inefficiency needed. All new critical cells prototyped and tested.**
- **TBM (module controller chip): need new design of uplink part**

Sensor: baseline is present technology

Target date for insertion: 2014. Not approved yet by CMS

Backup Slides

New module mounting

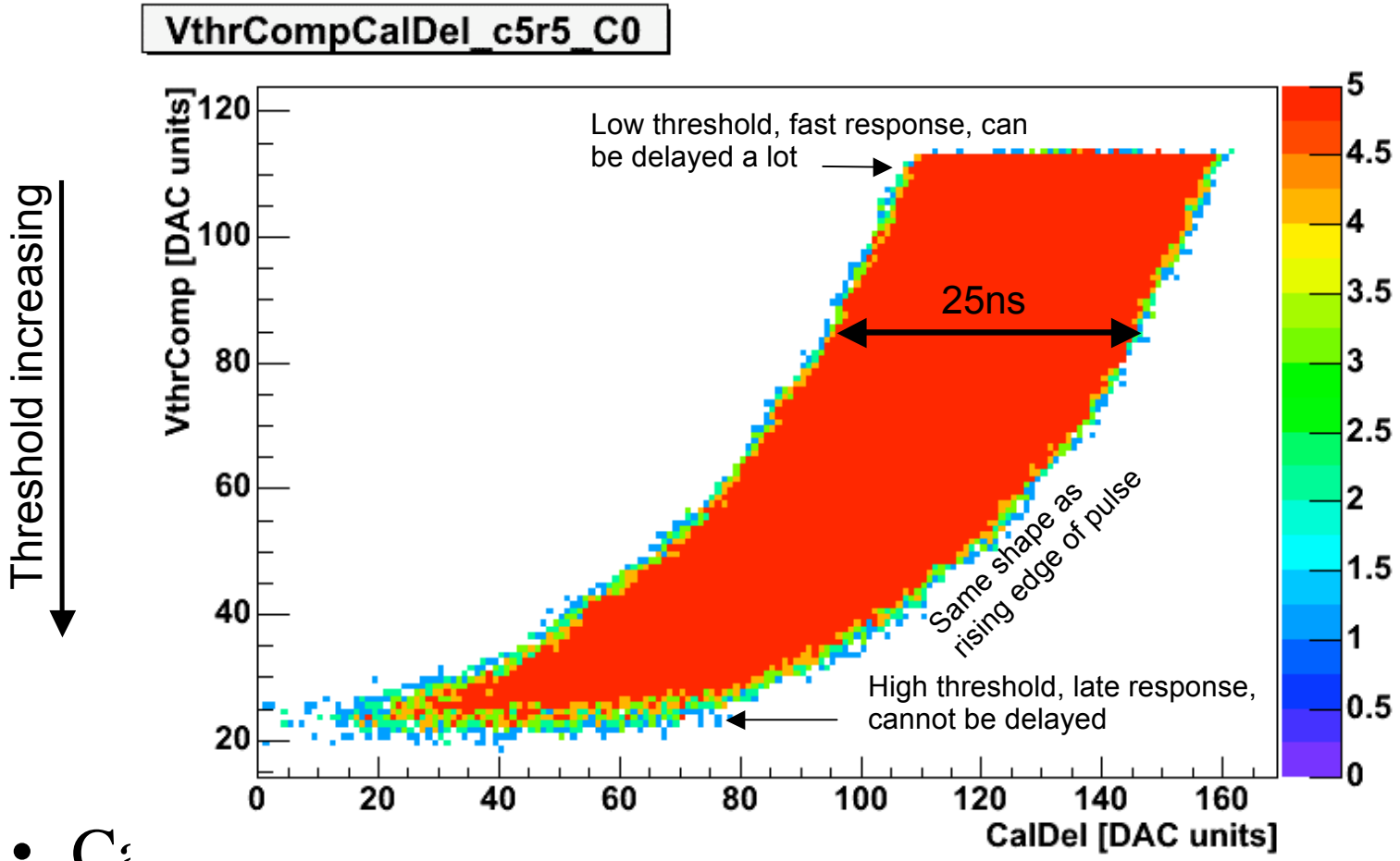


Data Rate Estimations

- Preliminary phase I geometry (4 layers, radii ~correct, ladder not yet correct, still halfmodules)
- Assuming 24 bits per hit, 100kHz L1A
- Peak lumi=$2x10^{34}cm^{-2}s^{-1}$, σ_{tot}=80mb, σ_{signal}=1.5mb
- Data rate includes headers/trailers
- Bandwidth of present analog links ≈ 100 Mbit/sec peak

Layer	1	2	3	4
Pixel fluence [MHz/cm^2]	224	96	48	27
Hits / trigger / module	68	31	15	8.4
MBit/link/sec	194	93.6	55.9	40.0
# links	128	224	352	512

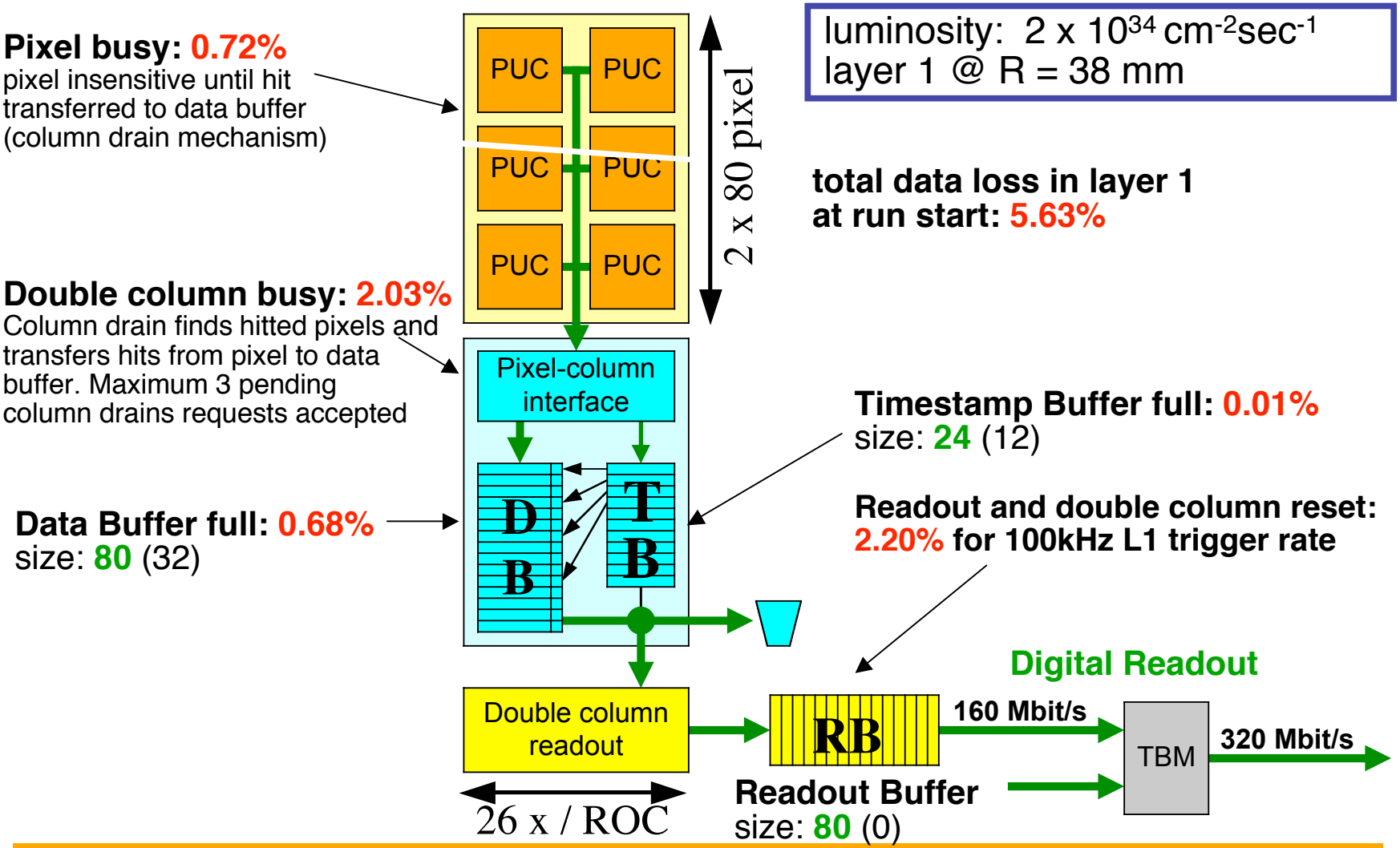
Rise time of preamplifier



- Cannot directly be measured (no "transparent" mode)
- Presented method is very indirect and time

- Use feature to delay injection of calibration signal
- Now have to calibrate both axis

Data loss Mechanisms in ROC



Basic Idea of digital module