Refinements of Positron Accumulation Technique at ATRAP

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13 August 2009

Basic Outline

- Introduction to ATRAP
- Introduction to positron trapping
- Summary of summer work
- Explanation of final project

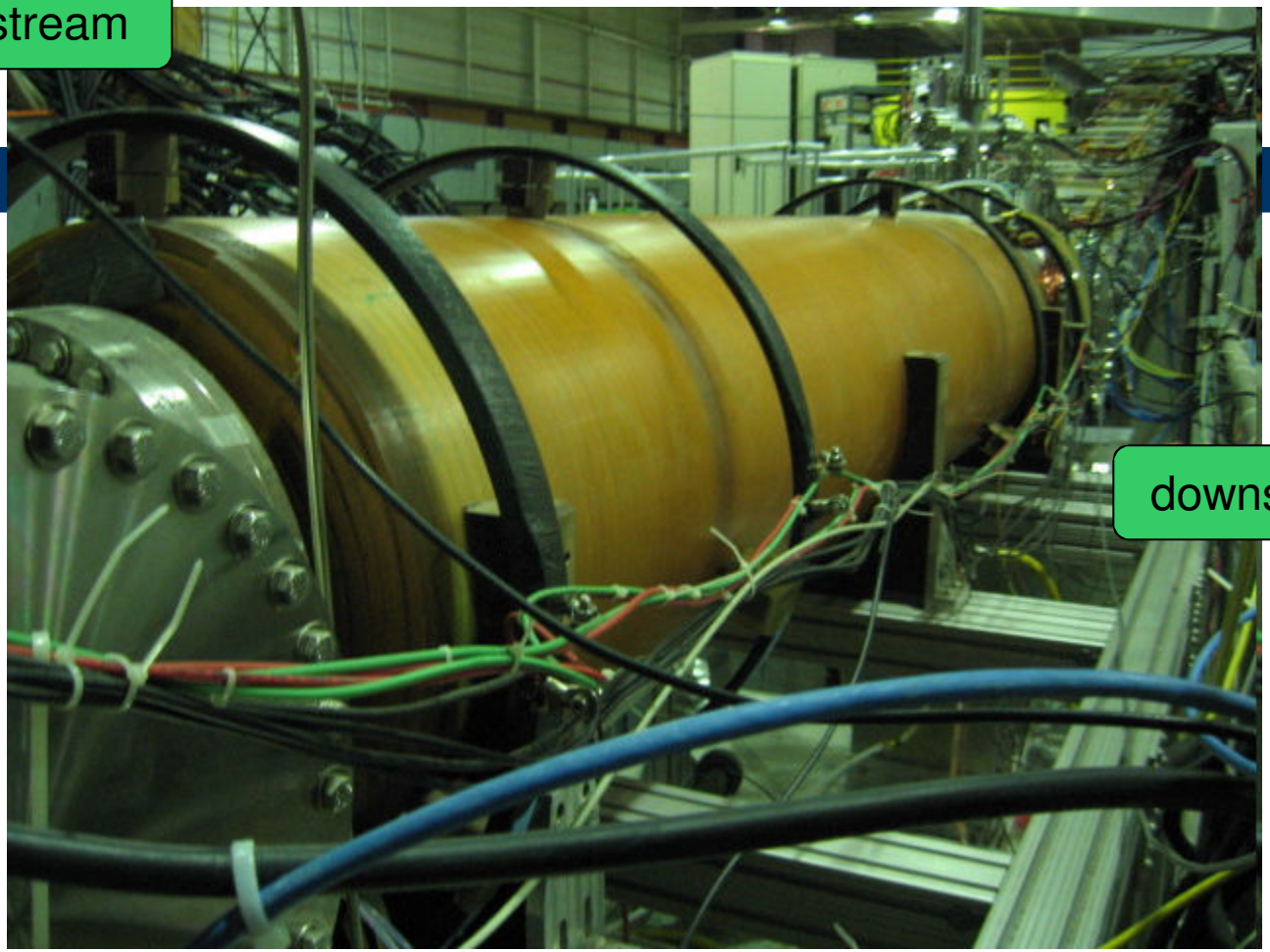
ATRAP in Brief

- ATRAP (Antihydrogen TRAP) seeks to form antihydrogen atoms by cooling and trapping positrons obtained from a Na-22 radioactive source and antiprotons obtained from the AD (Antiproton Decelerator)
- Antiproton (p-bar) beam time shared between ATRAP, ALPHA, ASACUSA and ACE experiments
- ATRAP contributing teams from Harvard University, Mainz University, York University, Juelich

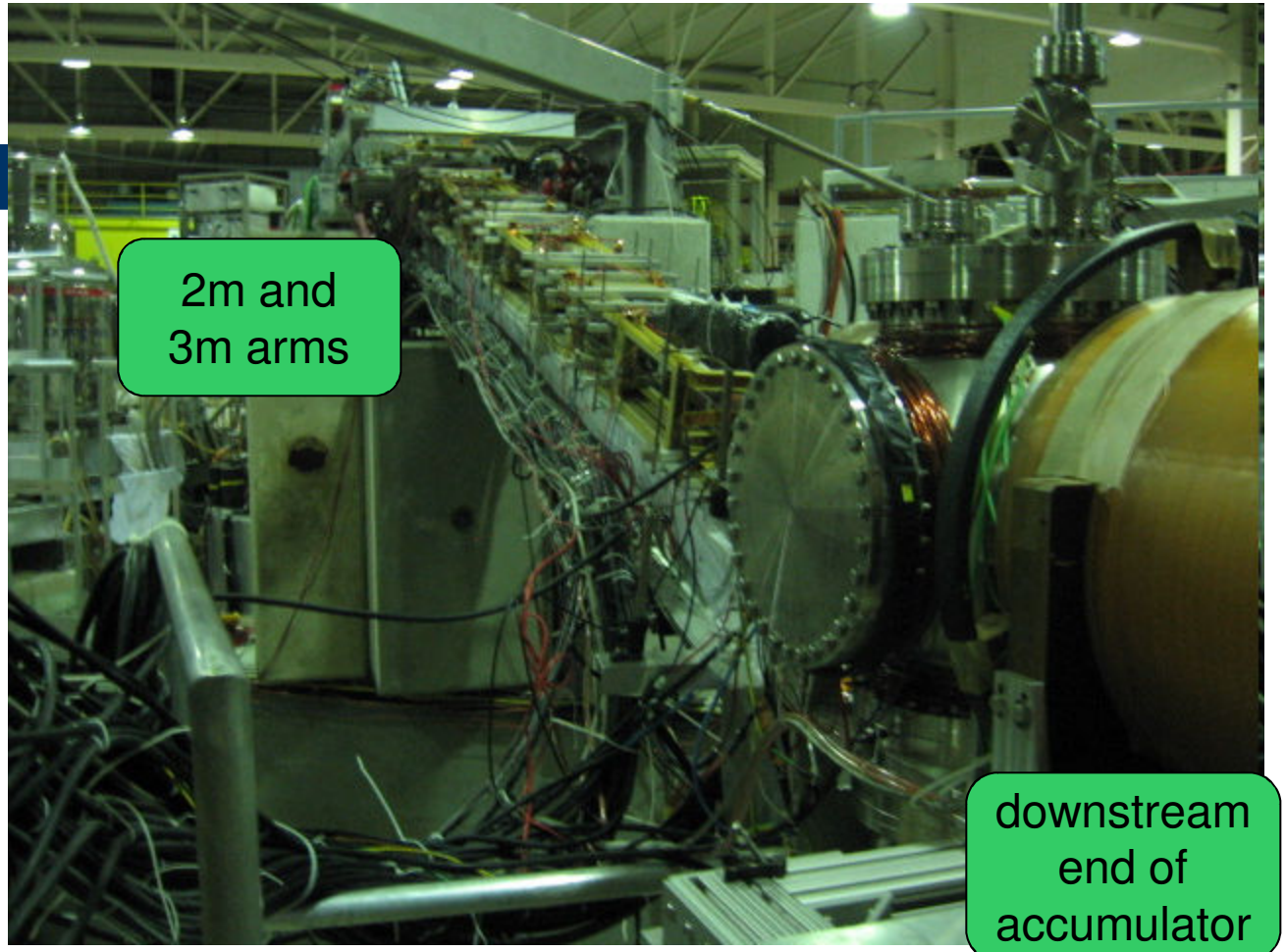
Positron Accumulation and Trapping

- Controlled by team from York University
- Source: radioactive Na-22 (half-life 2.6 y), positrons are cooled by passing through a Ne moderator.
- Positrons are further cooled after they collide with gas molecules in a Penning trap and are then transferred to the antiprotons using 95 electromagnets (located in 3m and 2m sections)
- Goal: get cooled positrons into a nested Penning-Ioffe trap (combination of electric and magnetic fields) with cooled antiprotons (courtesy of Harvard team)

upstream



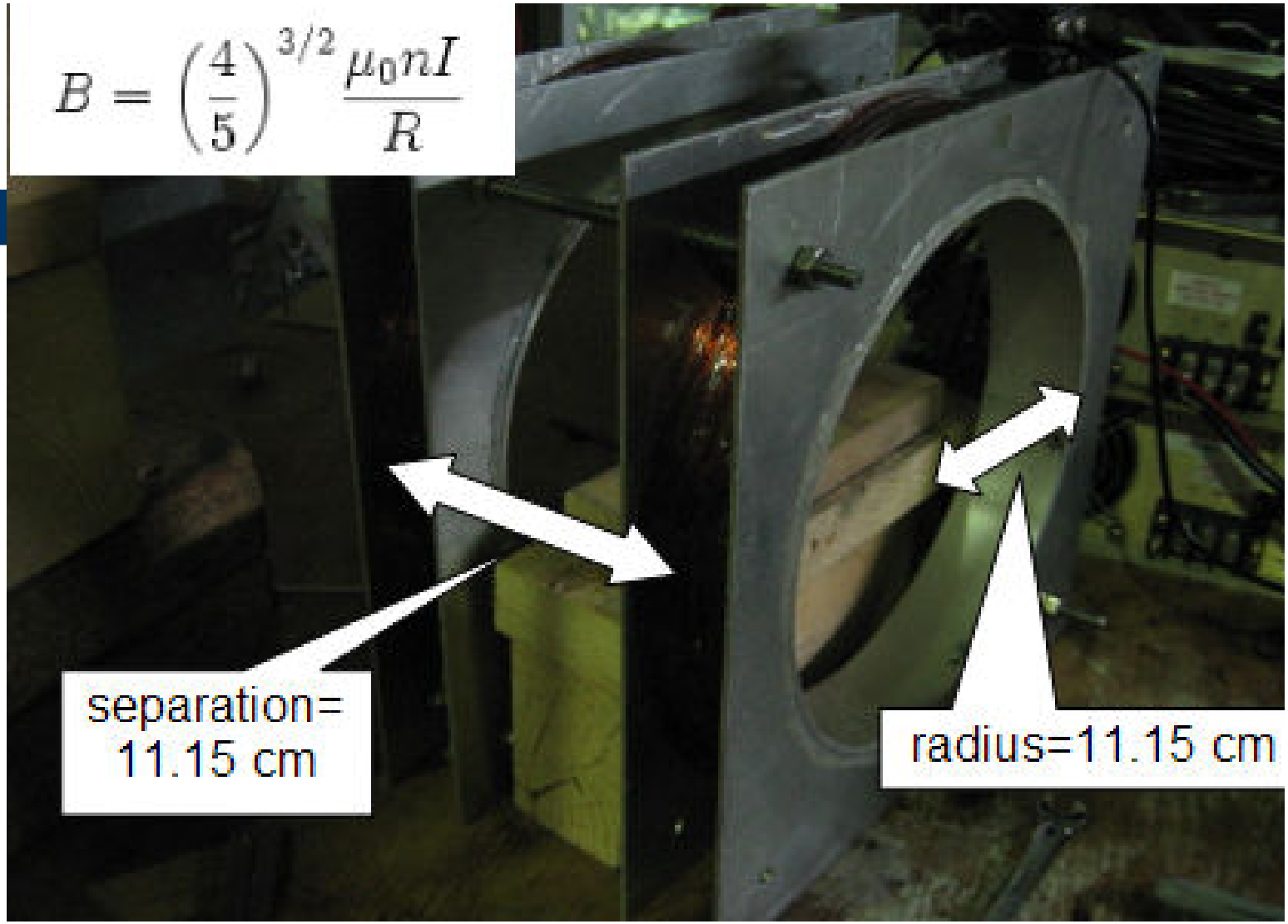
downstream


2m and
3m arms
downstream
end of
accumulator

Past Projects

- Increasing the accuracy of the program that controls temperatures for moderator regrowth
- Optimizing the efficiency of database retrieval for comparing values from past log files
- Recalibrating magnetic field sensors in response to unexpected readings for the magnetic field around the accumulator

$$B = \left(\frac{4}{5}\right)^{3/2} \frac{\mu_0 n I}{R}$$



Background values with old calibration

Background (V)			Background (gauss)		
x	y	z	x	y	z
2.220	2.210	2.215	-9.664	-9.727	-9.377
2.220	2.210	2.215	-9.664	-9.727	-9.377
2.220	2.210	2.215	-9.664	-9.727	-9.377
2.220	2.210	2.215	-9.664	-9.727	-9.377
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2.220	2.210	2.215	-9.664	-9.727	-9.377
2.220	2.210	2.215	-9.664	-9.727	-9.377

Background values with new calibration

Background (V)			Ba		ound (gauss)
x	y	z	x	y	z
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
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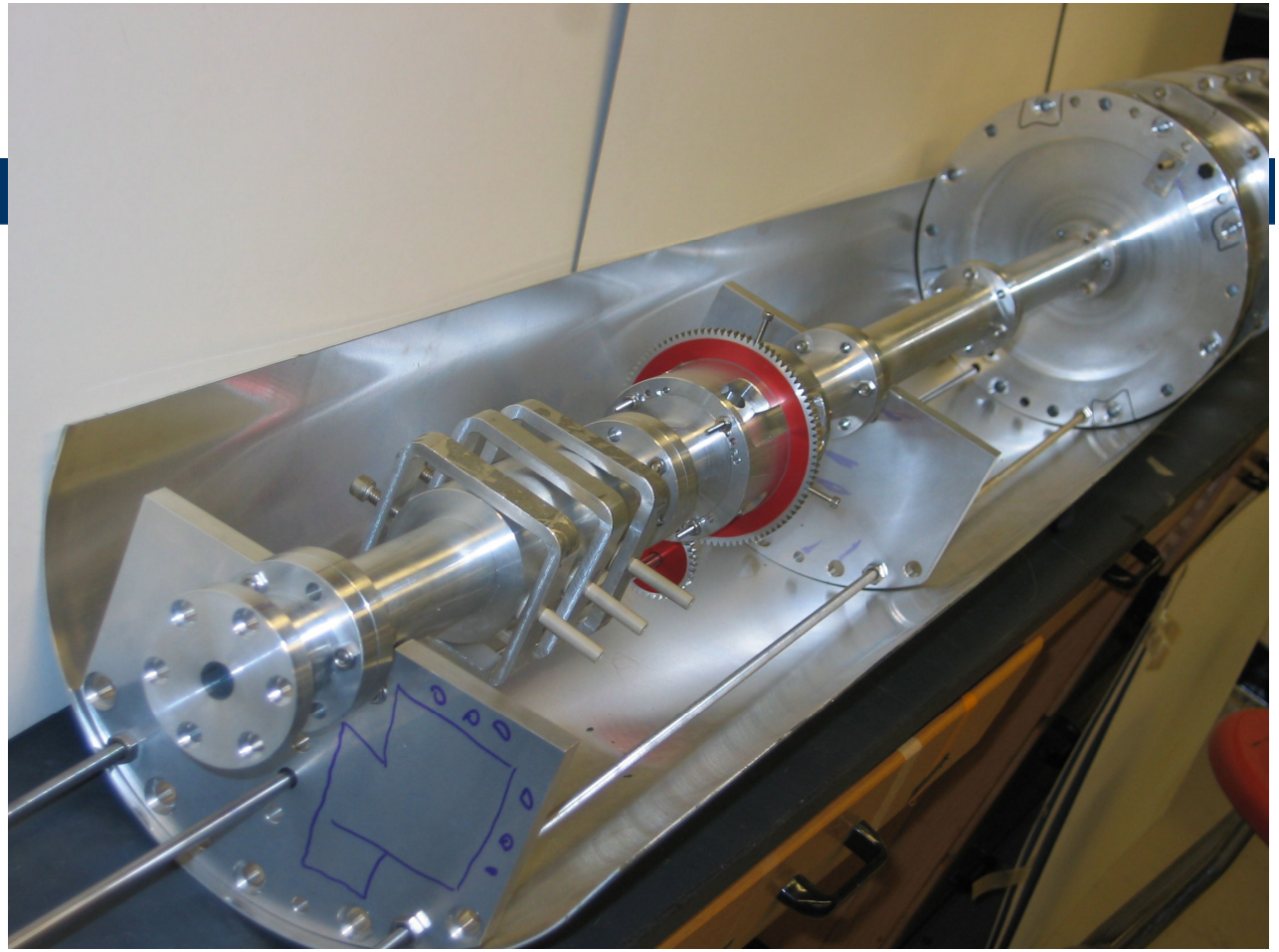
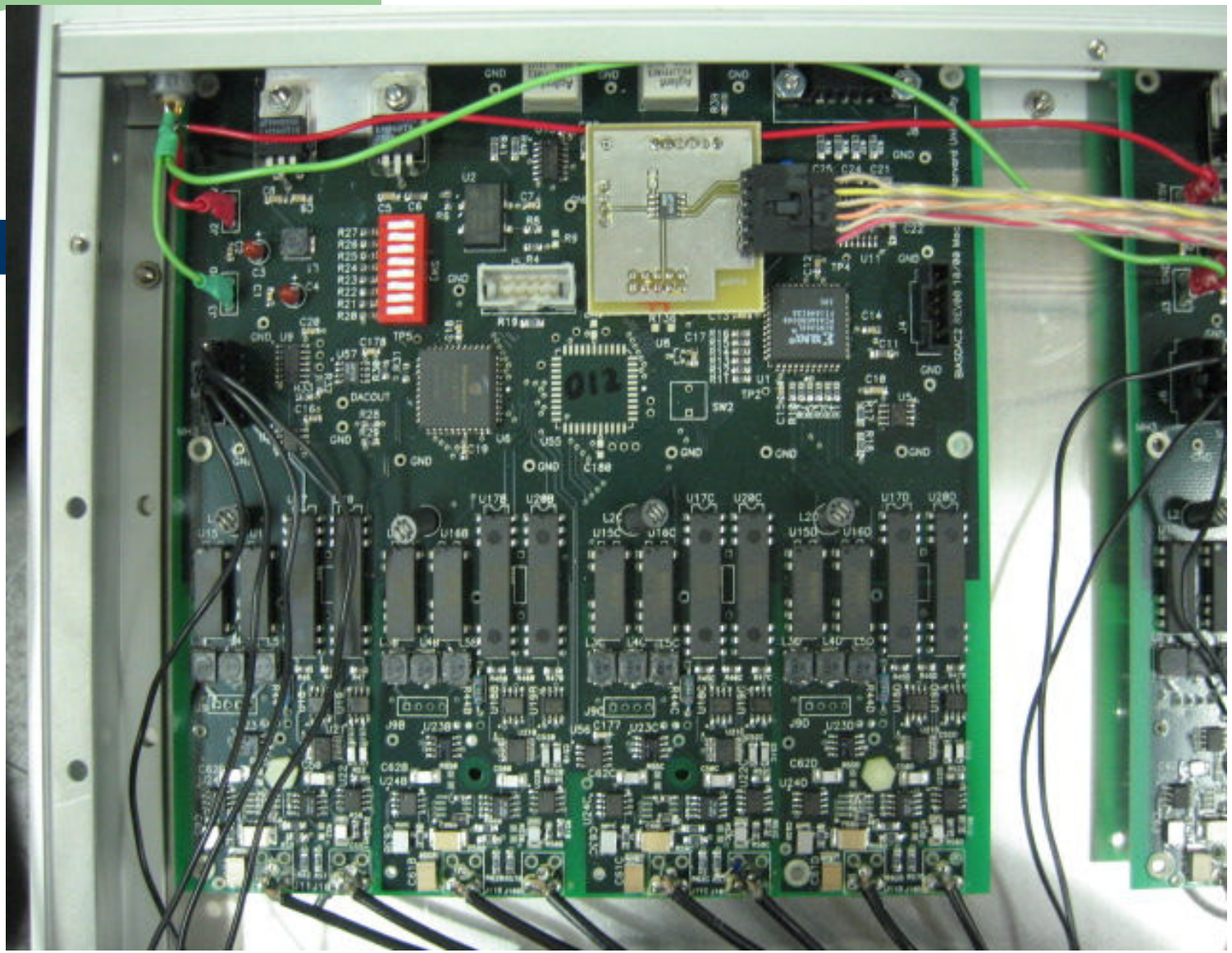
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279
2.220	2.210	2.215	-0.416	-1.031	-5.279

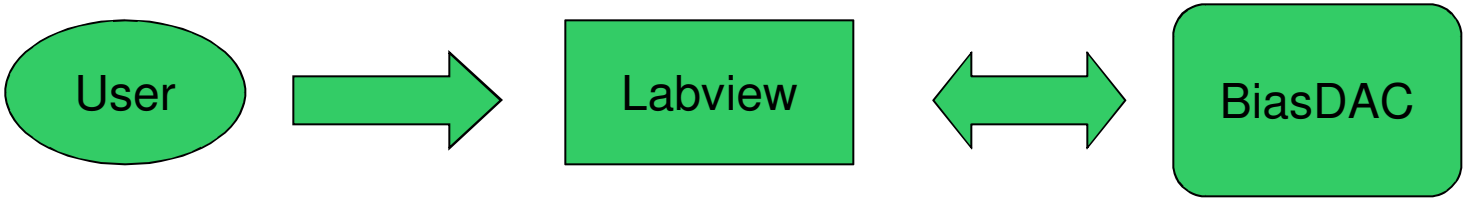
Final Project

- Improve the functionality and reliability of the accumulator electrodes by changing the method of controlling their voltages
- Voltages for the ten electrodes are controlled by four biasDACs (biasDAC: four-channel digital-to-analog converter board)
- Advantages of biasDACs: low drift, can be programmed to run independently

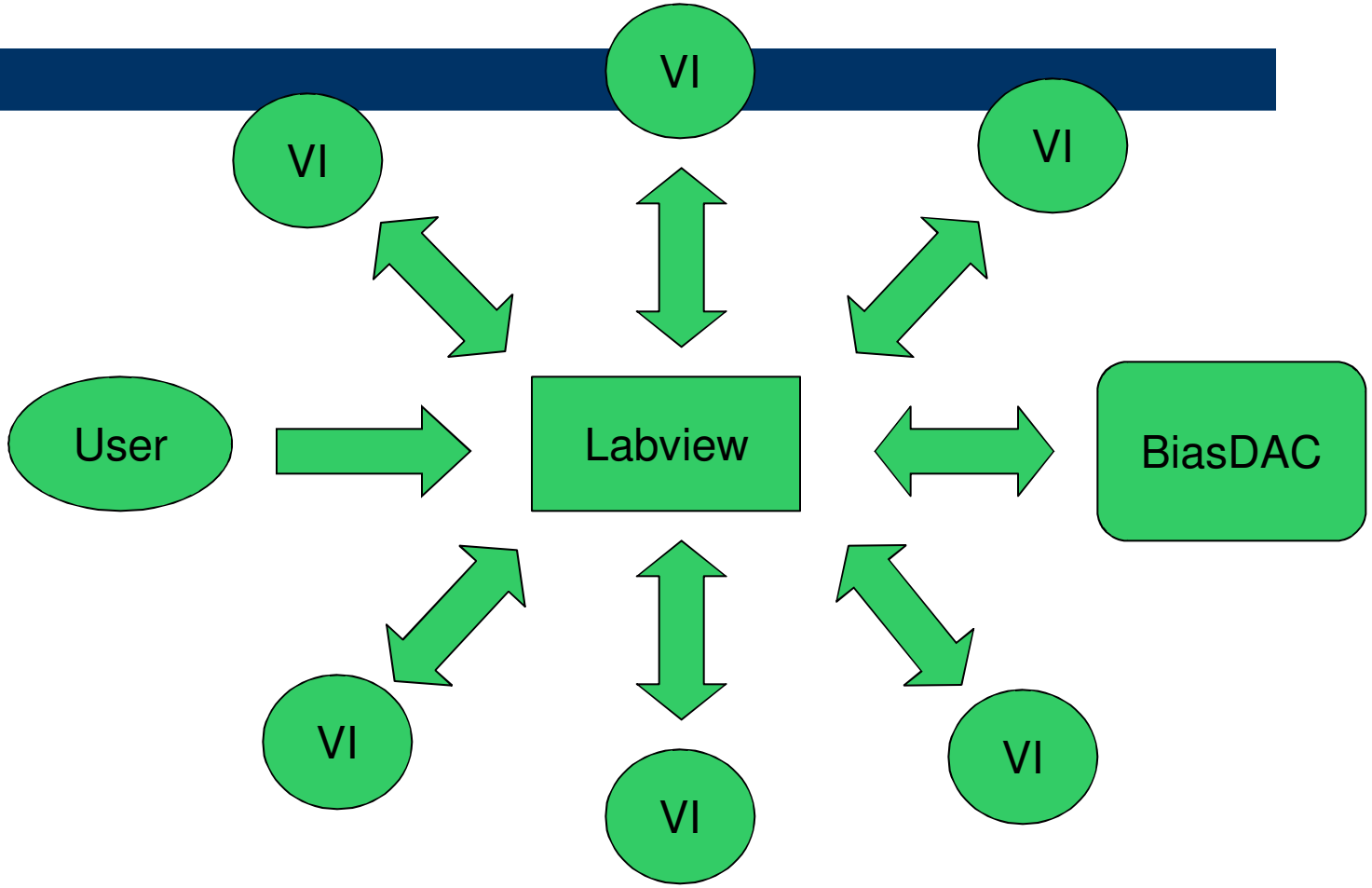



GND
U2
R4
R19
DACOUT
SW2
TP2
TP4
TP5
U1
U11
U17
U20
U15
U16
J9B
J9C
J9D
U23B
U23C
U23D
U24B
U24C
U24D
C62B
C62C
C62D

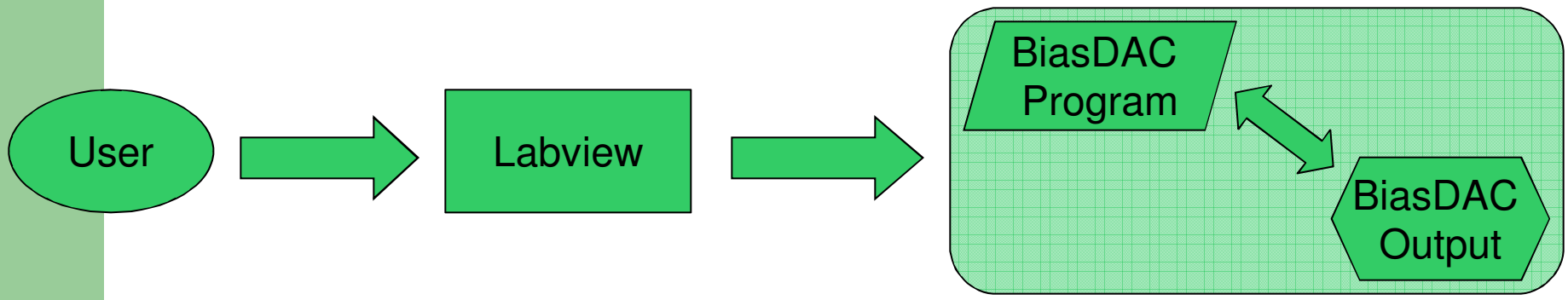
Original Setup



So What's the Problem?



Ideal Setup



Goals of Final Project

- Gain a thorough understanding of the biasDACs and the commands that control them
- In addition to the Labview-dependent biasDAC controls, develop an alternative that allows the biasDAC to run its program independently of Labview once started
- Retain the ability to trigger on signals from the AD and send signals to the Harvard team

BiasDAC Test Setup

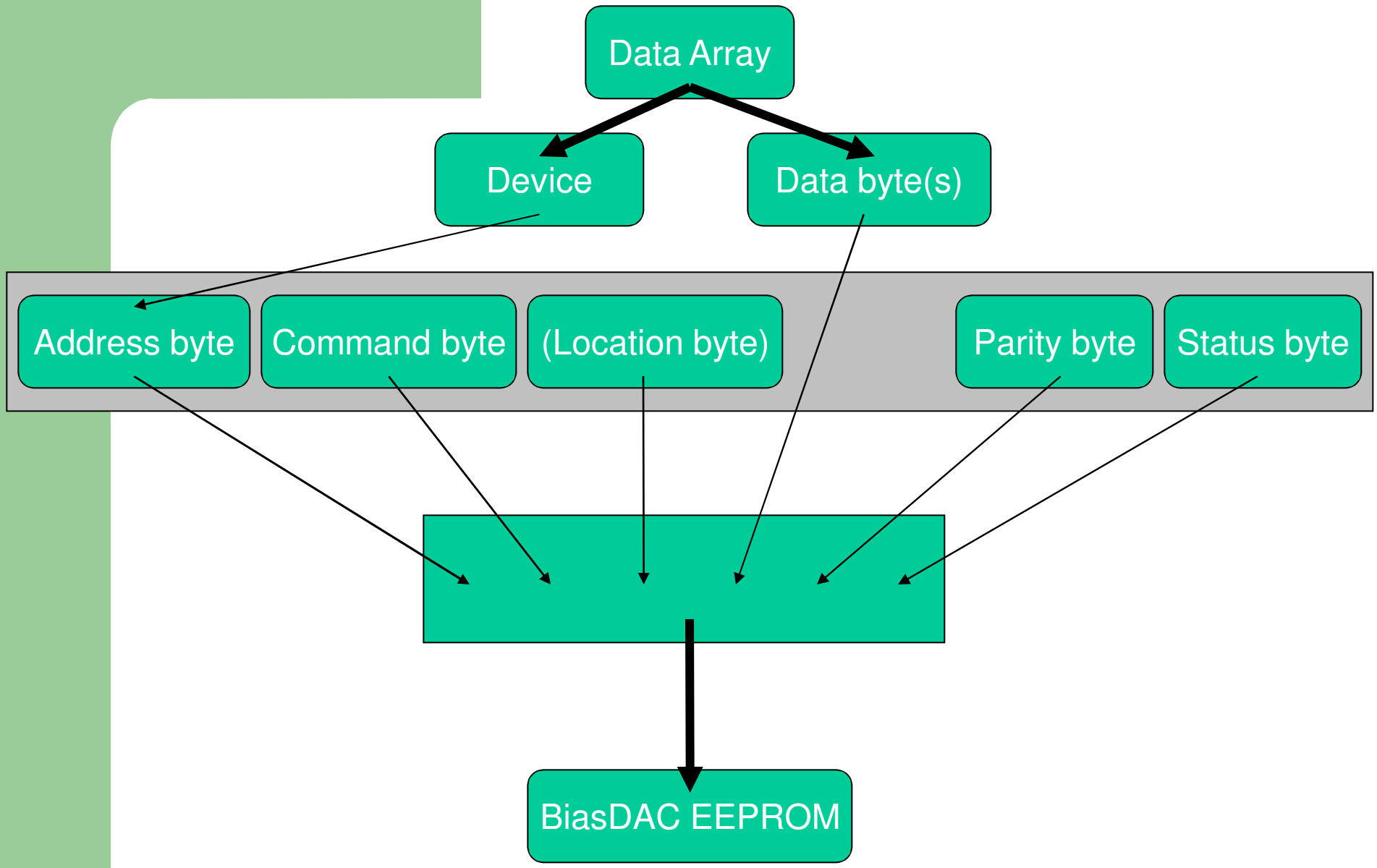
- Two biasDAC boards (devices), each controlling four channels
- Master-slave arrangement connected by RS-485
- Can be connected to serial port directly or through fiber-optic ring and fiber-optic/RS-232 converter
- Output range: -10V to +10V

BiasDAC Programming

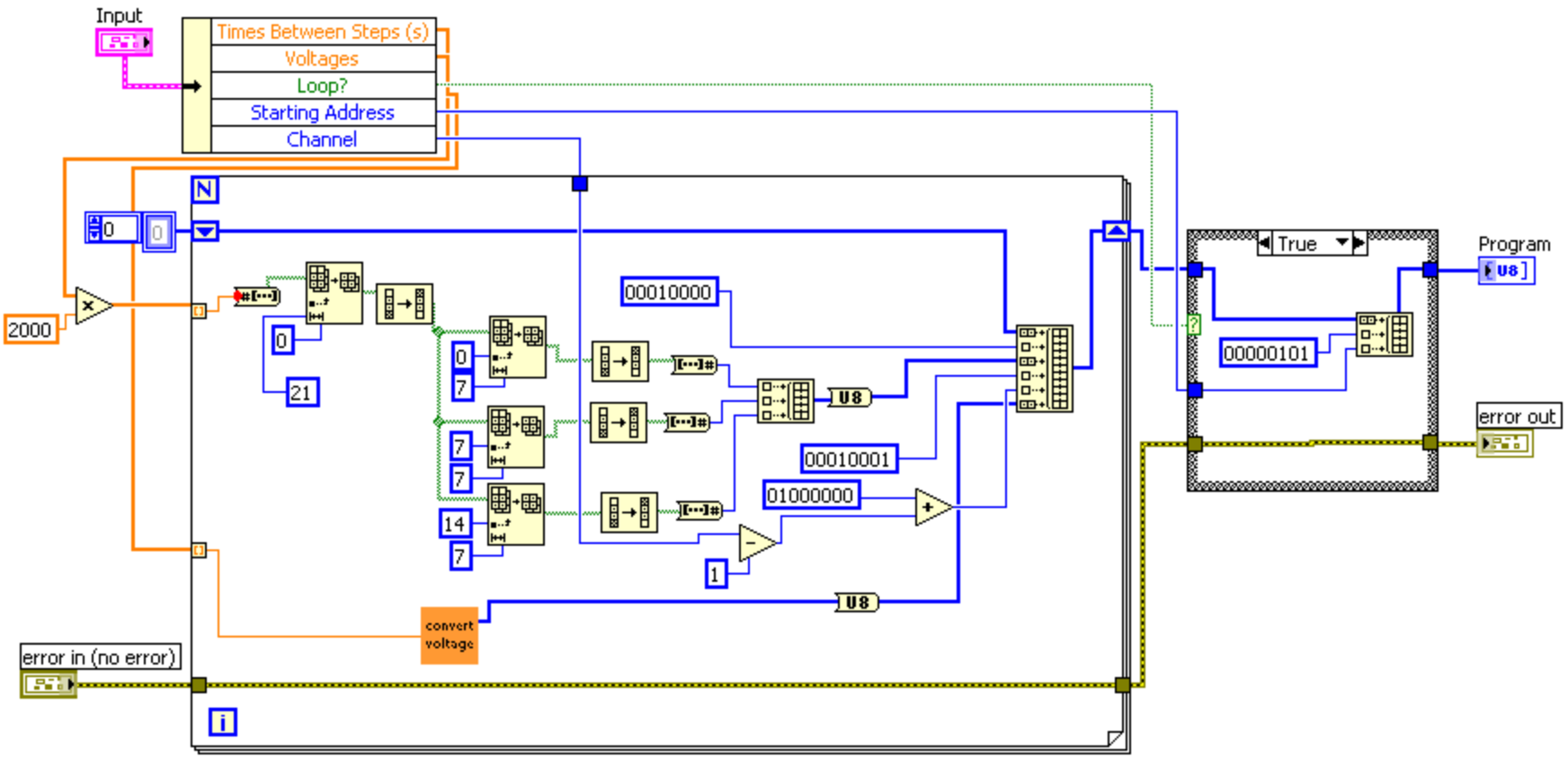
- Goal: store sequence of voltage settings and wait times as program in biasDAC memory (EEPROM, 128 bytes)
- Necessary for each program byte: address byte, command byte, location byte, parity byte, status byte
- Limitations: time to wait between storing program bytes (at least 10 ms), 128-byte limit of device EEPROM

Prototype Program

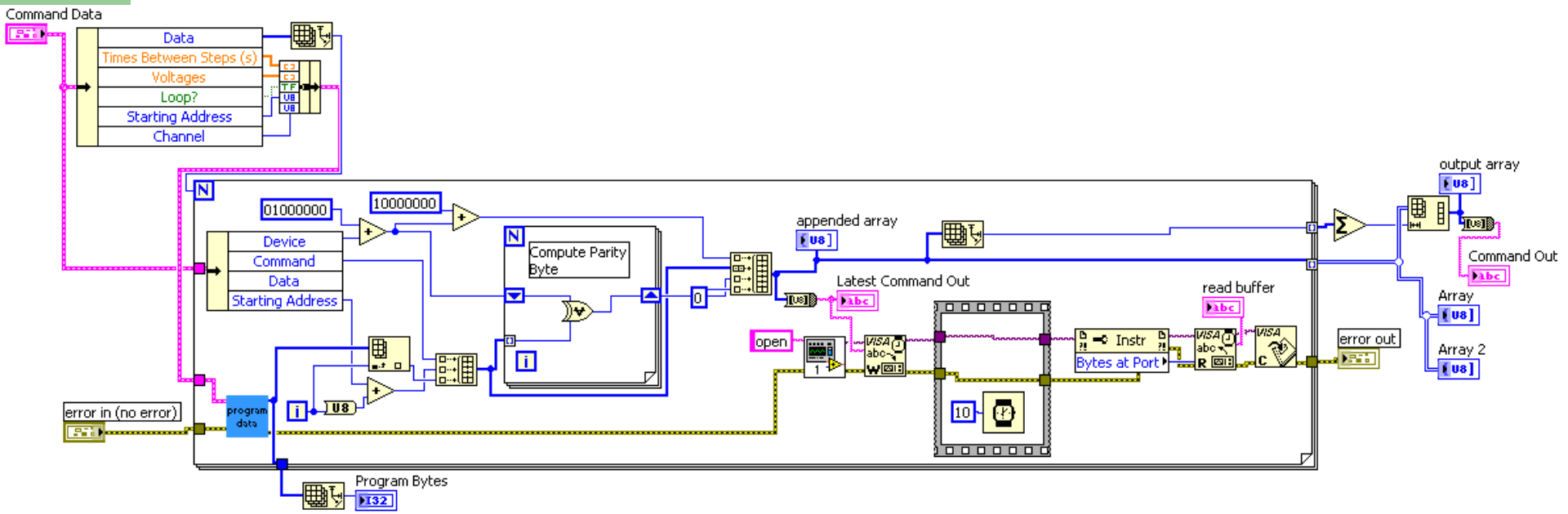
- Writes program to one specified channel of one device
- User enters voltages and wait times, specifies device, channel, and starting address for program
- Labview VI calculates and appends address, command, location, parity, and status bytes
- Options to loop program and to stop program from Labview panel

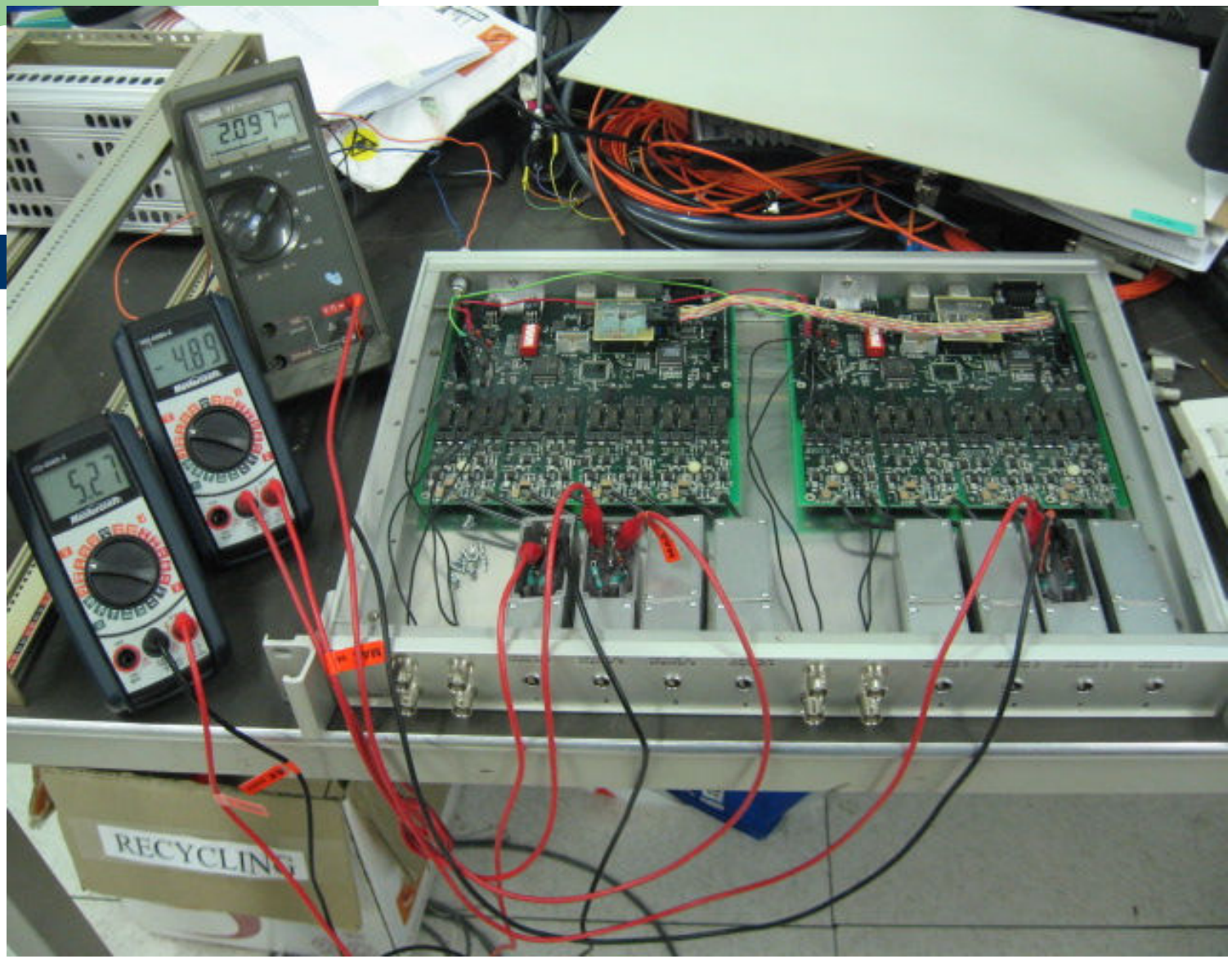

Data Array
Device
Data byte(s)
Address byte
Command byte
(Location byte)
Parity byte
Status byte
BiasDAC EEPROM

Prototype Program



Prototype Program



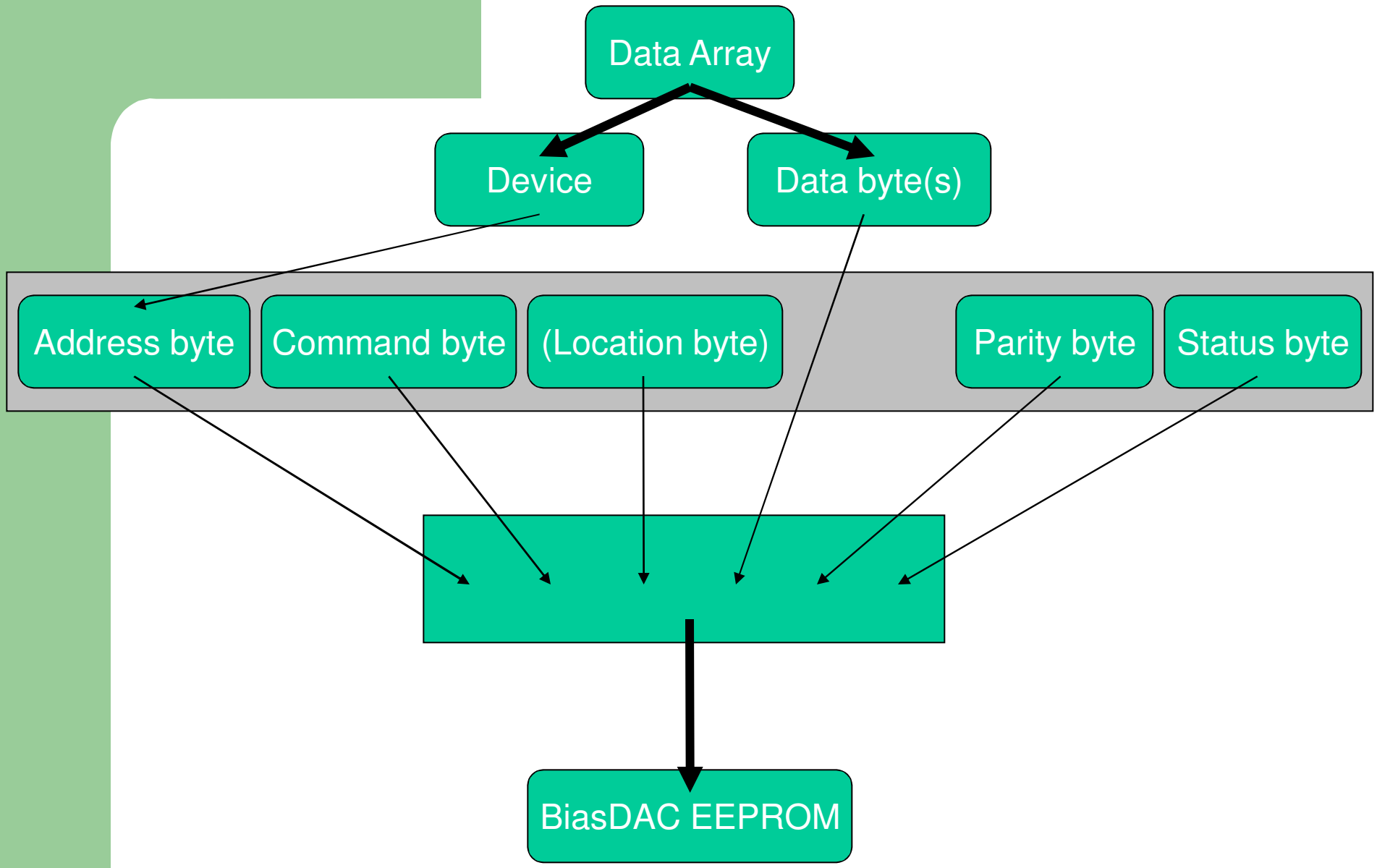

RECYCLING

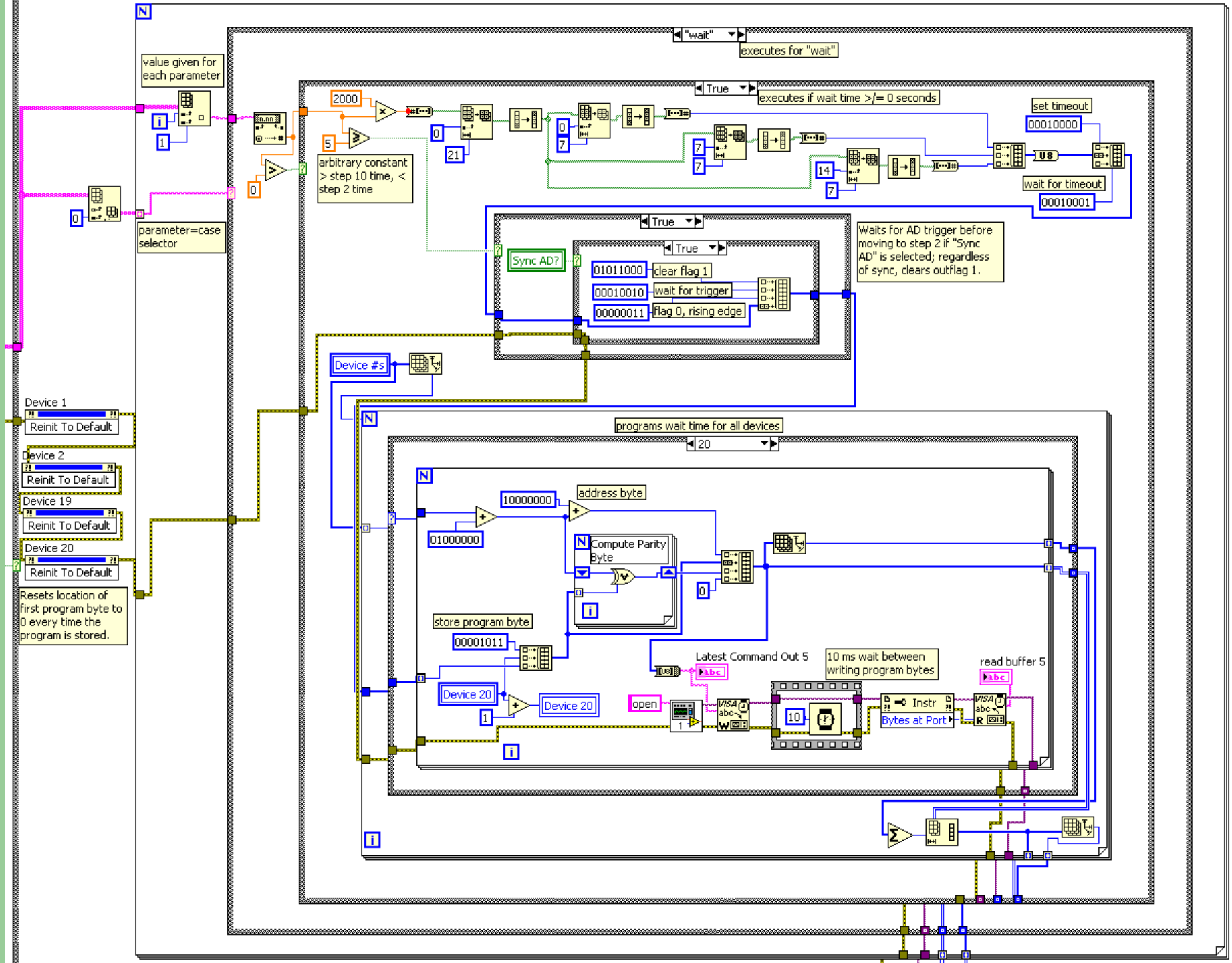
Adaptation and Improvement

- Program must be able to write to any of four channels, depending on the parameter name specified in the input array
- Ideally, program-writing option should be available alongside the original Labview-controlled method
- Must receive trigger from the Antiproton Decelerator and send signal to the antiproton accumulation side of the project

Final Form of Program

- Integrated with existing Labview VI to control biasDAC voltages, leaving the option to use step-by-step Labview control
- Featured options: write program as loop or one-time run, write program to cycle automatically or wait for AD triggers, run program with option to stop loop from Labview front panel


Data Array
Device
Data byte(s)
Address byte
Command byte
(Location byte)
Parity byte
Status byte
BiasDAC EEPROM


"wait"
executes for "wait"
value given for each parameter
True
executes if wait time >/= 0 seconds
2000
5
arbitrary constant > step 10 time, < step 2 time
set timeout
00010000
wait for timeout
00010001
parameter=case selector
True
True
Sync AD?
01011000
clear flag 1
00010010
wait for trigger
00000011
flag 0, rising edge
Waits for AD trigger before moving to step 2 if "Sync AD" is selected; regardless of sync, clears outflag 1.
Device #s
Device 1
Reinit To Default
Device 2
Reinit To Default
Device 19
Reinit To Default
Device 20
Reinit To Default
Resets location of first program byte to 0 every time the program is stored.
programs wait time for all devices
20
10000000
address byte
01000000
Compute Parity Byte
store program byte
00001011
Device 20
Device 20
Latest Command Out 5
10 ms wait between writing program bytes
read buffer 5
open
Instr
Bytes at Port

Acknowledgments

- Joseph Borbely (York), Gerald Gabrielse (Harvard), the ATRAP collaboration
- Jean Krisch, Myron Campbell, Homer Neal, Jeremy Herr, Steve Goldfarb, the UM-CERN REU staff
- The Marcus Group at Harvard (mesoscopic physics research)

Thanks for a great summer at CERN!


IT'S
ATRAP!