MTCA.4 as a new Frontend Platform
Status & Plans

BE-BI Technical Board

Geneva, 14 September 2017
Agenda

- Introduction
  - Front-end platforms: what are these?
  - Purpose
  - Scope
  - Why MTCA.4?

- MTCA.4 Proof of Concept
  - SPS Low Level RF renovation

- Summary
Front-Ends: what are these?

Bus:
- PCI
- VME
- WorldFIP
- MIL1553
- Ethernet

Multiple platforms:
- PICMG 1.3
- VME/VME64x
- PXI/PXIe
- CompactPCI

Devices controlling the accelerator
- Digital I/O
- Sensor
- Timing
- Switch
- Power converter
- ADC
- DAC
- Function generator
Current Front-End Platforms

VME/VME64x

PICMG1.3 Industrial PCs

PLCs

CompactPCI

MTCA.4 as a new Frontend Platform
Purpose

Evaluate, choose and introduce modern hardware platform(s) for the Front-End tier, by the end of LS2.

- Deal with technical drawbacks of VME systems (low bandwidth, no timing or standard management of crates)
- Avoid making custom VME derivatives
- VME, despite being very strong at CERN is loosing users. Major labs (e.g. DESY, SLAC) already departed from VME camp. New platforms (MTCA.4 or VPX) are gaining market
- Deal with issues with PICMG1.3 (power dissipation, maintenance difficulties)
- BE-CO mandate: work together with the users and provide a centrally supported platform that meets their needs
Scope (overall)

- Define the strategy for future front-end platforms:
  - Choose the successor(s) of VME
  - Define a date to start recommending the new platform for new developments
  - Evolution of PICMG1.3 or another PCI/PCIe-based platform
  - Embedded devices in the front-end layer (e.g., Zynq FPGAs running Linux & FESA)

- Provide a standard hardware/software kit that users can build their applications upon:
  - Port the existing FMC kit to the chosen platforms
  - Provide a timing receiver for each new platform
  - Standard BE-CO SLC/CentOS support

- Provide reusable HDL cores and PCB templates:
  - Example: we have 3 or 4 different HDL cores for a VME slave interface, all of which are incomplete and buggy!
Scope (PoC projects)

- Gather necessary experience for possible future platforms by building Proof-of-Concept projects:
  - Discover drawbacks and advantages of the platforms in practice
  - Deal with aspects difficult to evaluate otherwise, e.g. mechanical reliability, ease of HDL/software/PCB design, efficiency of collaboration with hardware vendors, etc.
  - Gather in-depth technical expertise before taking any long-term decisions
- Ultimate go-for/no-go decision for each platform after completion of the respective PoC project
Why MTCA.4?

After a requirements survey involving BE-CO and the equipment groups (2016), MTCA.4 (and PXIe) are clear winners:

- Gigabit inter-board communication and timing in the backplane
- Standard means of management and monitoring (AMT, IPMI)
- Based on PCI Express: simplified driver model
- Support for RTMs and RF applications (MTCA.4)
- Significant investment in MTCA.4 (DESY) and growing number of applications (not only in accelerator/physics market)
MTCA.4 Proof-of-Concept
New Low-Level RF system for the SPS

- Controls the electromagnetic field in the accelerating cavities
- Measures the field in the cavity using an antenna
MTCA.4 Proof-of-Concept
New Low-Level RF system for the SPS

- Feedback loop algorithm in a FPGA:
  - Calculates RF frequency, phase and amplitude according to the current beam energy and position
  - Tunes the cavity to the current RF frequency
- Drives a powerful RF amplifier (klystron/IOT)
  - Provides the power to accelerate the particles
MTCA.4 Proof-of-Concept

Goals

- A replacement of the analog controls for 200 MHz TWT SPS cavities
- Joint effort between BE-RF and BE-CO (HT, IN, SRC)
- A playground for new LLRF ideas:
  - Fixed sample rate processing
  - Distributed clocking by White Rabbit
- Benefit from DESY’s LLRF for XFEL. Minimum hardware design effort required
  - PoC uses slightly modified off-the-shelf modules
  - Most effort in gateware development
MTCA.4 Proof-of-Concept Equipment

- MTCA.4 crates
- Vector Modulator/Downconverter
- CPU
- MCH (crate controller)
- SIS8300 (Struck) ADC/DAC FPGA for the feedback loop
- RF backplane

MTCA.4 as a new Frontend Platform
MTCA.4 Proof-of-Concept
Responsibilities and Deliverables

**BE-CO:**
- **OS support** (IN/S.Page)
- **Drivers, libraries, test programs** (HT/D.Cobas)
- **Remote management and monitoring** (IN/S.Page & SRC/F.Locci)
- **Basic FPGA framework** (PCIe, DDR4, DMA) (HT)
- **White Rabbit and GMT support for the modules used by RF**
- **MMC firmware:**
  - A microcontroller taking care of management of a MTCA.4 card
  - In collaboration with EP-ESE

**BE-RF:**
- **Feedback loop design**
- **FESA classes**
- **Customization of the hardware for particular SPS requirements**
MTCA.4 Proof-of-Concept

Status & outlook

- Strong commitment from CO and RF
  - Project well on track
- MTCA.4 hardware received Jun 2017
- CentOS 7 running on the system in the labs.
- FPGA framework development in progress:
  - White Rabbit running on Kintex Ultrascale FPGAs.
  - Integration of AXI4, Wishbone and Cheburashka/Gena busses.
- Driver development ongoing:
  - PCI support in Encore.
- Excellent support from the MTCA.4 system vendor (NAT)
Key milestones

- Oct 2017: first milestone of the MTCA.4 PoC (single cavity controller)
- Dec 2017: cavity controller operational in the lab with a dummy cavity. Debriefing of the MTCA.4 PoC.
- 2019: standard HW kit and timing kit available for selected users
- Beginning of 2021: new hardware in stock, platforms available for general use
Summary

- PoC developments well on track
- Challenges:
  - Tame the complexity
  - Provide easy-to-use environment for our clients
- Done from the beginning in collaboration with the users
- Go/No-Go decision at the end of this year
Thank you!
Questions?