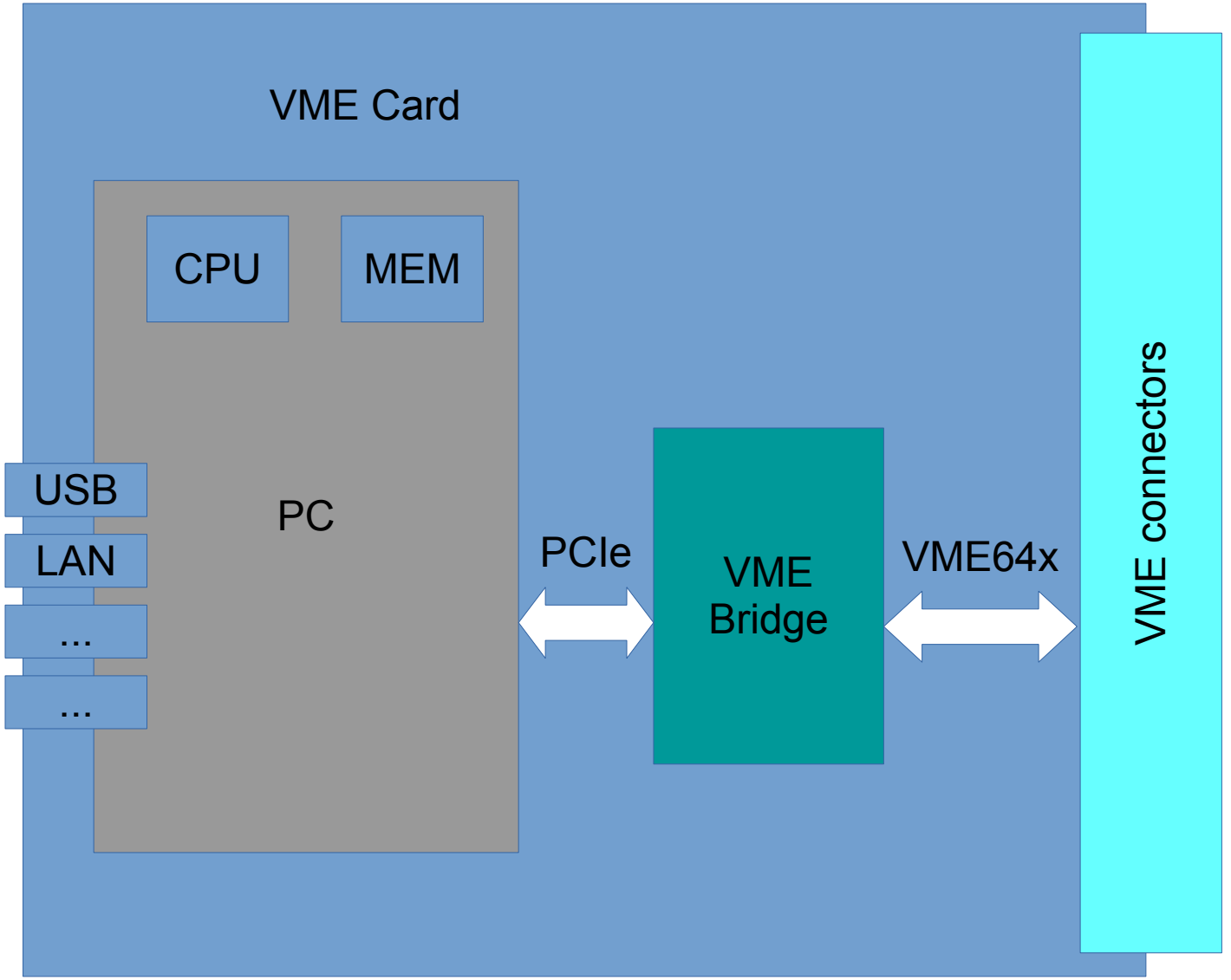
Status and plans for the MEN-A25 VME CPU

Adam Wujek on behalf of
D.Cobas, G. Daniluk, M. Suminski
BE-CO-HT

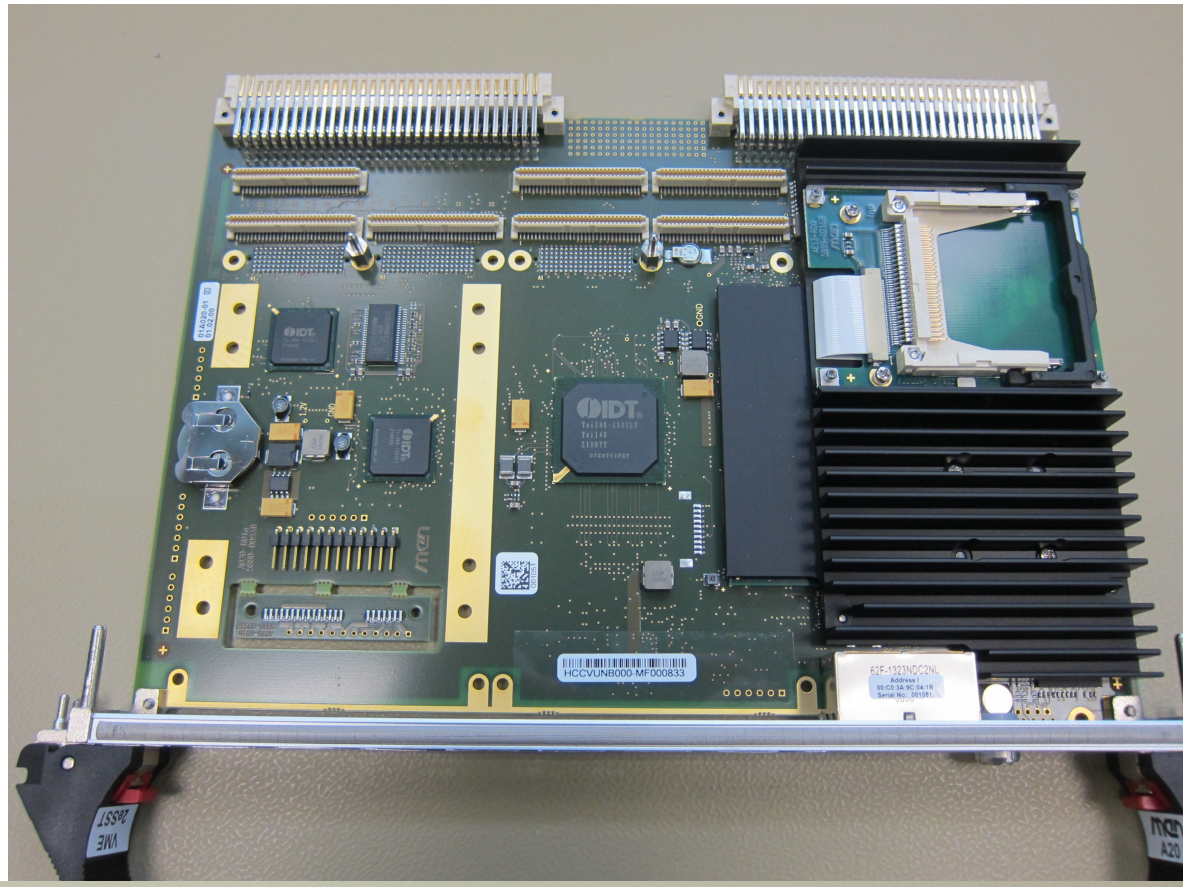
BI-TB, 14 September 2017

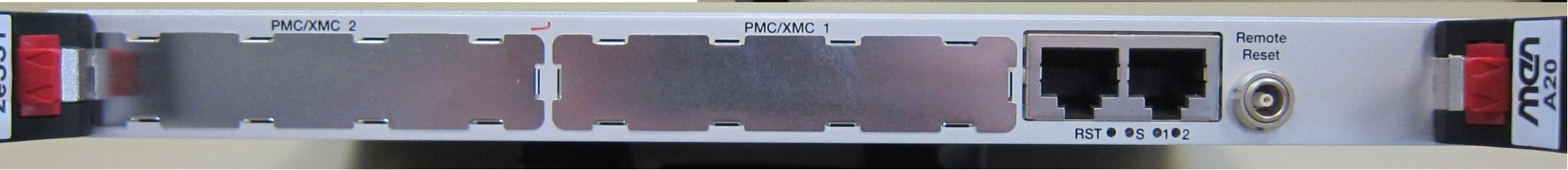
VME Single Board Computer Card



MEN A20 – the present

- Intel Core 2 Duo L7400 (1.5GHz)
- 1GB RAM
- Serial console
- 1GbE
- VME bridge based on TSI148 chip
- Running Linux
- 2x PMC/XMC slots





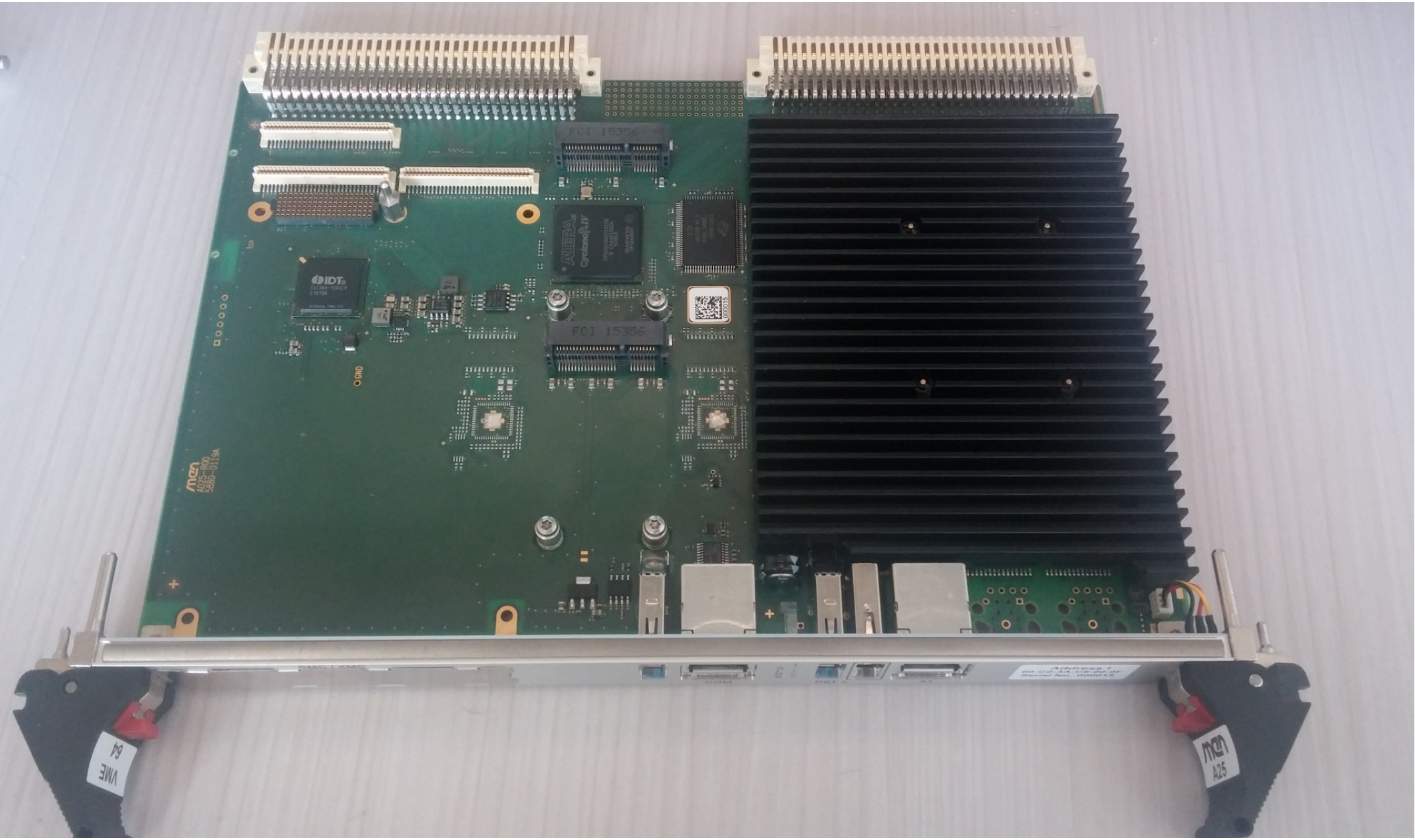
What's wrong with A20?

- Not possible to order more
- VME bridge TSI 148
  End of life mid-2015
- VME is far from dead
- Deployed more than 800 of A20's
- New requests for VME masters

Call for tender

- Replacement for MEN A20
- 3 options:
  - Buy enough TSI 148 chips
  - Use Tundra Universe II (predecessor of TSI 148)
  - Implement an open source bridge in FPGA
    - possible since predecessor of A20 had it, but closed source, lacking features
- No preferred solution!
- Option with an open source bridge in FPGA won (MEN)!
  It was the cheapest!

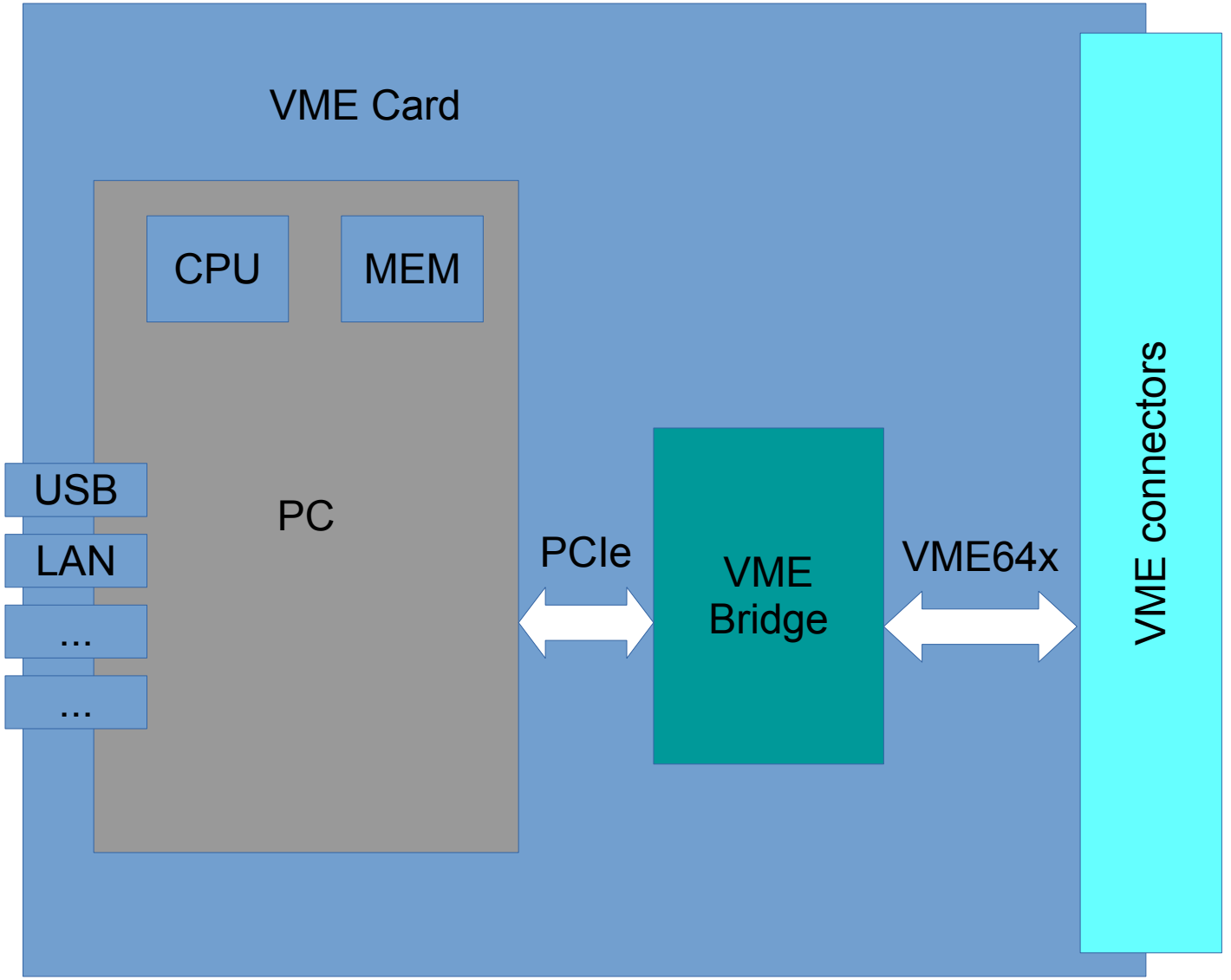
MEN A25 – the future



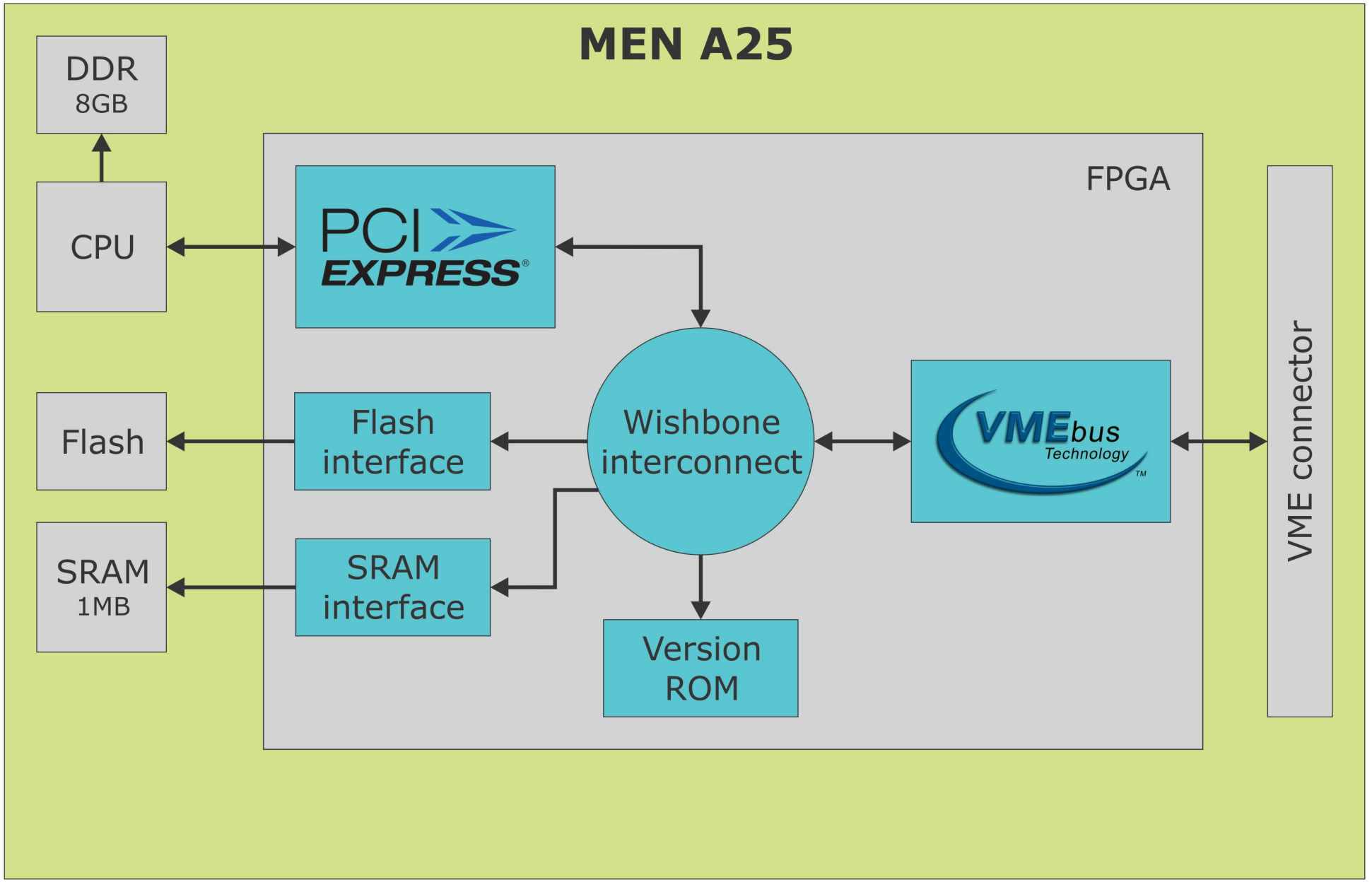
MEN A25 – the future

	MEN A20	MEN A25
CPU	Intel Core 2 Duo L7400 (1.5GHz)	Intel Pentium D1519 (1.50GHz, turbo 2.1GHz)
Cores/threads	2/2	4/8
Launch date	Q3'06	Q2'16
RAM	1GB	8GB
Storage	CF	mSATA, microSD
VME bridge	TSI148	Open source implementation in FPGA
PMC/XMC	2	1
Ethernet ports	1x1Gb	1x1Gb
Other		2x USB 3.0

PCIe to VME bridge



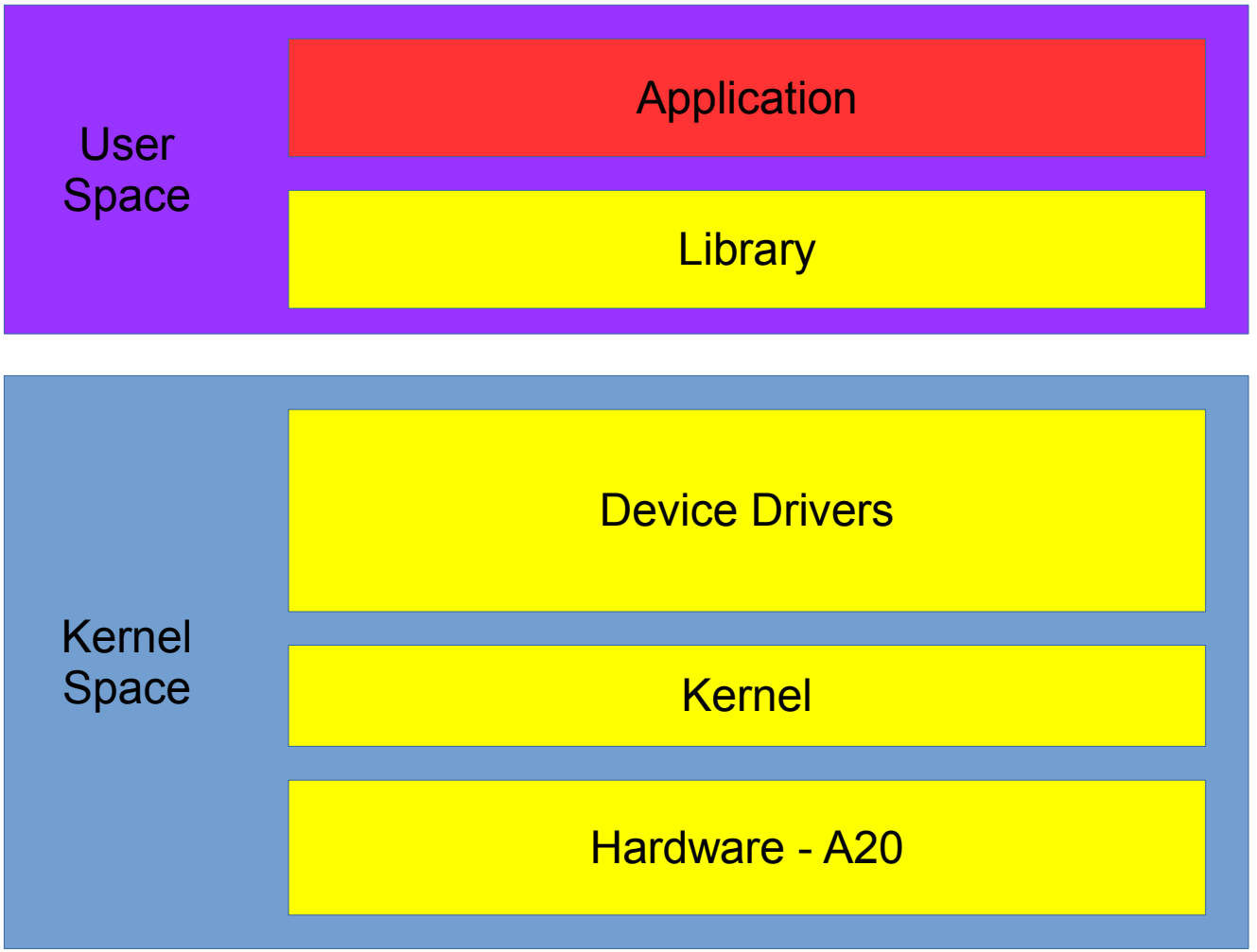
PCIe to VME bridge



PCIe to VME bridge

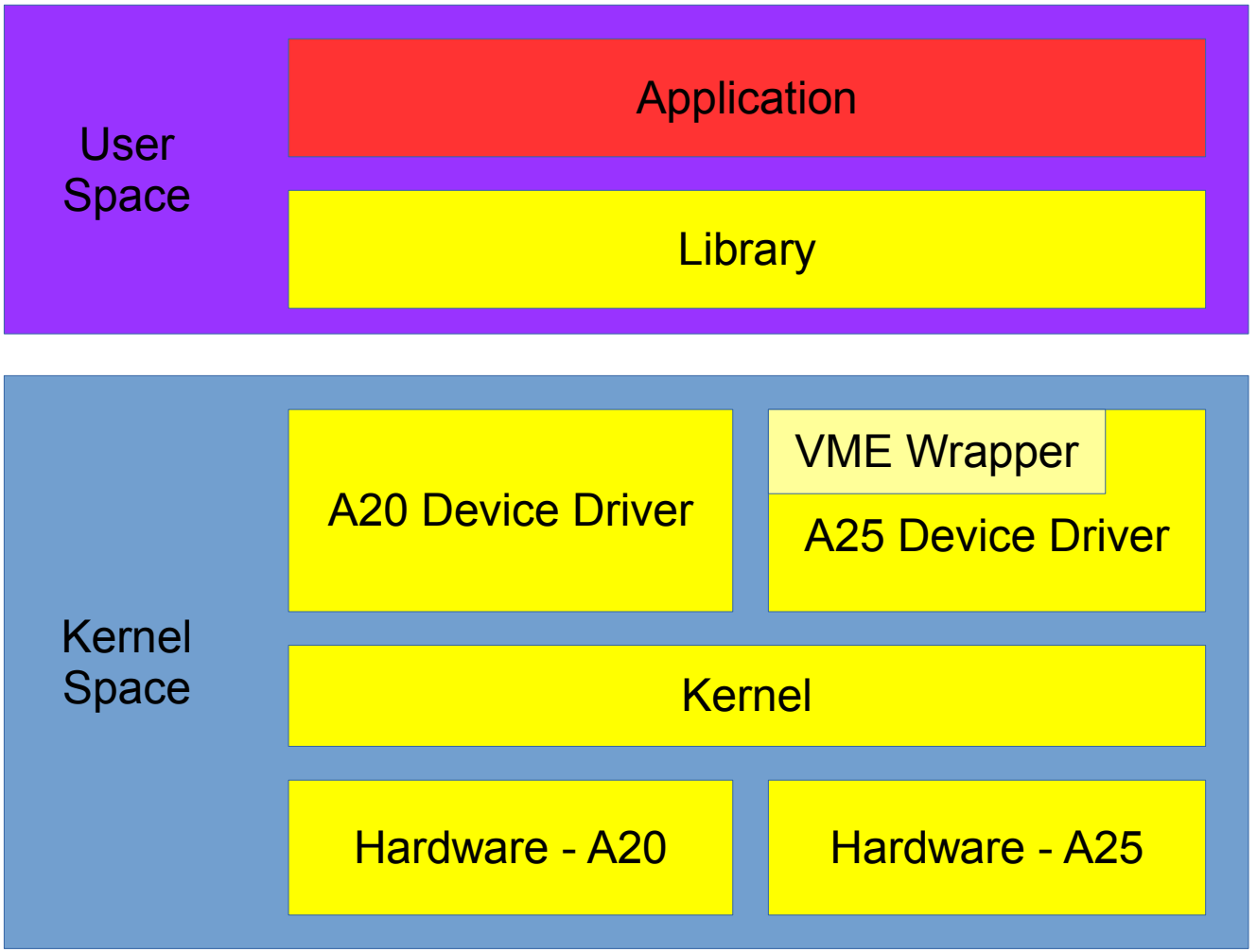
- Solves PCIe-to-VME bridging problem
  - … till the end of VME lifetime
  - … for us and all the other institutes
- Altera Cyclone IV and can be ported to any other FPGA
- Uses ~30% of FPGA logic elements
- More features can be added

Software replacement level



Yellow – provided by BE-CO; Red – provided by users

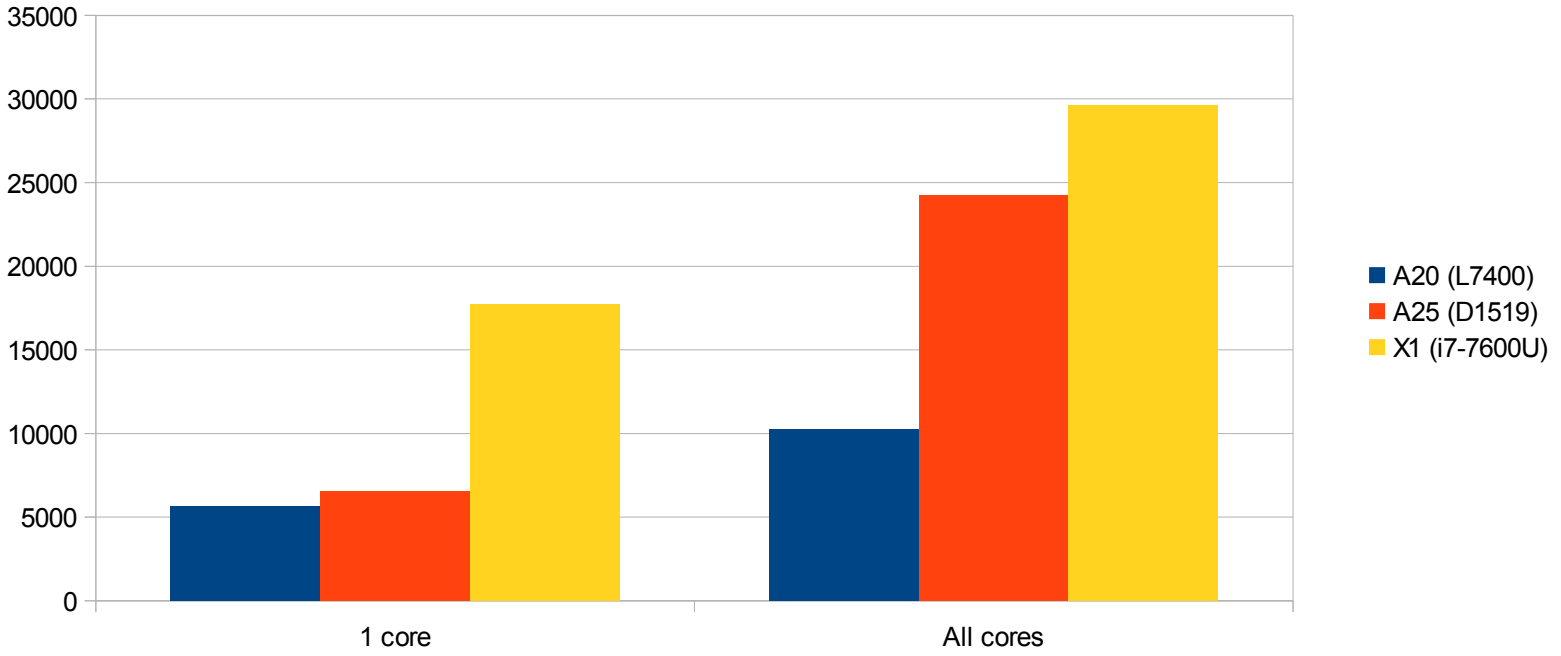
Software replacement level



Yellow – provided by BE-CO; Red – provided by users

CPU performance

	A20 Intel Core 2 Duo L7400 (1.5GHz)	A25 Intel Pentium D1519 (1.50GHz, turbo 2.1GHz)	X1 Intel i7-7600U (2.80GHz, turbo 3.90GHz)
1 core	5612	6515	17712
All cores	10228	24224	29614

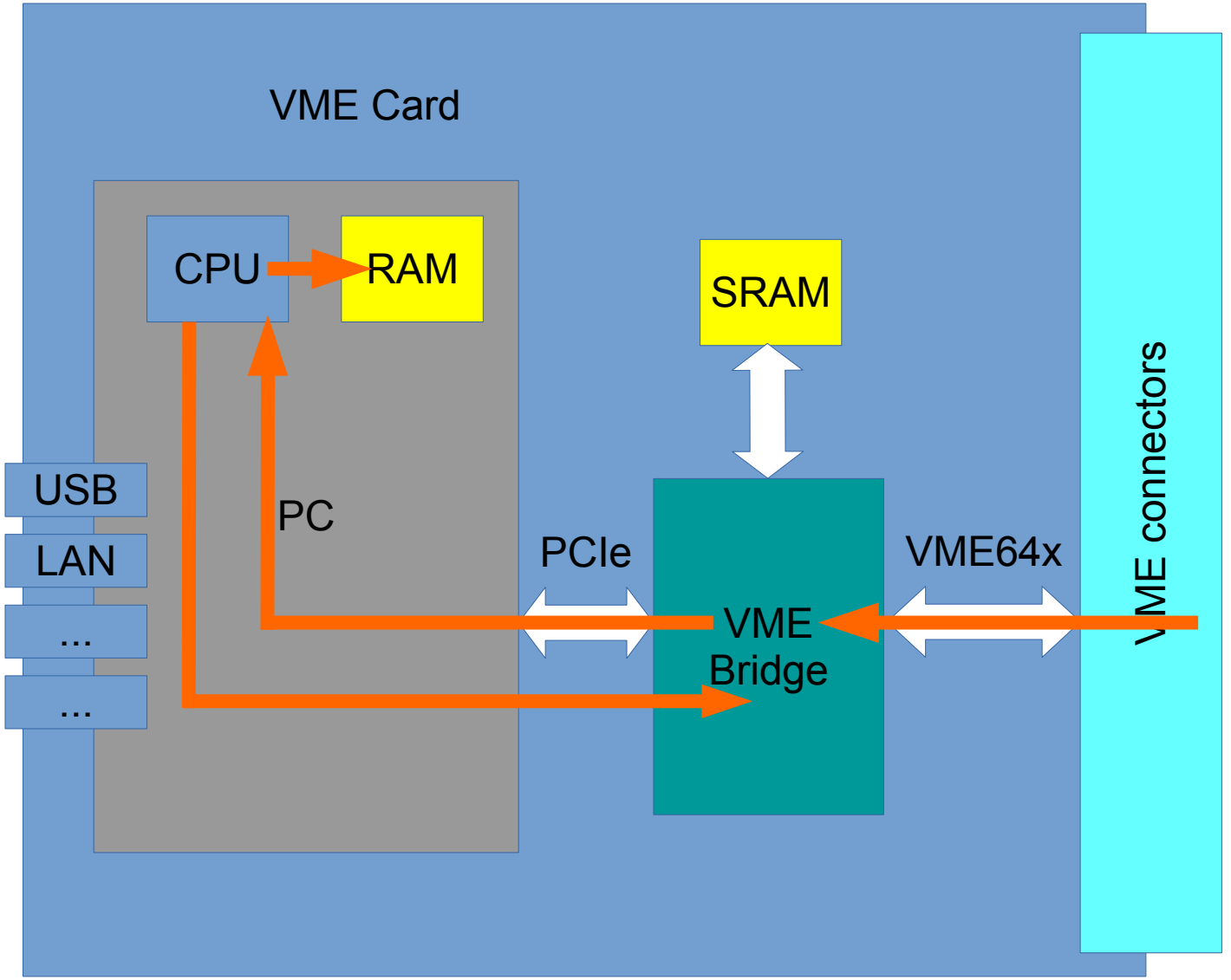


stress-ng --cpu <cpu_num> --cpu-method matrixprod --metrics-brief -t 60

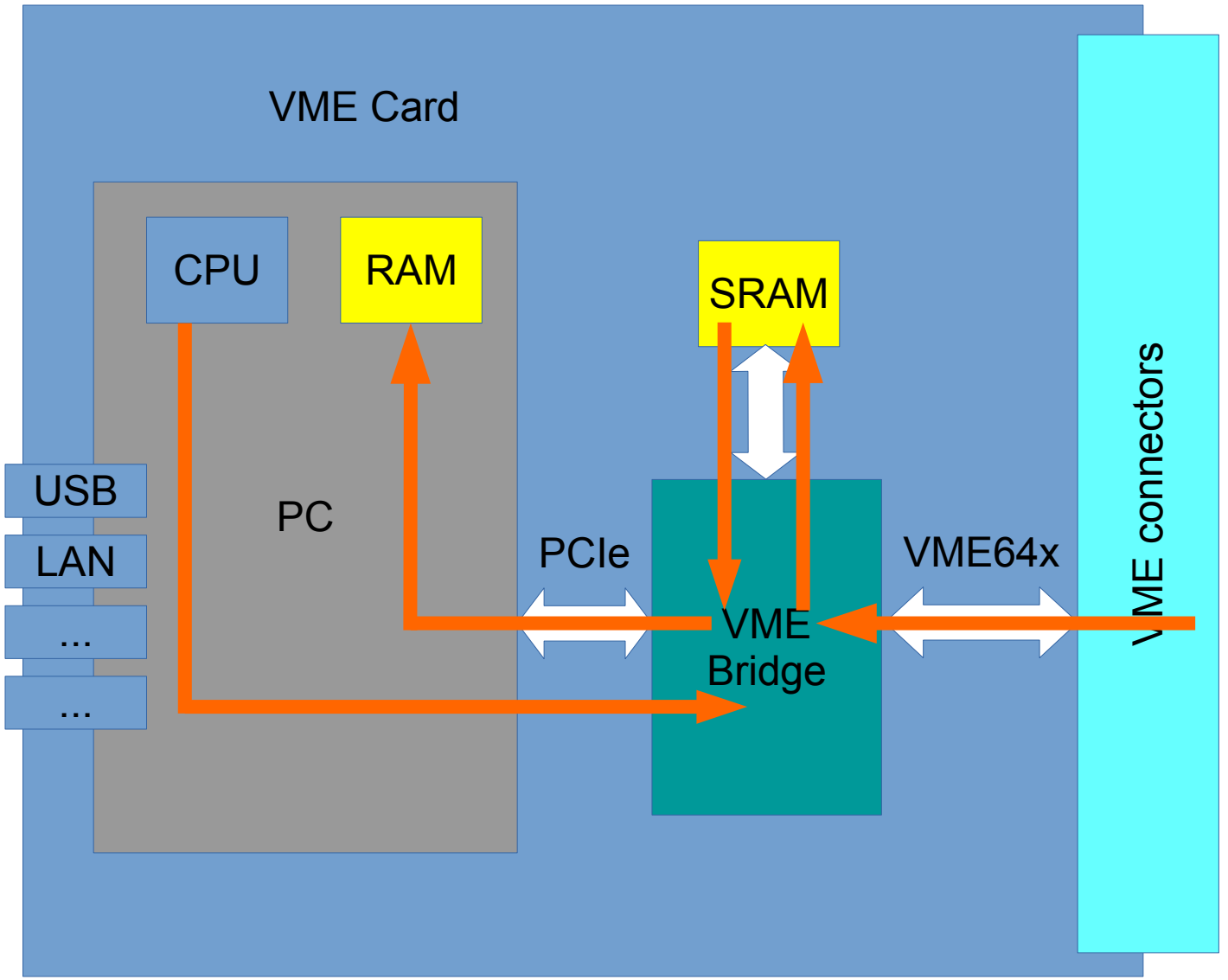
VME performance

- Type of transfers:
  - Memory mapped IO for single access mode
    - D8, D16, D32 bits
    - A16, A24, A32
  - DMA
    - Bounce-buffer (temporary solution)
    - Zero-copy (not working yet)

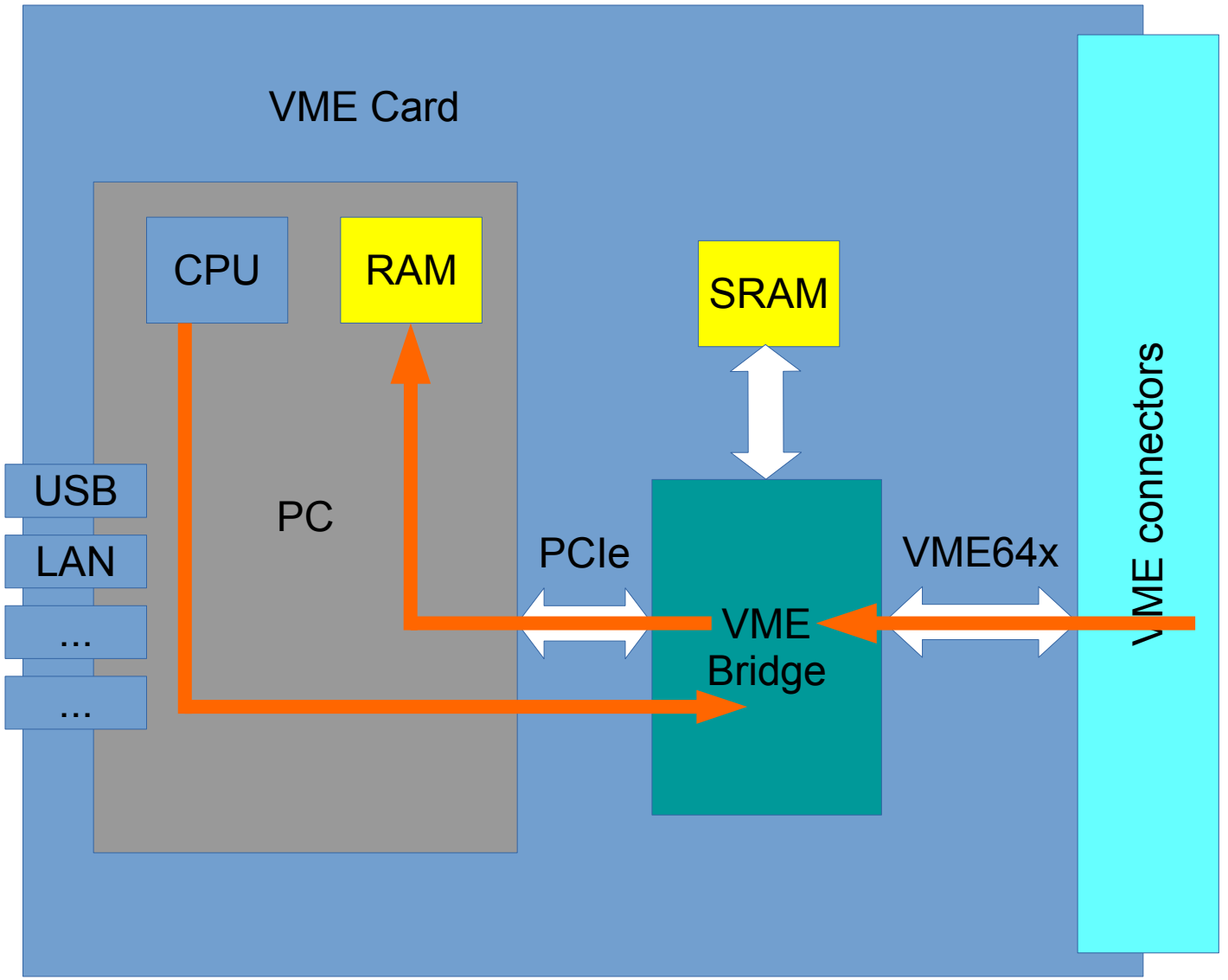
Memory mapped IO for single accesses



DMA Bounce Buffer



DMA Zero-copy

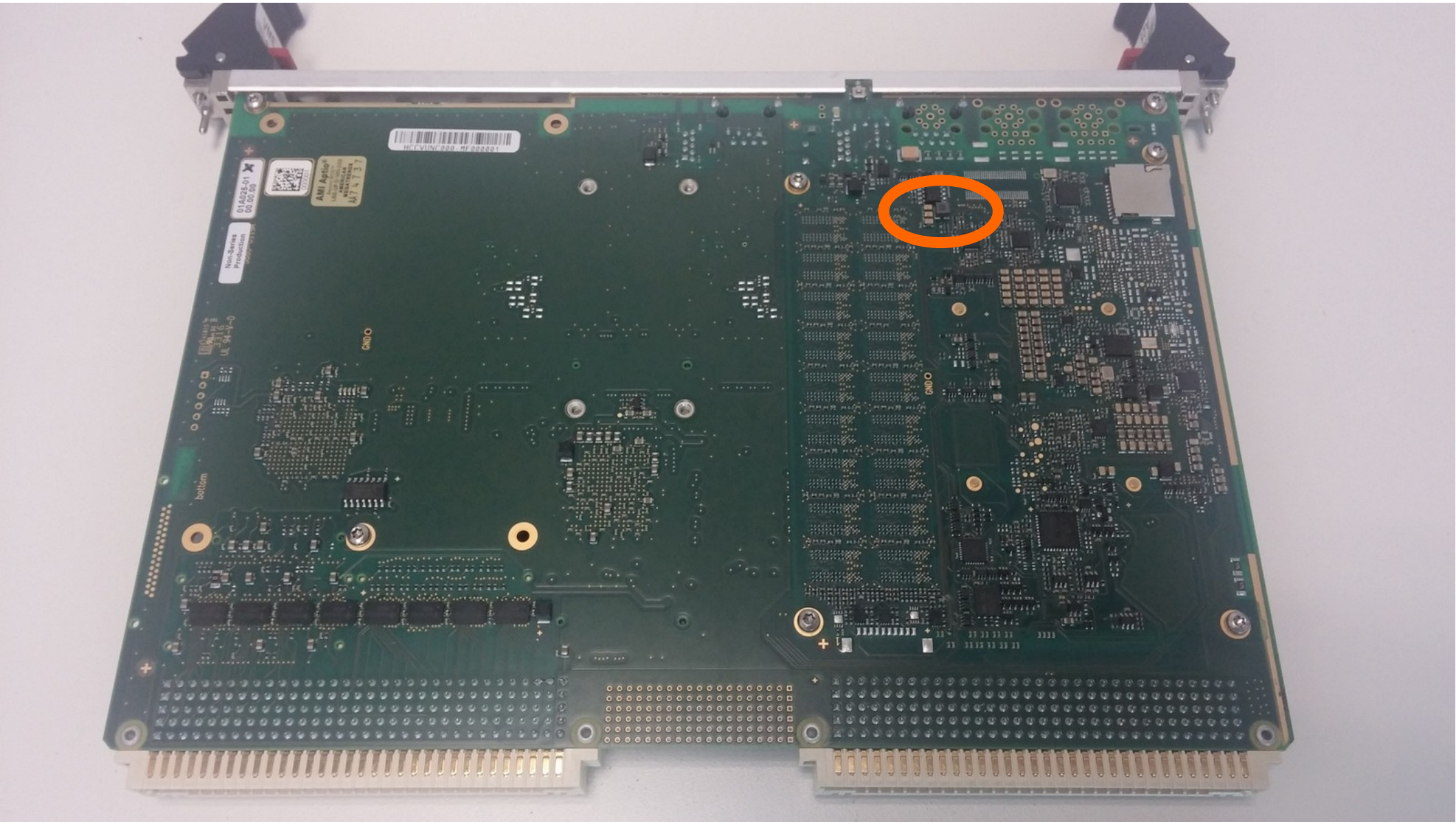


VME performance

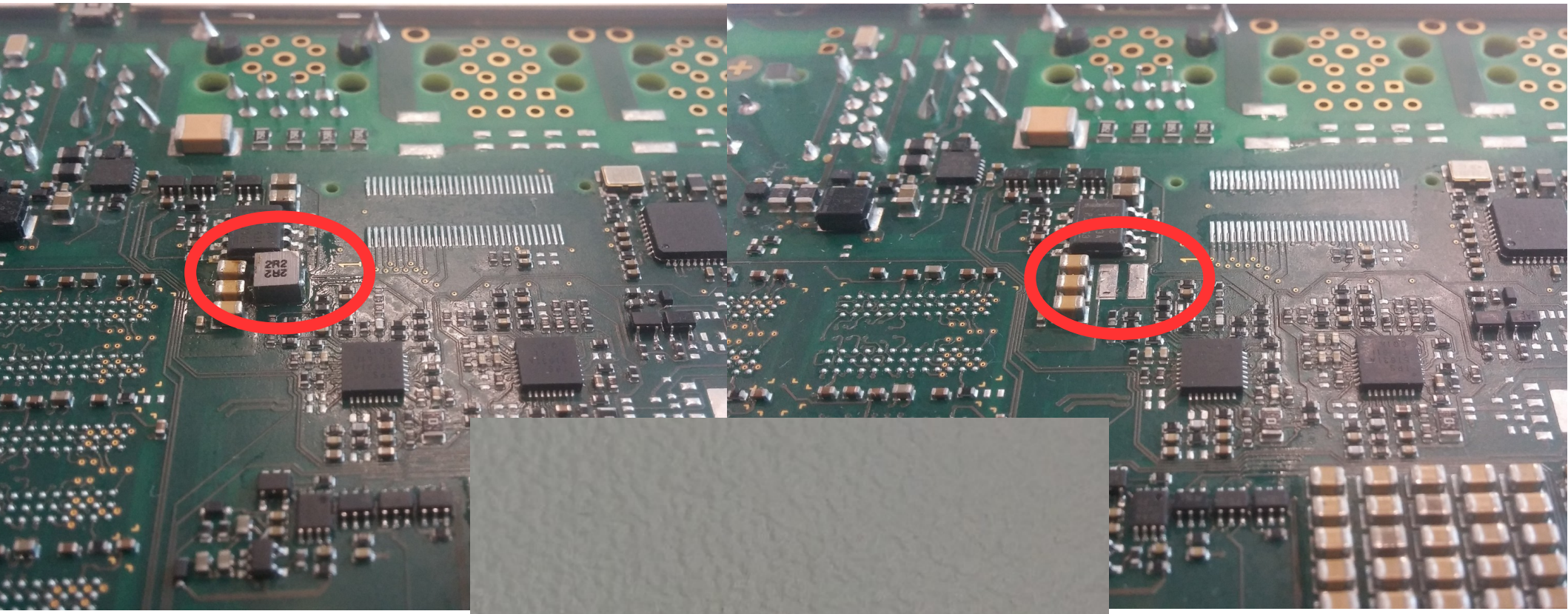
	A20	A25
Single accesses (32bit)	~1500 KB/s	~2300 KB/s
DMA Bounce-buffer *	-	~900 KB/s
DMA Zero-copy	~17 MB/s	In progress

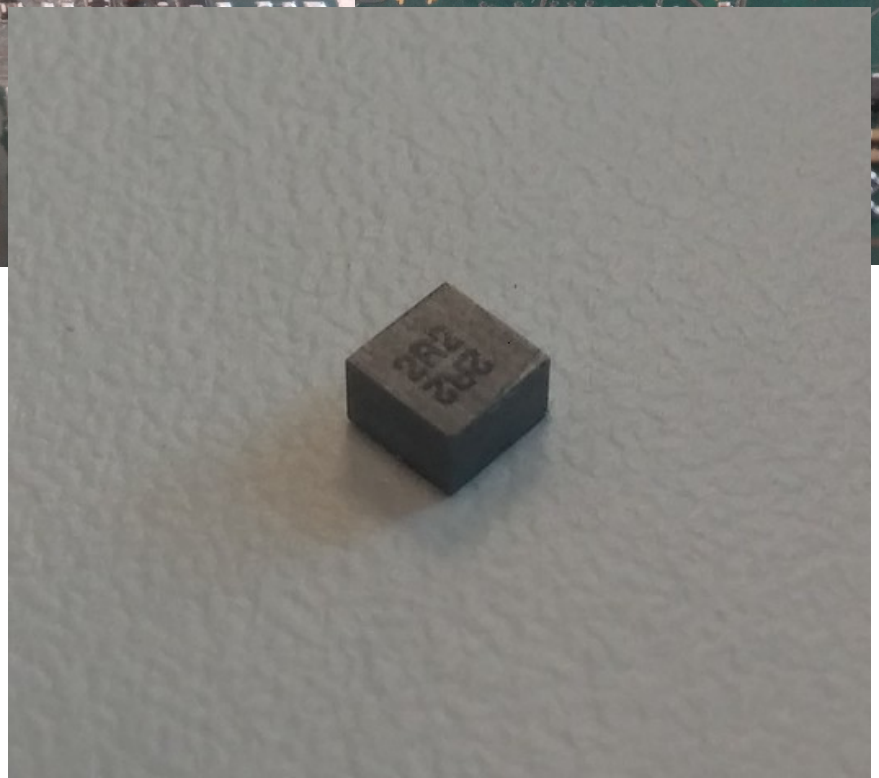
* - temporary solution

How to brake an A25?

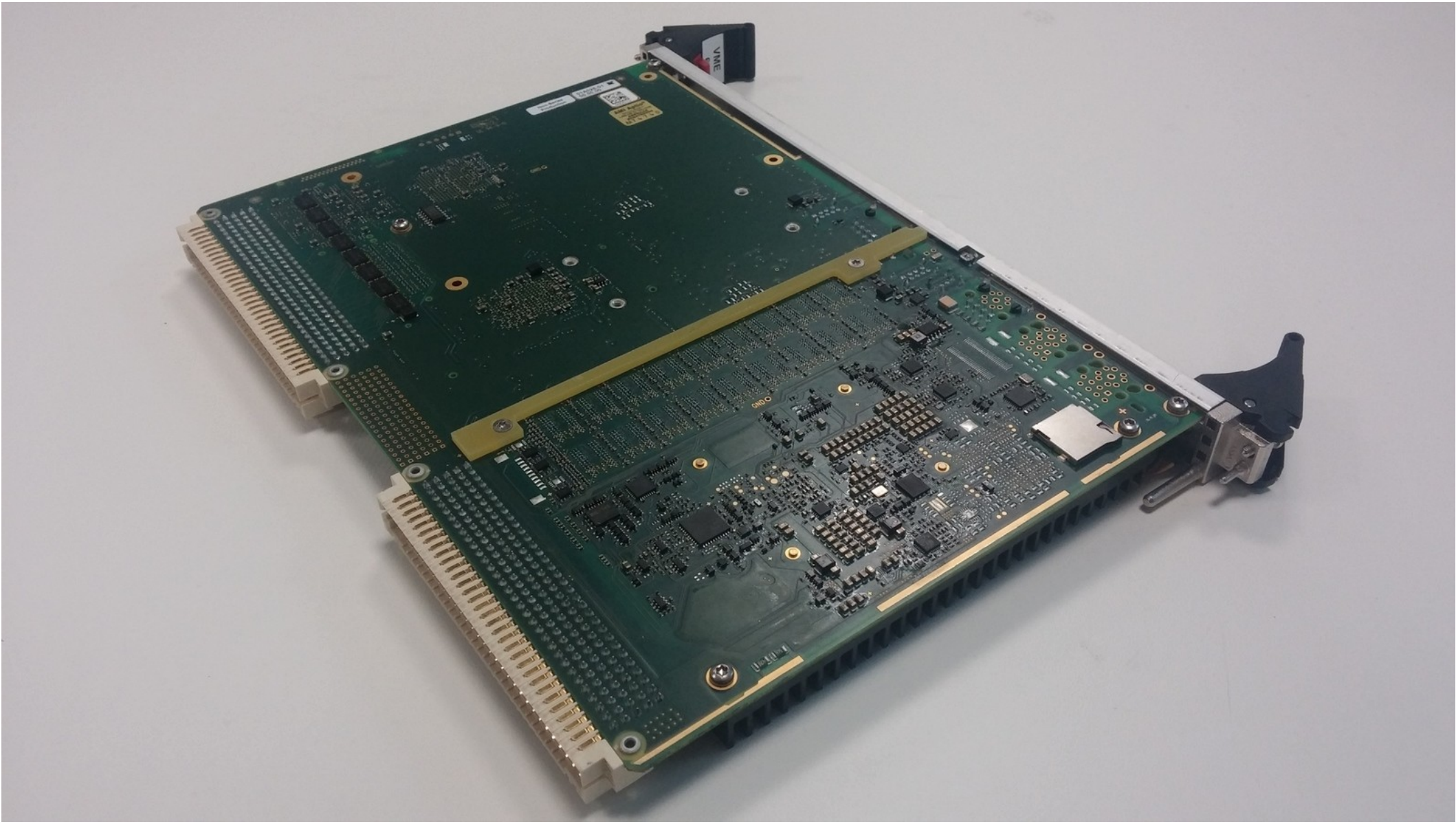


How to brake an A25?





How to protect an A25?



MEN A25
status and plans

Done:

- Single accesses in various modes
- CR/CSR
- Bus error status registers
- Support of SLC6/CentOS 7 (64bit support)
- Interrupts
- BIOS (also an update)
- Reproducibility of a FPGA bitstream
- Field programmable FPGA firmware
- Physical protection of a bottom side of a board
- API wrapper for VME bridge's driver

MEN A25
status and plans

To do:

- Performance tests (ongoing)
- Stability tests (partly done, successful read of 515GB over (long) weekend)
- Improve DMA performance (ongoing)
- Finish an API wrapper for VME bridge's driver (ongoing)

Timeline

- August: Last batch of 40 MEN A20
- October/November: Batch of 10-20 MEN A25
- End of November: Invite early access users for testing
- End of 2017: Batch of 80-90 MEN A25
- Beginning of Q1 2018: Invite interested users to collaborate in the validation
- MEN A25 expected to be ready in March 2018

Summary

- TSI148/A20 End of life motivates a search of a new VME bridge
- A25 – new board to replace A20
- Open implementation of a VME bridge will reduce the risk of using VME in the future
- Validation process is ongoing
- MEN A25 for operational deployment expected to be ready at the end of Q1 2018