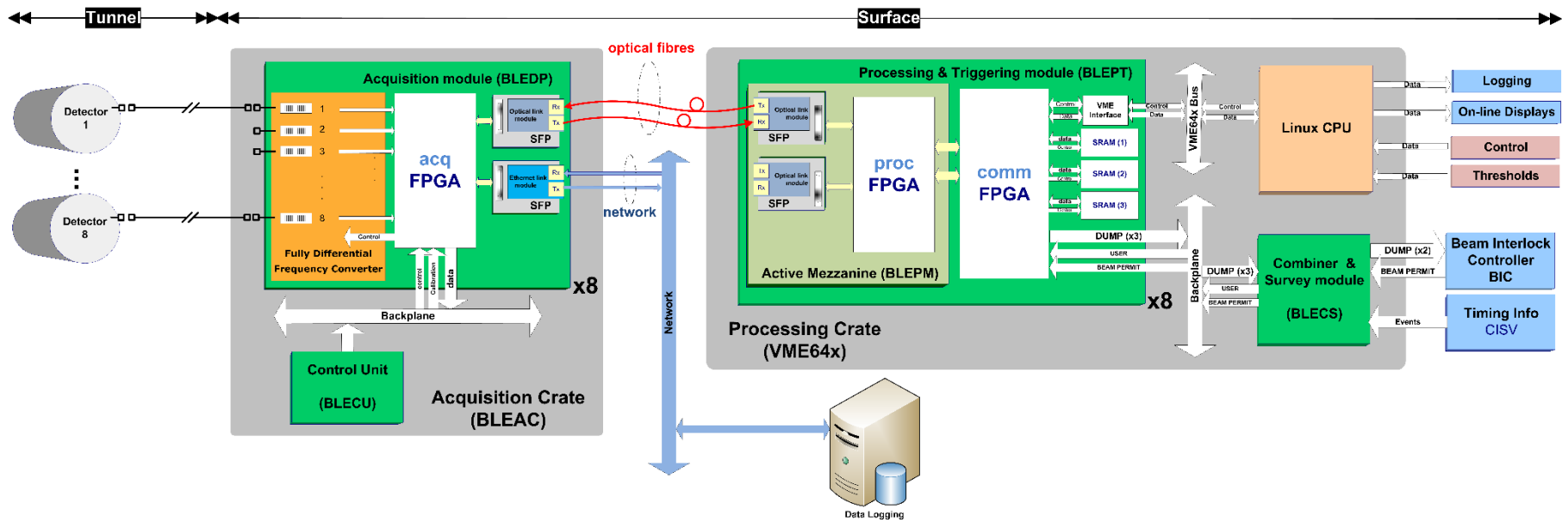# INJECTORS BLM SYSTEM:
PS AND PSB RING INSTALLATIONS AT EYETS

BI-TB 28/09/2017

Christos Zamantzas on behalf of the BLM team.

BLMINJ System Overview

BLMINJ Integration Periods

Continuously the processing electronics will calculate 4 **integration period values** for each channel:

- **2 μs**, **400 μs, 1 ms** and **1.2 s** (full period)
  - implemented as moving sum windows in the hardware
  - calculation refreshed at acquisition frequency

- Compare with predefined thresholds
  - **Machine protection** with hardware implementation comparisons on each refresh
  - **Limit radiation levels** with software implementation comparisons at end of cycle/period
  - See also next slide.

- Calculate for each channel the maximum values recorded on each integration period during the cycle
  - Publish them for the online displays and
 - the long-term logging

BLMINJ Threshold Comparisons

Hardware implementation part:

■ All calculated **integration period values**, i.e from **2 µs** to **1.2 s**, will be constantly checked against their threshold values:
  ▪ 4 threshold values, one for each of the integration periods.
  ▪ Comparisons happen at the refresh period – that is, every 2 µs
  ▪ In the case the measured values exceed those the beam permit signal will be removed for **all users**
  ▪ The **blocked** beam permit signal will be **latched** until an operator acknowledges.

■ The **threshold values** will be need to be set **unique per channel:**
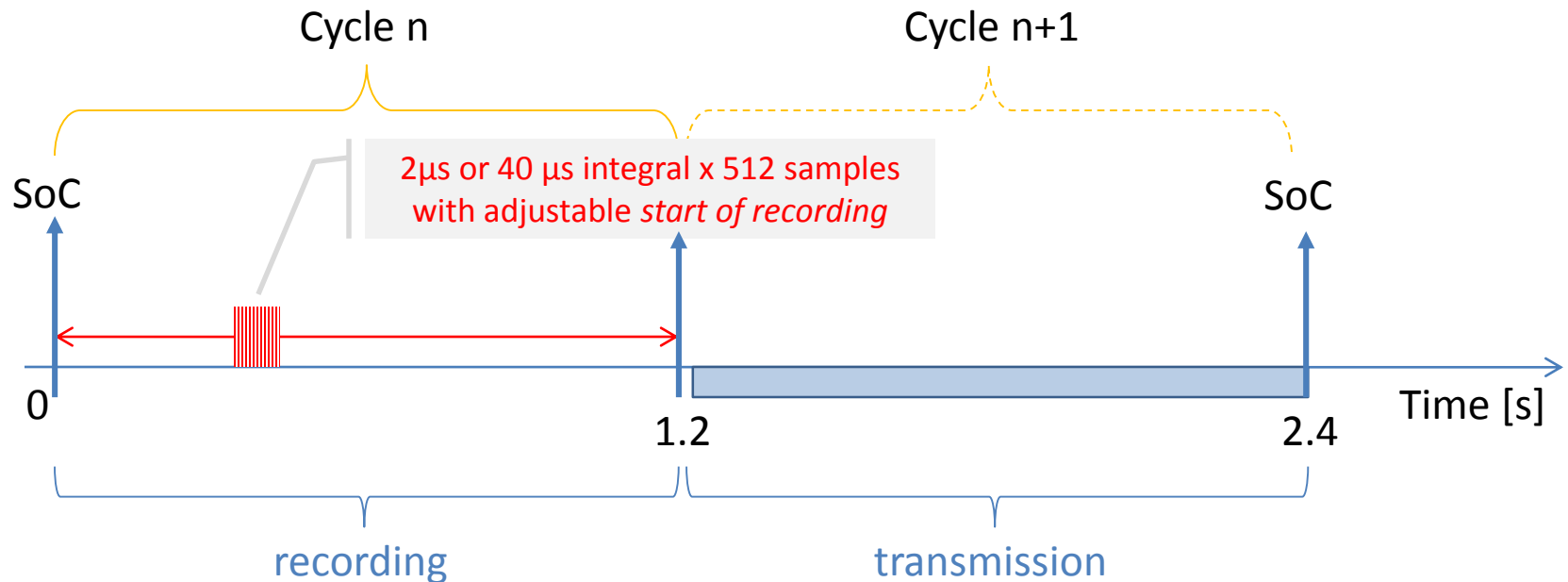 ▪ Each card will process 8 channels

Software implementation part:

■ All maximum **integration period values** recorded on the cycle will be checked against a second set of threshold values. The outputs will be used for **repeated over threshold function**
  ▪ Additional threshold values for the same integration periods will also be required.
  ▪ In the case found to be over threshold repeatedly n times it will be required to block **that user's injections**.
  ▪ The **blocked** beam permit signal will be **latched** until an operator acknowledges.
  ▪ The repeat value n will be settable per monitor in the range of 1 to 16.

■ The **threshold values** will need to be **unique per user and per channel:**
  ▪ Each CPU will process 8 cards x 8 channels
  ▪ The information of the current user has to be obtained from the telegram per cycle -> dedicated **timing card**
  ▪ Memory for 32 users will be reserved.

BLMINJ Loss Evolution Buffer
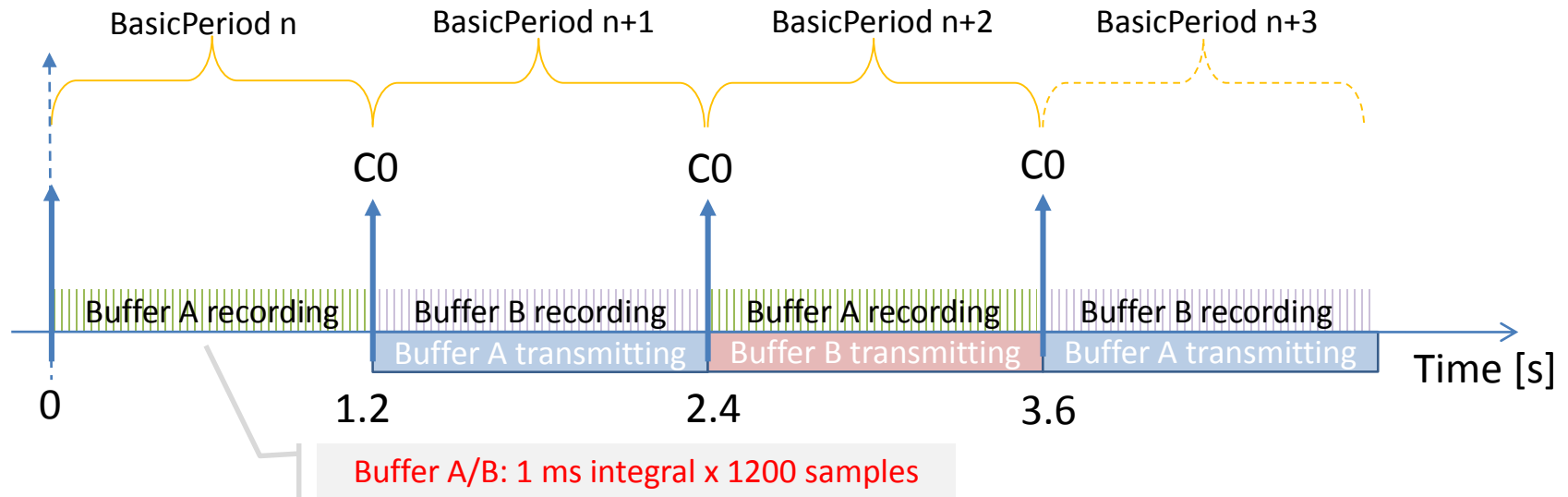
- Record 1ms integrals for the complete period
- Published in the on-line displays already on the next period
- Will be logged in the DB on-demand

BLMINJ Capture Buffer

Cycle n   Cycle n+1

2μs or 40 μs integral x 512 samples
with adjustable *start of recording*

SoC   SoC

0   1.2   2.4   Time [s]

recording   transmission

- Pre-selection of 2 or 40 μs integrals and the start time
- Recording of 512 samples

PSB Expert Name Convention

Vertical Position:
(0 to 2 letters; only for BR, BI, BT)
1,2,3 or 4 – ring separation
12 or 34 – across rings
None – all rings

Detector type:
I – IC
S – SEM
L – LIC
F – FIC
D – Diamond
A – ACEM

Radial Position:
E – external
I – internal
T – top
B – bottom
L – left to beam direction
R – right to beam direction
X – between beam pipes

BR12.BLMID.04L2.E_BSW1

Accelerator (2 or 3 letters):

LT – LINAC Transfer
LTB – LINAC Transfer to Booster
LBE – LINAC to Booster Emittance
LBS – LINAC to Booster Spectrometer
BR – Booster Ring
BI – Booster Injection
BE – Booster Extraction
BT – Booster Transfer
BTP – Booster Transfer to PS
BTM – Booster Transfer to Measurement
BTY – Booster Transfer to Isolde

System type:
B – BLEDP
O – OASIS
V – VFC/ADC

Period/Section (2 to 4 letters):

for the ring:
01-16 – period & L1-L5 – fixed
or for the transfer lines:
xxx – distance [m] (BTY line)
xx – 10, 20 for first, second etc. (for all other lines)

PS Expert Name Convention

Detector type:
- I – IC
- S – SEM
- L – LIC
- F – FIC
- D – Diamond
- A – ACEM

Magnet (2 letters):

for the ring:
00-99 – magnet
…

PR.BLMIB04

Accelerator (2 or 3 letters):

- PR – PS Ring
- F16 – F16 (TT2) line
- FTA – FTN line
- …

System type:
- B – BLEDP
- O – OASIS
- V – VFC/ADC
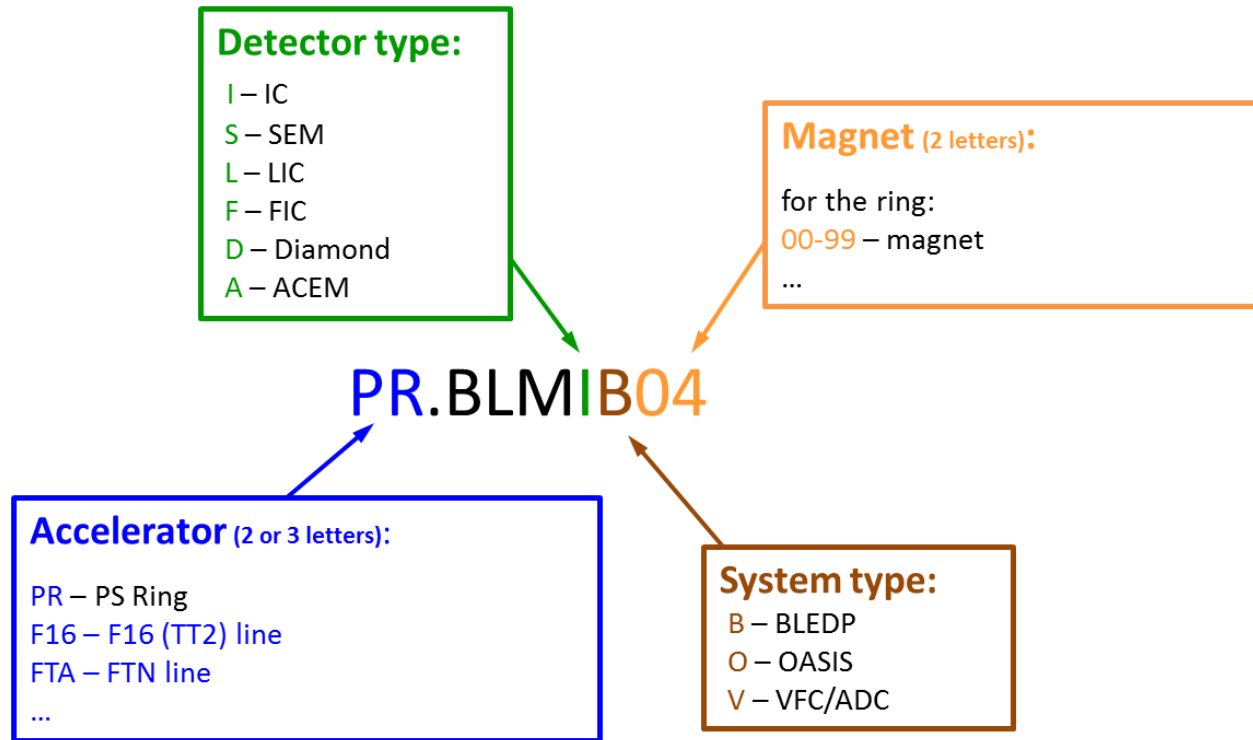
Not final; need to clarify transfer lines

INSTALLATIONS DURING EYETS

28/09/2017

PSB New Rack at BAT41E

- **Complete new rack installed**
  - Acquisition crate
  - Processing crate
  - HV crate
  - HV distribution

- **4 module pairs**
  - acquisition and processing cards

- **32 Channels connected**
  - FIC detectors

- **8 channels spare**

- **Two HV power supplies**
  - Second PSU is for redundancy

PS New Racks at B359

- **Complete new set of four racks installed.**

- **Two racks for BLMINJ, with each hosting:**
  - Acquisition crate
  - Processing crate
  - HV crate
  - HV distribution
  - Cable management

- **14 module pairs**
  - acquisition and processing cards

- **100 Channels connected**
  - Ionisation Chamber detectors

- **28 channels spare in total**

- **Two HV power supplies on each rack**
  - Second PSU is for redundancy
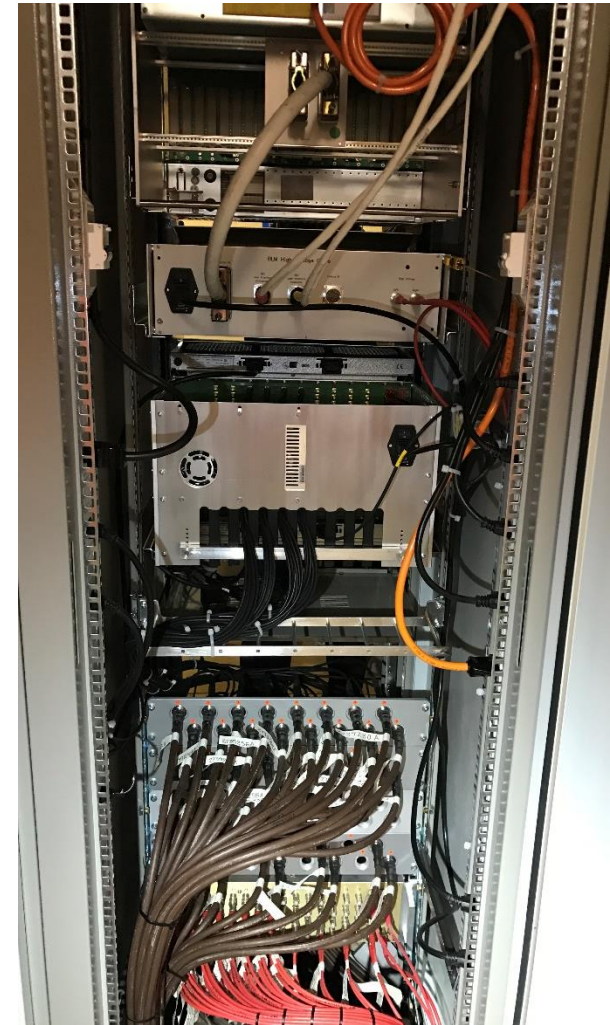
PSB Supports
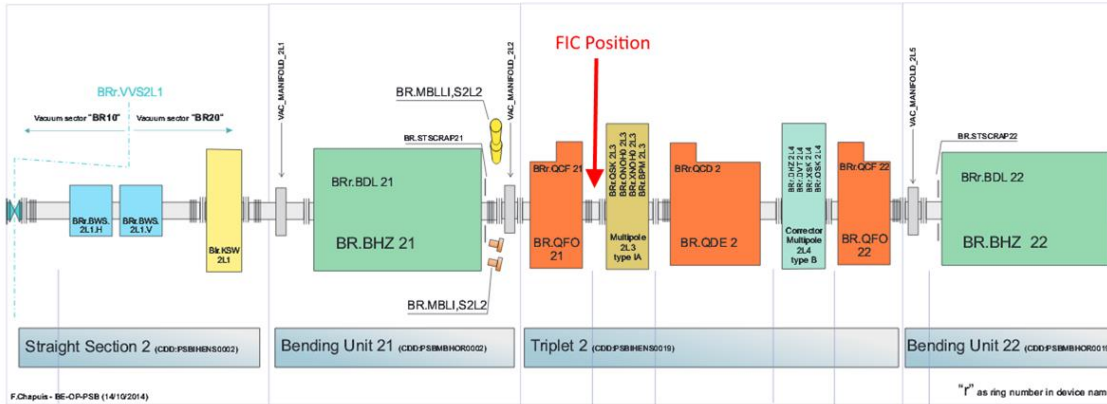
- **Detector and cables are attached on the magnet nuts**
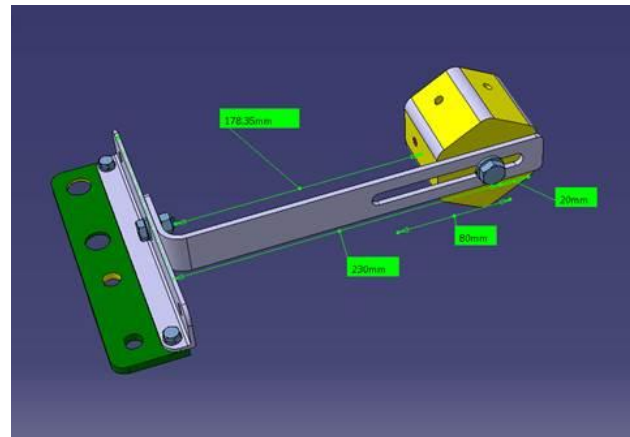
PSB Custom Supports

- Special supports for:
  - BR12.BLMFB.3L3.E
  - BR12.BLMFB.10L3.E

- Non standard installation of the vacuum clamps
  - Not enough space to fit detector

- Need to verify the signal difference
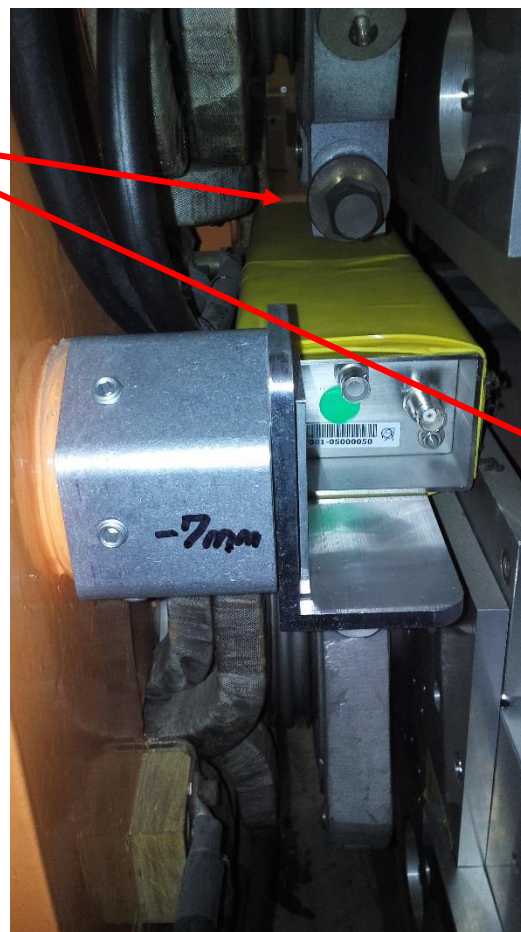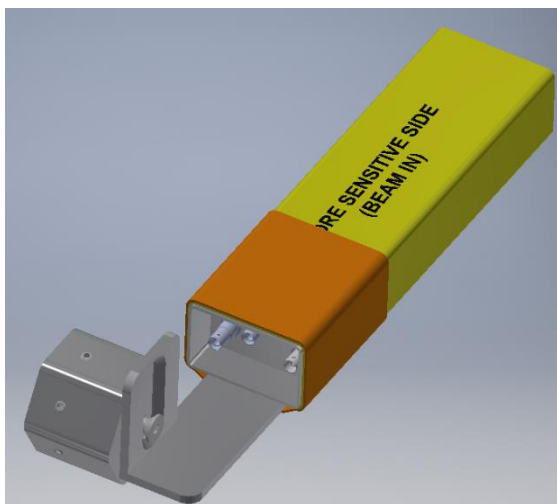
PS Tunnel Installation

■ Installation was modified several times to fit and satisfy all requests

    ■ Mostly issues with cabling and patchcords
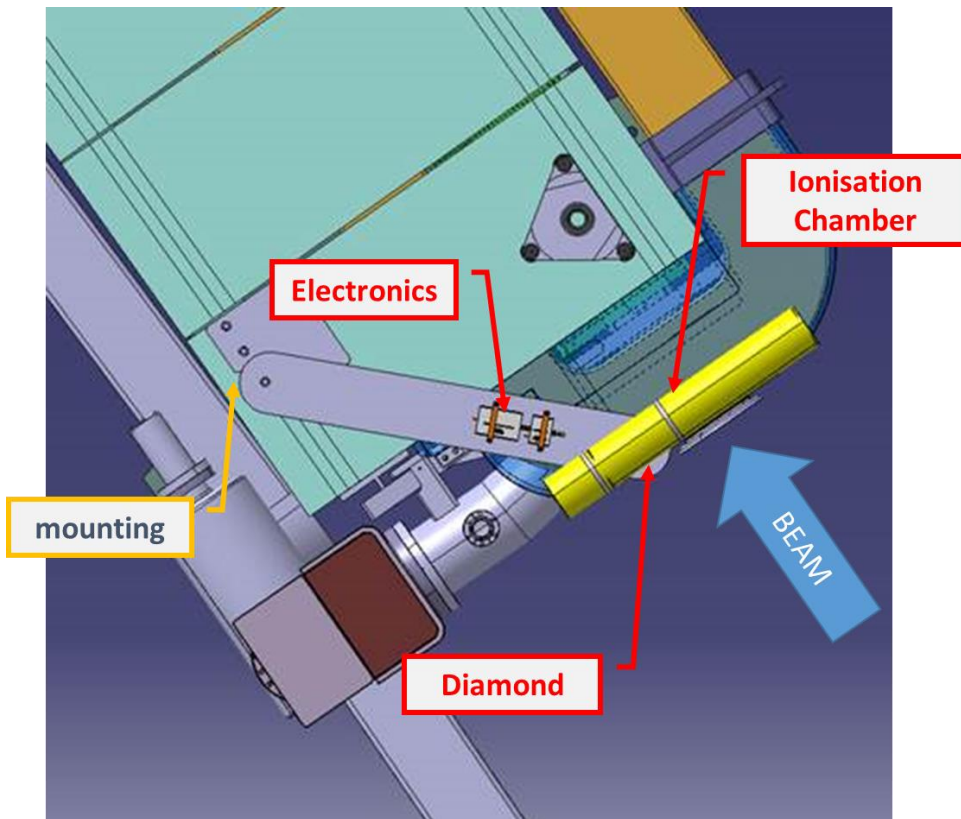
Top view

- **Preparation of the installation**
  - All dBLMs have been equipped with splitters and amplifiers
  - Connections done and tested in the lab before deployment

PS Diamond Installation

- **HV and LV Power supply unit** for the Diamond bias and the amplifier
  - **Ethernet connection** for control
  - **FESA class** to control and log values is under development
  - OP will have the ability to switch off/on (seems not necessary with the latest info; matrix will terminate input when a channel is not used/digitised)
  - Only Experts will have the ability to set/modify the voltage values

PS Diamond Installation

- Signal cables arrive at the OASIS rack

- With adapters and patchcords are connected to the OASIS Matrix

- With another set of patchcords signals arrive to the 4 OASIS Digitisers

- Aim is to intercept the signals before the matrix and add a protection circuit.
  - This will also reduce the adaptors and patchcords used

- Circuit is ready and tested in the lab.
  - A PCB has been designed to fit in a small box and is under production
  - Will have the ability to add attenuation if needed in the future

BNC MALE - BNC FEMELLE   N MALE - N FEMELLE
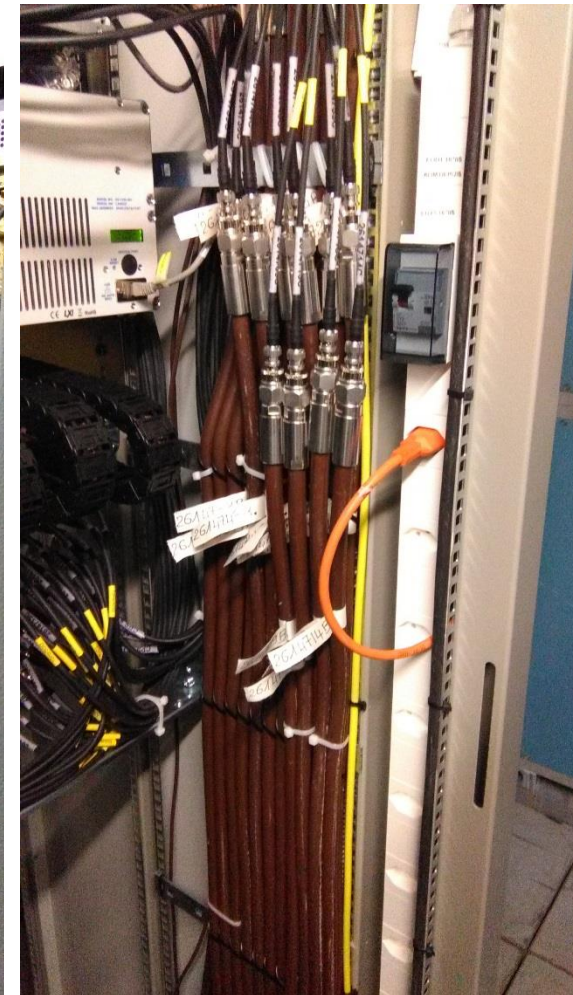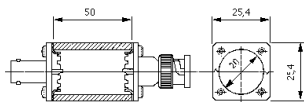
DEVELOPMENT

System Development

- **Firmware and Software available to stable versions with all major features available.**

- **Direct Ethernet connection to each acquisition module available for detailed analysis and debugging.**
  - 2 µs samples continuously

- **Through FESA class, system provides synchronised with the basic period**
  - Several integrals (2 µs – 1.2 s, BeamPresence and Ambience)
  - 'Evolution' data for the complete cycle.
  - Data are 'tagged' with the USER

- **Functionalities under verification:**
  - loading of settings/thresholds,
  - system status information

- **Functionalities to be developed:**
  - On-demand Capture buffer with 2 µs samples
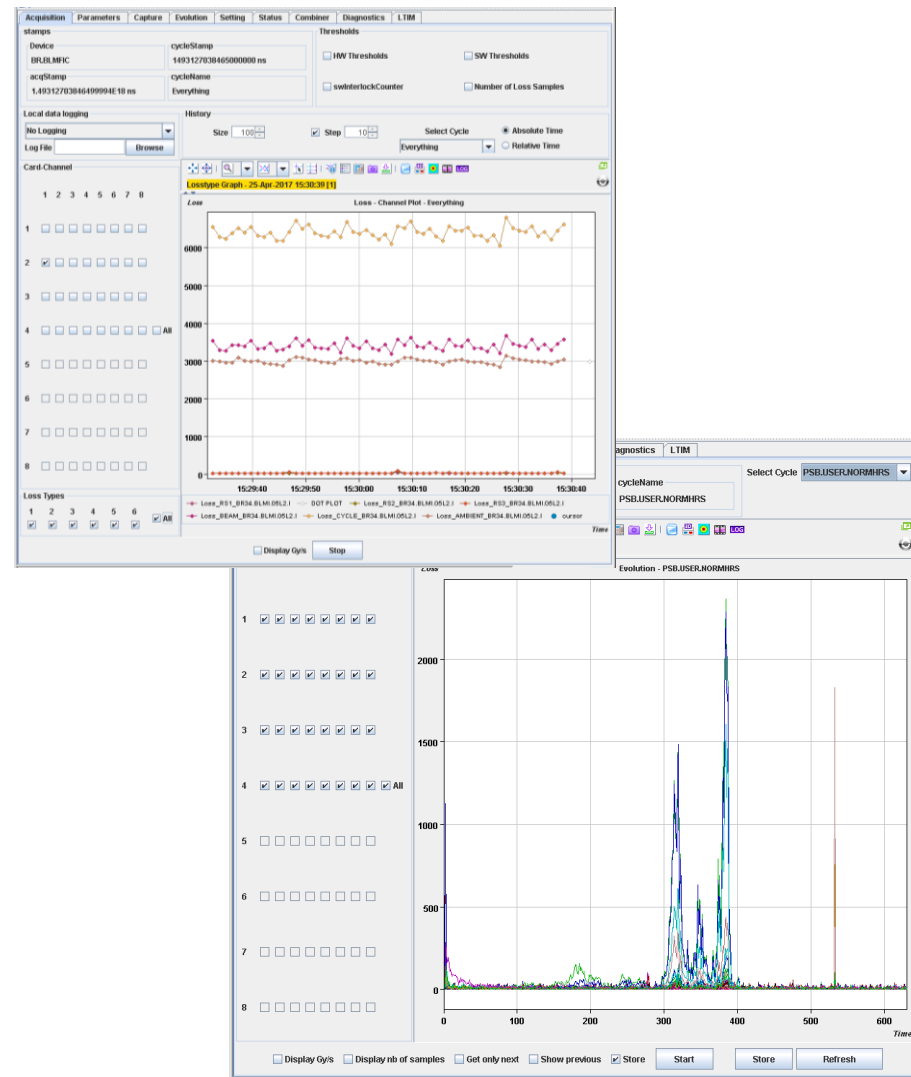
PS Evolution Buffer

- Firmware: double buffer at the FPGA
  - One records when the other transmits
  - Toggle operation with basic period
  - No blind time

- Software: two properties from FESA
  - Data per basic period
  - Data per cycle
  - Units: Gy/s or bits
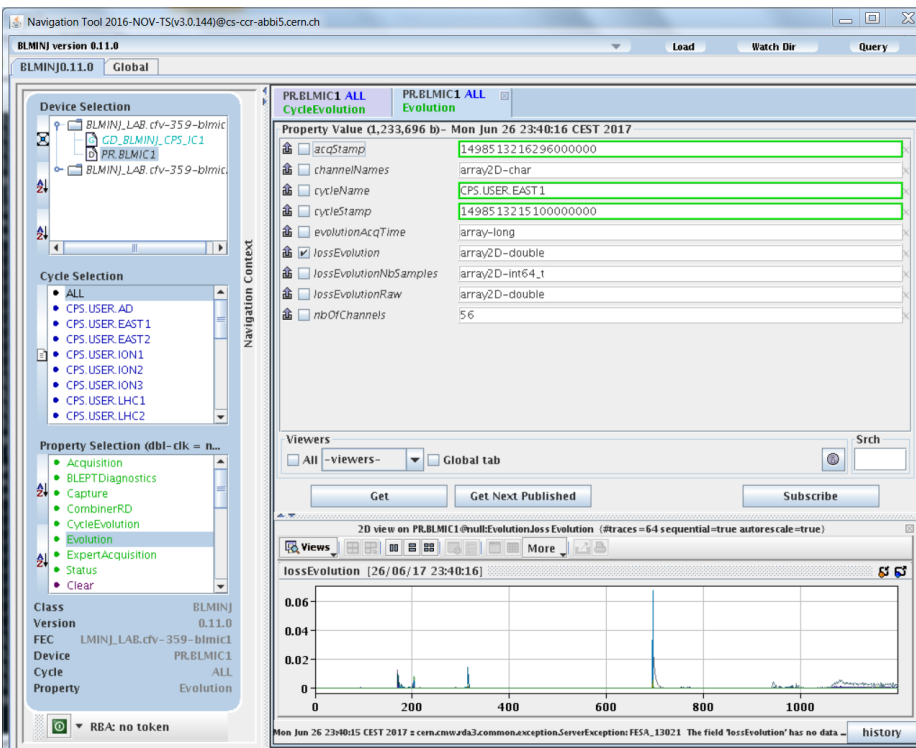
per Basic Period

per Cycle

■ System information: firmware version, card serials, temperature and humidity

■ System information: Optical links performance
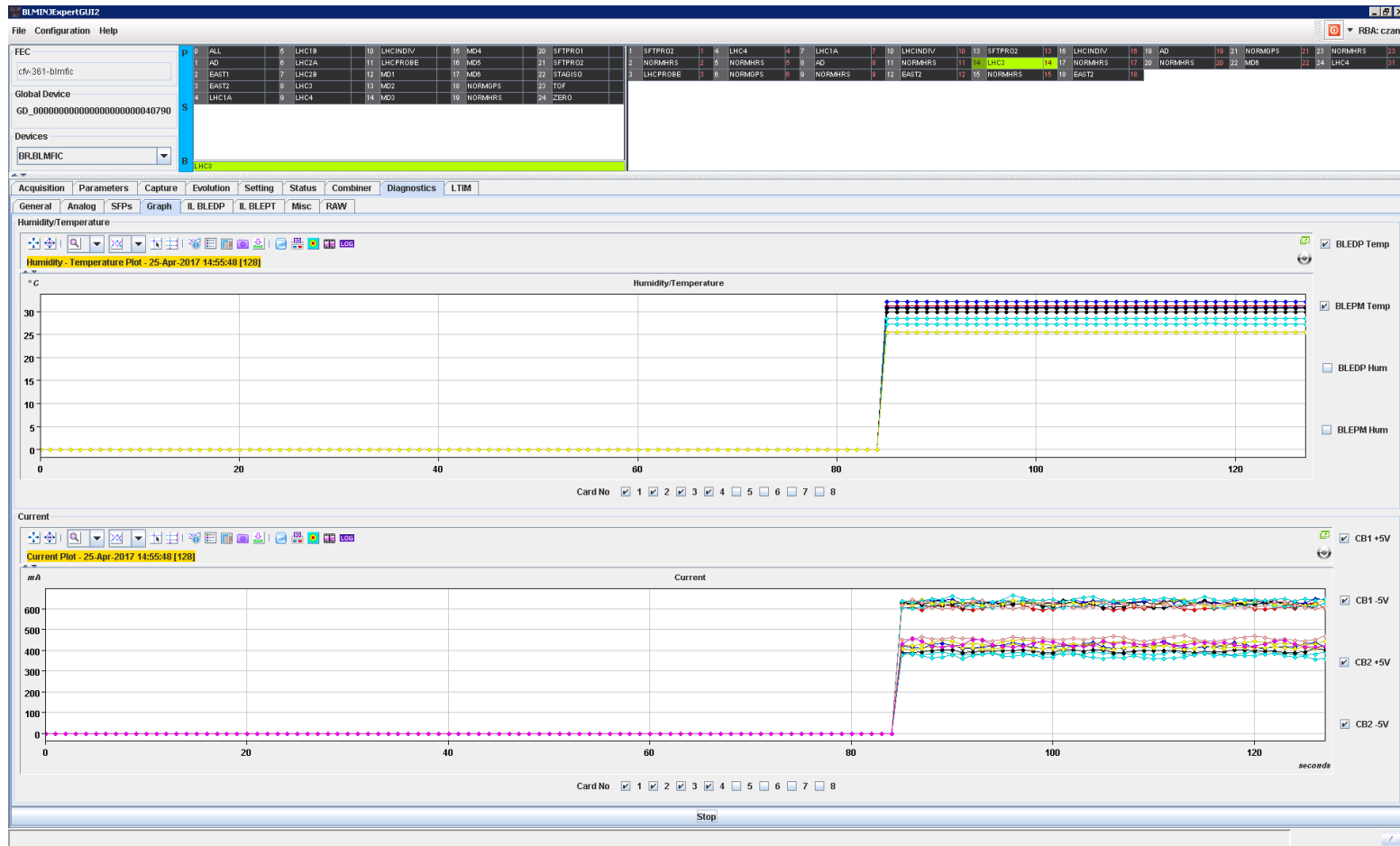
■ System information: power supplies and rack conditions

Parameters Setup

■ Channel names, Threshold values, masks, BIS outputs

■ State of the interlock outputs (software and firmware produced)
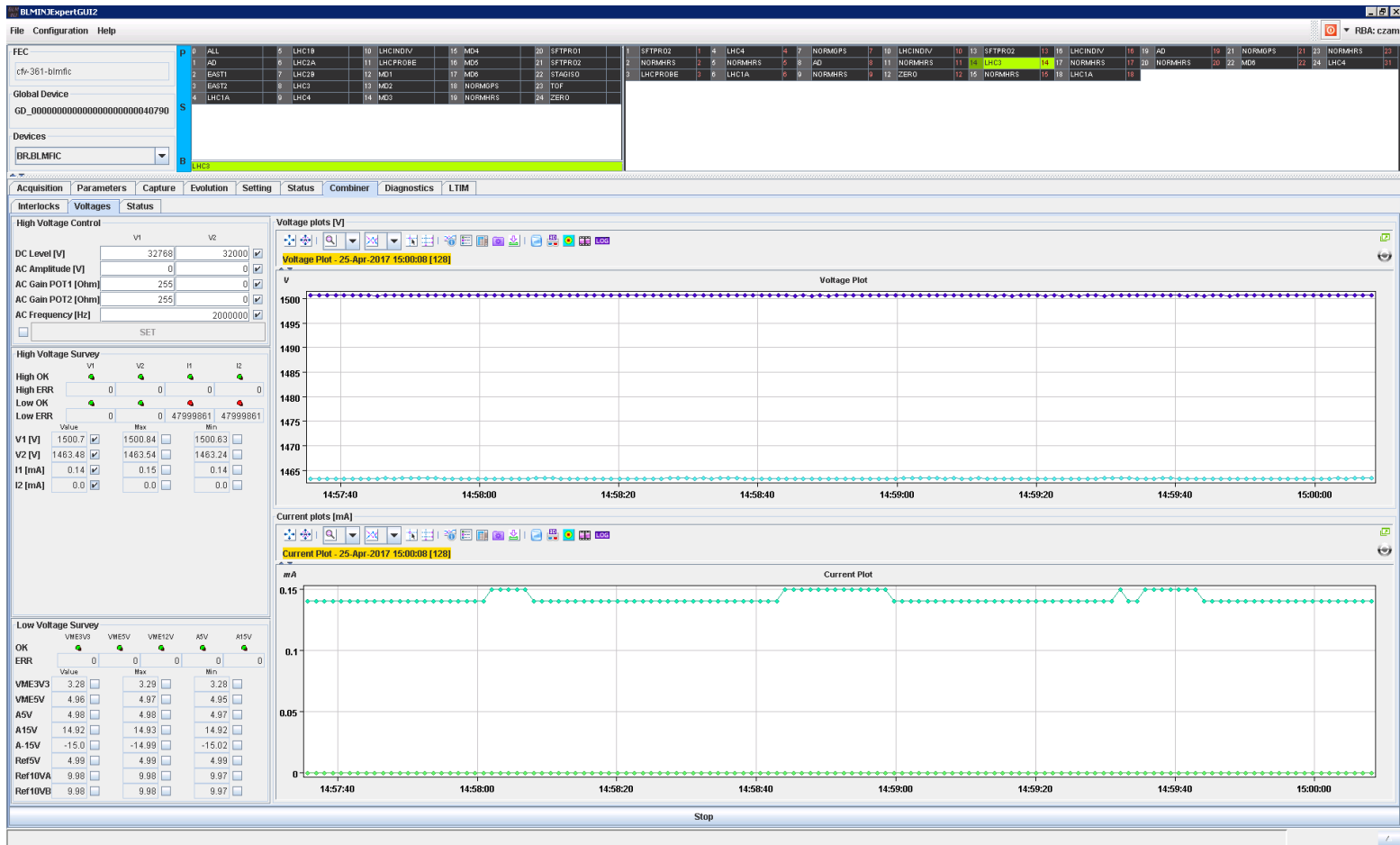
■ Power supply control and survey

- Timing distribution survey in the crate

BEAM MEASUREMENTS

27/06/2017
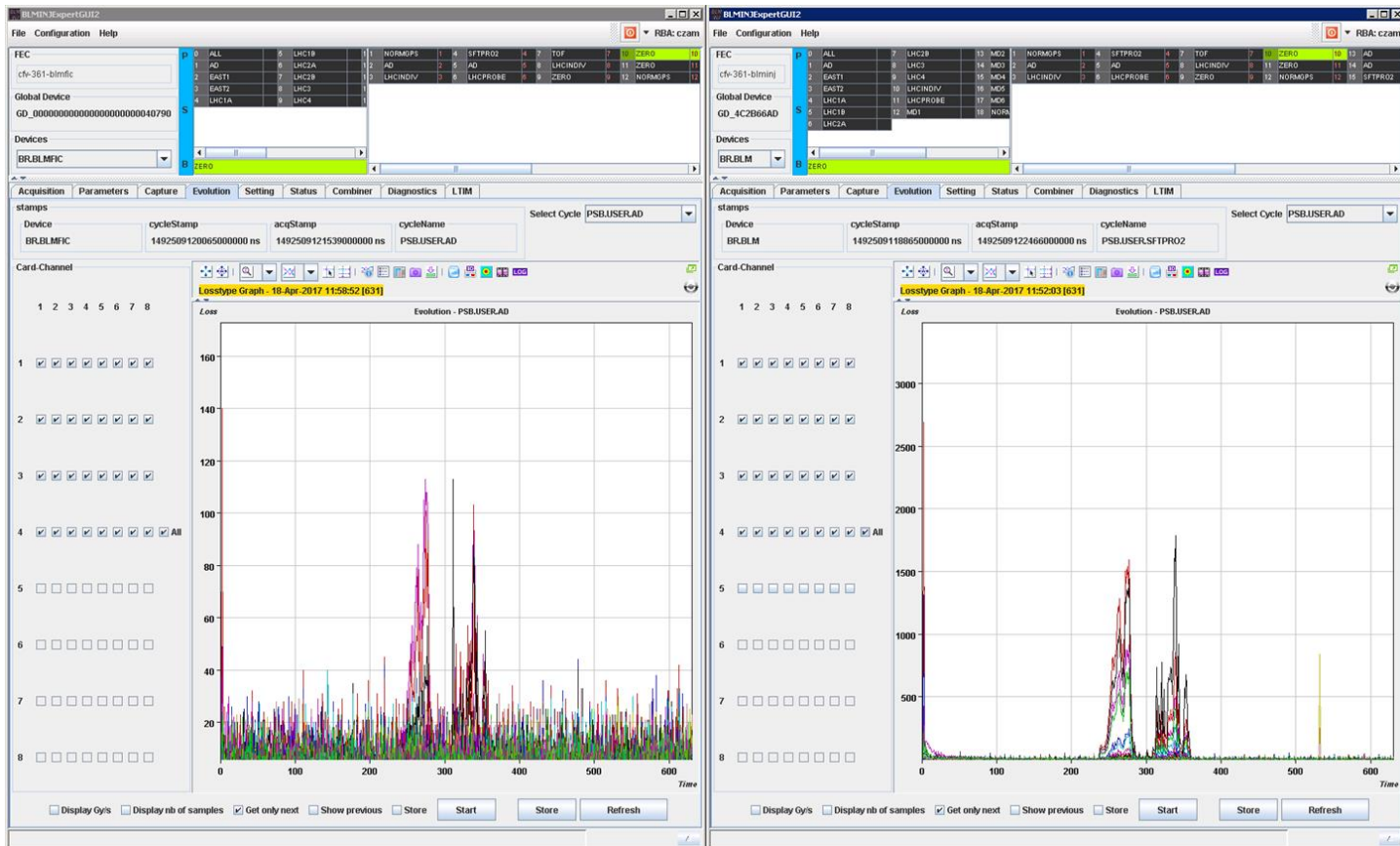
■ All channels operational
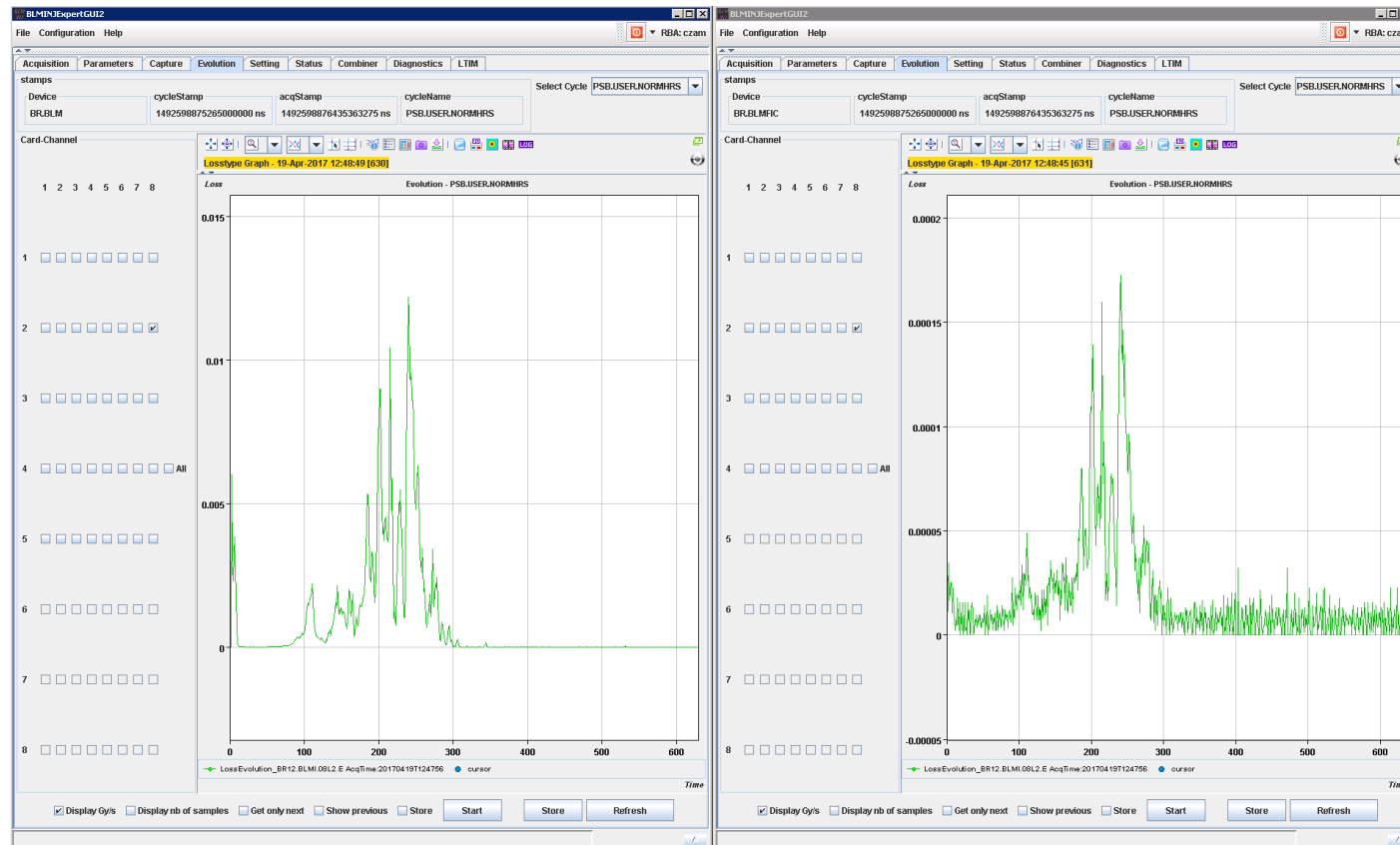
■ Pattern of losses seems identical in most locations

■ More noise visible since much smaller signal to measure

PR.BLMIB.01 – PR.BLMIB.50

PR.BLMIB.51 – PR.BLMIB.00
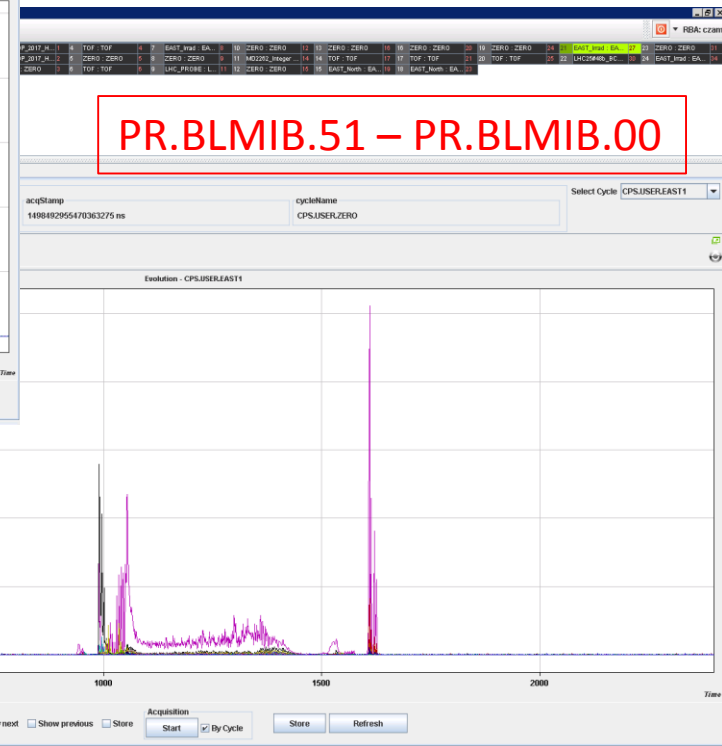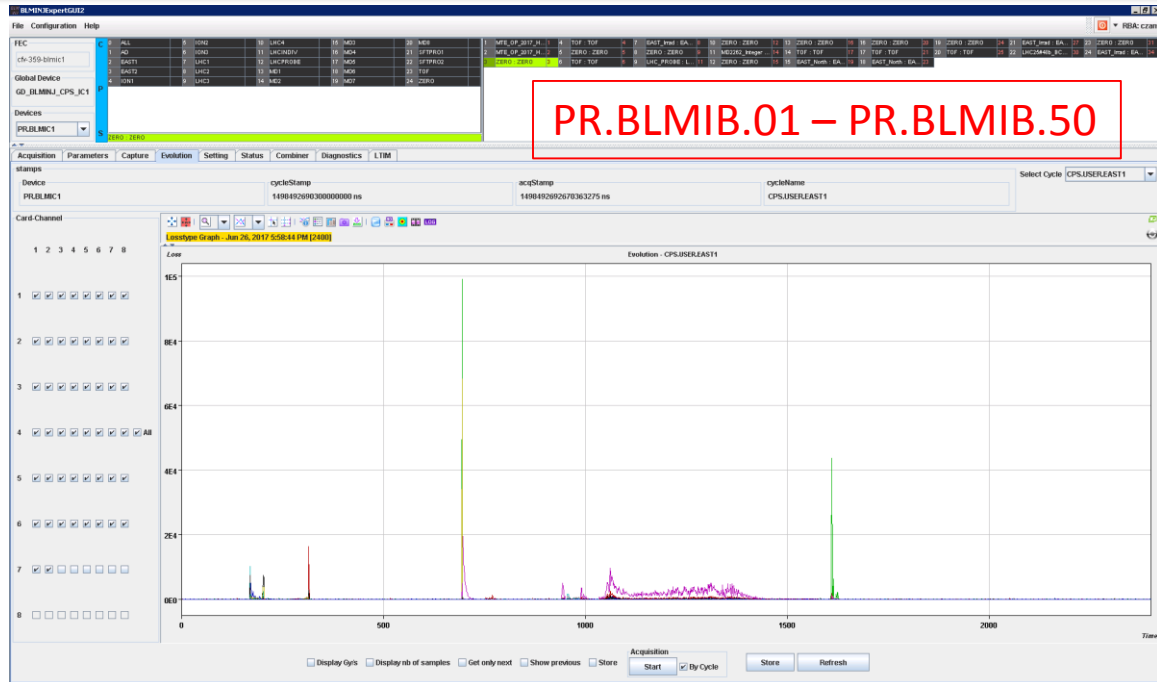
■ All channels operational, no significant noise issues

■ Length of Evolution buffer adjusts automatically based on the user

Channels: PR.BLMIB.15 – PR.BLMIB.19
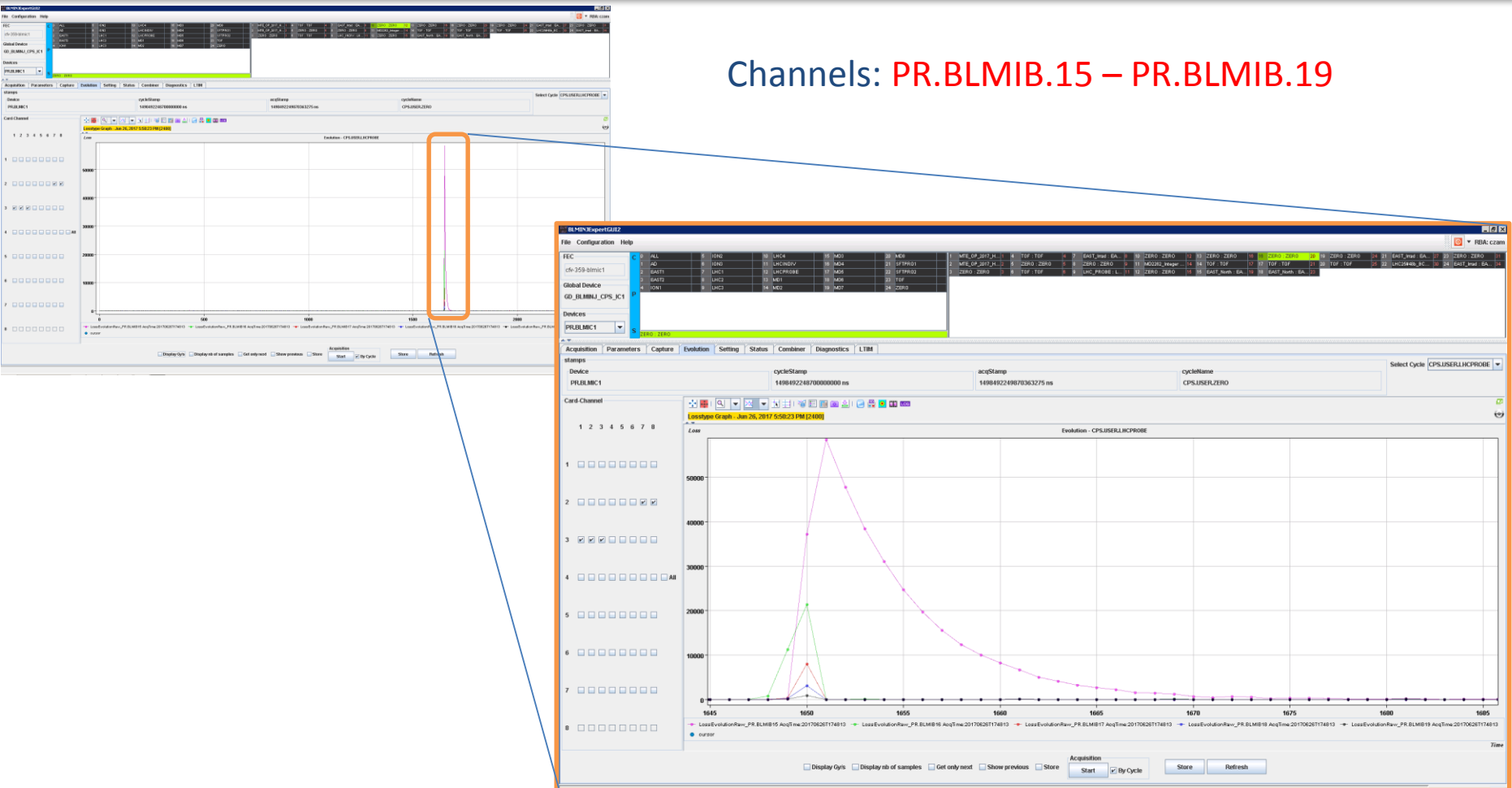
■ Zoom in: extraction of an LHCPROBE

NEXT STEPS & SUMMARY

TODO List

- Add in LAYOUT DB the configuration
  - Surface and tunnel installations

- Request data logging
  - ~~Measurements (Running Sums & Evolution buffer)~~
  - System Diagnostic and Monitoring
  - Threshold values (on change)

- Add the OASIS server for the Evolution buffer data

- Setup Threshold DB (InCA)
  - Connect to the update property

- Update electronics with the final versions
  - Acquisition electronics during YETS
  - Processing electronics during LS2

Summary

- **PSB**: Installation of 32 FIC detectors completed despite serious integration issues. In addition, 16 spare cables added around the ring.

- **PS**: Two complete systems with 134 channels have been produced, assembled and deployed under strict and short deadline
  - Original plan for both was LS2 (after decabling)
  - Solution was only found few months before EYETS
  - After cabling campaign very short period given to check for errors

- **All** connections and installations were done correctly and on-time
  - During the whole cabling campaign at least one person was next to the cabling installation teams

- BLMINJ system: Firmware and Software are ready for the Validation and Commissioning steps

- dBLM/OASIS system:
  - All amplified channels are already connected to OASIS. Finally, good decision to go for this as many channels will need it.
  - For the non-amplified channels a protection circuit has been prepared tested.
  - Priority was given to 15 & 16 locations in June (w/ handmade versions)

Installations, hardware, firmware

FUTURE DEVELOPMENTS

BLMINJ Installation Status

Machine/Area		Channels	Cables	Detector Type	Status
PSB	Ring (L2 position)	32	80	LHC-IC	Completed (LS1)
	Injection & BI line	11	22	LHC-IC	LS2
	Injection (observation)	8	40	Diamond	LS2
	Ring (L3 position)	32	80	FIC	Completed (EYETS)
	Extraction	25	60	LHC-IC	LS2

Machine/Area		Channels	Cables	Detector Type	
PS	Ring	100	200	LHC-IC	Completed (EYETS)
	Ring (observation)	17	85	Diamond	Completed (EYETS)
	Transfer Lines	51	102	LHC-IC	LS2

Machine/Area		Channels	Cables	Detector Type	
SPS	TT10	30	60	LHC-IC	LS2

- **Total copper cable length installed:** 40 km (PSB) + 58 km (PS)

- **Expected:**
  - 11 km (PSB)
  - 4 km multiwire with signal and HV boxes + xx km (PS/SPS TL)
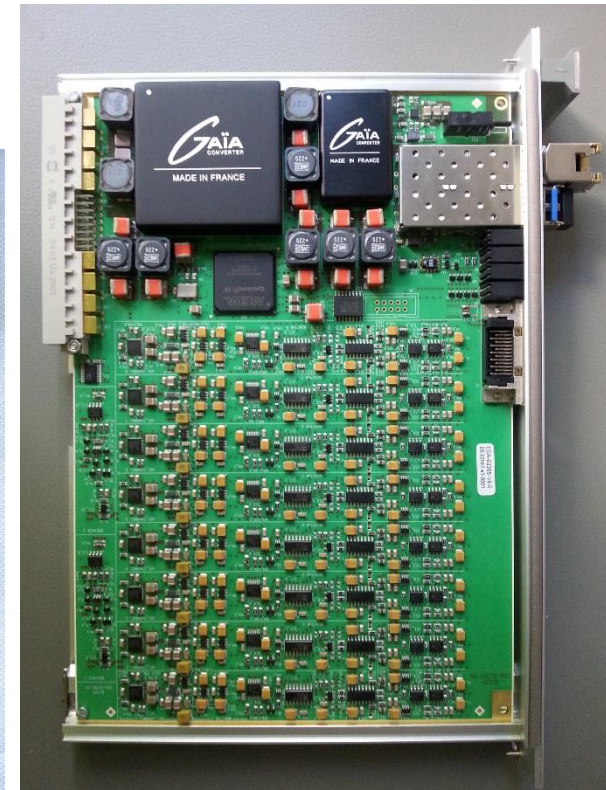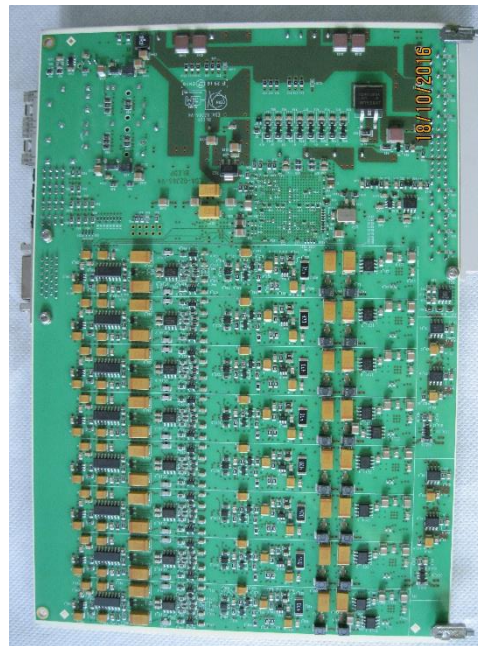
BLEDP series production

Series production of has just been received
55 acquisition modules

■ Next weeks:
  ▪ Visual inspection
  ▪ Programming
  ▪ Verification

YETS: Upgrade PS installation
LS2: new installations

Control & Survey Card Upgrade

Upgrade of the control and survey card by a remotely controlled version.
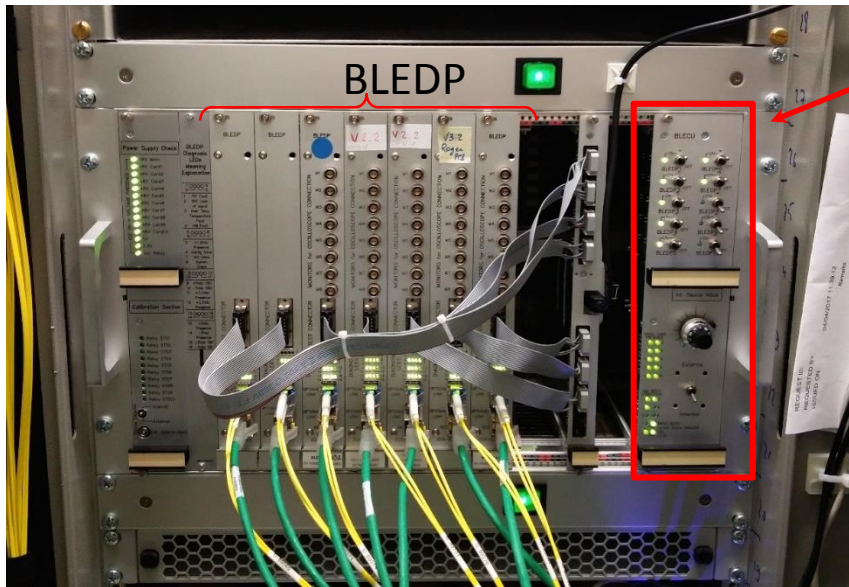

Photo with manual BLECU version

Remotely execute and control the

- calibration procedure and
- tests of the BLEDP cards
  - An embedded current source can be switched on and modulated to measure (almost) the full acquisition chain response of every channel.

Survey several parameters

- the power status of the crate and cards, temperature, humidity, etc.

FW spec (review on going)

FW design

FW prototype
Starting lab tests

Series installation

2017	2018	2019

HW design

HW specs

HW prototype

Series components refurbishing

Series production

Series Test & validation

Processing Module Upgrade

Upgrade the processing module to the VFC carrier

DAB64x + Mezzanine

VFC-HD
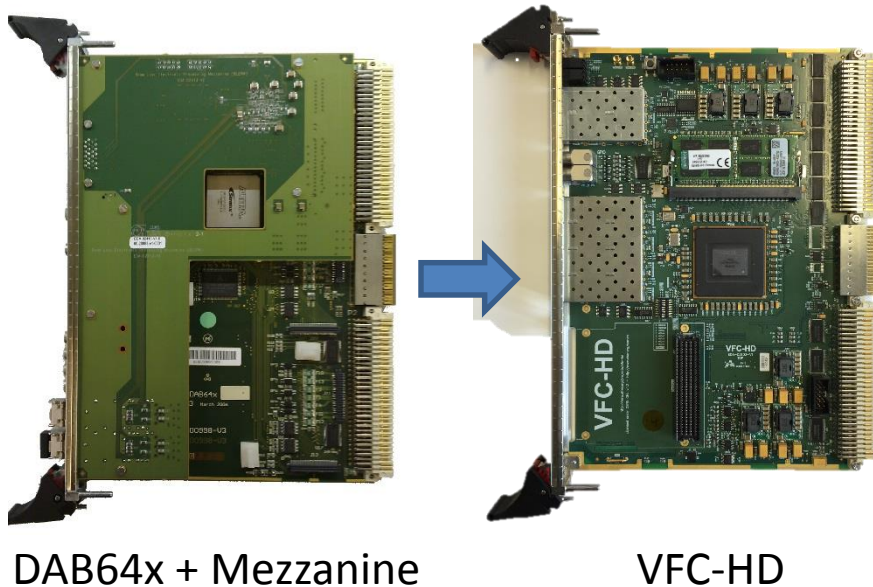
Common module for all BLM systems

Porting has started
- Working parts:
  - VME bus + GA
    - SCT, BLT and MBLT
  - Temperature
  - Serial number
  - LEDs
- Next:
  - I2C expander
  - SFPs (optical and Ethernet)
  - DDR3 (not needed)

Needed for installation during LS2

Firmware development

- Remote update through FESA server
  - First version deployed during last TS
- Automatic switching of the two acquisition methods
  - Needs lots of testing to choose best method
- Integration of the Connectivity Check
- Expose as settings the different configurations per machine
  - Currently hardcoded and each machine needs its own firmware compilation
- Implement the Capture Buffer

Thank you