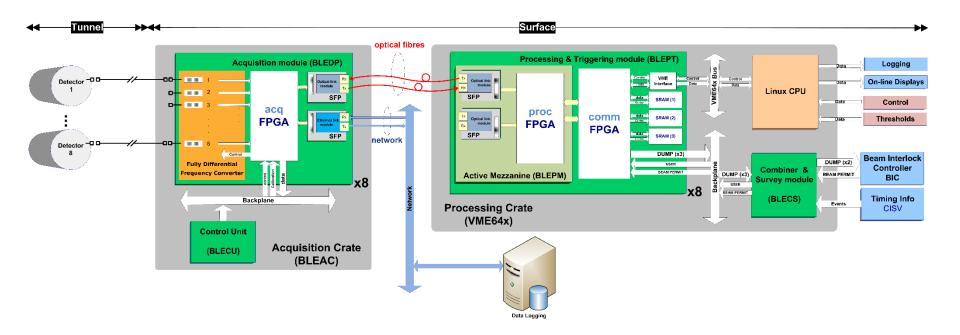
INJECTORS BLM SYSTEM: PS AND PSB RING INSTALLATIONS AT EYETS

BI-TB 28/09/2017

Christos Zamantzas on behalf of the BLM team.

BLMINJ System Overview



BLMINJ Integration Periods

Continuously the processing electronics will calculate 4 **integration period values** for each channel:

- **2** μs, **400** μs, **1** ms and **1.2** s (full period)
 - implemented as moving sum windows in the hardware
 - calculation refreshed at acquisition frequency
- Compare with predefined thresholds
 - Machine protection with hardware implementation comparisons on each refresh
 - Limit radiation levels with software implementation comparisons at end of cycle/period
 - See also next slide.
- Calculate for each channel the maximum values recorded on each integration period during the cycle
 - Publish them for the online displays and
 - the long-term logging

BLMINJ Threshold Comparisons

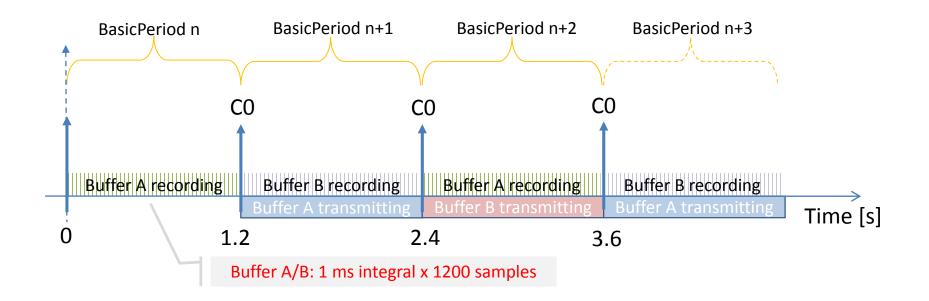
Hardware implementation part:

- All calculated integration period values, i.e from 2 μs to 1.2 s, will be constantly checked against their threshold values:
 - 4 threshold values, one for each of the integration periods.
 - Comparisons happen at the refresh period that is, every 2 μs
 - In the case the measured values exceed those the beam permit signal will be removed for all users
 - The **blocked** beam permit signal will be **latched** until an operator acknowledges.
- The threshold values will be need to be set unique per channel:
 - Each card will process 8 channels

Software implementation part:

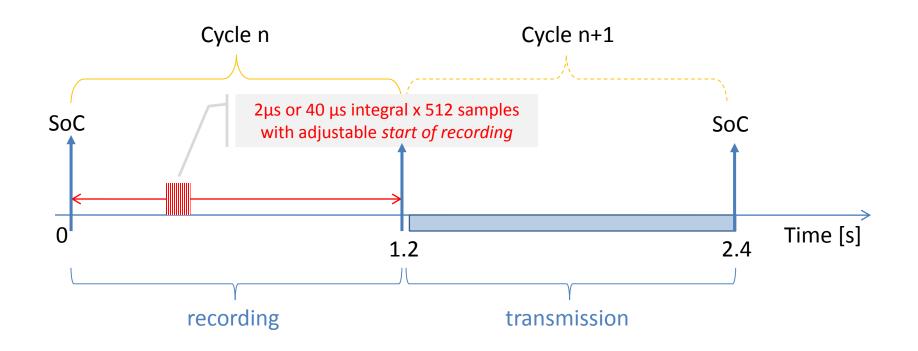
- All maximum integration period values recorded on the cycle will be checked against a second set of threshold values. The outputs will be used for repeated over threshold function
 - Additional threshold values for the same integration periods will also be required.
 - In the case found to be over threshold repeatedly *n* times it will be required to block **that user's injections**.
 - The **blocked** beam permit signal will be **latched** until an operator acknowledges.
 - The repeat value *n* will be settable per monitor in the range of 1 to 16.
- The threshold values will need to be unique per user and per channel:
 - Each CPU will process 8 cards x 8 channels
 - The information of the current user has to be obtained from the telegram per cycle -> dedicated timing card
 - Memory for 32 users will be reserved.

BLMINJ Loss Evolution Buffer



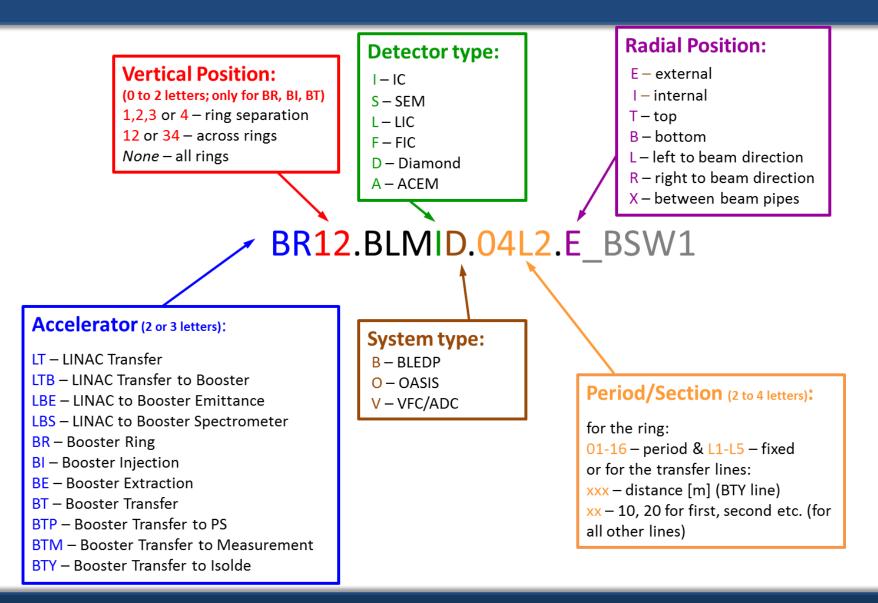
- Record 1ms integrals for the complete period
- Published in the on-line displays already on the next period
- Will be logged in the DB on-demand

BLMINJ Capture Buffer

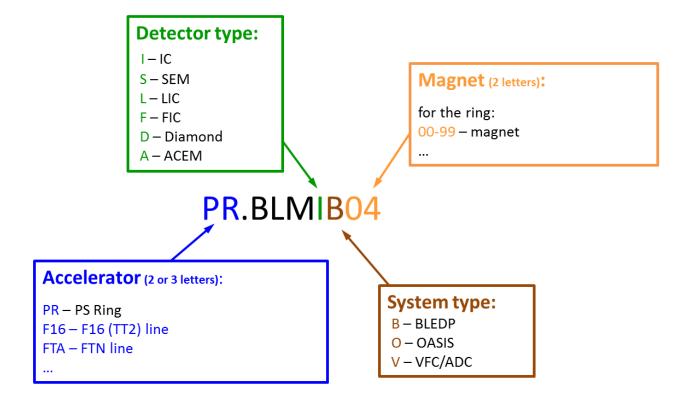


■ Pre-selection of 2 or 40 µs integrals and the start time
 ■ Recording of 512 samples

PSB Expert Name Convention



PS Expert Name Convention



Not final; need to clarify transfer lines

INSTALLATIONS DURING EYETS

PSB New Rack at BAT41E

Complete new rack installed

- Acquisition crate
- Processing crate
- HV crate
- HV distribution

■ 4 module pairs

- acquisition and processing cards
- 32 Channels connected
 - FIC detectors
- 8 channels spare
- Two HV power supplies
 - Second PSU is for redundancy





PS New Racks at B359

- Complete new set of four racks installed.
- Two racks for BLMINJ, with each hosting:
 - Acquisition crate
 - Processing crate
 - HV crate
 - HV distribution
 - Cable management

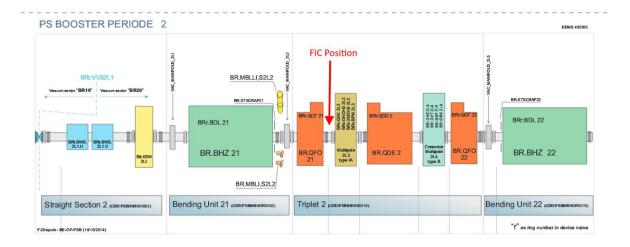
■ 14 module pairs

- acquisition and processing cards
- 100 Channels connected
 - Ionisation Chamber detectors
- 28 channels spare in total
- Two HV power supplies on each rack
 - Second PSU is for redundancy



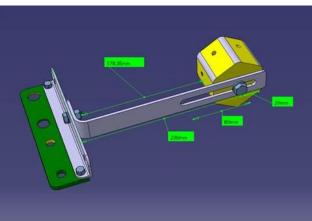


PSB Supports



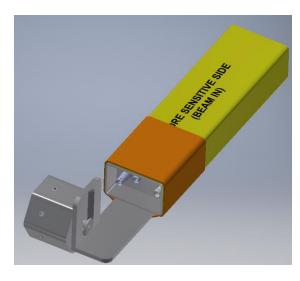
 Detector and cables are attached on the magnet nuts

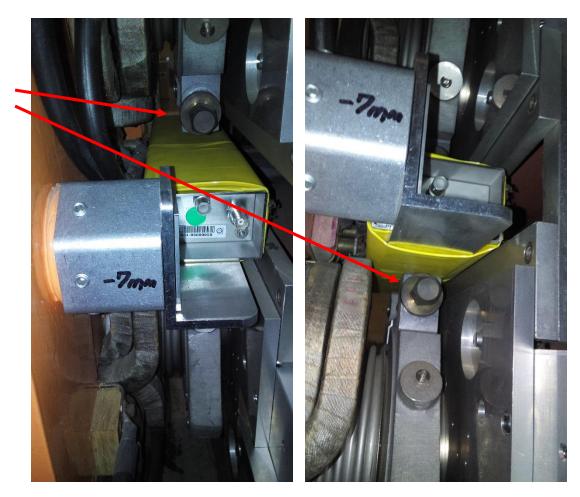




PSB Custom Supports

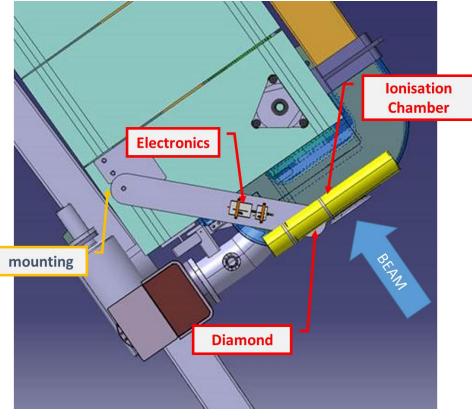
- Special supports for:
 - BR12.BLMFB.3L3.E
 - BR12.BLMFB.10L3.E
- Non standard installation of the vacuum clamps
 - Not enough space to fit detector
- Need to verify the signal difference





PS Tunnel Installation

- Installation was modified several times to fit and satisfy all requests
 - Mostly issues with cabling and patchcords





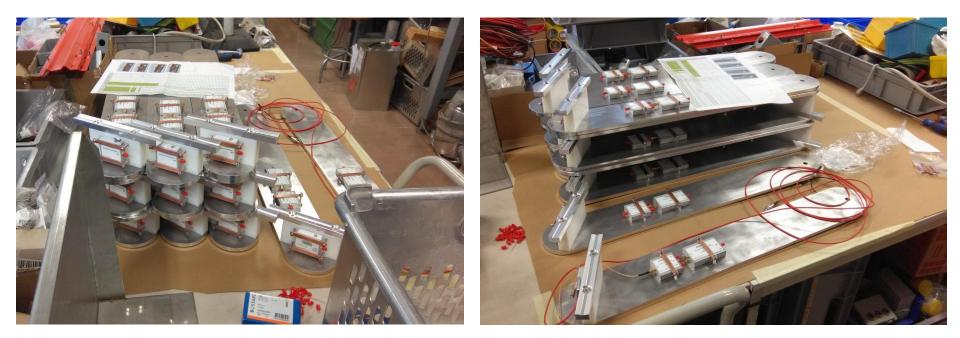




PS Diamond Installation

Preparation of the installation

- All dBLMs have been equipped with splitters and amplifiers
- Connections done and tested in the lab before deployment



PS Diamond Installation

HV and LV Power supply unit for the Diamond bias and the amplifier

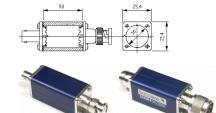
- Ethernet connection for control
- FESA class to control and log values is under development
- OP will have the ability to switch off/on (seems not necessary with the latest info; matrix will terminate input when a channel is not used/digitised)
- Only Experts will have the ability to set/modify the voltage values

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Group 1				Group 2			
LV Channel	PR.BLMD014	PR.BLMD015	Monitor3Name	LV Channel	PR.BLMD016	PR.BLMD017	PR.BLMDO18
V [V] 12.5	0.00 V [V] 500	-0.01 V [V] 500 + -0.0		V [V] 12.5 🐥	0.00 V [V] 500 🐥 -0.00	V [V] 500 + -0.01	V [V] 500 + -0.00
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Status	0 Status	b5bd0100 Status b5cd010	0 Status 0000	Status	0 Status b5cf0100	Status b5c30100	Status b5bd0100
ON OFF	OFF ON OFF	OFF ON OFF OF	F ON OFF OFF	ON OFF	OFF ON OFF OFF	ON OFF OFF	ON OFF OFF
Group 3				Group 4			
LV Channel	PR.BLMD040	PR.BLMD041	Monitor3Name	LV Channel	PR.BLMD042	PR.BLMD043	Monitor3Name
V [V] 12.5	0.00 V [V] 500	0.01 V [V] 500 + -0.0	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	V [V] 12.5	0.00 V [V] 500 🗘 0.00	V [V] 500 🗘 0.00	V [V]
I [A]	0.00 I [A]	-0.00 [A]	1 [A] 0		0.00 I [A] -0.00	I [A]	1 [A]
Status	0 Status	b5c70100 Status b5bf010	Status 0000	Status	0 Status b5b70100	Status b5b30100	Status 0000
ON OFF	OFF ON OFF	OFF OF OF	F ON OFF OFF	ON OFF	OFF OFF OFF	ON OFF OFF	ON OFF OFF
Group 5				Group 6			
LV Channel	PR.BLMD044	PR.BLMD045	Monitor3Name	LV Channel	PR.BLMDO46	PR.BLMDO49	Monitor3Name
V [V] 12.5	0.00 V [V] 500	0.02 V [V] 500 🗘 0.0	0 V [V] 0	V [V] 12.5	0.00 V [V] 500 2 0.01	V [V] 500 2 0.00	V [V] 500 🗘 (
I [A]	0.00 I [A] I	-0.00 I [A] .	. I [A] 0	1 [A]	0.00 I [A] 00.0	I [A]	1 [A]
Status	0 Status	b5b90100 Status b5ab010	0 Status 0000	Status	0 Status b5a90100	Status b59f0100	Status 0000
ON OFF	OFF ON OFF	OFF OF OF	F ON OFF OFF	ON OFF	OFF OFF OFF	ON OFF OFF	ON OFF OFF
Group 7				Group 8			
LV Channel	PR.BLMD071	PR.BLMD075	Monitor3Name	LV Channel	PR.BLMD079	PR.BLMD083	Monitor3Name
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Status	0 Status	b59d0100 Status b5b4010	0 Status 0000	Status	0 Status b5c20100	Status b5c60100	Status 0000
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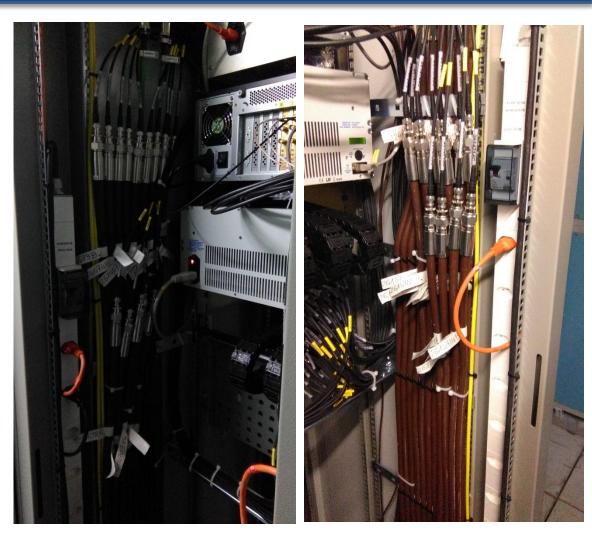


PS Diamond Installation

- Signal cables arrive at the OASIS rack
- With adapters and patchcords are connected to the OASIS Matrix
- With another set of patchcords signals arrive to the 4 OASIS Digitisers
- Aim is to intercept the signals before the matrix and add a protection circuit.
 - This will also reduce the adaptors and patchcords used
- Circuit is ready and tested in the lab.
 - A PCB has been designed to fit in a small box and is under production
 - Will have the ability to add attenuation if needed in the future



BNC MALE - BNC FEMELLE

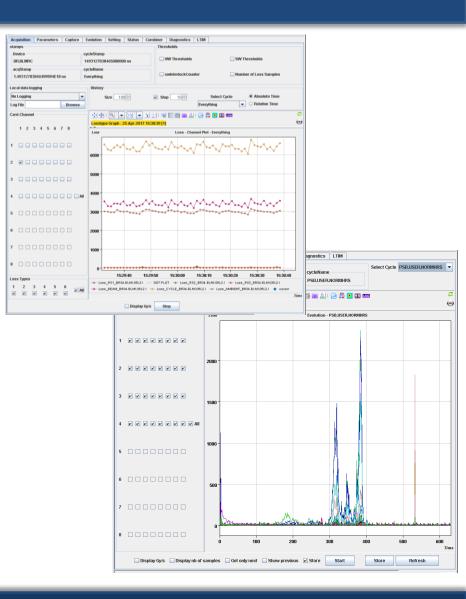


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DEVELOPMENT

System Development

- Firmware and Software available to stable versions with all major features available.
- Direct Ethernet connection to each acquisition module available for detailed analysis and debugging.
 - 2 μs samples continuously
- Through FESA class, system provides synchronised with the basic period
 - Several integrals (2 μs 1.2 s, BeamPresence and Ambience)
 - 'Evolution' data for the complete cycle.
 - Data are 'tagged' with the USER
- Functionalities under verification:
 - loading of settings/thresholds,
 - system status information
- Functionalities to be developed:
 - On-demand Capture buffer with 2 μs samples



PS Evolution Buffer

Firmware: double buffer at the FPGA 🛛

- One records when the other transmits
- Toggle operation with basic period
- No blind time

- Software: two properties from FESA
 - Data per basic period
 - Data per cycle
 - Units: Gy/s or bits

Navigation Tool 2016-NOV-TS(v3.0.144)@cs-ccr-abb	bbi5.cern.ch	Navigation Tool 2016-NOV-TS(v3.0.144)@cs-ccr-abbi5.cern.ch
MINJ version 0.11.0	Load Watch Dir Query	BLMIN version 0.11.0 Load Watch Dir Query
LMINJ0.11.0 Global		BLMINJ0.11.0 Global
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per Basic Period

per Cycle

System Diagnostic Data [1/3]

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perature	31.25 °C	32.2 °C	30.68 °C	28.58 °C	0 °C	0 °C	0 °C	0 °C
idity	29.96 %	25.33 %	28.67 %	30.9 %	0 %	0 %	0 %	0 %
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System information: firmware version, card serials, temperature and humidity

System Diagnostic Data [2/3]

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System information: Optical links performance

System Diagnostic Data [3/3]

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System information: power supplies and rack conditions

Parameters Setup

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Thresholds											
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General											
	FW Ver	sion			Chip ID			Temperature Thresh	old (°C)		
SFP1						SFP2					
Temperature Threshol	1(°C)					Temperature Threshol	d(°C)				
Power Threshold (°C)						Power Threshold (°C)					
				Read All		Set All	Set				
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Channel names, Threshold values, masks, BIS outputs

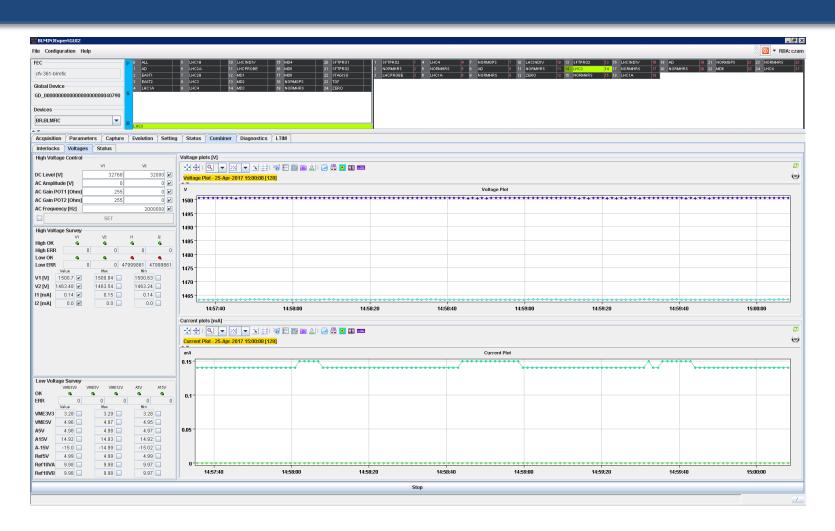
Beam Interlocks [1/3]

	7 ×
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ware watchdog	
107 Time to interlock (ms)	
100 Watchdog timeout (ms)	
Set watchdog timeout (ms)	
Stop	-
	7

■ State of the interlock outputs (software and firmware produced)

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Beam Interlocks [2/3]



Power supply control and survey

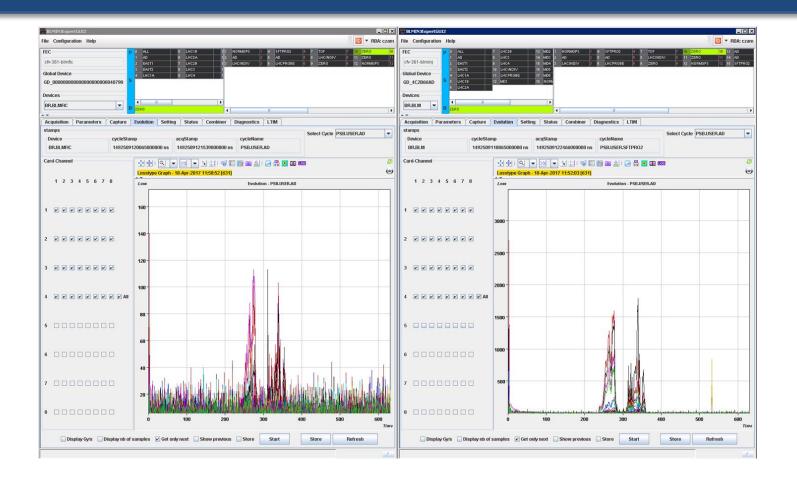
Beam Interlocks [3/3]

BLMINJExp	pertGUI2													_ <i>B</i> ×
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FEC			p 0 ALL	5 LHC18	10 LHCINDIV	16 MD4 :	20 SFTPRO1	1 SFTPR02 1 4			10 13 SFTPRO2 13	16 LHCINDIV 16 19 A	D 19 21 NORMG	PS 21 23 NORMHRS 23
cfv-361-blm	nfic		1 AD 2 EAST1	6 LHC2A 7 LHC2B	11 LHCPROBE 12 MD1	16 MD5	21 SFTPRO2 22 STAGISO	2 NORMHRS 2 5 3 LHCPROBE 3 6	ORMHRS 5 8 AD HCIA 8 9 NORMH	8 11 NORMHRS HRS 9 12 ZERO	11 14 LHC3 14 12 15 NORMHRS 15	17 NORMHRS 17 20 N 18 LHC1A 18	ORMHRS 20 22 MD6	22 24 ZER0 25
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■ Timing distribution survey in the crate

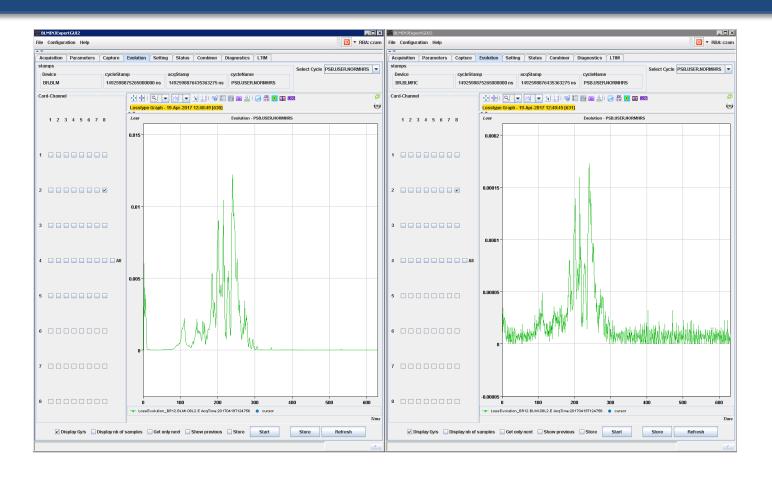
BEAM MEASUREMENTS

PSB First Measurements [1/2]



All channels operational

PSB First Measurements [2/2]



- Pattern of losses seems identical in most locations
- More noise visible since much smaller signal to measure

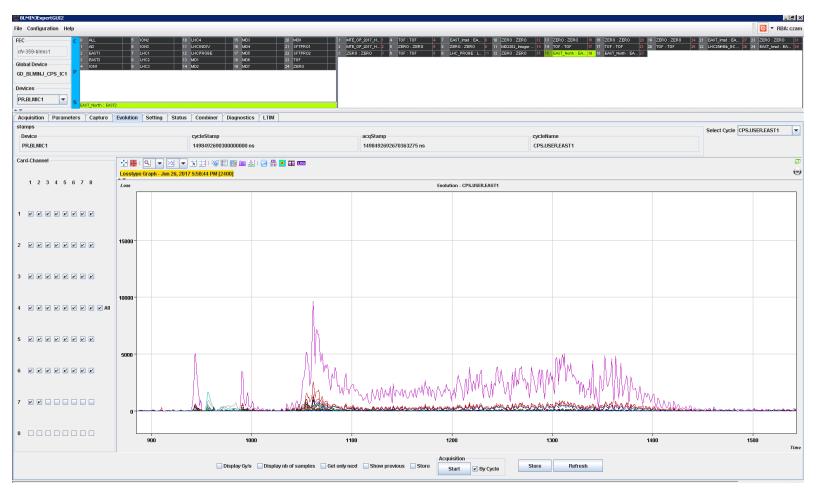
PS First Measurements [1/3]

BLMIN/BepertGU12 File Configuration Help					_ () • RBA: cza			
FEC C ALL 1 A0 2 66-359-bimic1 2 64511 2 64512	6 1040 10 UKC4 16 MO3 28 1 6 1040 11 UKC14 16 M04 21 7 UKC1 12 UKCPR088 17 M05 22 0 UKC2 10 M01 10 M01 31	4C0 1 MTE_OP_32 EFTPR01 2 MTE_OP_32 EFTPR02 3 2ERO 2EE 10F	972_H1 4 TOF : TOF 4 7 EAST_HH#: EA9 19 2280 972_H2 5 2280 : 2280 5 8 2280 : 2280 9 11 MD22 80 3 6 TOF : TOF 5 9 LHC_PROME: L 31 12 2280	D: ZERO IZ IX ZERO IM IX IX ZERO IX IX ZERO IX IX ZERO IX IX ZERO IX IX <thix< th=""> <thix< th=""> <thix< th=""></thix<></thix<></thix<>	16 20F0 20E0 0 01 01 045 0645 064 07 02 20E0 20E0 0 01 26 TOF : TOF 25 22 UHC254465_8C 38 24 6455_863 : 6A 34	4		
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■ All channels operational, no significant noise issues

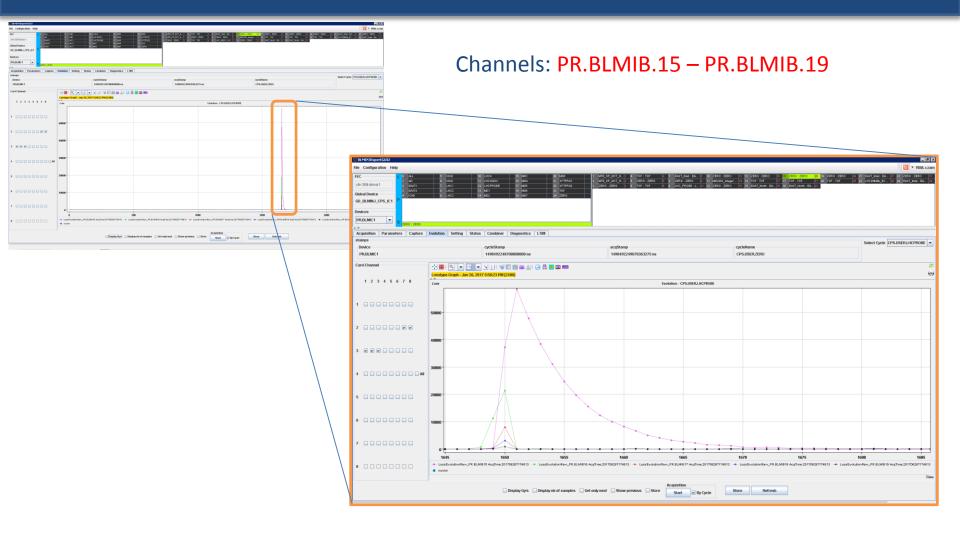
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PS First Measurements [2/3]



Length of Evolution buffer adjusts automatically based on the user

PS First Measurements [3/3]



■ Zoom in: extraction of an LHCPROBE

NEXT STEPS & SUMMARY

TODO List

- Add in LAYOUT DB the configuration
 - Surface and tunnel installations
- Request data logging
 - Measurements (Running Sums & Evolution buffer)
 - System Diagnostic and Monitoring
 - Threshold values (on change)
- Add the OASIS server for the Evolution buffer data
- Setup Threshold DB (InCA)
 - Connect to the update property
- Update electronics with the final versions
 - Acquisition electronics during YETS
 - Processing electronics during LS2

Summary

- PSB: Installation of 32 FIC detectors completed despite serious integration issues. In addition, 16 spare cables added around the ring.
- PS: Two complete systems with 134 channels have been produced, assembled and deployed under strict and short deadline
 - Original plan for both was LS2 (after decabling)
 - Solution was only found few months before EYETS
 - After cabling campaign very short period given to check for errors
- All connections and installations were done correctly and on-time
 - During the whole cabling campaign at least one person was next to the cabling installation teams
- BLMINJ system: Firmware and Software are ready for the Validation and Commissioning steps
- dBLM/OASIS system:
 - All amplified channels are already connected to OASIS. Finally, good decision to go for this as many channels will need it.
 - For the non-amplified channels a protection circuit has been prepared tested.
 - Priority was given to 15 & 16 locations in June (w/ handmade versions)

Installations, hardware, firmware

FUTURE DEVELOPMENTS

BLMINJ Installation Status

	Machine/Area	Channels	Cables	Detector Type	Status
	Ring (L2 position)	32	80	LHC-IC	Completed (LS1)
	Injection & BI line	11	22	LHC-IC	LS2
PSB	Injection (observation)	8	40	Diamond	LS2
	Ring (L3 position)	32	80	FIC	Completed (EYETS)
	Extraction	25	60	LHC-IC	LS2
	Machine/Area	Channels	Cables	Detector Type	
	Ring	100	200	LHC-IC	Completed (EYETS)
PS	Ring (observation)	17	85	Diamond	Completed (EYETS)
	Transfer Lines	51	102	LHC-IC	LS2
	Machine/Area	Channels	Cables	Detector Type	

	Machine/Area	Channels	Cables	Detector Type	
SPS	TT10	30	60	LHC-IC	LS2

■ Total copper cable length installed: 40 km (PSB) + 58 km (PS)

Expected:

- 11 km (PSB)
- 4 km multiwire with signal and HV boxes + xx km (PS/SPS TL)

BLEDP series production

Series production of has just been received 55 acquisition modules

Next weeks:

- Visual inspection
- Programming
- Verification

YETS: Upgrade PS installation LS2: new installations





Control & Survey Card Upgrade

Upgrade of the control and survey card by a remotely controlled version.

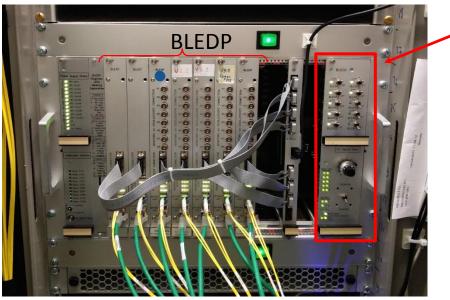


Photo with manual BLECU version

Remotely execute and control the

- calibration procedure and
- tests of the BLEDP cards
 - An embedded current source can be switched on and modulated to measure (almost) the full acquisition chain response of every channel.

Survey several parameters

- the power status of the crate and cards, temperature, humidity, etc.

	FW spec (reviev FW design	v on going)	ts		Series installation			
	2017			2018			2019	
HW :	HW design	HW prototyp)e	Series components refurbishing		eries oduction	Series Test & validation	
	christos zamantzas	@cern.ch		28/09/2017				40

Processing Module Upgrade

Upgrade the processing module to the VFC carrier



DAB64x + Mezzanine

VFC-HD

Common module for all BLM systems

Porting has started

- Working parts:
 - VME bus + GA
 - SCT, BLT and MBLT
 - Temperature
 - Serial number
 - LEDs
- Next:
 - I2C expander
 - SFPs (optical and Ethernet)
 - DDR3 (not needed)

Needed for installation during LS2

Firmware development

- Remote update through FESA server
 - First version deployed during last TS
- Automatic switching of the two acquisition methods
 - Needs lots of testing to choose best method
- Integration of the Connectivity Check
- Expose as settings the different configurations per machine
 - Currently hardcoded and each machine needs its own firmware compilation
- Implement the Capture Buffer

Thank you