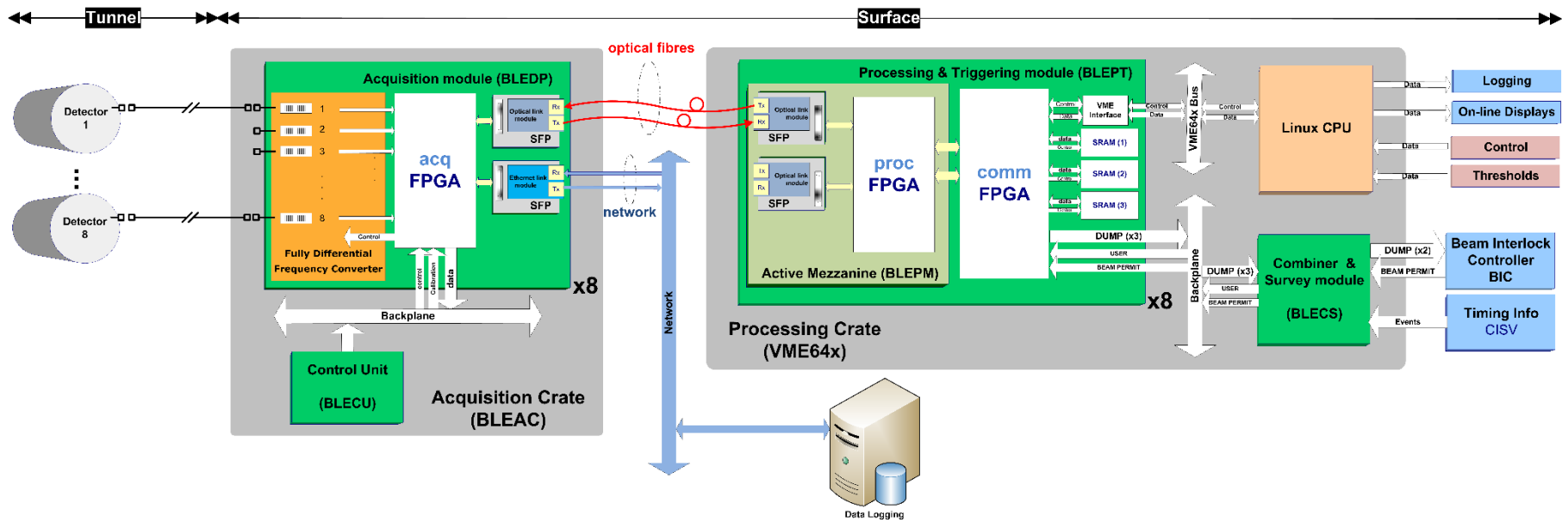


INJECTORS BLM SYSTEM: PS AND PSB RING INSTALLATIONS AT EYETS

BI-TB 28/09/2017

Christos Zamantzas on behalf of the BLM team.

BLMINJ System Overview



BLMINJ Integration Periods

Continuously the processing electronics will calculate 4 **integration period values** for each channel:

- **2 μs , 400 μs , 1 ms and 1.2 s** (full period)
 - implemented as moving sum windows in the hardware
 - calculation refreshed at acquisition frequency
- Compare with predefined thresholds
 - **Machine protection** with **hardware** implementation comparisons on each refresh
 - **Limit radiation levels** with **software** implementation comparisons at end of cycle/period
 - See also next slide.
- Calculate for each channel the **maximum** values recorded on each integration period during the cycle
 - Publish them for the online displays and
 - the long-term logging

BLMINJ Threshold Comparisons

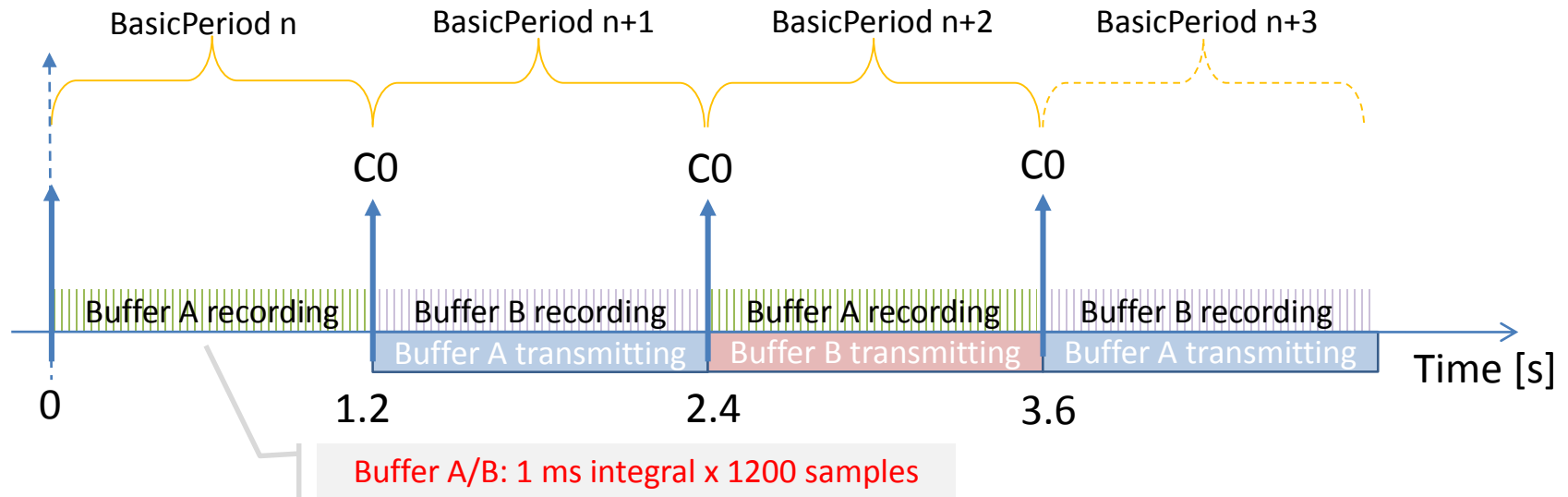
Hardware implementation part:

- All **calculated integration period values**, i.e from **2 μ s** to **1.2 s**, will be constantly checked against their threshold values:
 - 4 threshold values, one for each of the integration periods.
 - Comparisons happen at the refresh period – that is, every 2 μ s
 - In the case the measured values exceed those the **beam permit signal** will be removed for **all users**
 - The **blocked** beam permit signal will be **latched** until an operator acknowledges.
- The **threshold values** will be need to be set **unique per channel**:
 - Each card will process 8 channels

Software implementation part:

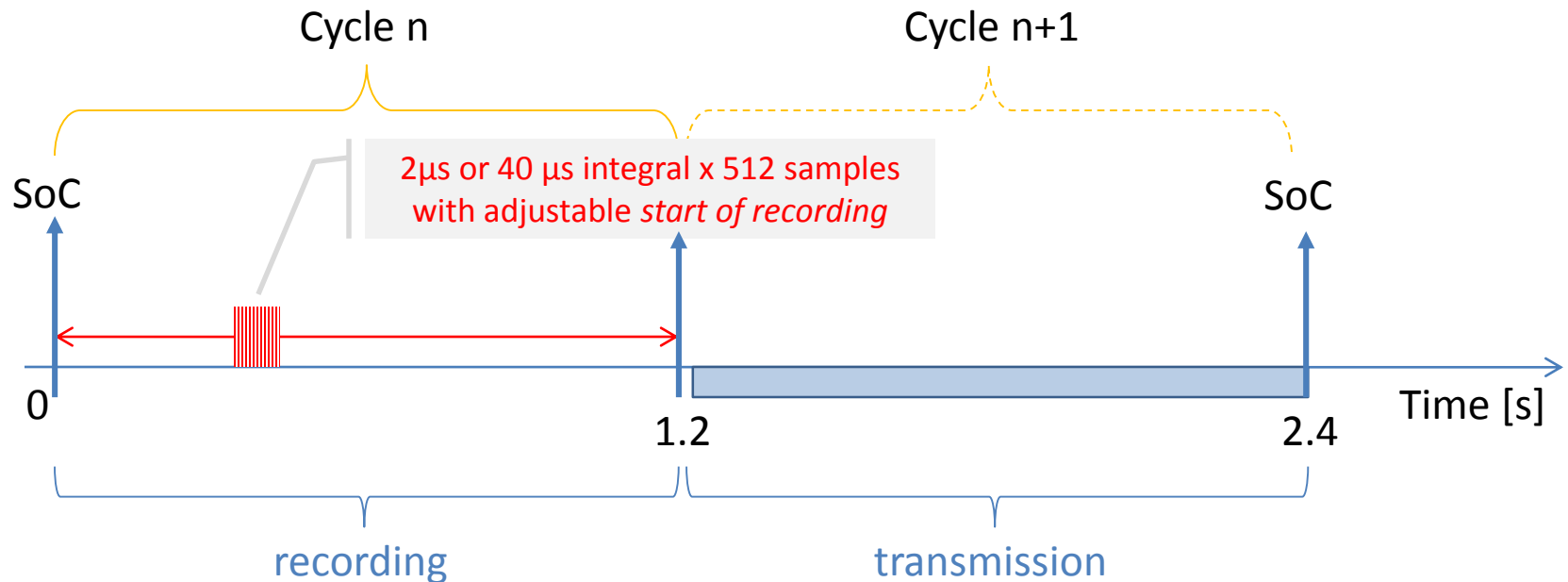
- All **maximum integration period values** recorded on the cycle will be checked against a second set of threshold values. The outputs will be used for **repeated over threshold function**
 - Additional threshold values for the same integration periods will also be required.
 - In the case found to be **over threshold repeatedly n times** it will be required to block **that user's injections**.
 - The **blocked** beam permit signal will be **latched** until an operator acknowledges.
 - The repeat value n will be settable per monitor in the range of 1 to 16.
- The **threshold values** will need to be **unique per user and per channel**:
 - Each CPU will process 8 cards x 8 channels
 - The information of the current user has to be obtained from the telegram per cycle -> **dedicated timing card**
 - Memory for 32 users will be reserved.

BLMINJ Loss Evolution Buffer



- Record 1ms integrals for the complete period
- Published in the on-line displays already on the next period
- Will be logged in the DB on-demand

BLMINJ Capture Buffer



- Pre-selection of 2 or 40 μs integrals and the start time
- Recording of 512 samples

PSB Expert Name Convention

Vertical Position:

(0 to 2 letters; only for BR, BI, BT)

1,2,3 or 4 – ring separation

12 or 34 – across rings

None – all rings

Detector type:

I – IC

S – SEM

L – LIC

F – FIC

D – Diamond

A – ACEM

Radial Position:

E – external

I – internal

T – top

B – bottom

L – left to beam direction

R – right to beam direction

X – between beam pipes

Accelerator (2 or 3 letters):

LT – LINAC Transfer

LTB – LINAC Transfer to Booster

LBE – LINAC to Booster Emittance

LBS – LINAC to Booster Spectrometer

BR – Booster Ring

BI – Booster Injection

BE – Booster Extraction

BT – Booster Transfer

BTP – Booster Transfer to PS

BTM – Booster Transfer to Measurement

BTY – Booster Transfer to Isolde

System type:

B – BLEDP

O – OASIS

V – VFC/ADC

Period/Section (2 to 4 letters):

for the ring:

01-16 – period & L1-L5 – fixed

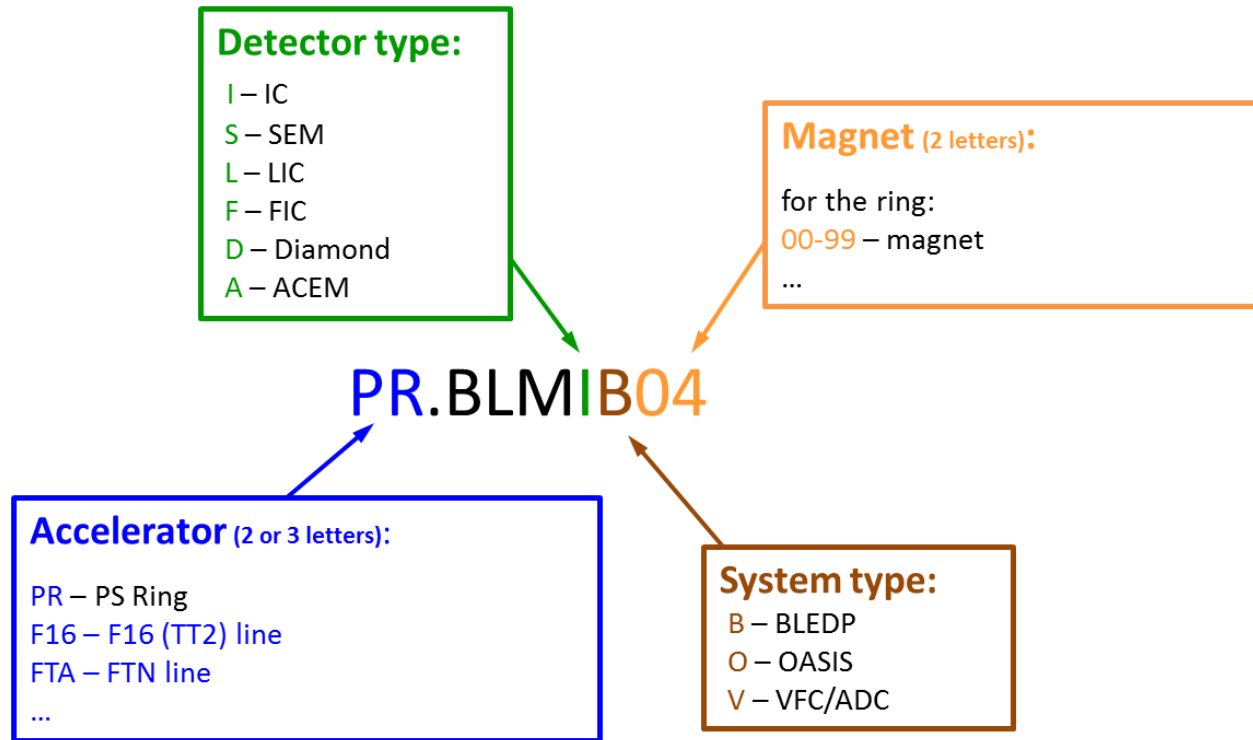
or for the transfer lines:

xxx – distance [m] (BTY line)

xx – 10, 20 for first, second etc. (for all other lines)

BR12.BLMID.04L2.E_BSW1

PS Expert Name Convention



Not final; need to clarify transfer lines

INSTALLATIONS DURING EYETS

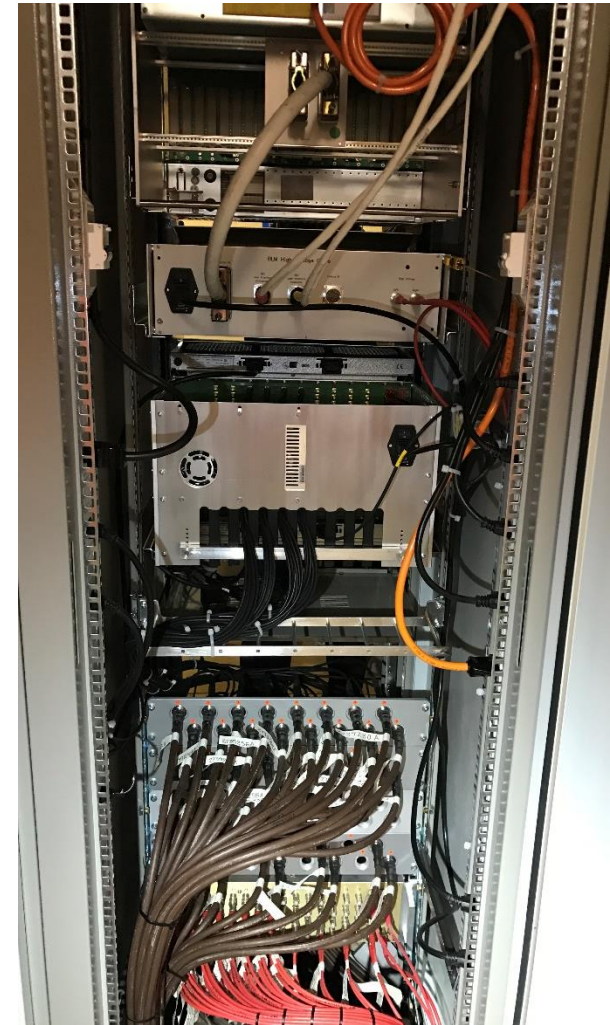
PSB New Rack at BAT41E

- Complete new rack installed
 - Acquisition crate
 - Processing crate
 - HV crate
 - HV distribution
- 4 module pairs
 - acquisition and processing cards
- 32 Channels connected
 - FIC detectors
- 8 channels spare
- Two HV power supplies
 - Second PSU is for redundancy



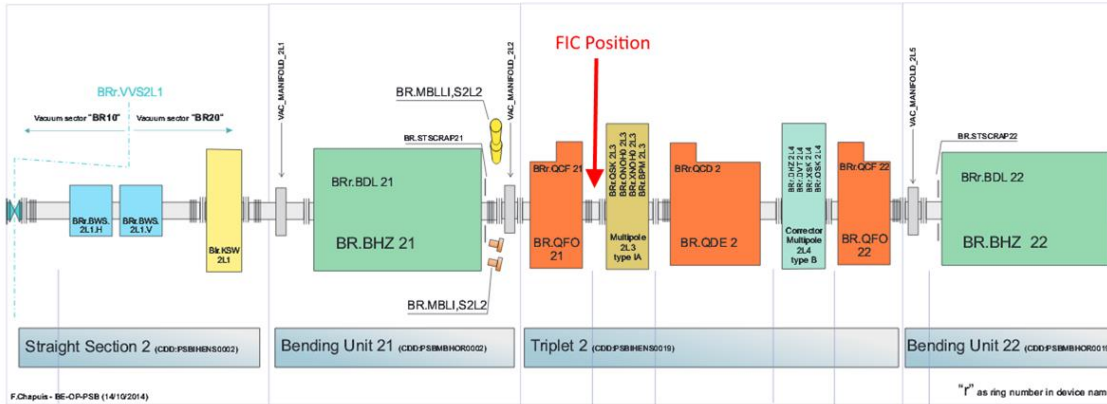
PS New Racks at B359

- Complete new set of four racks installed.
- Two racks for BLMINJ, with each hosting:
 - Acquisition crate
 - Processing crate
 - HV crate
 - HV distribution
 - Cable management
- 14 module pairs
 - acquisition and processing cards
- 100 Channels connected
 - Ionisation Chamber detectors
- 28 channels spare in total
- Two HV power supplies on each rack
 - Second PSU is for redundancy

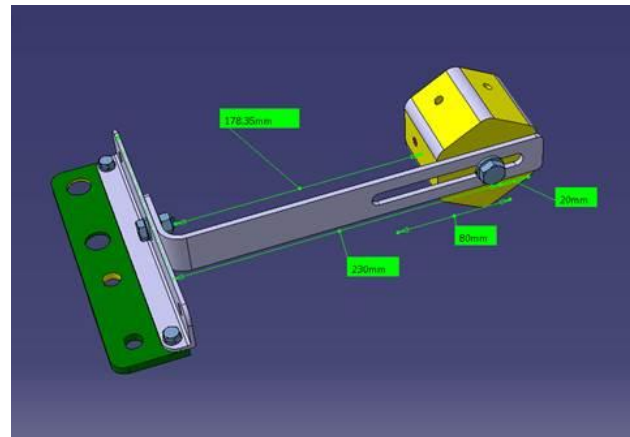


PSB Supports

PS BOOSTER PERIODE 2

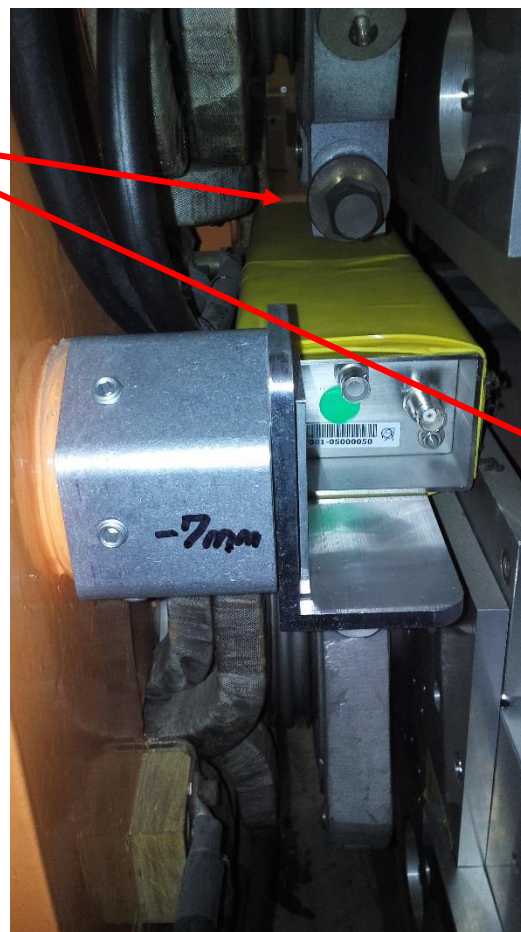
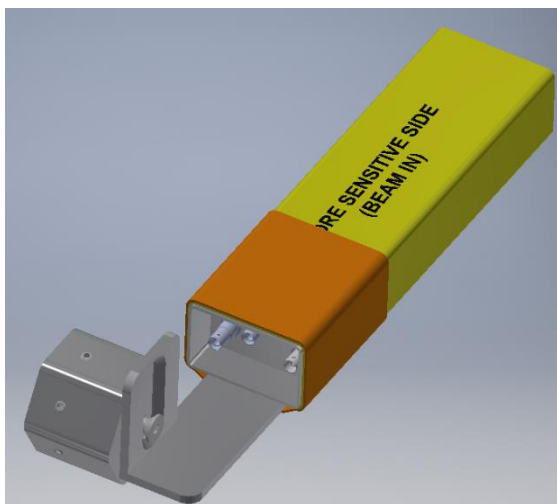


- Detector and cables are attached on the magnet nuts



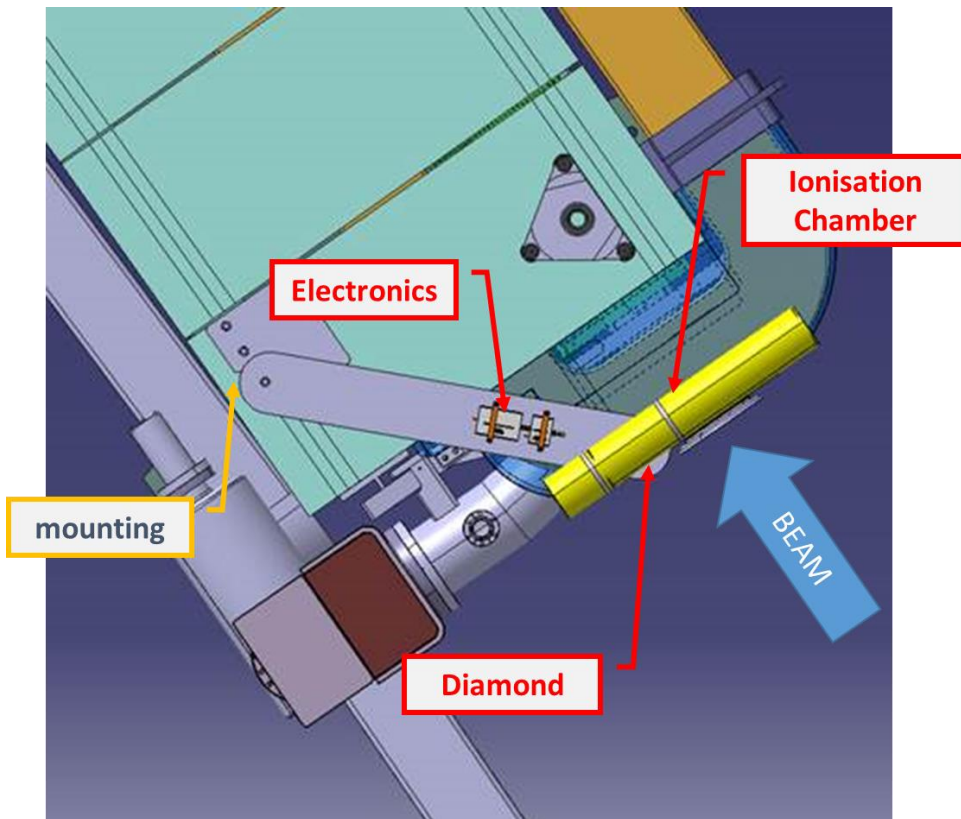
PSB Custom Supports

- Special supports for:
 - BR12.BLMFB.3L3.E
 - BR12.BLMFB.10L3.E
- Non standard installation of the vacuum clamps
 - Not enough space to fit detector
- Need to verify the signal difference



PS Tunnel Installation

- Installation was modified several times to fit and satisfy all requests
 - Mostly issues with cabling and patchcords



Top view



PS Diamond Installation

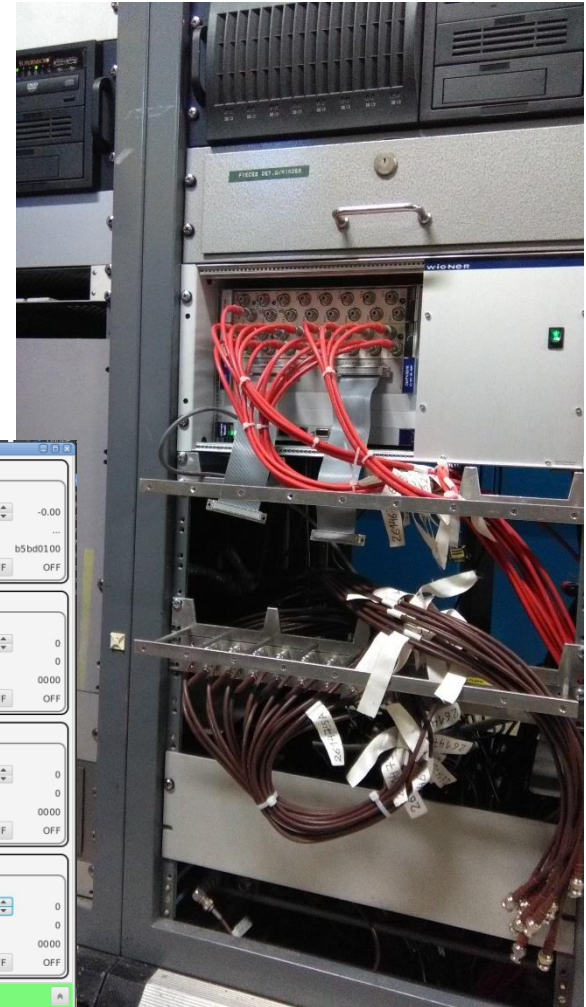
■ Preparation of the installation

- All dBLMs have been equipped with splitters and amplifiers
- Connections done and tested in the lab before deployment



PS Diamond Installation

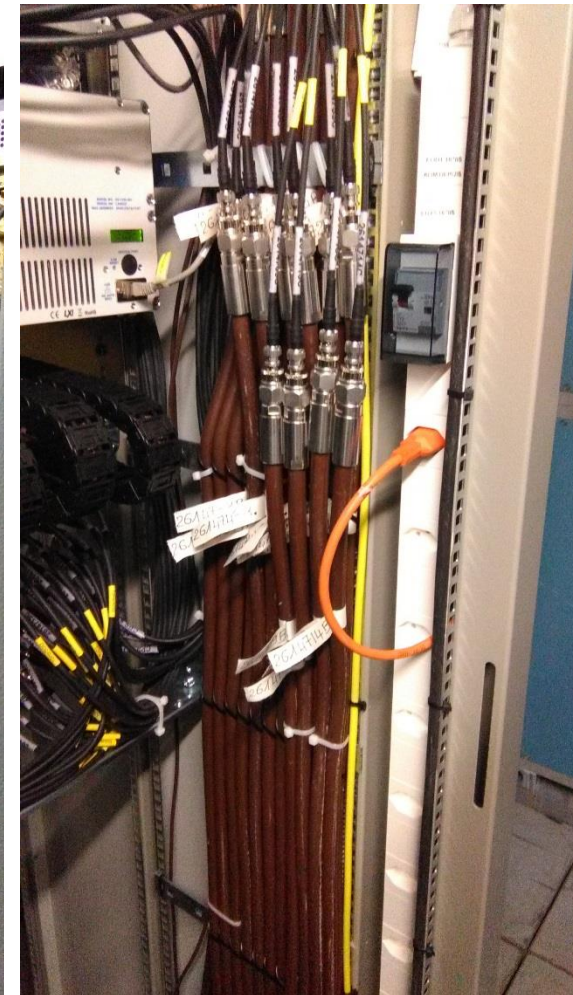
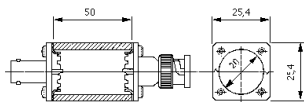
- HV and LV Power supply unit for the Diamond bias and the amplifier
 - Ethernet connection for control
 - FESA class to control and log values is under development
 - OP will have the ability to switch off/on (seems not necessary with the latest info; matrix will terminate input when a channel is not used/digitised)
 - Only Experts will have the ability to set/modify the voltage values



Group	Channel	V [V]	I [A]	Status	ON/OFF
Group 1	PR.BLMD014	500	-0.01	b5b00100	OFF
	PR.BLMD015	500	-0.00	b5c00100	OFF
	PR.BLMD016	500	-0.00	b5c0100	OFF
	PR.BLMD017	500	-0.01	b5c30100	OFF
Group 2	PR.BLMD018	500	-0.00	b5b00100	OFF
	PR.BLMD040	500	0.01	b5c70100	OFF
	PR.BLMD041	500	-0.00	b5b00100	OFF
	PR.BLMD042	500	0.00	b5b70100	OFF
Group 3	PR.BLMD043	500	0.00	b5b30100	OFF
	PR.BLMD044	500	0.02	b5b90100	OFF
	PR.BLMD045	500	0.00	b5a00100	OFF
	PR.BLMD046	500	0.01	b5a90100	OFF
Group 4	PR.BLMD047	500	-0.00	b590100	OFF
	PR.BLMD048	500	-0.00	b5c20100	OFF
	PR.BLMD049	500	0.00	b590100	OFF
	PR.BLMD071	500	0.01	b590100	OFF
Group 5	PR.BLMD075	500	0.00	b5b40100	OFF
	PR.BLMD079	500	0.00	b5c20100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
Group 6	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
Group 7	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
Group 8	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF
	PR.BLMD083	500	0.01	b5c60100	OFF

PS Diamond Installation

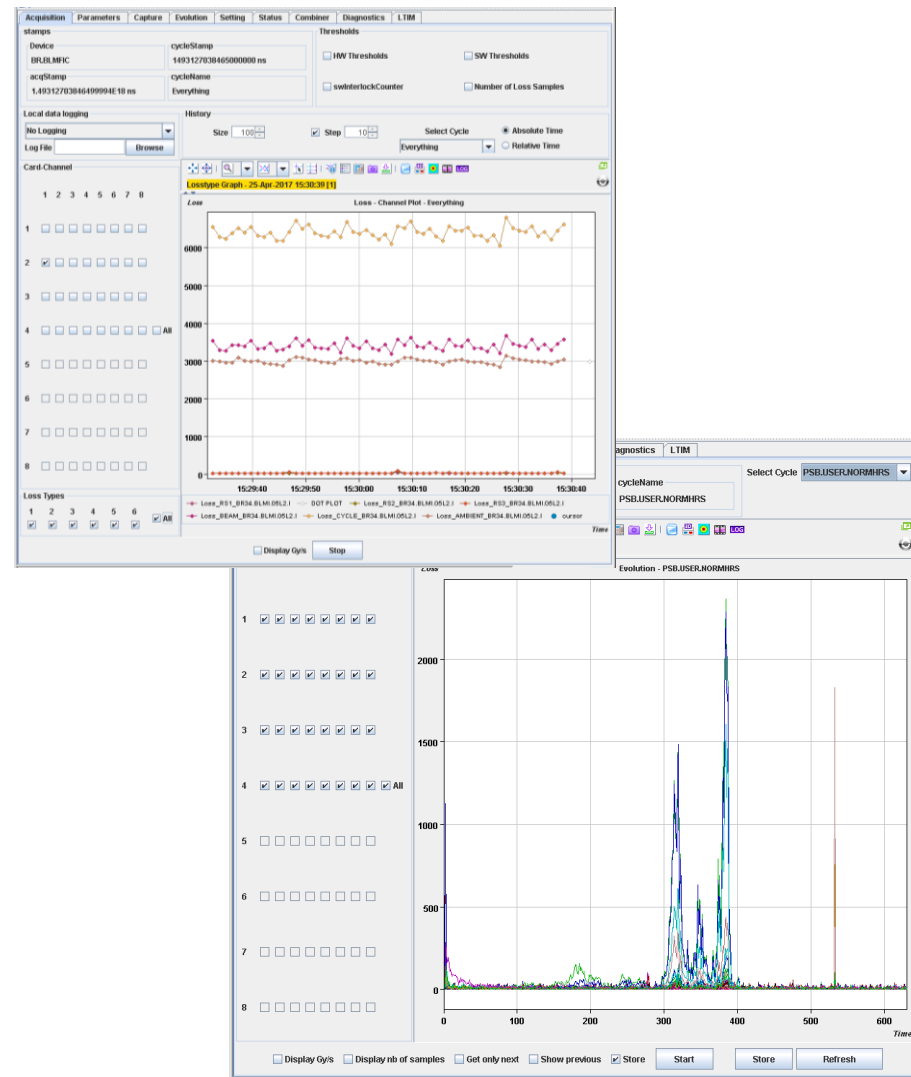
- Signal cables arrive at the OASIS rack
- With adapters and patchcords are connected to the OASIS Matrix
- With another set of patchcords signals arrive to the 4 OASIS Digitisers
- Aim is to intercept the signals before the matrix and add a protection circuit.
 - This will also reduce the adaptors and patchcords used
- Circuit is ready and tested in the lab.
 - A PCB has been designed to fit in a small box and is under production
 - Will have the ability to add attenuation if needed in the future



DEVELOPMENT

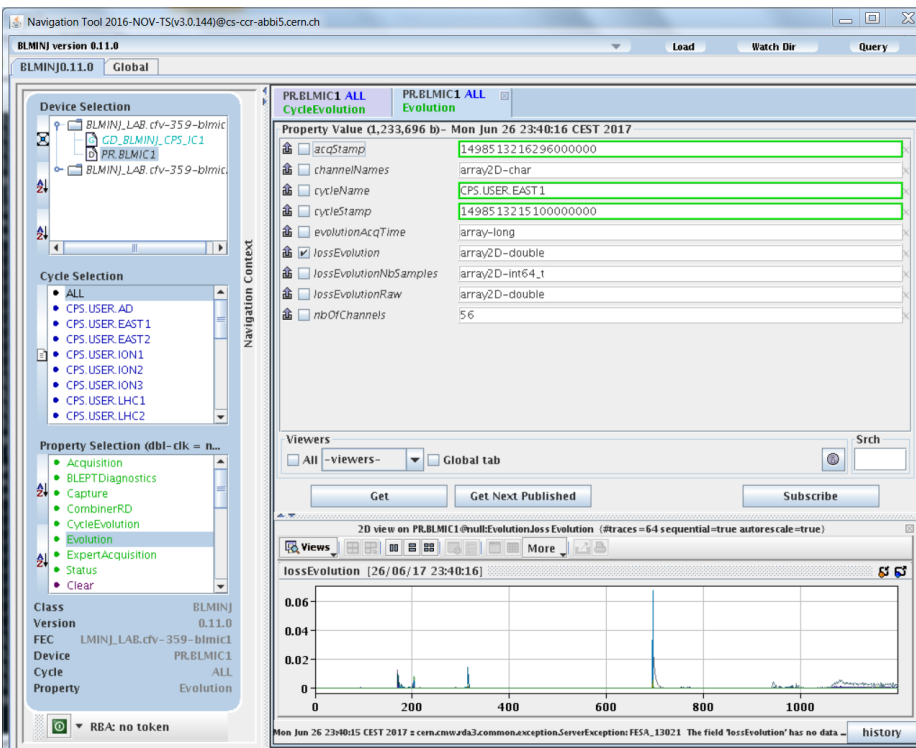
System Development

- Firmware and Software available to stable versions with all major features available.
- Direct Ethernet connection to each acquisition module available for detailed analysis and debugging.
 - 2 μ s samples continuously
- Through FESA class, system provides synchronised with the basic period
 - Several integrals (2 μ s – 1.2 s, BeamPresence and Ambience)
 - 'Evolution' data for the **complete cycle**.
 - Data are 'tagged' with the USER
- Functionalities under verification:
 - loading of settings/thresholds,
 - system status information
- Functionalities to be developed:
 - On-demand **Capture buffer** with 2 μ s samples

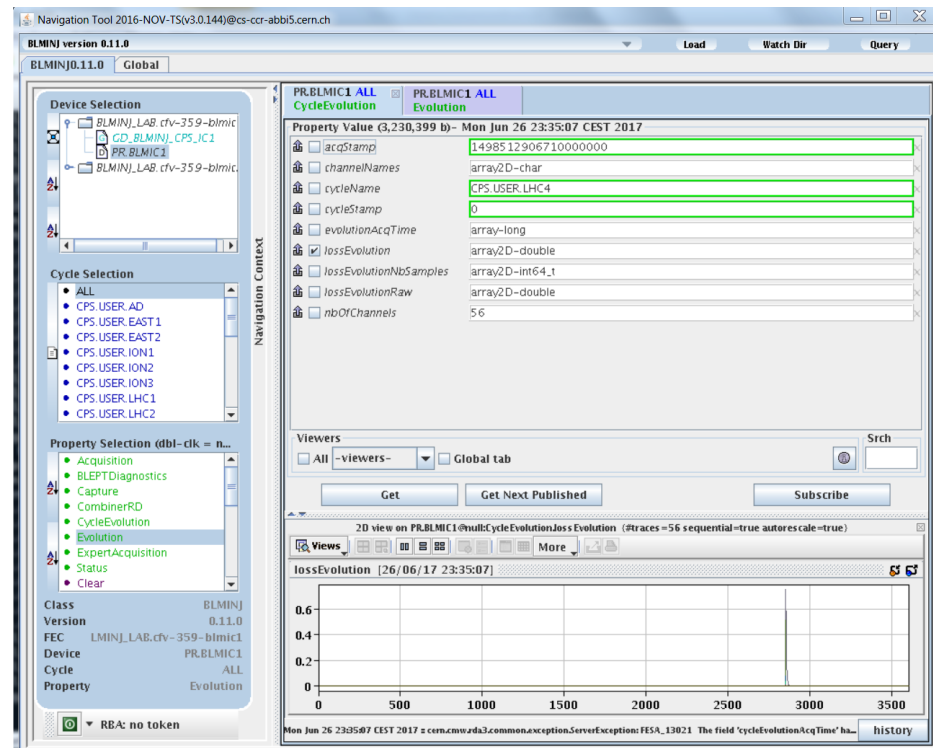


PS Evolution Buffer

- Firmware: double buffer at the FPGA
 - One records when the other transmits
 - Toggle operation with basic period
 - No blind time
- Software: two properties from FESA
 - Data per basic period
 - Data per cycle
 - Units: Gy/s or bits



per Basic Period



per Cycle

System Diagnostic Data [1/3]

BLMExpertGUI2

File Configuration Help

GD_00000000000000000000000040790

Devices

BRBLMFC

Acquisition Parameters Capture Evolution Setting Status Combiner Diagnostics LTIM

General Analog SFPs Graph IL BLEDP IL BLEPT Misc RAW

BLEDP

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
FW Version	0x1612070a	0x1612070a	0x1612070a	0x1612070a	0x00000000	0x00000000	0x00000000	0x00000000
Chip ID	0x600000177f254001	0x290000177f374601	0x70000177f38f001	0x900000177f24f101	0x0000000000000000	0x0000000000000000	0x0000000000000000	0x0000000000000000
Geo Address	0x101	0x110	0x111	0x1000	0x0	0x0	0x0	0x0
Temperature	31.25 °C	32.2 °C	30.68 °C	28.58 °C	0 °C	0 °C	0 °C	0 °C
Humidity	29.96 %	25.33 %	28.67 %	30.9 %	0 %	0 %	0 %	0 %

BLEPM

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
FW Version	0x1612060c	0x1612060c	0x1612060c	0x1612060c	0x00000000	0x00000000	0x00000000	0x00000000
Chip ID	0x9a000018ca59ce01	0xe1000018ca922e01	0xea000018ca5ba01	0xf0000018ca464a01	0x0000000000000000	0x0000000000000000	0x0000000000000000	0x0000000000000000
Temperature	30.86 °C	29.91 °C	27.32 °C	25.48 °C	0 °C	0 °C	0 °C	0 °C
Humidity	25.95 %	26.73 %	30.9 %	34.99 %	0 %	0 %	0 %	0 %

DAB64x

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
FW Version	0x1612060a	0x1612060a	0x1612060a	0x1612060a	0x00000000	0x00000000	0x00000000	0x00000000
Chip ID	0xb0000010595a4401	0xb000001059484f01	0xc0000010595bbe01	0x280000105980a301	0x0000000000000000	0x0000000000000000	0x0000000000000000	0x0000000000000000
Geo Address	0x4	0x5	0x6	0x7	0x0	0x0	0x0	0x0
Temperature	26.12 °C	26.81 °C	25.81 °C	24.56 °C	0 °C	0 °C	0 °C	0 °C

Stop

- System information: firmware version, card serials, temperature and humidity

System Diagnostic Data [2/3]

BLMINExpertGUI2

File Configuration Help

cfv361-bimfmc

Global Device: GD_00000000000000000000000040790

Devices: BRBLMFC

Acquisition Parameters Capture Evolution Setting Status Combiner Diagnostics LTIM

General Analog SFPs Graph IL BLEDP IL BLEPT Misc RAW

BLEDP SFP1

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
Serial Number	FTB140918061	FTB140918064	12061020	FTB140918072				
Part Number	FT3A05D	FT3A05D	FT3A05D	FT3A05D				
Temperature	37.31	37.97	41.66	32.66				
VCC	3287.2	3307.2	3251.2	3281.2				
TX Power	233.6	189.6	506.4	214.4				
RX Power	179	233.1	225.1	166.2				
TX Bias	16336	9200	10608	10240				
Warnings								

BLEDP SFP2

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
Serial Number								
Part Number								
Temperature	0							
VCC	0							
TX Power	0							
RX Power	0							
TX Bias	0							
Warnings								

BLEPM SFP1

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
Serial Number	FTB16111024	FTB16111023	FTB16111022	FTB16111021				
Part Number	FT3A05D	FT3A05D	FT3A05D	FT3A05D				
Temperature	30.16	30.59	31.39	30.59				
VCC	3275.2	3272.8	3270.4	3275.2				
TX Power	205.6	234.4	264.8	240				
RX Power	178.3	234.3	409.5	187.2				
TX Bias	12016	11984	12080	12160				
Warnings								

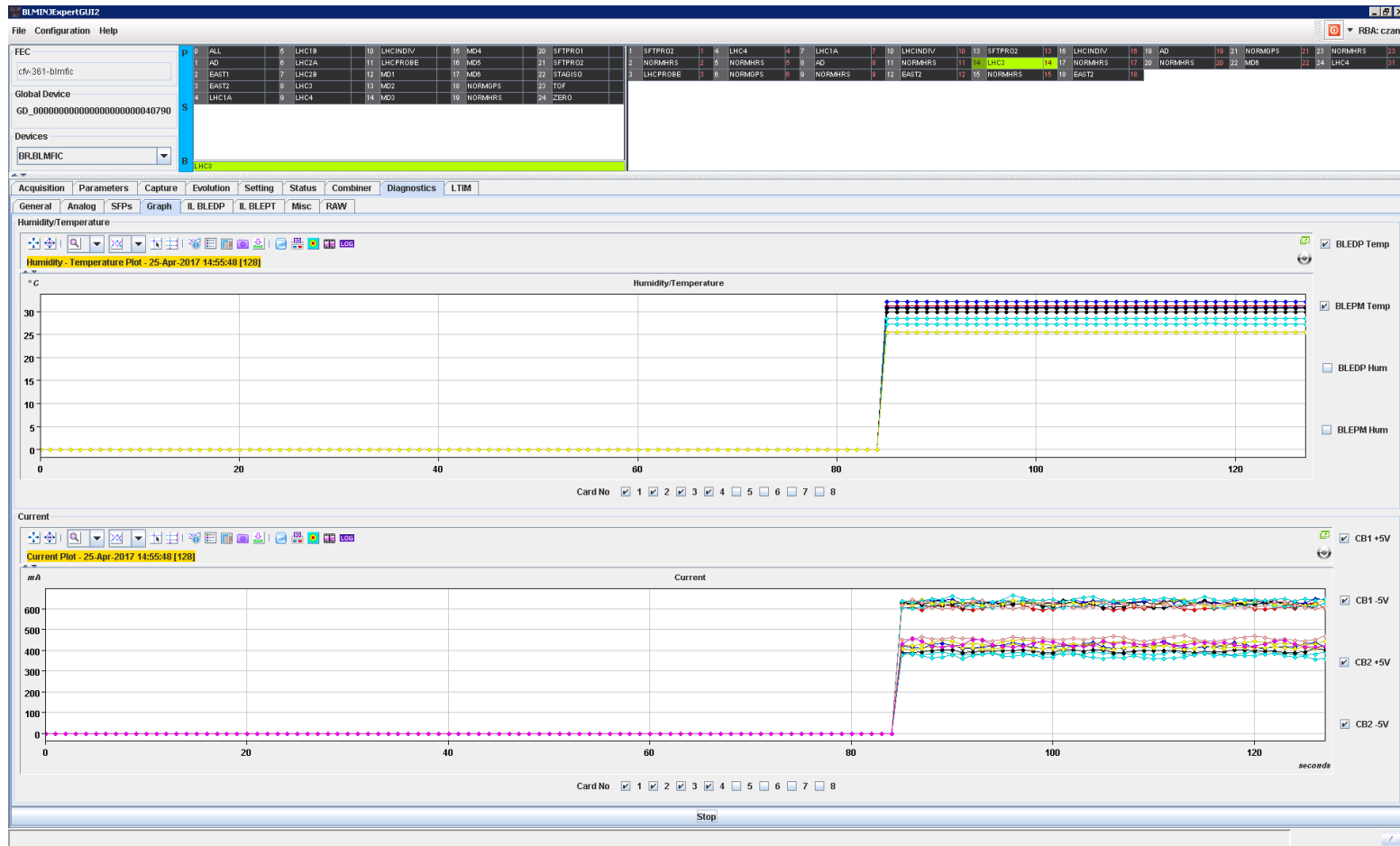
BLEPM SFP2

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
Serial Number								
Part Number								
Temperature	0							
VCC	0							
TX Power	0							
RX Power	0							
TX Bias	0							
Warnings								

Stop

System information: Optical links performance

System Diagnostic Data [3/3]



■ System information: power supplies and rack conditions

Parameters Setup

The screenshot displays the BLMINExpertGUI2 software interface, specifically the Parameters Setup window. The window is organized into several functional areas:

- ChannelRelated:** A table with 8 columns (ChannelNumber 1-8) and 5 rows (ChannelName: RS1, RS2, RS3, BEAM, CYCLE). Buttons for 'Copy' and 'Paste' are located to the right.
- Capture:** Includes a 'Capture Start Time' input field and a 'Select' table with checkboxes for channels 1-8 and 'All'.
- Interlock:** Features a 'Mask' row with checkboxes and a 'BIS Select' row with dropdown menus for each channel.
- General:** Contains fields for 'FWVersion', 'Chip ID', and 'Temperature Threshold (°C)'. It also has sub-sections for SFP1 and SFP2, each with 'Temperature Threshold (°C)' and 'Power Threshold (°C)' fields.

Buttons for 'Read All', 'Set All', and 'Set' are positioned at the bottom of the General section.

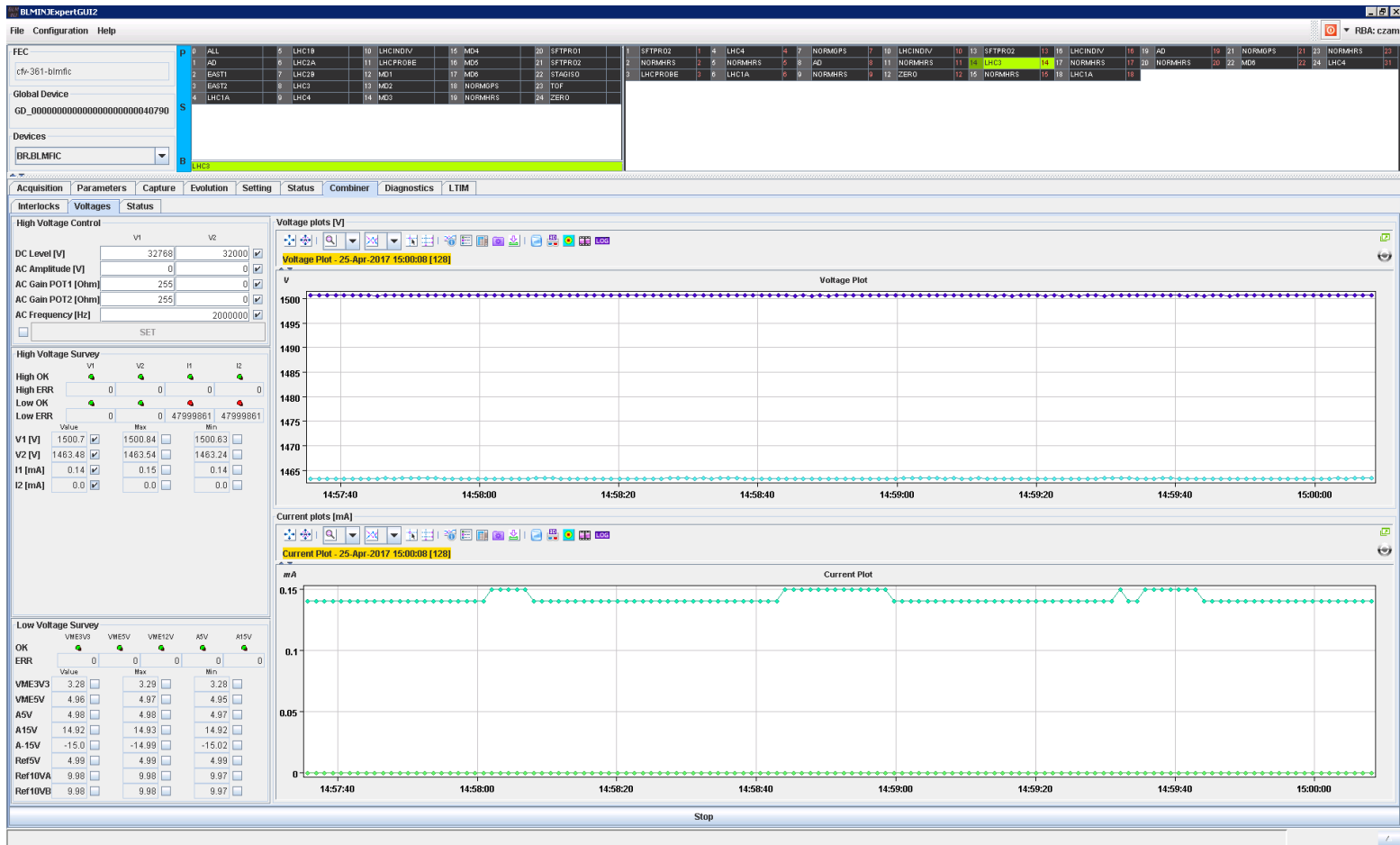
- Channel names, Threshold values, masks, BIS outputs

Beam Interlocks [1/3]

The screenshot displays the BL-MIN3ExpertGUI2 interface. At the top, there is a menu bar with 'File', 'Configuration', and 'Help'. Below the menu is a table of interlock configurations with columns for channel numbers and device names. A 'Global Device' section shows 'GD_000000000000000000000000000040790'. The main window is divided into several sections: 'Interlocks' with 'Voltages' and 'Status' tabs; 'CIBU status' showing two channels with green bars; 'Hardware Interlocks' with 'Clear channel 1' and 'Clear channel 2' buttons; 'Software Interlock' with a grid of 32 columns (0-31) and 4 rows (User played, Channel 1, Channel 2) containing status icons; and 'Software watchdog' with input fields for 'Time to interlock (ms)' (2207), 'Watchdog timeout (ms)' (2400), and a 'Set watchdog timeout (ms)' button. A 'Stop' button is located at the bottom center.

- State of the interlock outputs (software and firmware produced)

Beam Interlocks [2/3]



■ Power supply control and survey

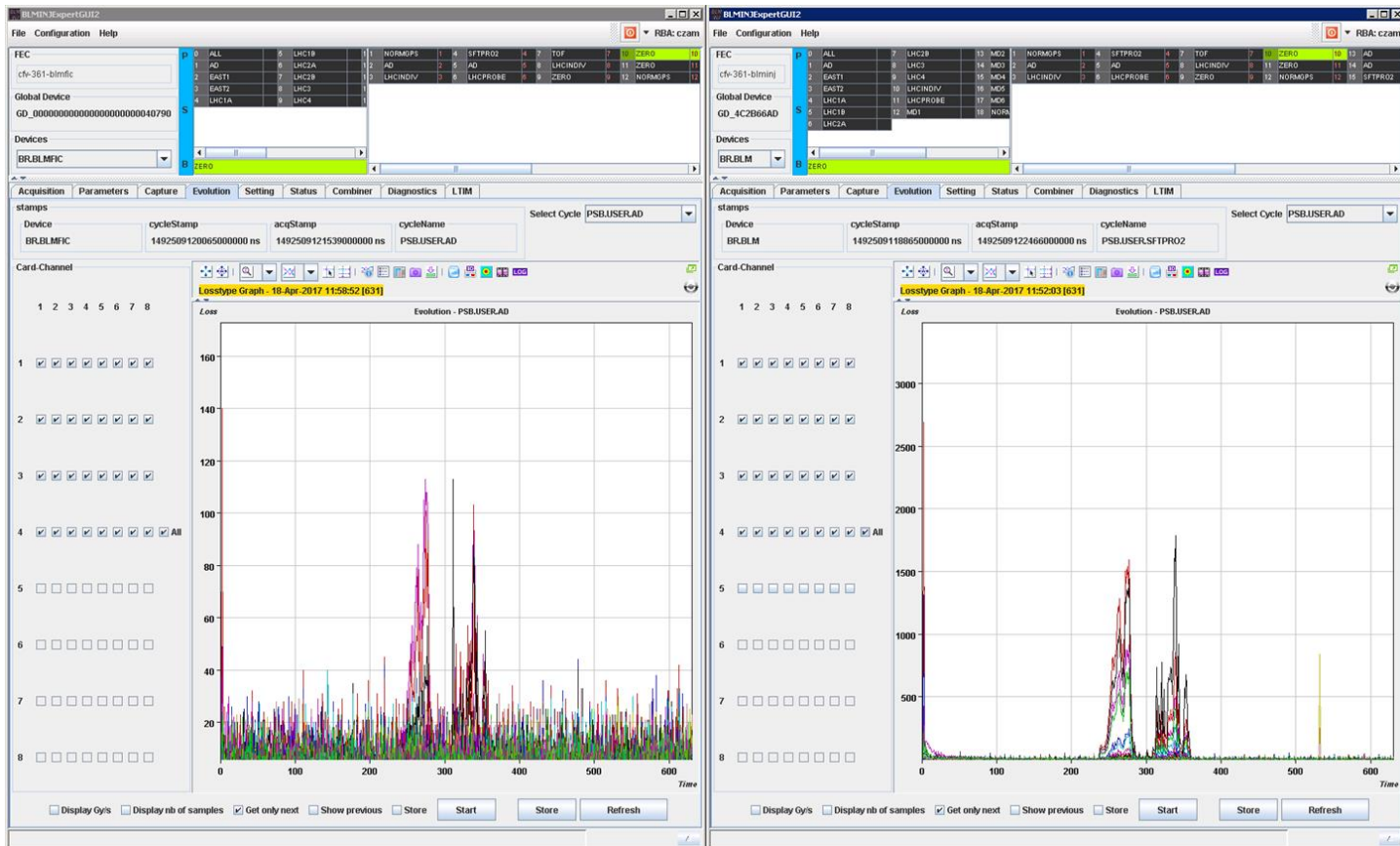
Beam Interlocks [3/3]

The screenshot displays the BL-MIN3ExpertGUI2 software interface. At the top, there is a menu bar with 'File', 'Configuration', and 'Help'. Below the menu bar is a table with columns for device names and IDs. The table is divided into two sections, 'S' and 'B'. The 'S' section lists devices like ALL, AD, EAST1, and LHC1A. The 'B' section lists devices like LHC1B, LHC2A, LHC2B, LHC2, LHC3, LHC4, LHC1A, LHC4, LHC3, and ZERO. Below the table, there is a 'Global Device' field with the value 'GD_0000000000000000000000000040790'. A 'Devices' dropdown menu is set to 'BRBLMFC'. The main window has tabs for 'Acquisition', 'Parameters', 'Capture', 'Evolution', 'Setting', 'Status', 'Combiner', 'Diagnostics', and 'L.TIM'. The 'Combiner' tab is active, showing 'Combiner Info' and 'Timing Info'. The 'Combiner Info' section includes fields for Board ID (0x6500000E32202C01), FW date (30082016), FW time (1049), and Temperature (22.87). The 'Timing Info' section includes Basic period [us] (1199986), Beam in [us] (272999), and Beam out [us] (904997). At the bottom of the window, there is a 'Stop' button.

- Timing distribution survey in the crate

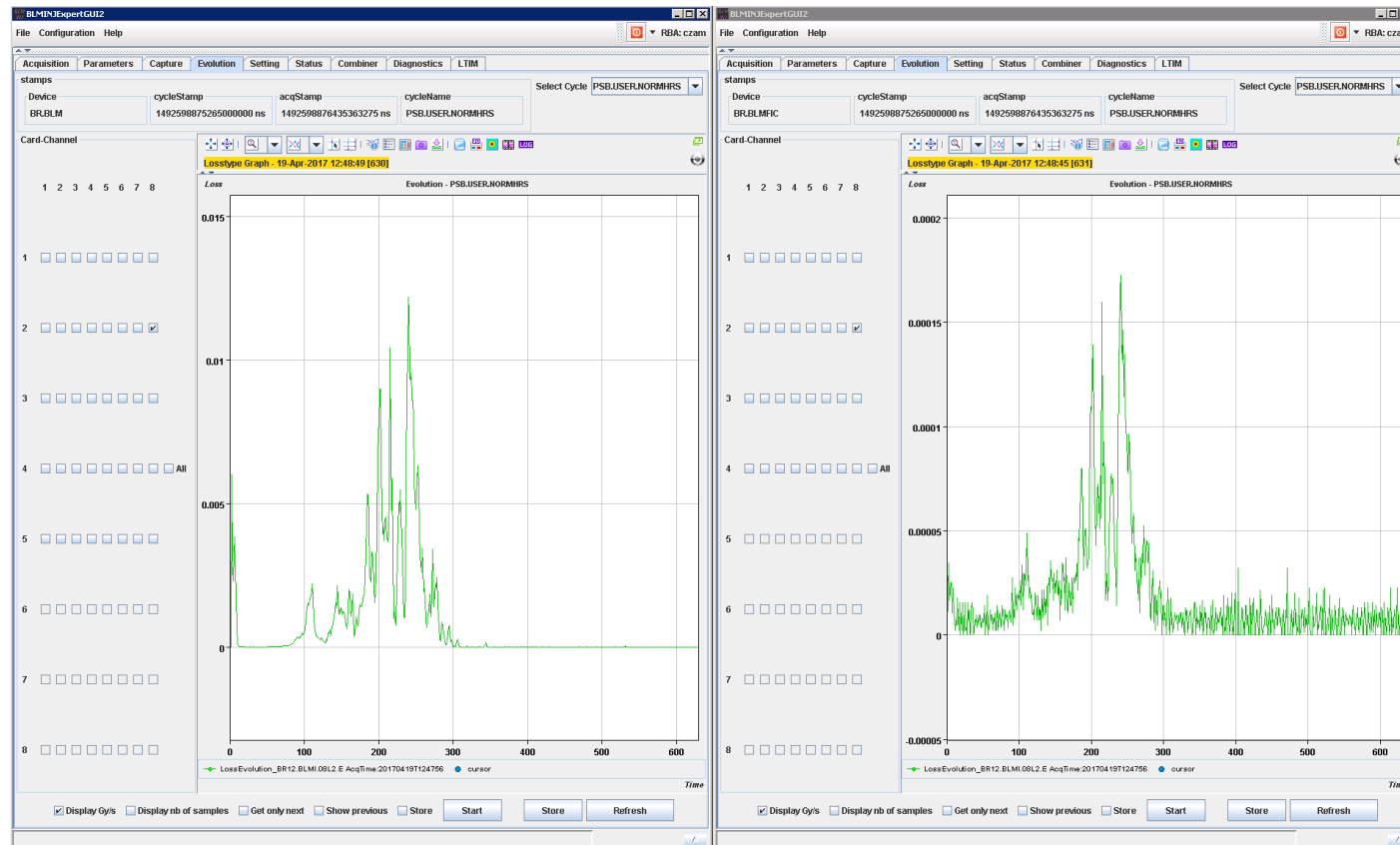
BEAM MEASUREMENTS

PSB First Measurements [1/2]



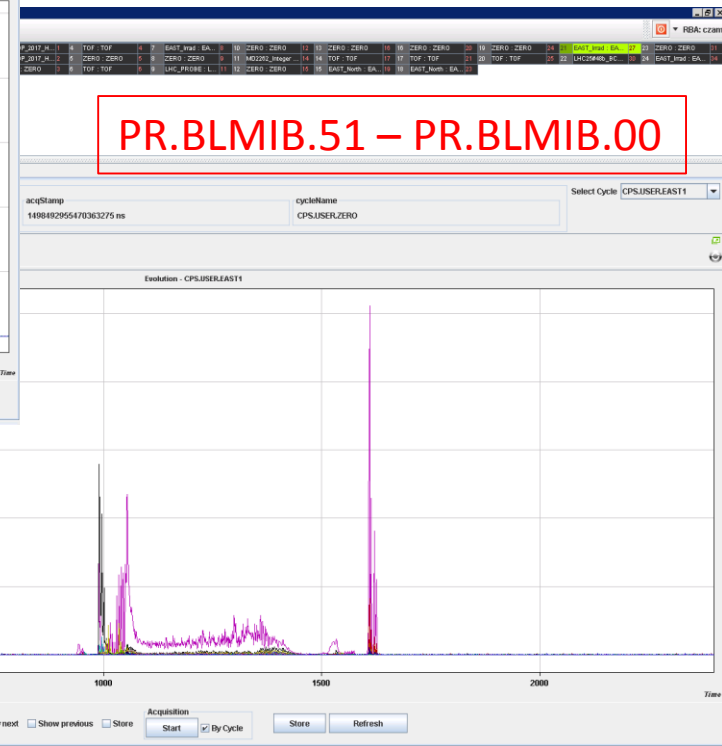
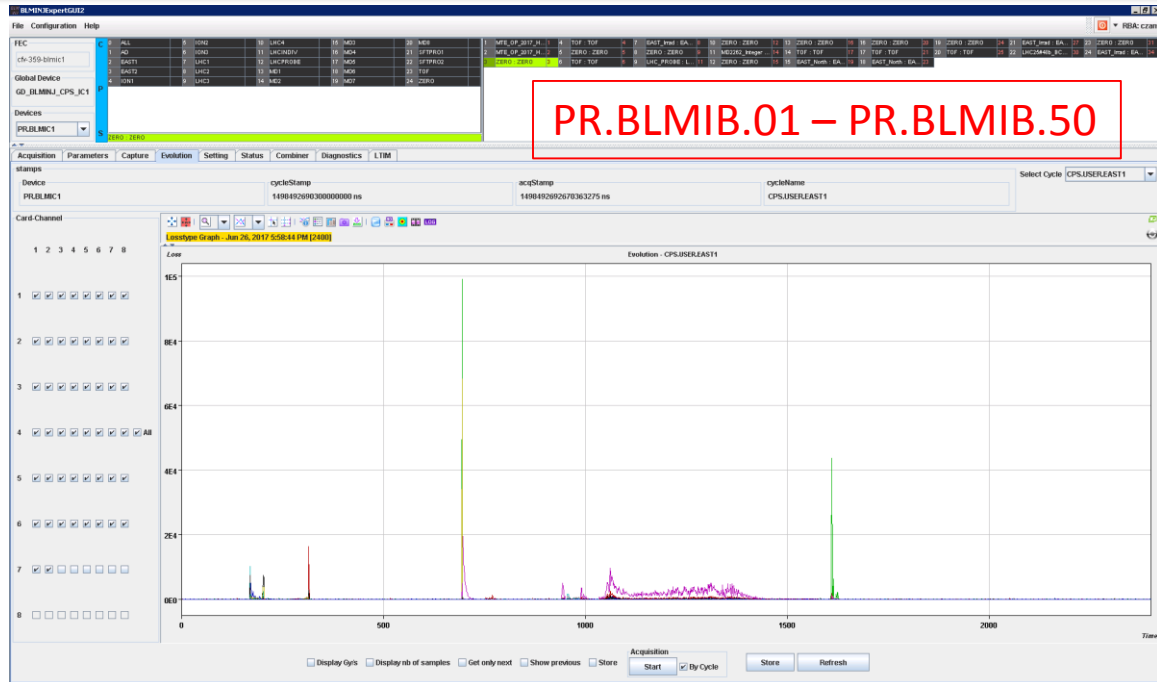
■ All channels operational

PSB First Measurements [2/2]



- Pattern of losses seems identical in most locations
- More noise visible since much smaller signal to measure

PS First Measurements [1/3]



■ All channels operational, no significant noise issues

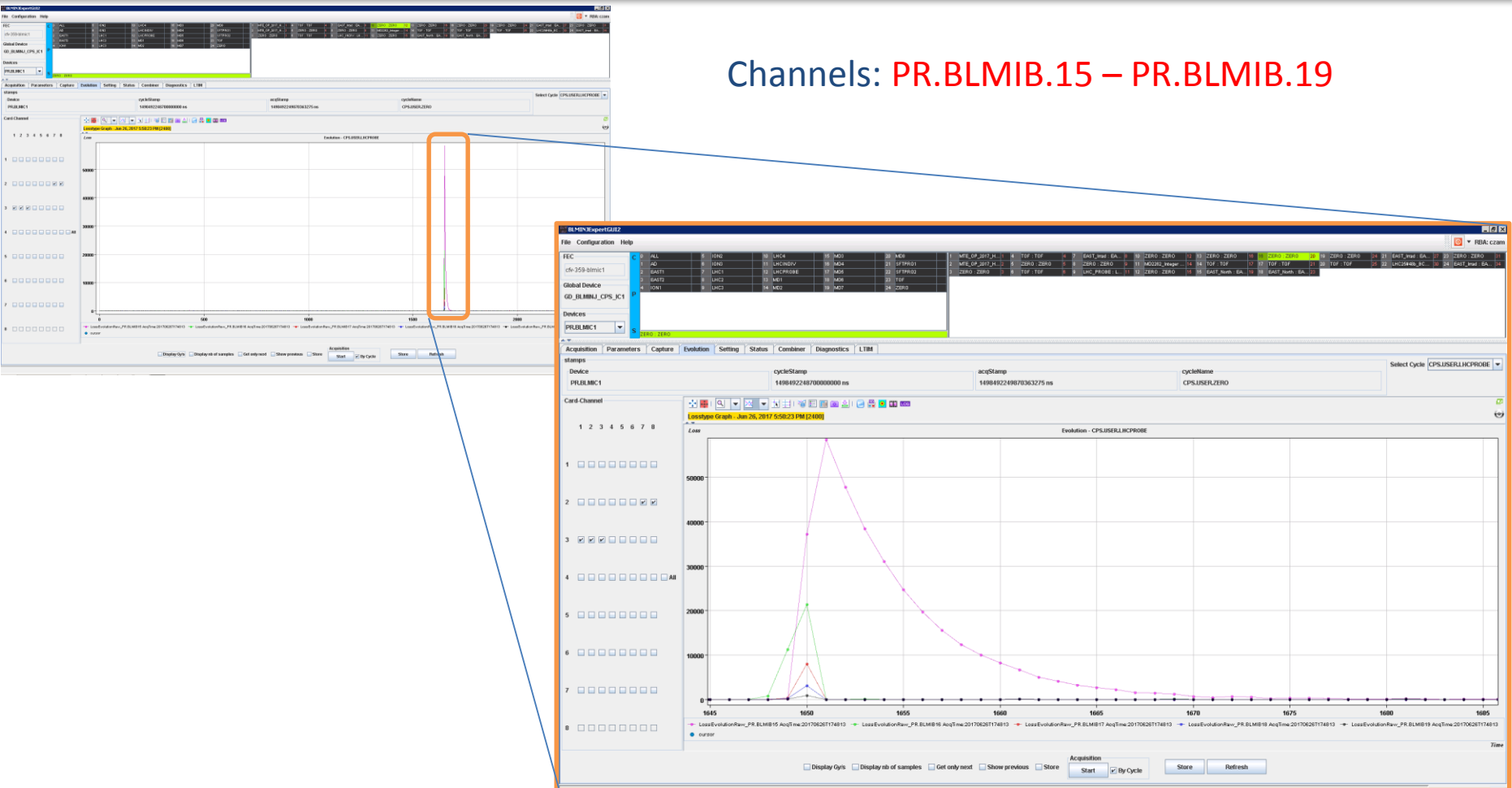
PS First Measurements [2/3]



■ Length of Evolution buffer adjusts automatically based on the user

PS First Measurements [3/3]

Channels: PR.BLMIB.15 – PR.BLMIB.19



■ Zoom in: extraction of an LHC PROBE

NEXT STEPS & SUMMARY

TODO List

- Add in LAYOUT DB the configuration
 - Surface and tunnel installations
- Request data logging
 - ~~Measurements (Running Sums & Evolution buffer)~~
 - System Diagnostic and Monitoring
 - Threshold values (on change)
- Add the OASIS server for the Evolution buffer data
- Setup Threshold DB (InCA)
 - Connect to the update property
- Update electronics with the final versions
 - Acquisition electronics during YETS
 - Processing electronics during LS2

Summary

- **PSB**: Installation of 32 FIC detectors completed despite serious integration issues. In addition, 16 spare cables added around the ring.
- **PS**: Two complete systems with 134 channels have been produced, assembled and deployed under strict and short deadline
 - Original plan for both was LS2 (after decabbling)
 - Solution was only found few months before EYETS
 - After cabling campaign very short period given to check for errors
- **All** connections and installations were done correctly and on-time
 - During the whole cabling campaign at least one person was next to the cabling installation teams
- **BLMINJ** system: Firmware and Software are ready for the Validation and Commissioning steps
- **dBLM/OASIS** system:
 - All amplified channels are already connected to OASIS. Finally, good decision to go for this as many channels will need it.
 - For the non-amplified channels a protection circuit has been prepared tested.
 - Priority was given to 15 & 16 locations in June (w/ handmade versions)

Installations, hardware, firmware

FUTURE DEVELOPMENTS

BLMINJ Installation Status

Machine/Area		Channels	Cables	Detector Type	Status
PSB	Ring (L2 position)	32	80	LHC-IC	Completed (LS1)
	Injection & BI line	11	22	LHC-IC	LS2
	Injection (observation)	8	40	Diamond	LS2
	Ring (L3 position)	32	80	FIC	Completed (EYETS)
	Extraction	25	60	LHC-IC	LS2

Machine/Area		Channels	Cables	Detector Type	Status
PS	Ring	100	200	LHC-IC	Completed (EYETS)
	Ring (observation)	17	85	Diamond	Completed (EYETS)
	Transfer Lines	51	102	LHC-IC	LS2

Machine/Area		Channels	Cables	Detector Type	Status
SPS	TT10	30	60	LHC-IC	LS2

- Total copper cable length installed: **40 km** (PSB) + **58 km** (PS)
- Expected:
 - 11 km (PSB)
 - 4 km multiwire with **signal and HV boxes** + xx km (PS/SPS TL)

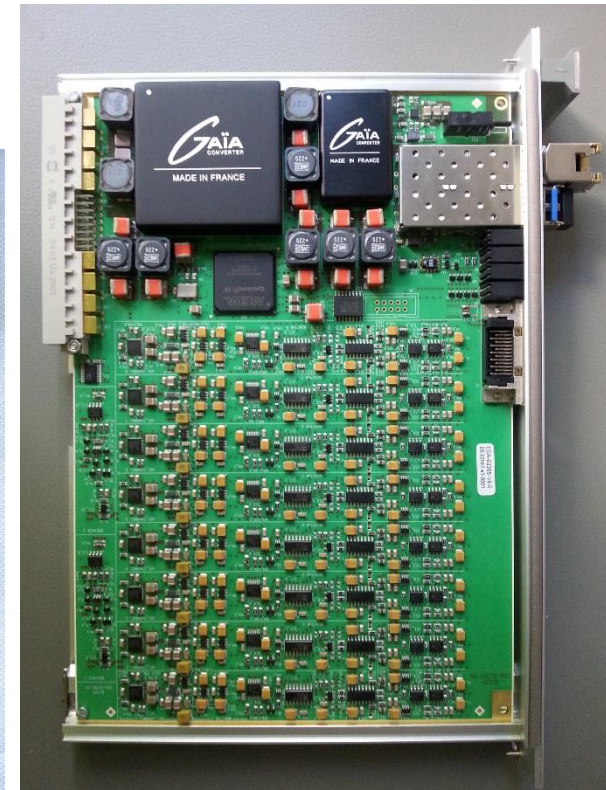
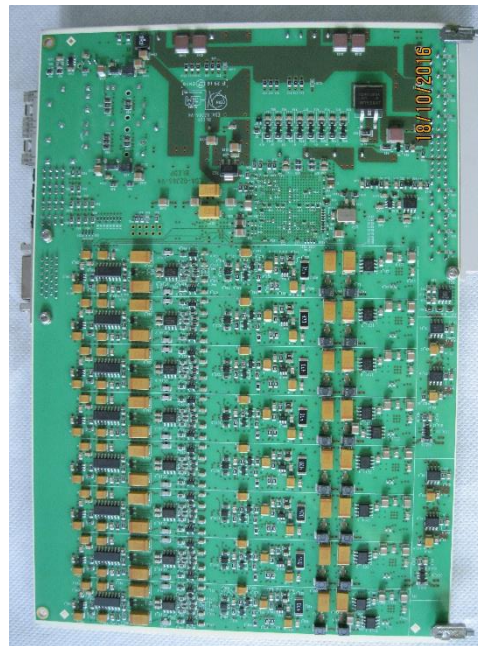
BLEDP series production

Series production of has just been received
55 acquisition modules

■ Next weeks:

- Visual inspection
- Programming
- Verification

YETS: Upgrade PS installation
LS2: new installations



Control & Survey Card Upgrade

Upgrade of the control and survey card by a remotely controlled version.

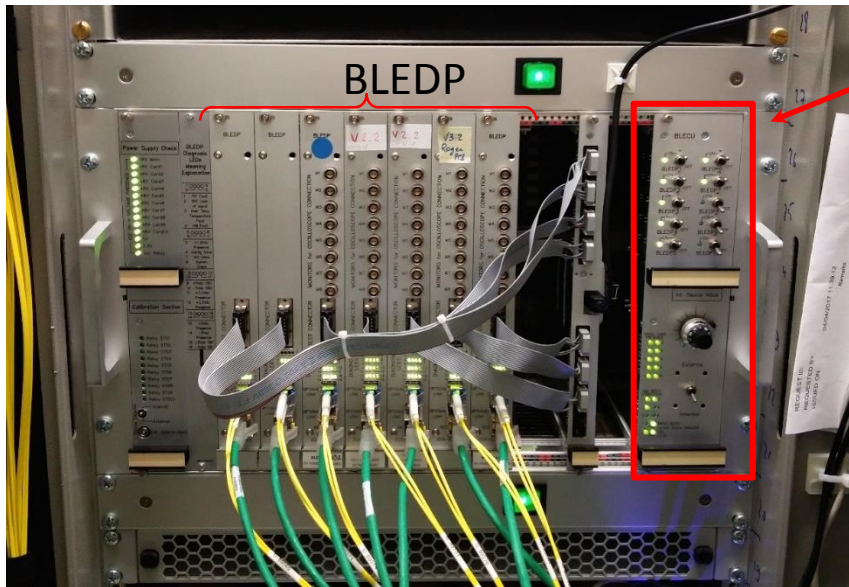


Photo with manual BLECU version

Remotely execute and control the

- calibration procedure and
- tests of the BLEDP cards
 - An embedded current source can be switched on and modulated to measure (almost) the full acquisition chain response of every channel.

Survey several parameters

- the power status of the crate and cards, temperature, humidity, etc.

FW spec (review on going)

FW design

FW prototype

Starting lab tests

Series

installation

2017

2018

2019

HW design

HW

prototype

Series

components
refurbishing

Series

production

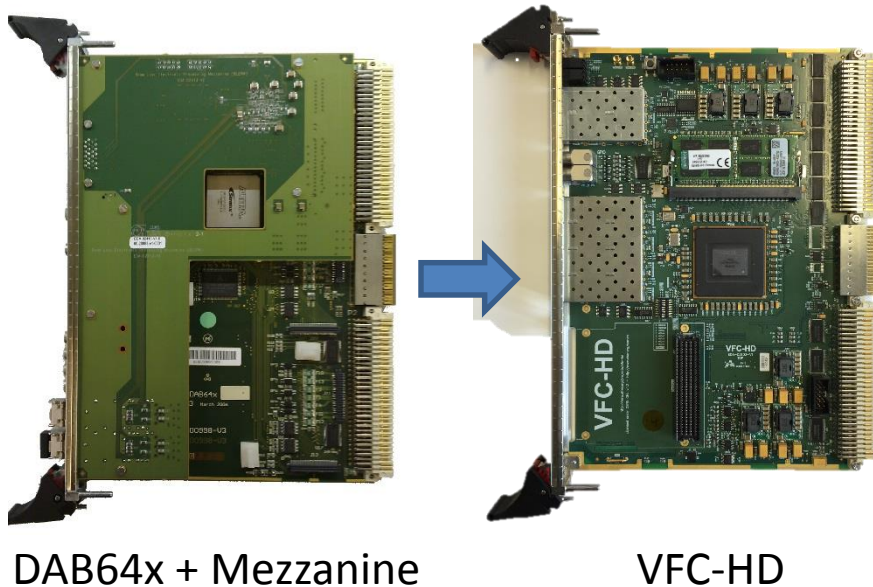
Series

Test & validation

HW specs

Processing Module Upgrade

Upgrade the processing module to the VFC carrier



Common module for all BLM systems

Porting has started

- Working parts:
 - VME bus + GA
 - SCT, BLT and MBLT
 - Temperature
 - Serial number
 - LEDs
- Next:
 - I2C expander
 - SFPs (optical and Ethernet)
 - DDR3 (not needed)

Needed for installation during LS2

Firmware development

- Remote update through FESA server
 - First version deployed during last TS
- Automatic switching of the two acquisition methods
 - Needs lots of testing to choose best method
- Integration of the Connectivity Check
- Expose as settings the different configurations per machine
 - Currently hardcoded and each machine needs its own firmware compilation
- Implement the Capture Buffer

Thank you