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Transformation and perspectives of digital superconducting electronics (lessons learned)

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A. Kirichenko, I. Vernik, D. Yohannes, I. Nevirkovets, T. Filippov, D. Amparo, M. Miller, A. Jafari Salim, P. Truitt, J. Vivalda, M. Kamkar, J. Walter, M. Renzullo, D. McAllister, O. Chernyashevskyy, C. Fourie, M. Volkmann, V. Semenov, A. Fujimaki and team, N. Yoshikawa and team, T. Ohki and team, P. Shevchenko, G. Gibson and team, S. Rylov, S. Benz and team, L. Johnson, S. Tolpygo, K. Berggren and team, M. Manheimer, S. Holmes

Transformation: Lessons Learned



From ~2011, superconducting electronics is experiencing a transformation:

- New devices are brought in and being integrated (magnetic devices, nanowires, etc.) to address hard problems of conventional Josephson electronics.
- New fabrication processes relying on chemical mechanical polishing are introduced.
- New memory ideas,
- New design tools.

Lessons Learned:

➤ Digital technology

- RSFQ to post-RSFQ
- Energy-efficient classical computing, QC control layer, neuromorphic circuits

➤ CAD tools

- NioCAD story
- PSCAN2 vs Spectre (\$70K vs 1M)- focused work vs simple adaptation
- Parameter extraction: L-meter replaced by InductEx
- Cell Libraries (Lego, Flex)
- Timing (Global vs Wave-pipelined)

➤ Memory

- JJ RAM to MRAM
- Physics/MatScience vs Engineering

Cryogenic Computing Complexity (C3)

- Approach based on:

- *Near-zero energy* superconducting **interconnect**
- *New SFQ logic* with no static power dissipation
- *New energy efficient* cryogenic **memory** ideas
- **Electrical or optical** inputs and outputs
- **Commercial** cryogenic refrigerators

**IARPA C3
program basis**



- **Logic thrust:** IBM team, NGES
- **Memory thrust:** Raytheon BBN team, NGES team
- **Gov. teams:** MIT-LL (fab), NIST (test verification), Sandia (failure analysis)



Manheimer, M.A., "Cryogenic Computing Complexity Program: Phase 1 Introduction," *IEEE Transactions on Applied Superconductivity*, vol.25, no.3, June 2015.

D. S. Holmes, A. L. Ripple, M. A. Manheimer, "Energy-efficient superconducting computing – power budgets and requirements," *IEEE Trans. Appl. Supercond.*, vol. 23, Jun. 2013.

➤ Digital technology

- RSFQ to post-RSFQ
- Energy-efficient classical computing, QC control layer, neuromorphic computing

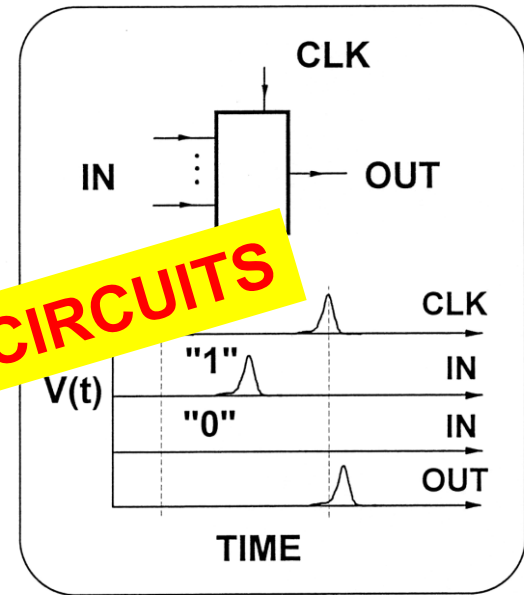
RSFQ has been a workhorse for last 20 years



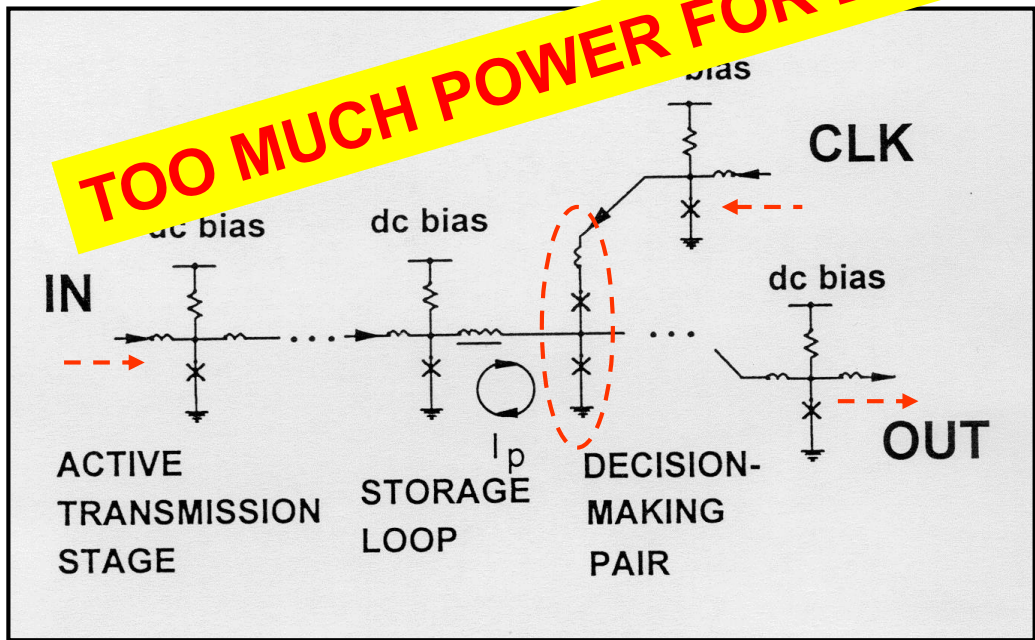
RSFQ - Rapid Single Flux Quantum (from late 80s) (also called SFQ - Single Flux Quantum logic)

Both Data and Clock are SFQ voltage pulses $V(t)$
with quantized areas

$$\int V dt = \Phi_0 = h/2e = 2.07 \text{ mV} \cdot \text{ps}$$



TOO MUCH POWER FOR LARGE SCALE CIRCUITS



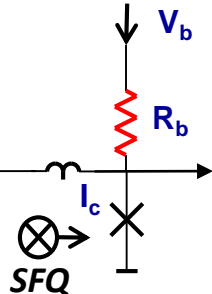
- 750 GHz digital frequency divider demonstrated
- internal memory
- gate-level pipelining
- high-throughput
- low switching power
- dc bias only
- local timing
- amendable for synchronous and asynchronous schemes

Static and Dynamic Power Dissipation

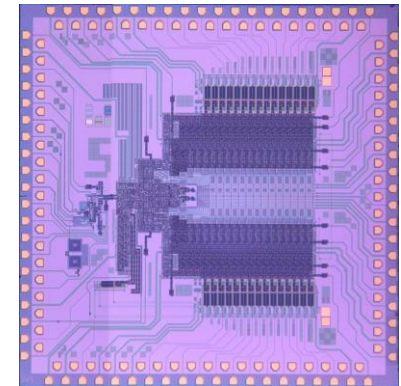


- In conventional RSFQ, **static power dissipation P_S** in bias resistors is dominant.
- However for low complexity integrated circuits (ICs) with $\sim 1,000$ gates, this was not a problem
- P_S will be a problem for high complexity ICs relevant for classical computing applications (such as supercomputers)
- P_S will be a problem for mK ICs needed for Quantum Computing applications

Conventional RSFQ

$$P_S = I_b V_b$$
$$I_b \sim \frac{3}{4} I_c$$
$$P_D = I_b \Phi_0$$


$P_S \gg P_D$



*Hypres Digital-RF
receiver
(~1000 gates)*

$$P_D \sim \frac{3}{4} \Phi_0 I_c \sim 2 \times 10^{-19} \text{ Joule}$$

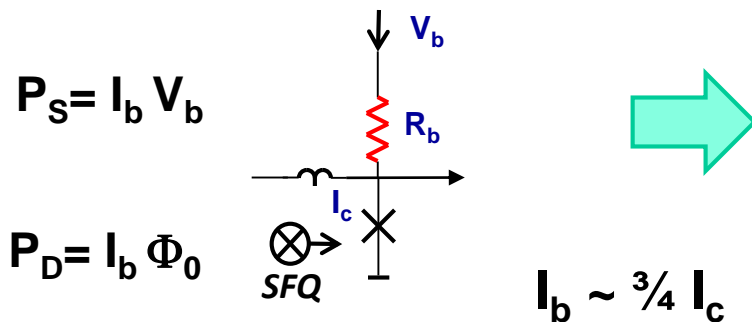
P_S is the problem

Energy-Efficient SFQ Logic

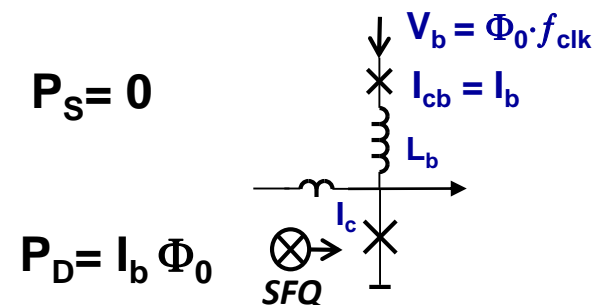


- Many new post-RSFQ logics: ERSFQ, eSFQ, RQL, LV-RSFQ, AQFP
- We focus here on ERSFQ (adaptive JJ phase balancing) and eSFQ (synchronous phase balancing)
- ERSFQ and eSFQ achieve the fundamental SFQ energy dissipation related to magnetic flux crossing Josephson junction $E_{\text{SFQ}} \sim I_{\text{bias}} \Phi_0 \sim 10^{-19}$ Joule
 - Eliminates static dissipation from bias resistors (dominating dissipation)
- Retains all advantages of conventional RSFQ:
 - dc-powered, amenable for serial biasing to reduce total dc bias current
 - ballistic interconnects (no extra power for integrate connections)
 - high speed operation (can work at 100s of GHz)
 - largely preserves already developed cell libraries

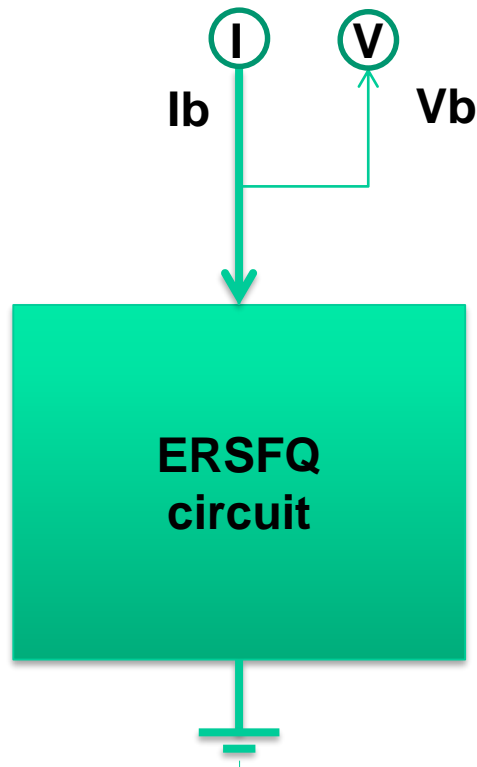
Conventional RSFQ



ERSFQ



Power Dissipation in ERSFQ/eSFQ



Dissipated energy per one clock period:

$$E = \int_0^T I(t) \cdot V(t) \cdot dt = I_b \cdot \int_0^T V(t) \cdot dt = I_b \cdot \Phi_0$$

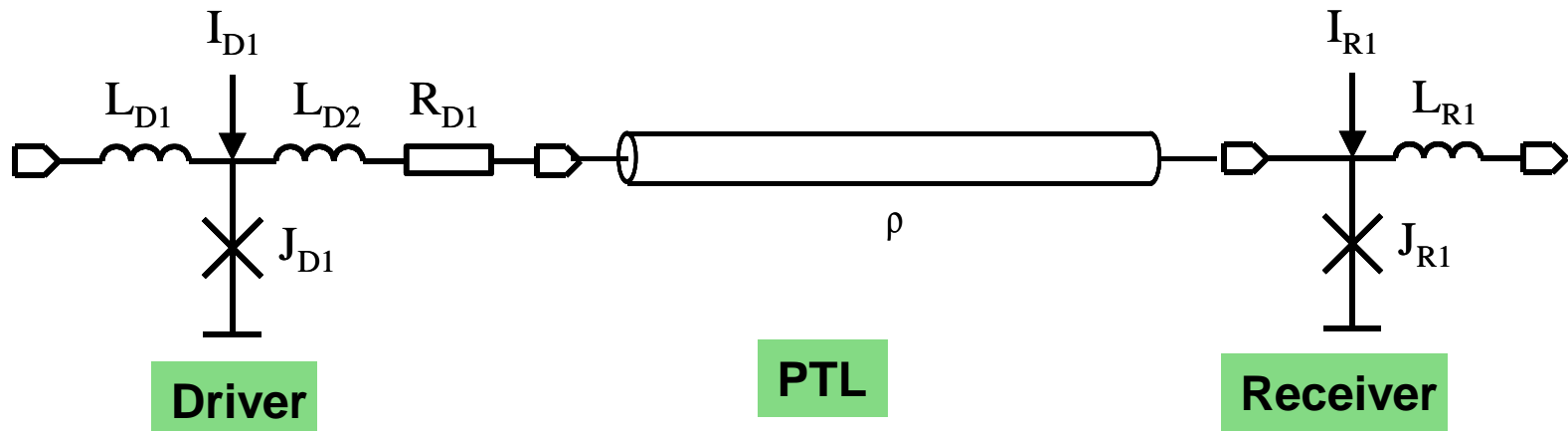
Total power dissipation:

$$P = f_{clk} \cdot I_b \cdot \Phi_0$$

Passive Transmission Lines (PTL)



- **Energy-efficient: Passive (no power regardless of length).**
- Delay is set by length (faster by x10 than JTL).
- Low time jitter.
- Only point-to-point (split by 2 is possible with insertion of resistors)



- Ballistic SFQ transport. One of the main advantages of SFQ circuits compare to any technologies.
- Typical PTL width – 2-4 μm (5 -11 Ohm impedance).
- Good for long interconnect. Not useful for short interconnect.
- **At present, does not help with circuit density.**

Scaling (miniaturization) - Tall Pole in the Tent



❑ CMOS progressed due to the ability to scale down

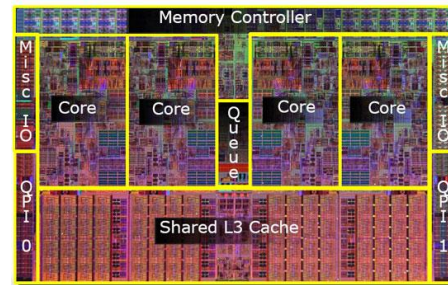
- Dennard scaling (transistors get smaller their power density stays constant) – propelled CMOS from 1974 to ~2006
- Moore's Law (transistor size reduction leads to more transistors per chip at the cost-effective optimum) - largely responsible for financial sustainability of CMOS technology

❑ Modern CMOS processor ~ 10^8 transistors per die, DRAM ~1 Gbit per die

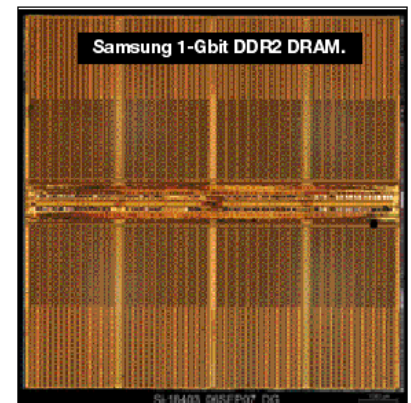
❑ Modern SFQ digital circuit:

~ 10^4 - 10^5 JJs per die

- Circuit components are too large
- Gate layouts are too large
- Circuit implementations are too complex
- SFQ EDA tools are not adequate for VLSI



Intel Core i7
Processor (Nehalem),
263 mm², 731 Million
transistors



Low superconducting circuit density is the bottleneck

➤ Computer Aided Design (CAD) tools: treacherous path

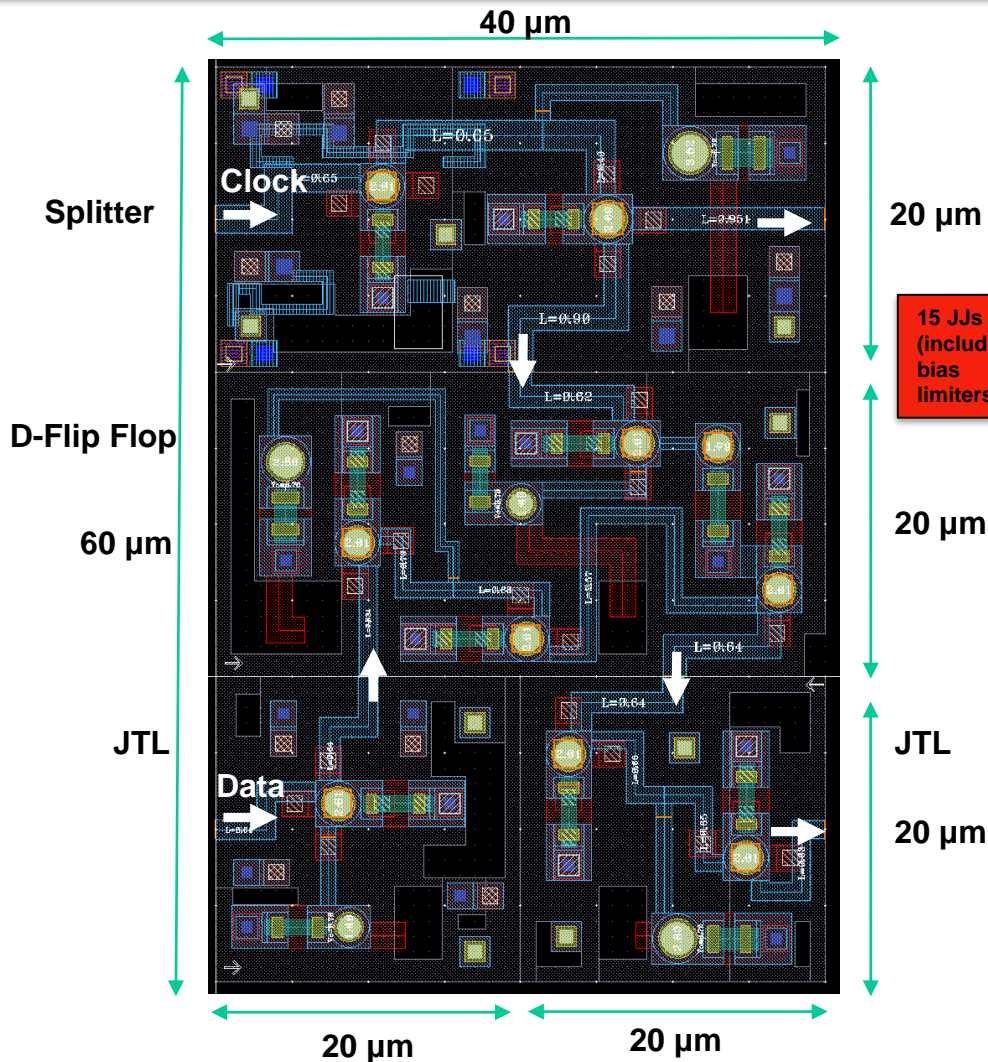
- Problem: low circuit density, large footprint
- Cell libraries (Lego-style vs Flexibility)
- NioCAD story
- InductEx success story
- PSCAN2 vs Spectre (\$70K vs \$1M investment)
- Timing (Global vs Wave-pipelined)

Cell Library Approaches



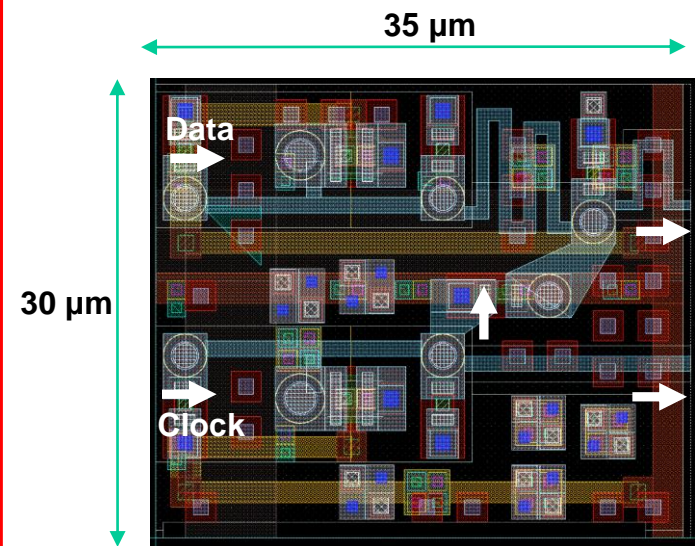
Lego lib – smaller number of gates, as all gates are composed of elementary cells

Flex lib – larger number of gates, as some gates tightly integrate multiple cells sharing JJs, inductors, etc.



Pre-C3 approach, still pursued by some due to simplicity

*x 2.3 smaller area,
x2 less JJs*



Learned from C3 experience

Cell Library Approaches

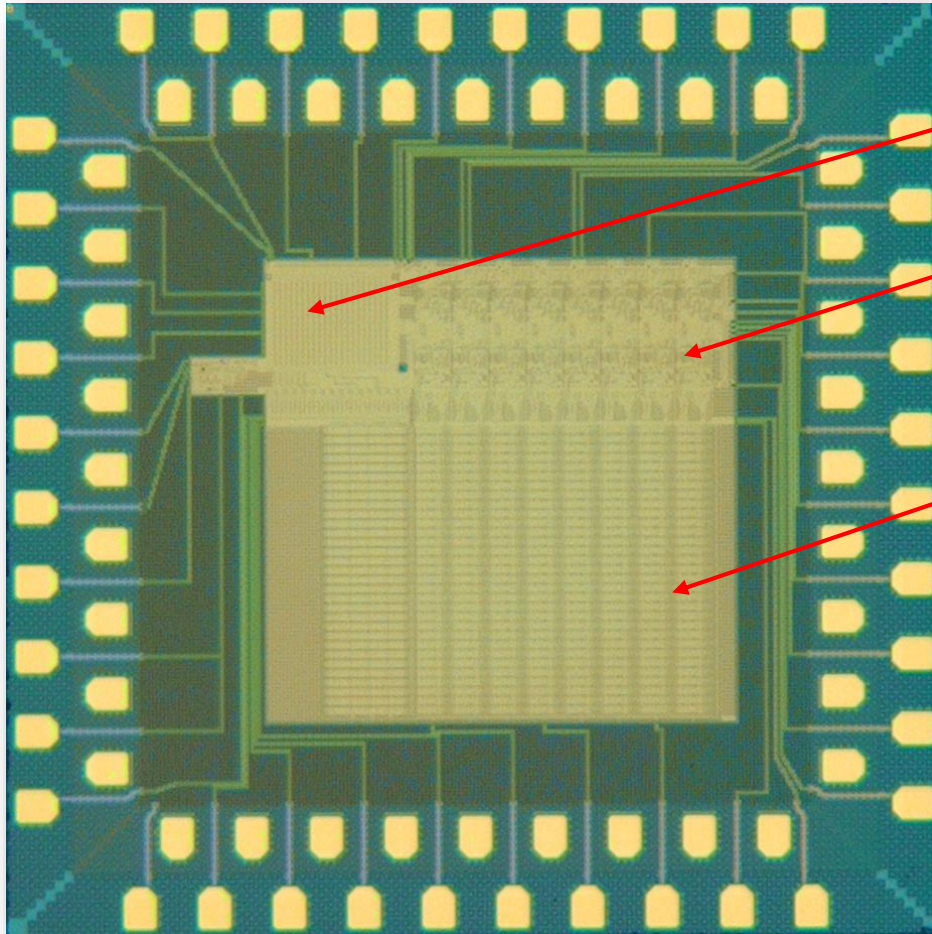


- **“Lego” - mostly practiced in the 90s and largely abandoned, current attempts to resurrect for new fab process**
 - Every port has predetermined location
 - Power plane and PTLs are included into cells
 - Easy for manual design, simple optimizers can be used
 - Results in excessively large area, large power
 - Easy verifiable (even manually)

- **“Flex” – boxed gates or larger subcircuits, JTLs are flexible (inductance p-cells)**
 - Ports are different
 - Power distribution and PTLs are added as the last stage of larger subcircuit design
 - More difficult for manual design, requires powerful optimizers
 - Results in minimum area and power
 - Not easy to verify (manually)

1. If one wants to design something really competitive and having practical significance (e.g. microprocessor), one has to use the most efficient, smallest footprint cell library.
2. For demo circuits to impress funding people, the “lego” circuit prototypes would be sufficient

8-bit Microprocessor (C3 project)



Instruction Memory
(8 bit x 13 instructions)

ALU (8 bit)

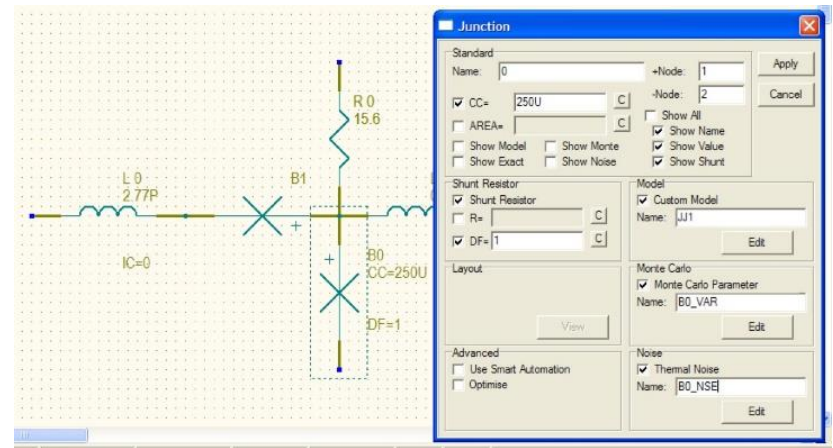
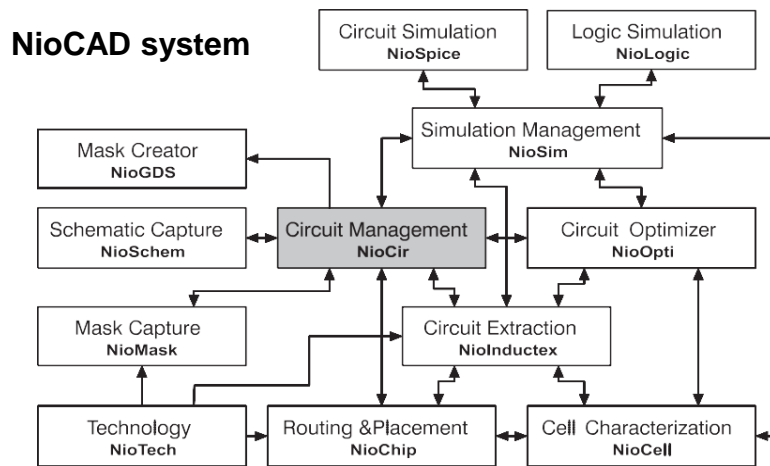
Register File
(8 bit x 31 words)

The bit width of the IM is defined by three 5 bit addresses (2 read and 1 write addresses) for Register File and a 6 bit instruction code for ALU (21 bits in total).

The total area of the CPU is $\sim 2.5 \times 2.5$ mm², total number JJs is $\sim 28,000$

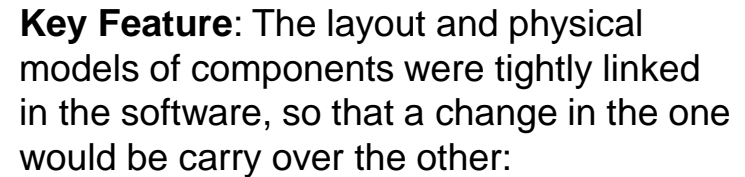
5 mm x 5 mm chip
Fabricated at MIT-LL in SFQ5ee process

EDA Tools: NioCAD (2007-2012)



A superconductor CAD package that would provide a complete and integrated solution for the development of superconducting circuits:

- Circuit capture – Drawing circuit elements using a schematic editor and/or a text editor;
- Circuit simulation – A SPICE simulator to verify circuit operation;
- Mask capture – A graphics editor to define layout structures;
- Component extraction – The 3D extraction of components from the circuit layout, using tools such as InductEx;
- Circuit optimization – A process of constantly changing circuit component values, simulating and evaluating the circuit in order to, for example, obtain better yield;
- Logic cell characterization - The characterization of a subcircuit in order to create a logical model that can be used in larger scale designs and logic simulations.



- From: W. Perold, Dr Eng dissertation, Stellenbosch Univ. 2017*

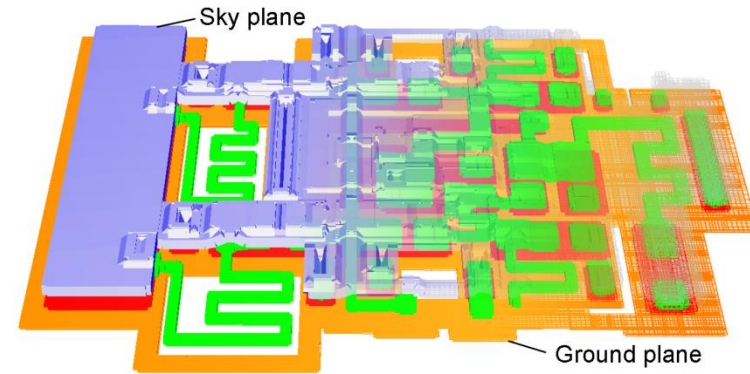
Success Story: Layout Extraction Tools

InductEx gives valuable extraction results for difficult design scenarios [1]

- Layouts with skyplanes, holes and coupling, parasitic coupling, inductors threading multiple ground planes, large and complicated coils
- Especially useful for eSFQ or ERSFQ gates, AQFP gates, layouts in 6+ layer advanced processes

Several features/improvements added last 2 years

- Full-circuit extraction (L, R, JJ area) from schematic netlist and layout files
- Optimised solvers for faster calculations (**x100 compared to old FastHenry**)
- New tetrahedral solver for Q4 2015: full impedance, hybrid meshes, chip-level modelling for bias current distribution and ground return currents.



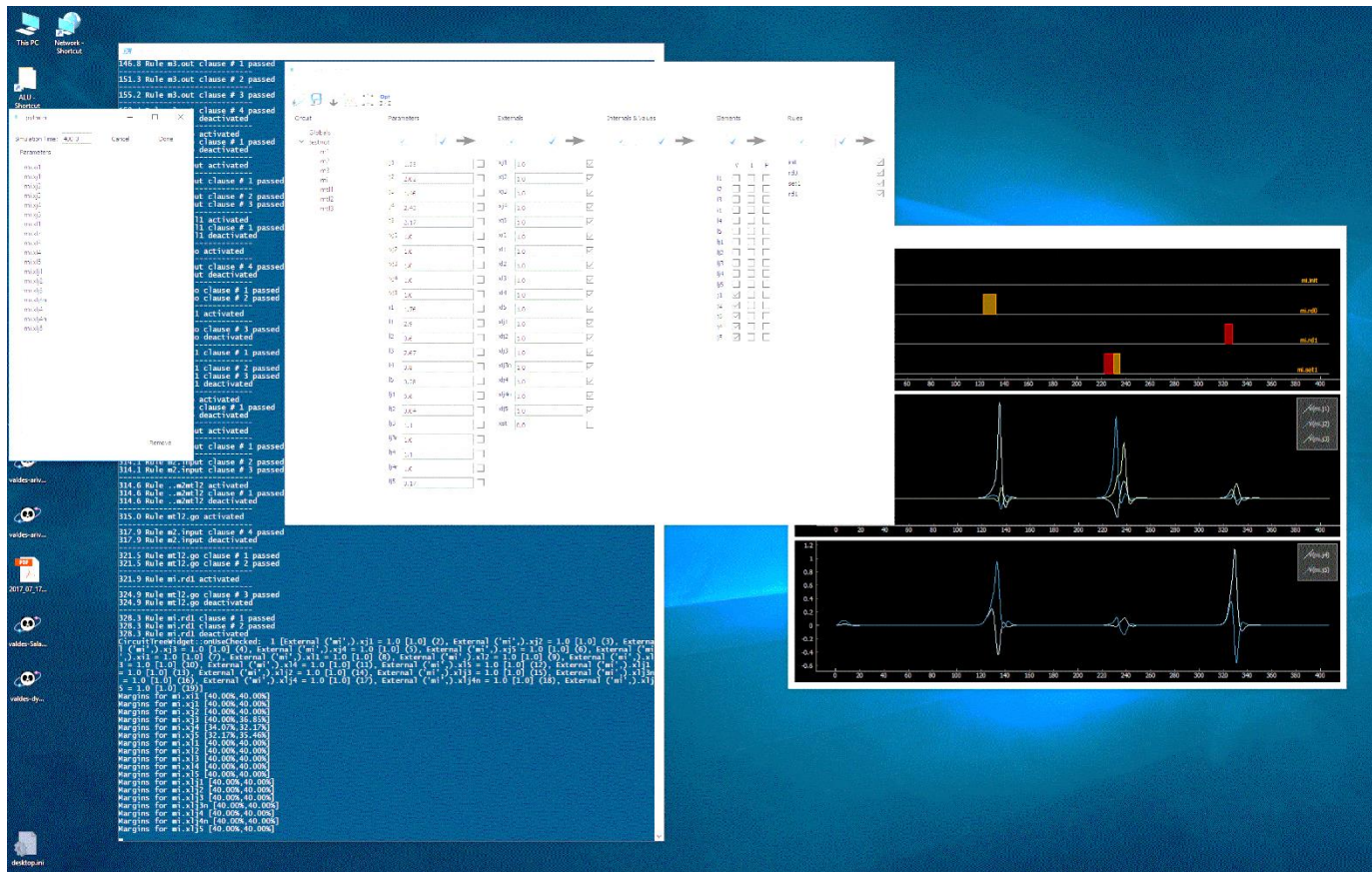
Rendering of full eSFQ cell meshed with InductEx for full-circuit extraction.

	InductEx	FastHenry standalone	Lmeter	3D-MLSI
Elements	Rectangular & <u>tetrahedral</u>	Rectangular	Triangular	Triangular
Complexity	<u>3D, holes, vias, multiple ground/sky planes</u>	<u>3D, holes, vias, multiple ground/sky planes</u>	Quasi-3D, vias, no sky planes	Quasi-3D (thin layer assumption), holes, <u>trapped flux</u> , no vias.
Circuit netlist extraction	<u>Full circuit, with coupling and resistance</u>	No	Superconductive only, coupling not certain, R separately	No
Support	<u>Active, continued development</u>	No	No	<u>Active, continued development</u>
Speed	<u>Fastest</u>	Slowest	Faster	Slower
CAD integration	<u>Cadence, LayoutEditor</u> , custom	No	<u>Cadence</u>	No
Extras	<u>Magnetic fields</u> , current density, outputs to MATLAB	Current density	None	Current density

Courtesy of C. Fourie

[1] C. J. Fourie, "Full-gate verification of superconducting integrated circuit layouts with InductEx," *IEEE Trans. Appl. Supercond.*, vol. 25, 1300209, 2015.

Success Story: Circuit Simulation and Optimization



Graphical User Interface (GUI) for PSCAN2 and COWBOY optimizer

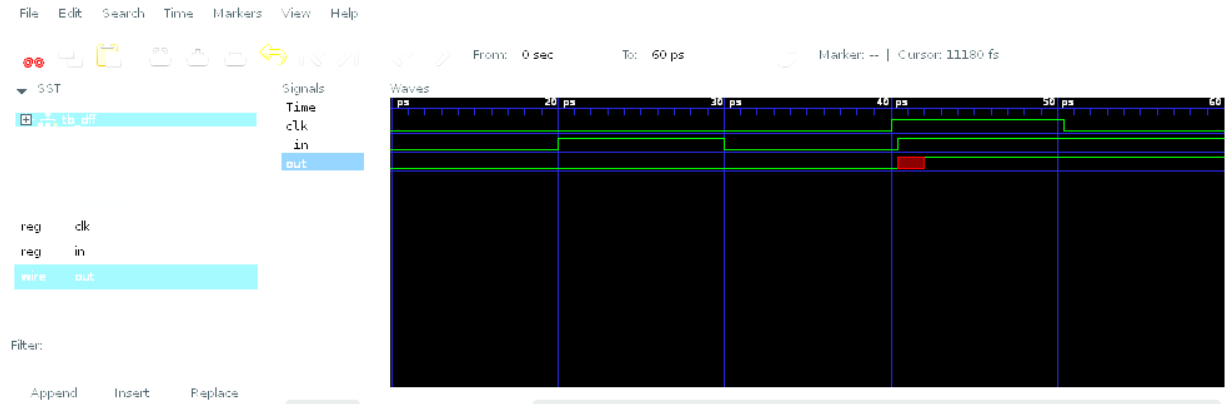
- Monte-Carlo optimizer can be easily added

- ❑ PSCAN2 works **x10 times faster** than the industry standard Spectre adopted to SFQ design while handling large complexity circuits ($\sim 10^3$ - 4 JJs).
- ❑ PSCAN2 development already used **>10x less funding** than was used for Spectre adaptation. The difference will be even greater with further development.

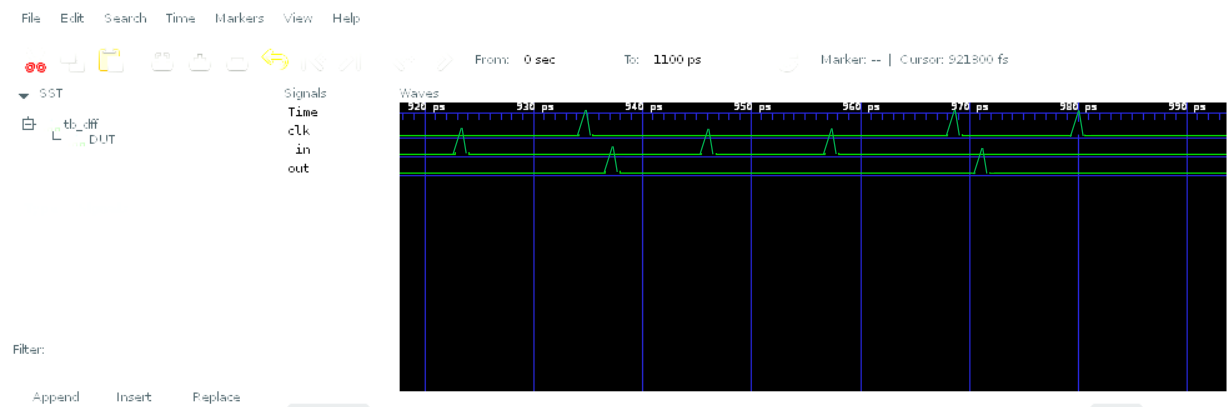
Circuit Timing (Clocking Methods)



CMOS is a level logic:
data are represented by
voltage levels



SFQ is a pulse logic:
clock and data are
represented by SFQ pulses
in RSFQ, ERSFQ, eSFQ



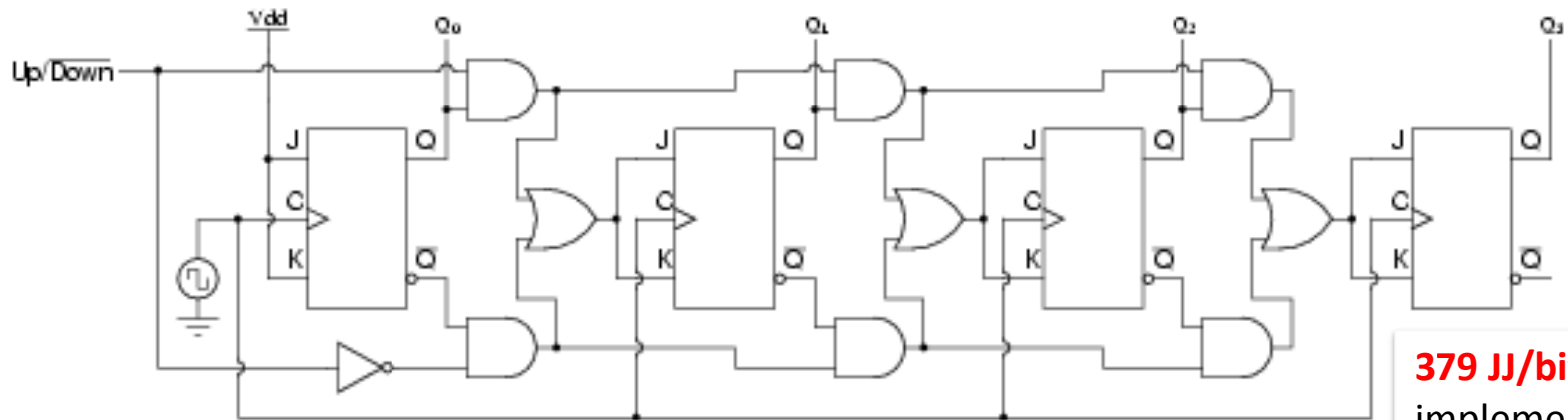
Should SFQ circuits follow the industry standards timing design (CMOS route) to make life easier?

Timing: Synchronous vs Wave Pipelined



Natural for CMOS

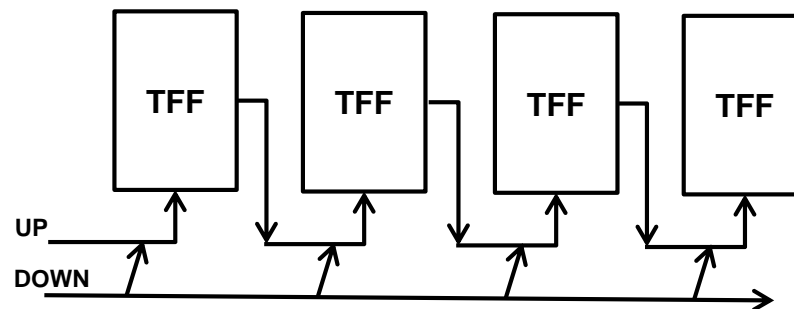
Synchronous design – assumes simultaneous clock distribution



379 JJ/bit when implemented in ERSFQ

Natural for SFQ

Wave-Pipelined design - uses SFQ pulse propagation



58 JJ/bit when implemented in ERSFQ

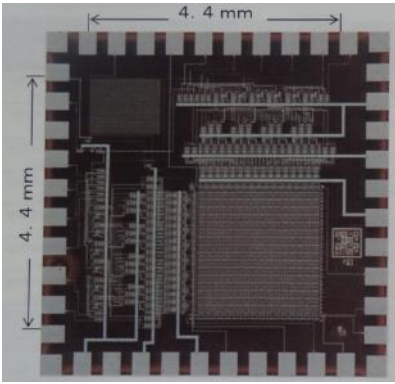
RESULT:
*x 8 smaller area,
x 7 less JJs*

Make natural choices rather than copy alien technology solutions

➤ Memory

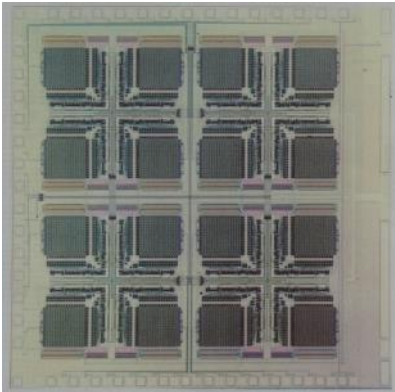
- SFQ Random Access Memory (RAM) to Magnetic RAM (MRAM)
- Memory Element vs Memory Cell
- Physics/MatScience vs Engineering

History of Josephson memories (only a selection)

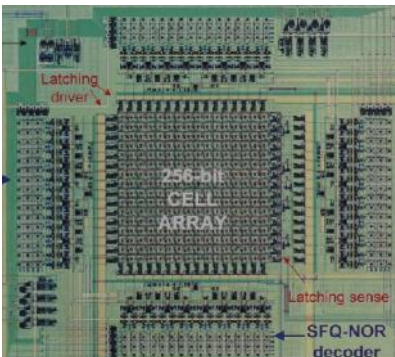


1987 NEC Japan,
1024 bit NDRO Josephson memory
Nagasawa et al., IEEE Journal of Solid state
circuits, Vol. 24, No. 5, (1989)

Josephson memory: memory made
with traditional elements: JJs,
SQUIDs, inductors, etc.

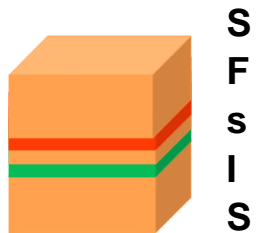
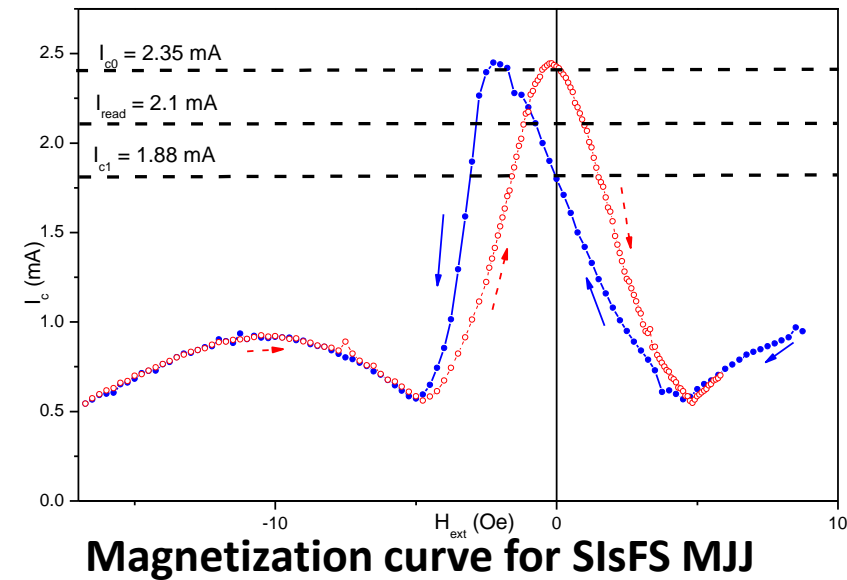


1999 NEC Japan, Dr. Nagasawa
4096 bit vortex transitional memory
256 x 16 bit organized
tested at 620 MHz
**S. Nagasawa et al., IEEE TAS, Vol. 9, No. 2, p. 3708, 1999*

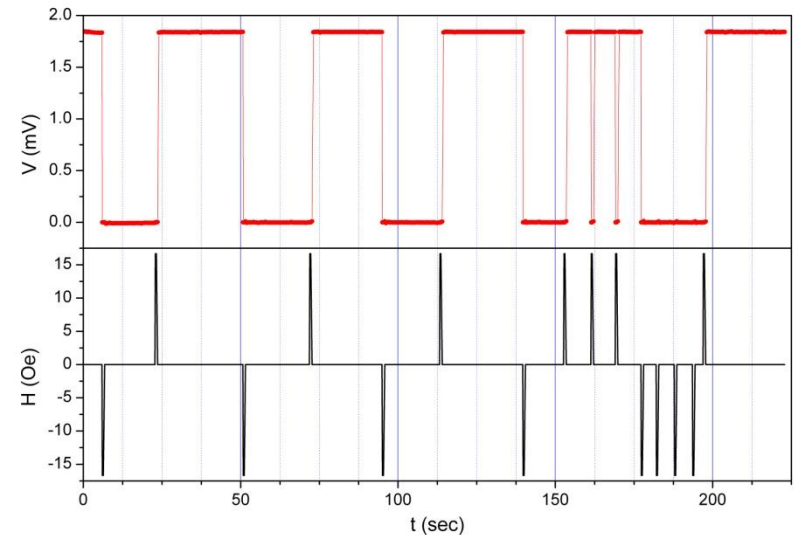


2000 ISTECS SRL Japan, Dr. Nagasawa
256 bit vortex transitional memory, all dc-powered

**Main Problem: large memory cell size
(SQUIDs are large) and ac power**



Memory Element Operation



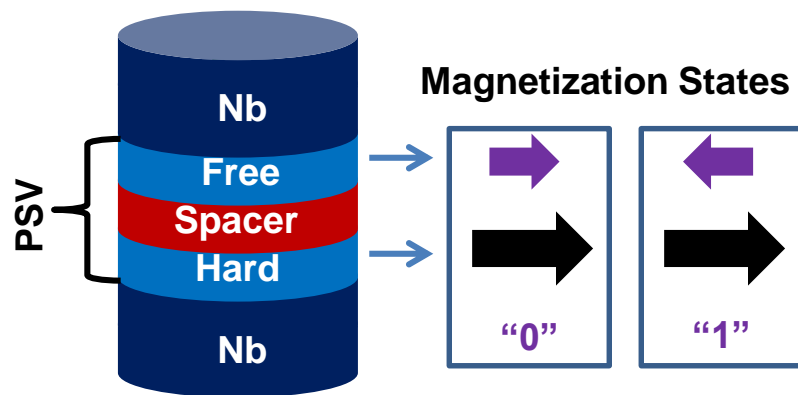
Electrical Switching of SIsFS MJJs

- SIsFS MJJs have high $I_c R_N$ - electrically compatible to conventional JJs
- No need for readout SQUIDs, can be used to build SFQ circuits similar to JJs
- Simple fabrication: large element, single ferromagnetic layer
- Memory element min size $\sim 1\text{-}2 \text{ }\mu\text{m}$. Limited scalability
- Nonvolatile storage

NIST Memory Element Based on a Pseudo-Spin-Valve-Barrier JJ

Device Structure:

JJ with two ferromagnetic barriers in series



Features:

- Demonstrated scalable switching of J_c
- Josephson phase can also switch between 0 & π
- Nonvolatile storage
- Demonstrated $\Delta J_c/J_c$ up to 500 %
- Write: similar to MRAM (field or current)

Challenges:

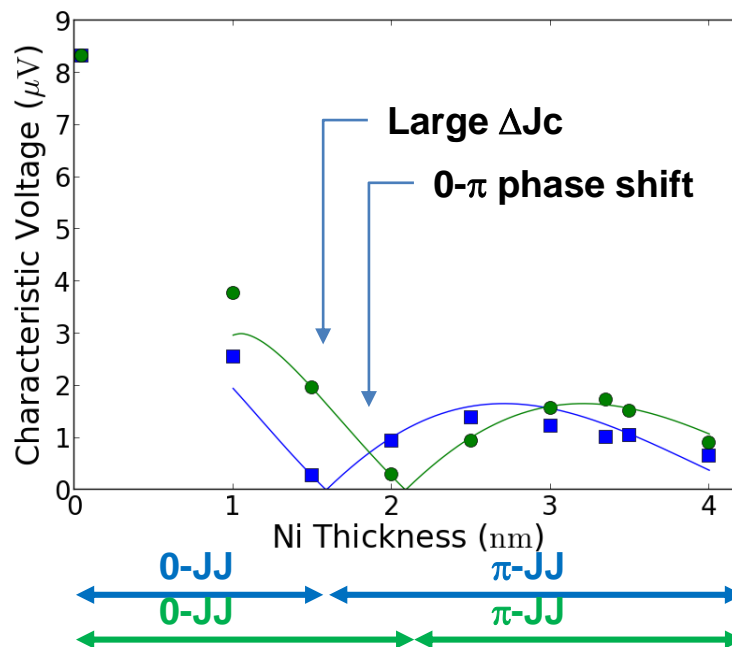
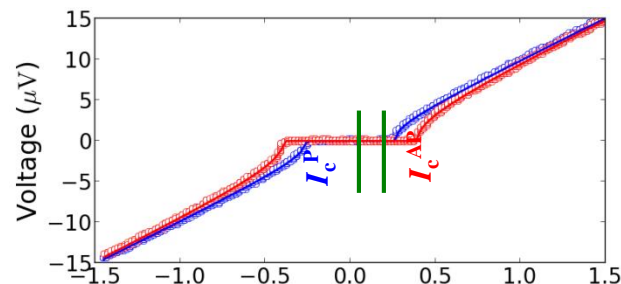
- Write efficiency and speed
- Electrical properties not compatible to SIS JJs
- Need additional elements to construct memory cell

Principle:

Exchange field effect on Josephson coupling

→ $J_c(\text{parallel}) \neq J_c(\text{anti-parallel})$

→ Also Phase(0 state) \neq Phase(π state)



Baek, B. et al. Nat. Commun. 5:3888 (2014)

Physics vs Engineering

☐ Which memory element to choose for dense MRAM?

- SIsFS is non-scalable below 1-2 μm
- SFNFS PSV is scalable to nanoscale (e.g., below 0.1 μm)
- The answer looks straightforward: SFNFS PSV

☐ Right? Wrong

☐ Memory element does not make Random Access Memory

☐ Addressable memory cell does

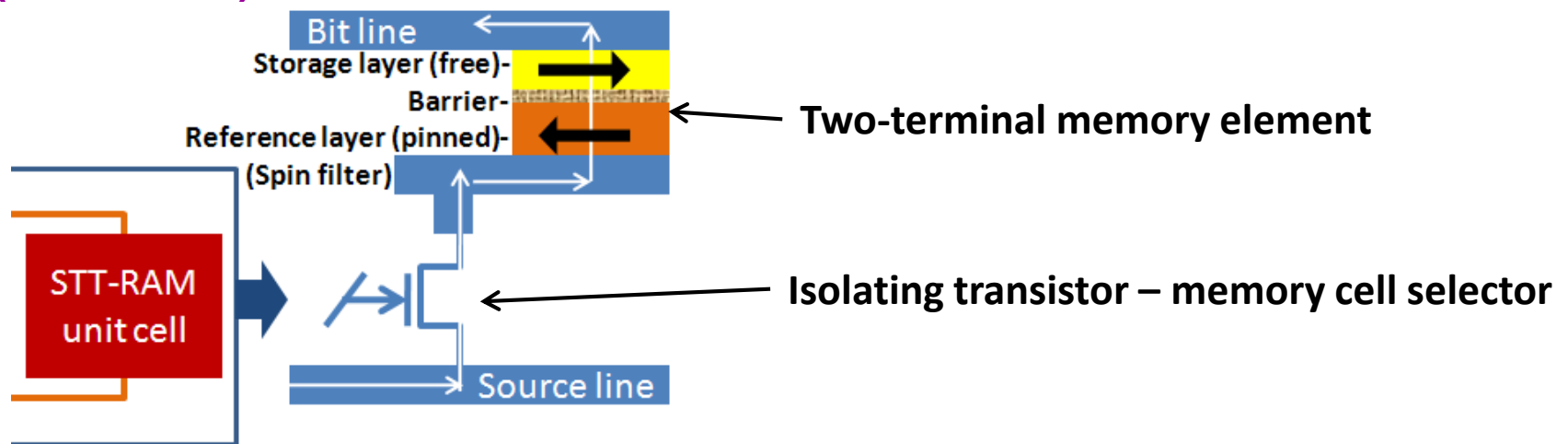
- Memory Cell is a combination of a memory element and a cell selector to enable addressing in RAM array
- Read/Write operation in RAM array should not cause half-select disturb in unselected memory cells

Memory Cell: Need for Cell Selector



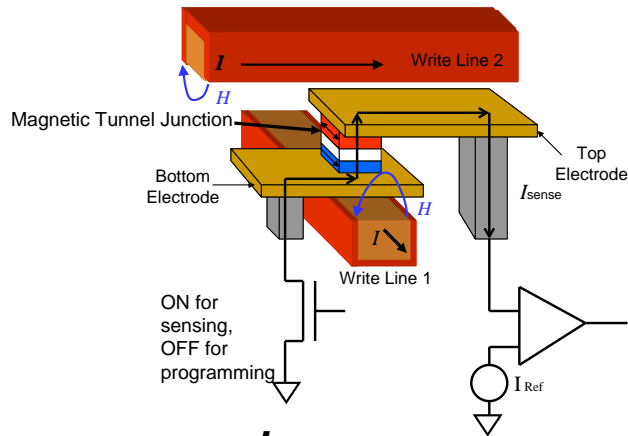
- ❑ MJJ is programmable JJ – a nonvolatile memory element. But it is a two-terminal device without input/output isolation
- ❑ For random access memory (RAM), one needs to address (select) an individual memory cell without disturbing neighboring cells in RAM array
 - Needs a 3 terminal device with good Input/output isolation is required

Example from room-temperature non-superconducting spintronic RAM (STT MRAM)



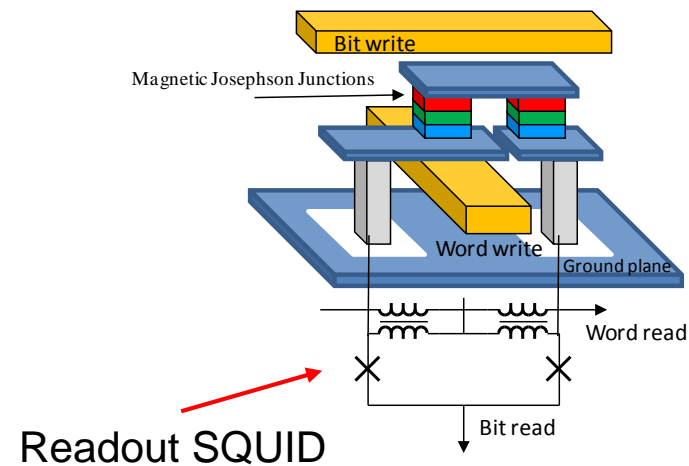
Addressable Memory Cells from NGES

Room-Temp. Toggle MRAM



www.everspin.com

Toggle JMRAM



**Memory cell is a magnetic tunnel junction with superconducting electrodes:
underlining physics demonstrated on SFS Josephson junction**

memory state – critical current magnetic hysteresis

write – spin reversal

read – Josephson effect

*n*Tron: Nanowire 3-terminal Device

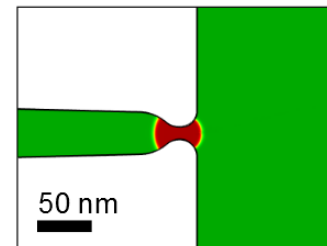
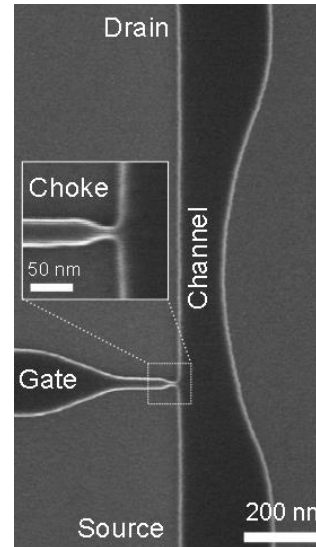
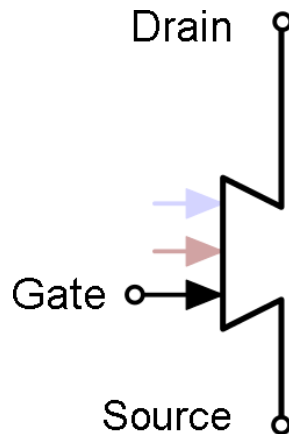
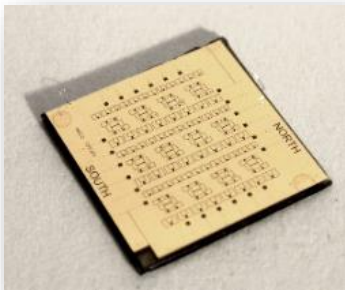


Can be used for RAM as line drivers and memory cell selector

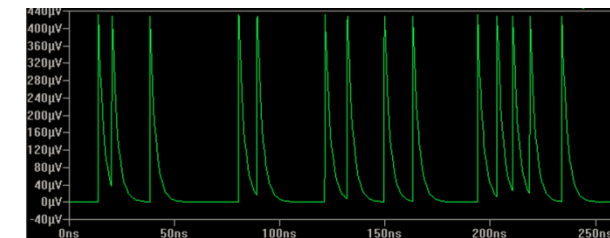
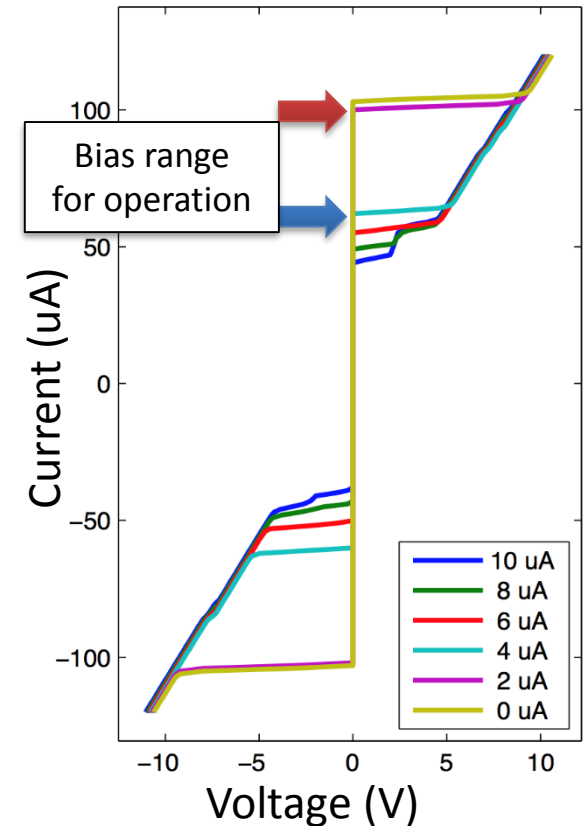
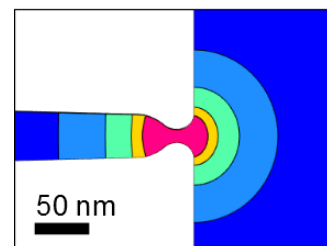
- Planar NbN or Nb, simple to fabricate
- SFQ compatible

Demonstrated:

- Comparator; 66nA grey zone
- Digital Logic, half adder
- 20x gain
- Good In/Out isolation
- High Z drive



J_c suppression



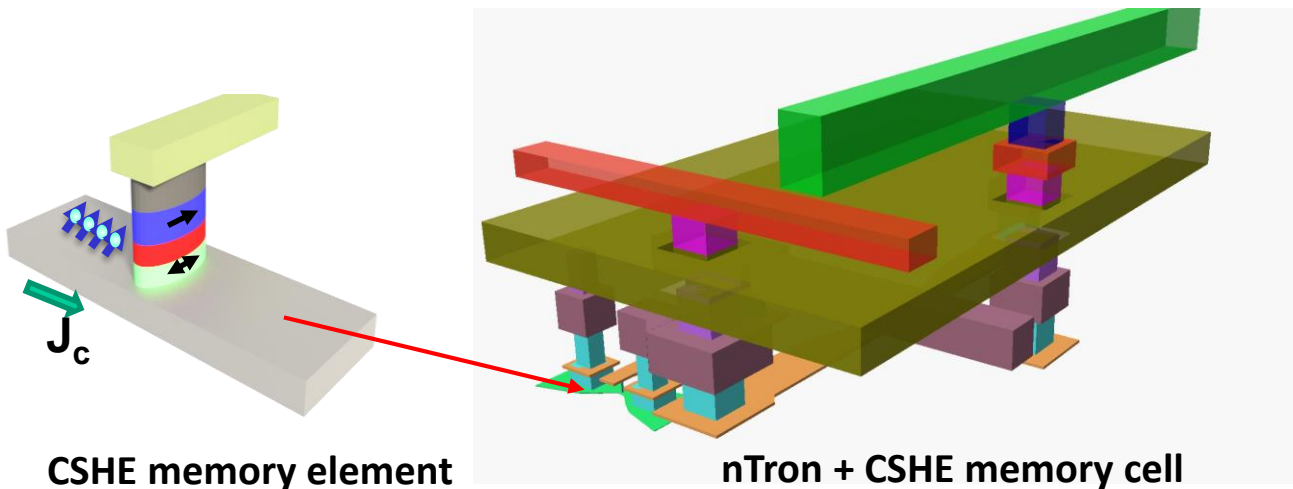
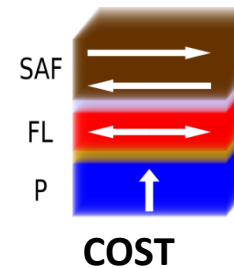
50 ps risetime pulses, potential of 100s of MHz rep rate



Courtesy of K. Berggren, T. Ohki

□ Hybrid circuits with cryogenic magnetoresistive memory elements (JJ+metal spintronics)

- Memory cell based on spintronic elements with addition of JJs (for low impedance) or nanowire switches (for high impedance)
- Memory devices:
 - Cryogenic Spin Torque transfer (CST)
 - Cryogenic Spin Hall effect (CSHE) elements
- JJ periphery (address decoders, sense, etc.)



PI: T. Ohki

Raytheon
BBN Technologies



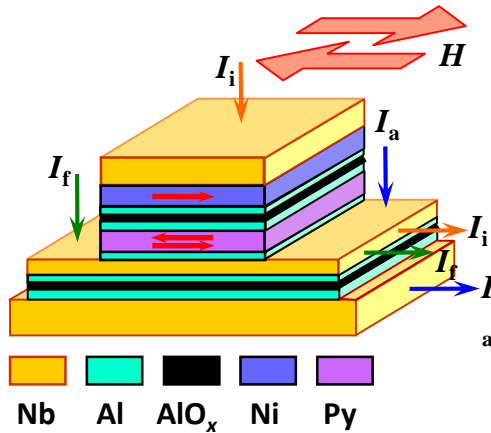
NYU



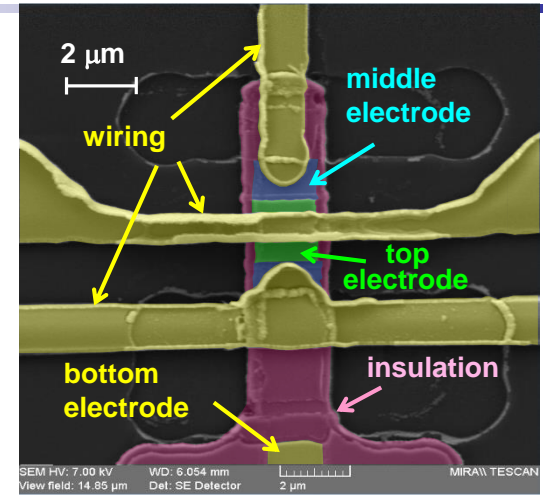
❑ Memory element (SFNFS, etc.) occupies a small fraction of memory cell area (<10% at best)

- This makes scalability of memory element hardly relevant for RAM array, memory element does not define memory cell size
- Size of addressing elements (not memory element) in memory cell defines RAM density
 - Readout SQUIDs are much larger than memory element
 - This makes size of MRAM cell close to the size of traditional Josephson memory
 - The only advantage left is nonvolatility (a small peanut)

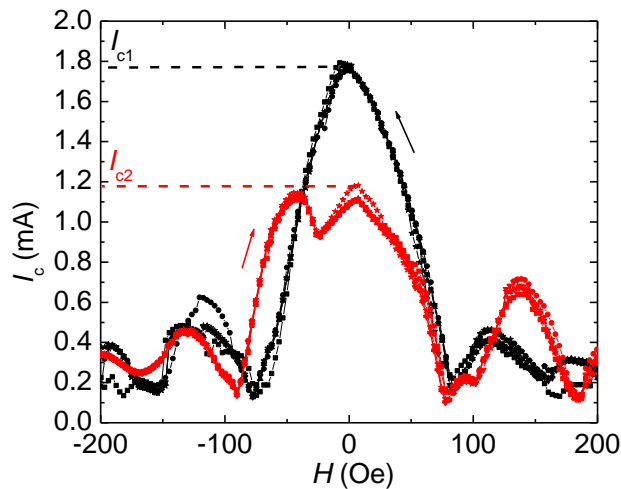
Memory Cell: Integrated memory and readout element



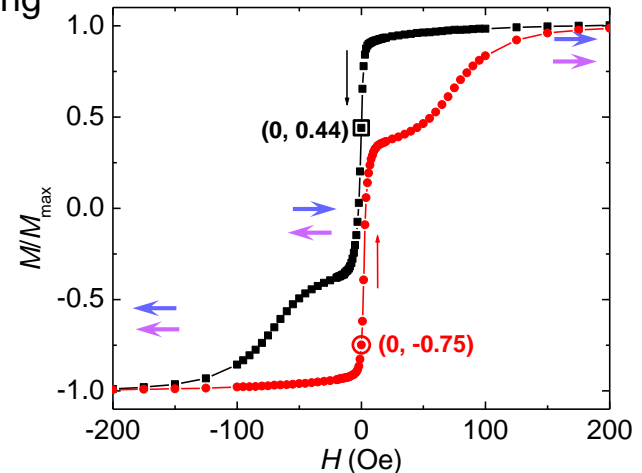
SEM micrograph of an actual SISF₁IF₂S device



Schematic view of a four-terminal SISF₁IF₂S device and its biasing



$I_c(H)$ dependence for the SIS junction while sweeping an external in-plane magnetic field in two opposite directions (five overlapped curves for five consecutive scans are shown).



$M(H)$ dependence at 10 K for 5 mm × 11 mm chip with unpatterned SISF₁IF₂S multilayer used to fabricate the four-terminal devices. $|M/M_{\max}|$ has two considerably different values at $H=0$, which correlates with the $I_c(H)$ dependence.

Courtesy I. Nevirkovets

Lessons learned

- Transformation is always challenging and not straightforward
- Energy and speed remains the main strength of superconducting electronics
- Memory still needs solution
 - Must be based on strong engineering, not just on interesting physics
- Adequate design tools are critical to achieving complexity
 - many hidden problems which can be easily underestimated

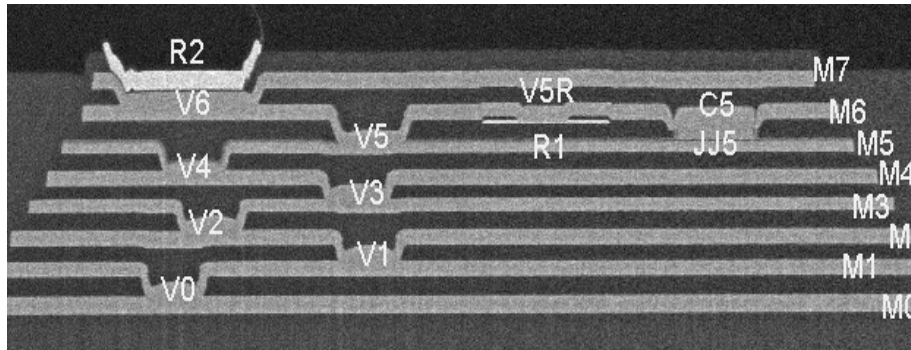


 **Thank you**

MIT-LL Fully-Planarized SFQ Process



SFQ4ee 8-Nb-layer Process



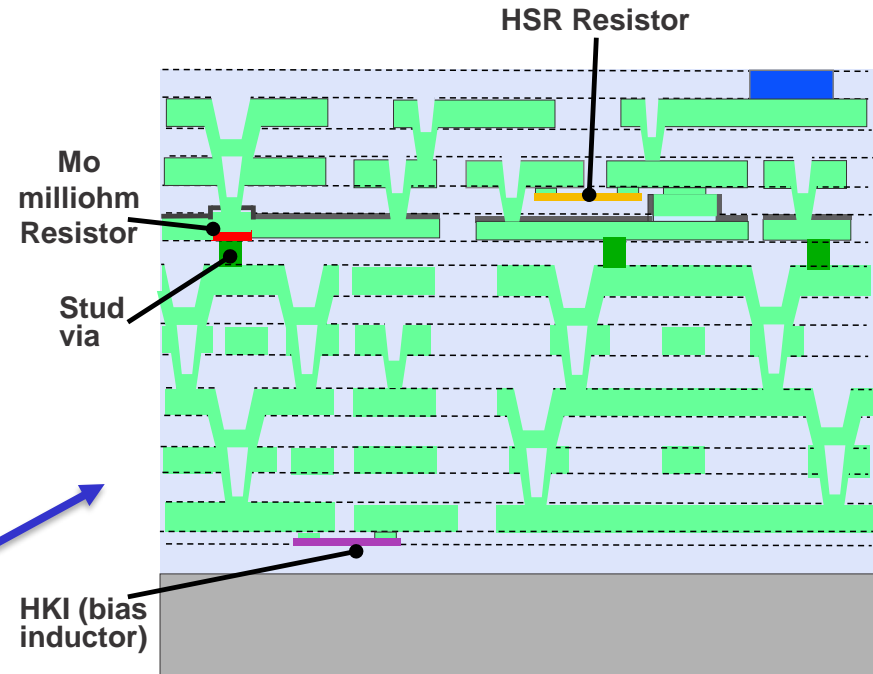
←→ 2 μm

SFQ5ee Process Features

(Primary IARPA C3 process node)

- 10 kA/cm² (100 $\mu\text{A}/\mu\text{m}^2$)
- Wafer size: 200-mm
- Min wiring feature size: 500 nm
- Min JJ size: 700 nm
- High Kinetic Inductance (HKI) layer: 8 pH/sq
- High Sheet Resistance (HSR) option: 6 Ω/sq

SFQ5ee 8-Nb-layer Process

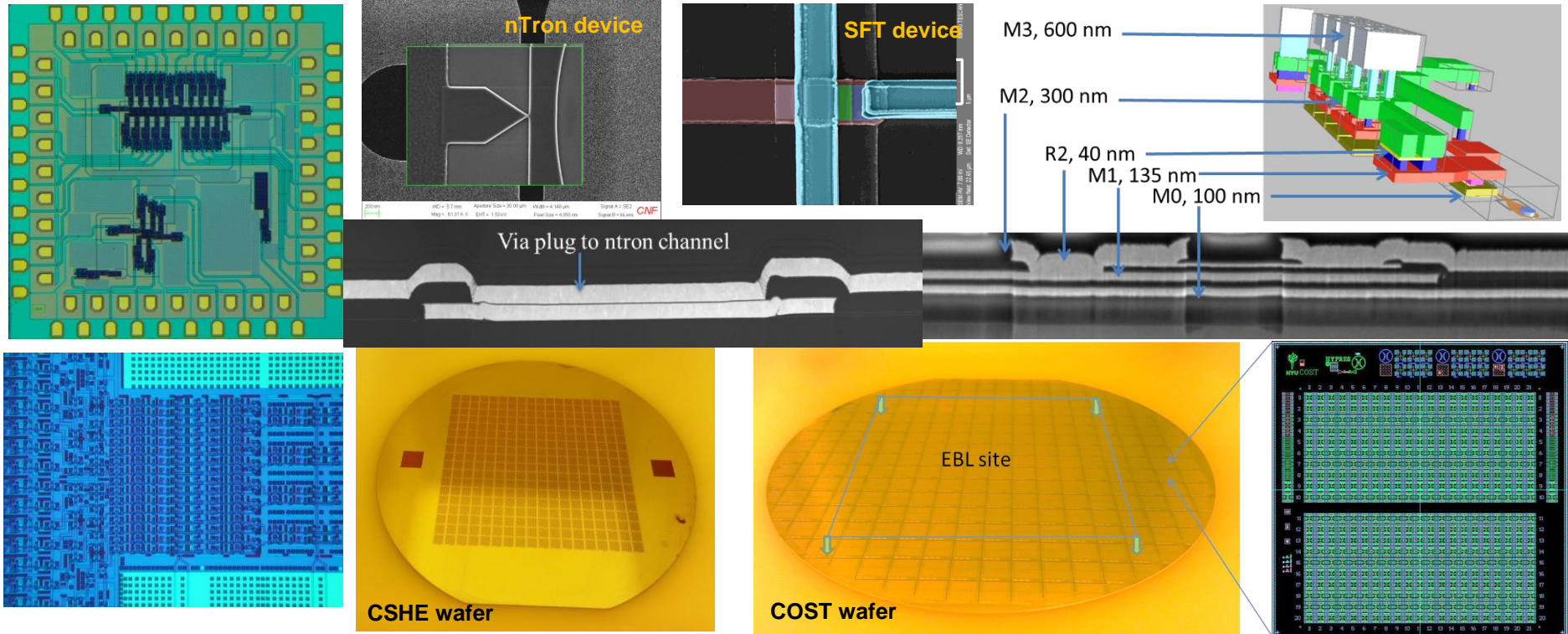


HYPRES Integrated Memory Process (IMP)



First of its kind “Digital+” fabrication process

150 mm wafer process integrating SFQ circuits, nTrons and MRAM devices



ERSFQ features

- 10 kA/cm²
- 3 Ohms/sq
- 7 superconducting layers
- Min size 500 nm



nTron features

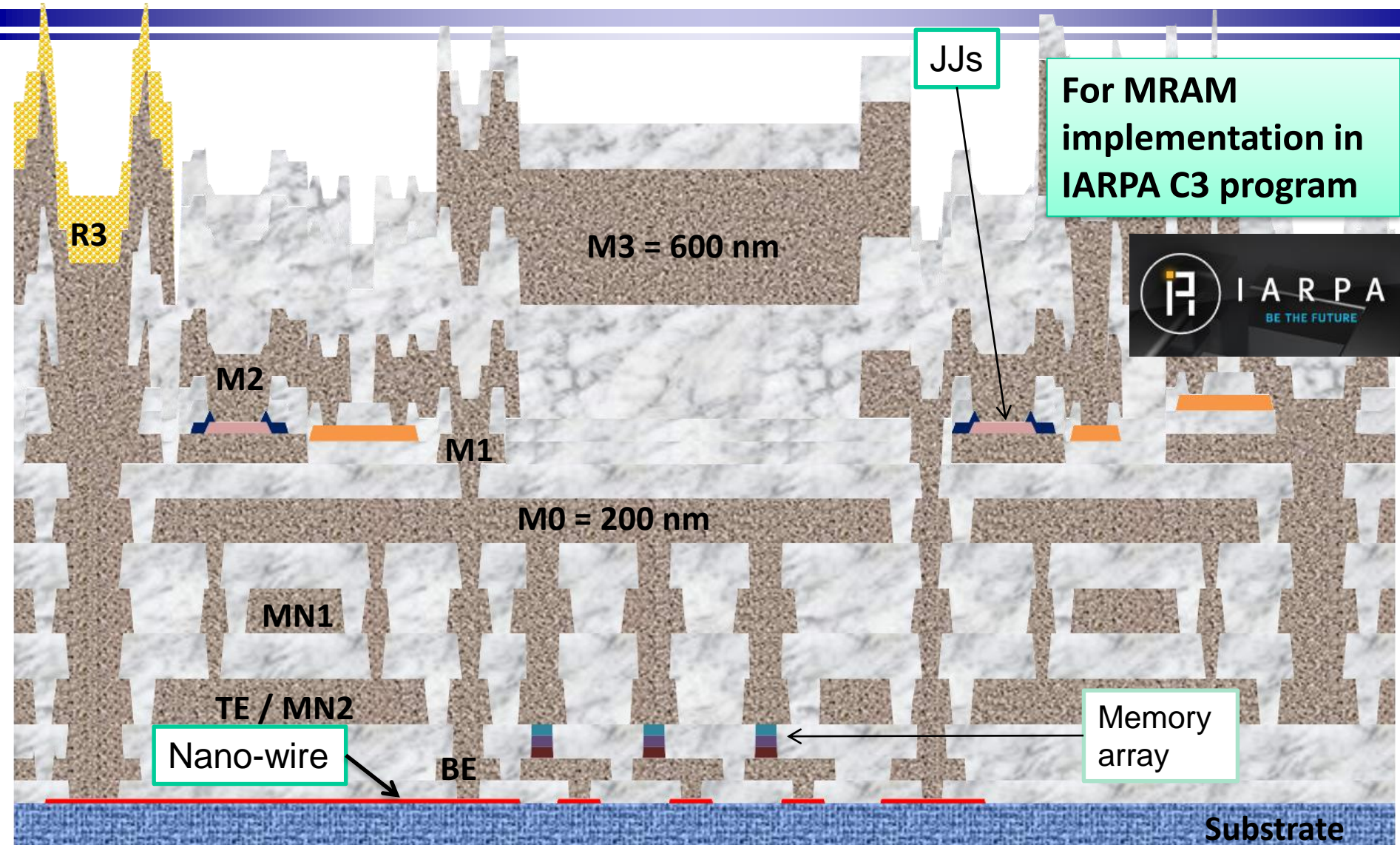
- Material = 15 nm thick NbN_x
- T_C = 12 K
- 10 – 30 nm gate size



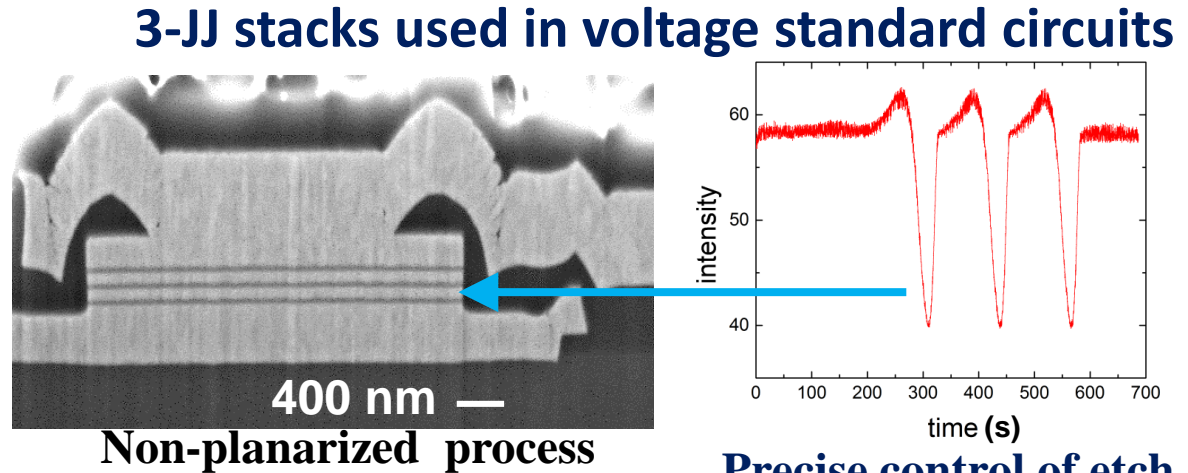
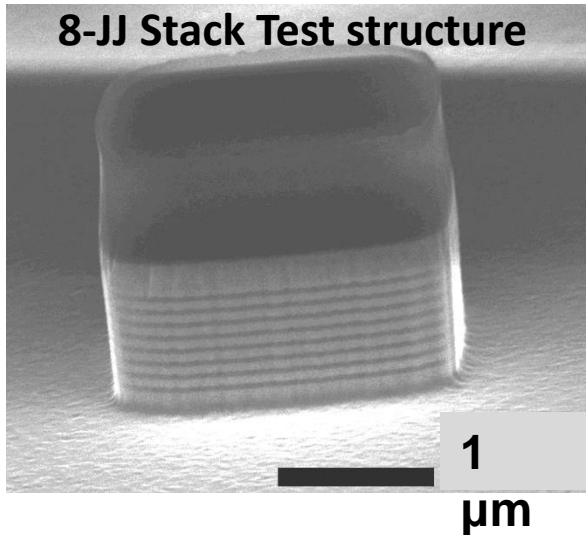
MRAM features

- Orthogonal Spin Transfer (COST)
- Spin Hall Effect (CSHE)
- EBL defined nano-pillars
- Optimized for < 0.1 mA

HYPRES Integrated Memory Process (IMP)



Vertical NbSi JJ Stacks



**Precise control of etch
with laser endpoint**

C_4F_8/SF_6 ICP/RIE etch yields vertical profile → Uniformity of JJs in stack

- 1. Self-shunted NbSi JJs eliminate need for shunt resistors**
- 2. Relatively thick barriers allow for uniform high- J_c JJs**
- 3. Josephson kinetic inductance of NbSi JJ stacks can replace inductors**

- Substantial increase in circuit density**
- Eliminate parasitic inductances**
- Increase operating margins and yield**

□ C3 program brought superconducting technology at HYPRES to the next level:

➤ **New design approaches dictated by complex IC**

- New libraries (dense, easily customized)
- New EDA tools (PSCAN2, InductEx)

➤ **New architecture solutions dictated by complex IC**

- Wave-pipelining clocking
- Current recycling

➤ **New fabrication processes**

- Integrated Memory Process (IMP): SFQ + new devices
 - nTrons, high-kinetic inductors
 - Magnetic devices (CST, CSHE)
 - Superconducting–Ferromagnetic Transistors (SFT)
- Proliferation of Chemical Mechanical Polishing (CMP) fabrication steps
 - Self-aligned contacts to nanopillars
 - Full planarization enabling >10 Nb layers stacks

➤ **New devices**

- Memory SFT

Ultimate Performance (Computing Efficiency)



Future supercomputer with superconducting fast nodes, quantum computing nodes, combined with conventional CMOS nodes.



Classical superconducting (SFQ) computing node – similar to conventional CMOS node, but faster (@20-60 GHz) connected to CMOS nodes using optics.

Quantum computing (QC) node – a nested system, in which the QC core is readout, controlled, loaded/unloaded, corrected using superconducting classical computing circuits, which in turn connected to SFQ and/or CMOS nodes using optics.

Note: Needs high data rate energy efficient optical data network

□ Two versions of new generation of RSFQ logic with zero static power dissipation $P_s = 0$:

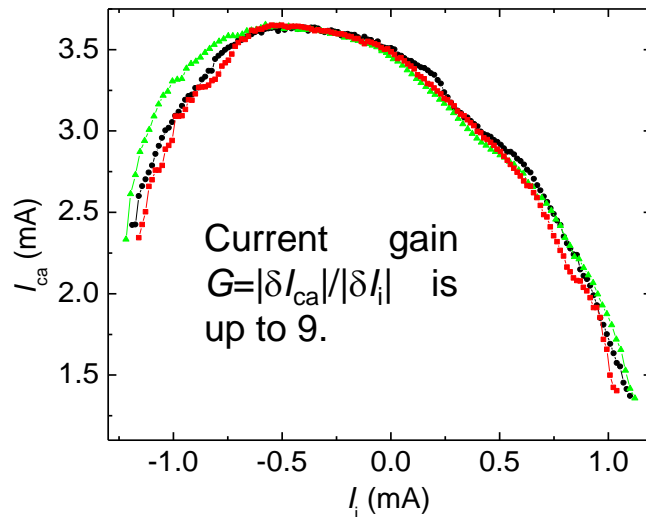
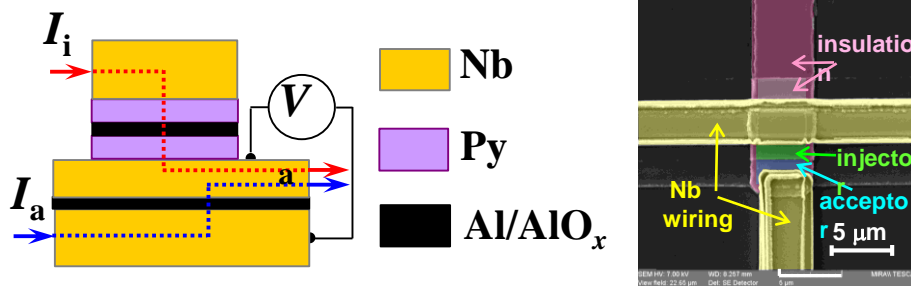
➤ **ERSFQ** - *Adaptive average voltage balancing*

- Preserves standard RSFQ cell design with exception of biasing network
- Needs relatively large bias inductors ($\sim 300\text{pH}$) – the area penalty will be avoided with more metal layers available
- **Natural first choice for implementation**

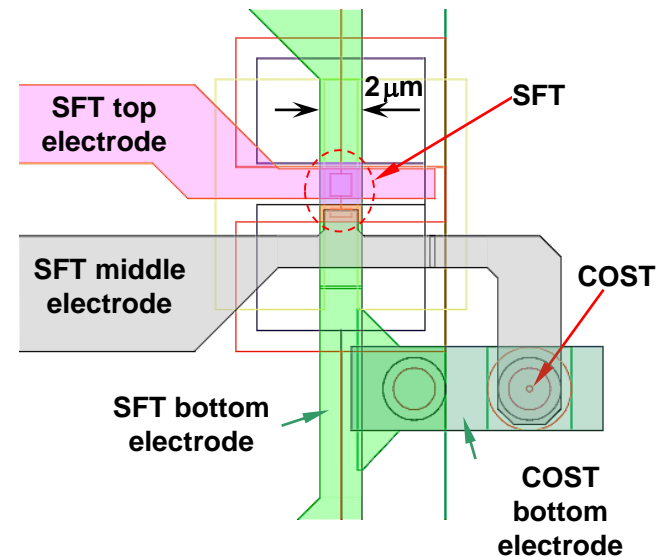
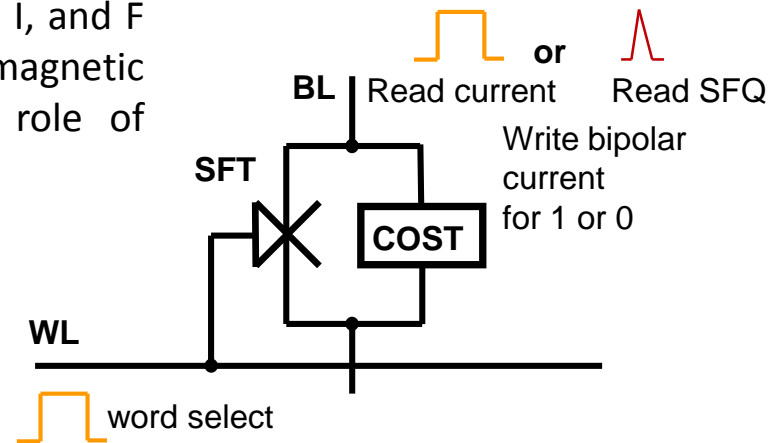
➤ **eSFQ** – *Synchronous phase balancing*

- Requires some re-optimization of standard RSFQ cell due to the required change of biasing point
- No large bias inductors are required
- Bias inductors can be formed by junction stacks to achieve ultimate circuit density
- dc bias is delivered via clock distribution network
- **Ultimately more compact version**

Superconducting-ferromagnetic transistor (SFT): SISFIFS; S, I, and F denote a superconductor, an insulator, and a ferromagnetic material, respectively. SIS and SFIFS junctions play a role of acceptor and injector, respectively.



Dependence of the SIS Josephson maximum current, I_{ca} , on the injection current, I_i for three nominally identical devices.



SFT + COST memory cell test circuit