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Superconductor Electronics Fabrication Process with MoN_x Kinetic Inductors and Self-Shunted Josephson Junctions

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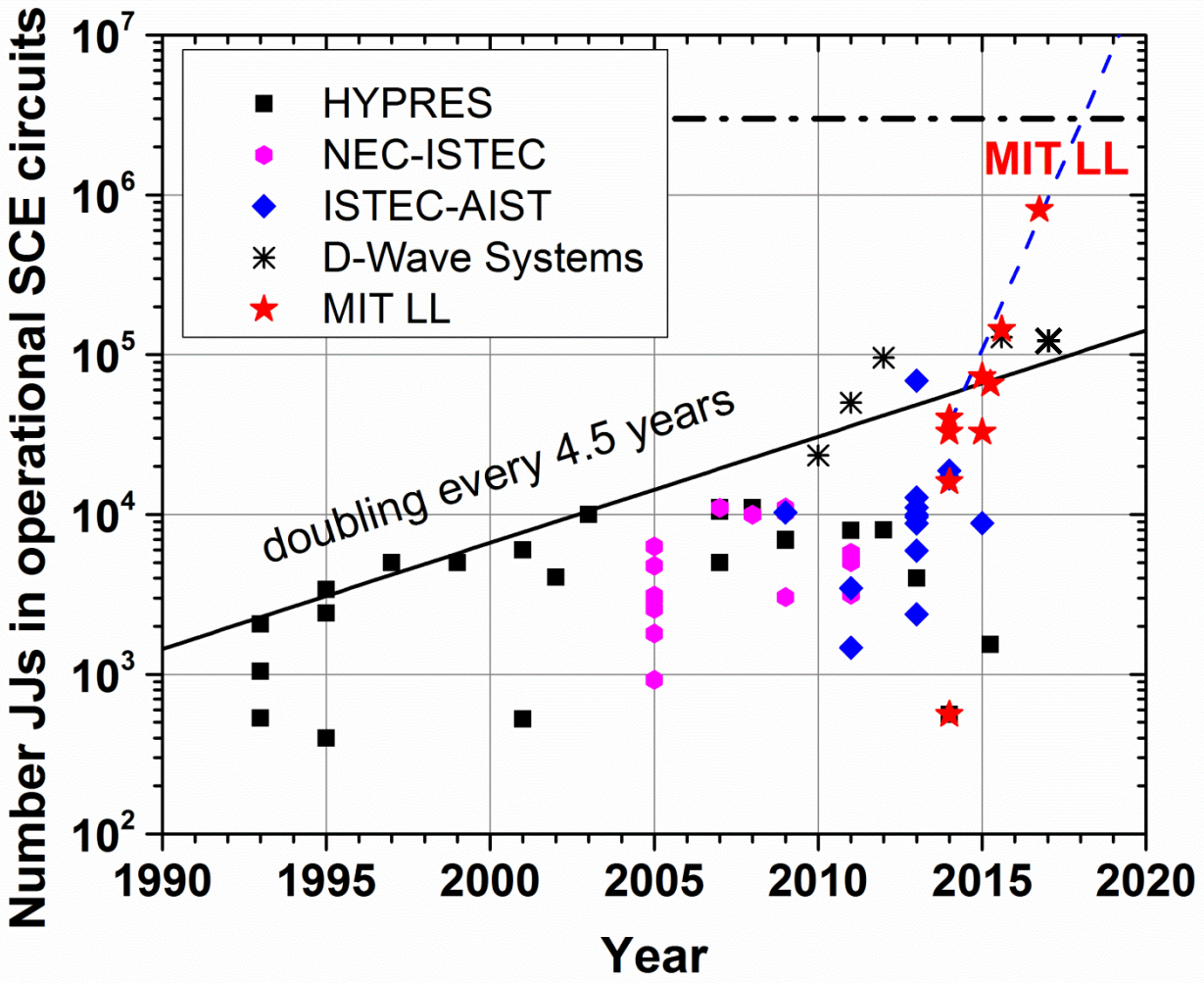
Outline

- **Introduction**
  - MIT LL superconductor electronics fabrication
  - Current SFQ5ee process node
  - Benchmark circuits at 10^6 JJ scale
- **Very Large Scale Integration (VLSI) and scaling limiters**
  - Resistively shunted junctions
  - Geometrical (magnetic) inductors
- **Process development directions**
  - Self-shunted high-J_c junctions
  - Kinetic inductors
  - Linewidth reduction to 250 nm and below
- **Conclusion**

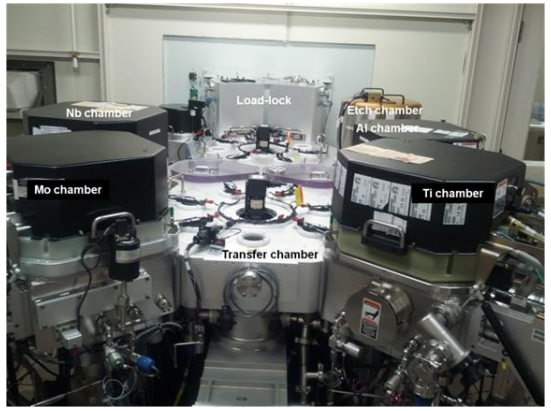
Superconducting Electronics Scaling Trend

- **JJ count – number of JJs in demonstrated circuits is a good metric of progress**
- **MIT LL/Stony Brook U. circuits with 810k resistively shunted Josephson junctions and JJ density of $1.33 \cdot 10^6$ cm^{-2} is the current World Record**
- **80x increase in integration scale during four years demonstrated**
- **The maximum JJ density in the current technology nodes is ~ 3×10^6 JJs/cm^2**
- **New technology developments are required to go beyond 10M JJs**



MIT LL technology enables very large scale integration of superconducting circuits

MIT LL Microelectronics Laboratory SCE Foundry



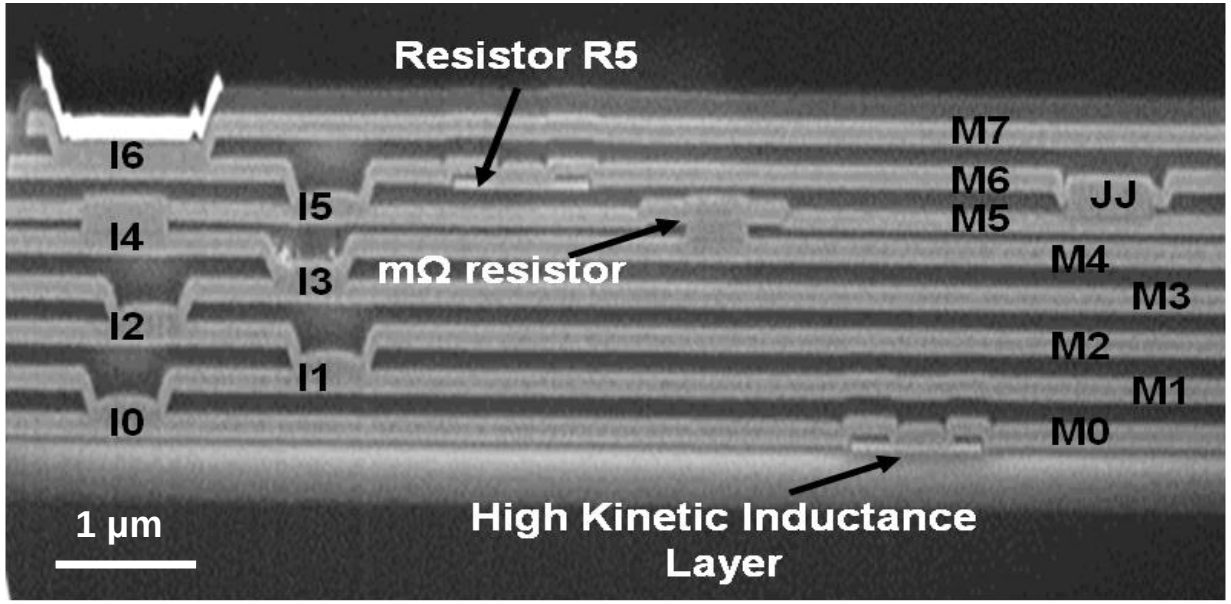
SCE Fab Leverages Facilities and Toolset of 90-nm CMOS Foundry in Microelectronics Lab

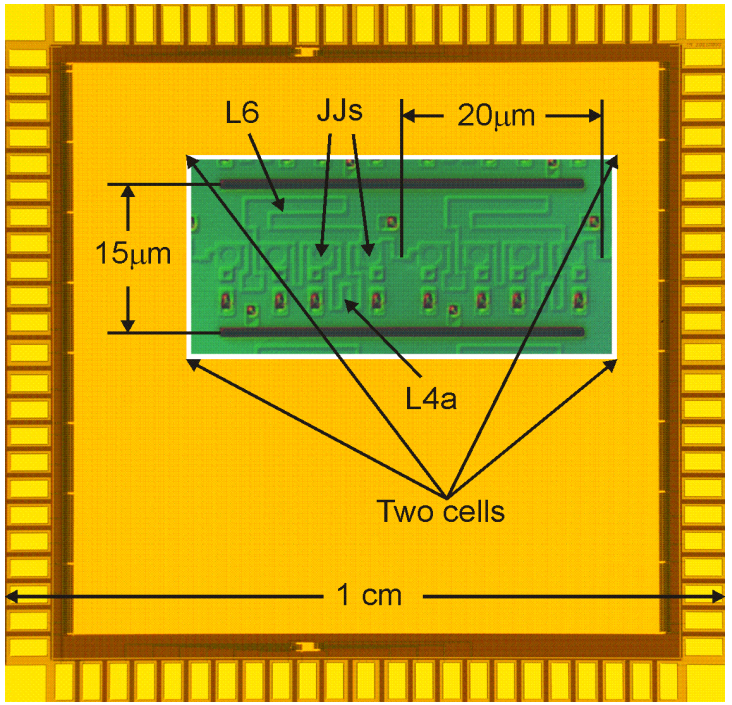
- Photolithography
  - 248-nm stepper (Canon) current process nodes
  - 193-nm scanner (ASML) for future nodes
- Photoresist processing and wafer cleaning tools
- Metal and dielectric deposition and etching tools
- Chemical-mechanical polishing
- Metrology tools: SEMs; film thickness, resistivity, and film stress mapping tools, etc.

Dedicated Tools Added to Enhance 200-mm SCE Fab Processing and Capabilities

- Sputter deposition tools for Nb, Mo, MoN_x, $NbTiN_x$
- High-density plasma (HDP) metal and dielectric etchers
- Low-temperature dielectric deposition tools
  - HDP gap fill and interlayer dielectric deposition
  - PECVD dielectric
- KLA-Tencor Altair defect inspection tool

MIT LL Current Technology Node SFQ5ee





Process Features

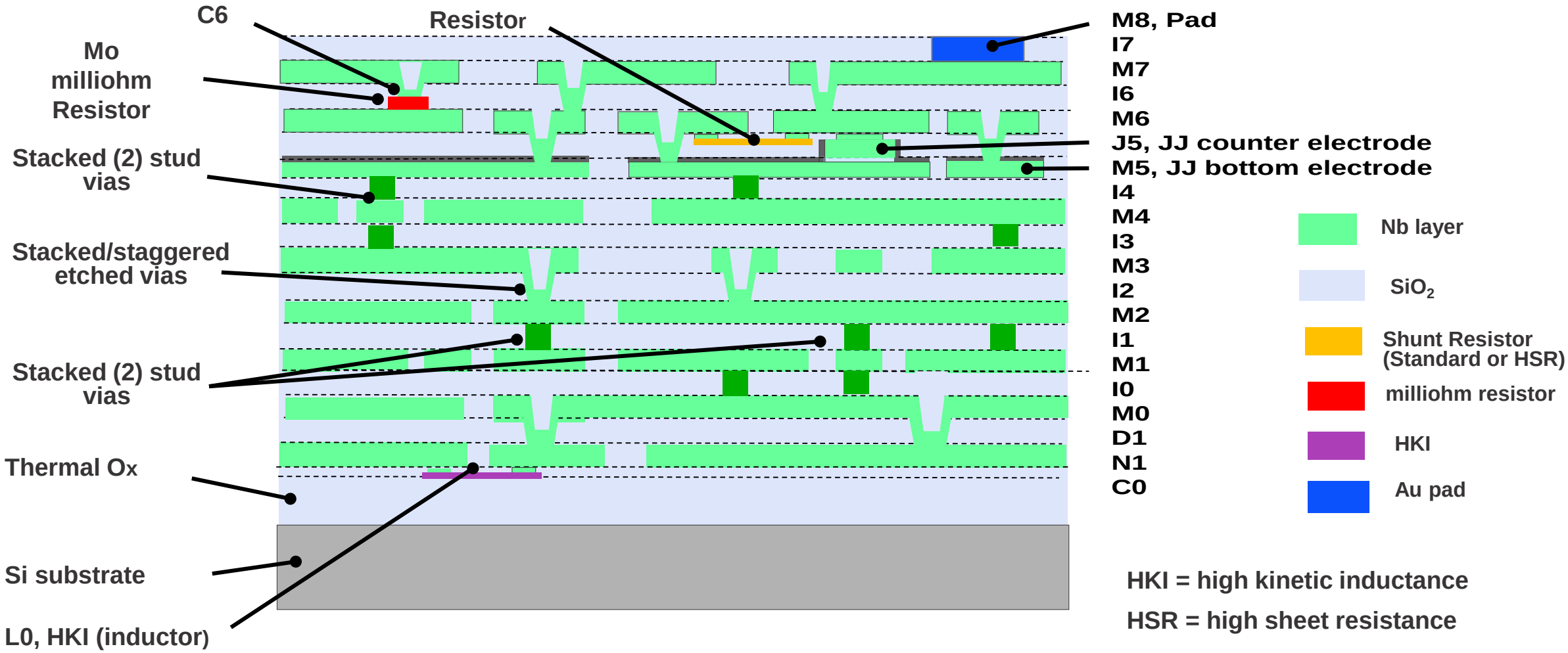
- Junctions: Nb/AlO_x-Al/Nb; J_c = 0.1 and 0.2 mA/μm^2
- Min JJ size: 700 nm
- Superconducting layers: 9
  - 8 niobium wiring layers
  - 1 layer of MoN_x (kinetic inductors)
- Resistors: 2 Ω/sq or 6 Ω/sq
- Min wiring linewidth: 350 nm

- AC-biased shift register: 202,280 bits
- 809,120 resistively shunted 1.25-μm^2 Josephson junctions − World record in JJ count
- Over 4 million inductors
- Fully operational; margins of all bit cells measured
- Integration scale: ≈ Intel's Pentium II, 0.8-μm process, 3.1M transistors on 294 mm^2 chip

V.K. Semenov, Y.A. Polyakov, and S.K. Tolpygo, *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4, 1301409, June 2017

SFQ6ee Process Node (1st Run Completed in Aug. 2017)

10 superconducting layers: 9 niobium + 1 MoN_x (kinetic inductors)
Pairs of stacked vias; smaller linewidth, surround, and spacing

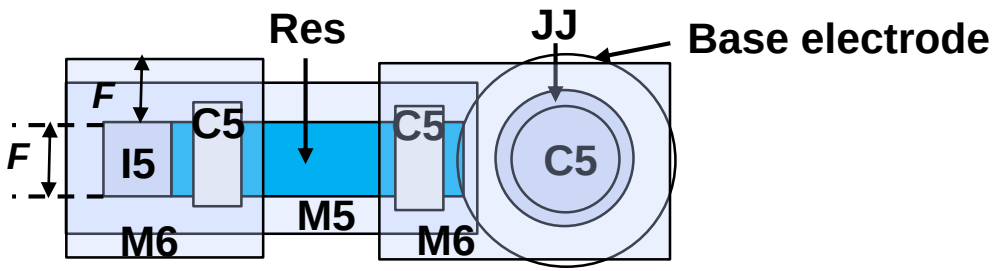


HKI = high kinetic inductance

HSR = high sheet resistance

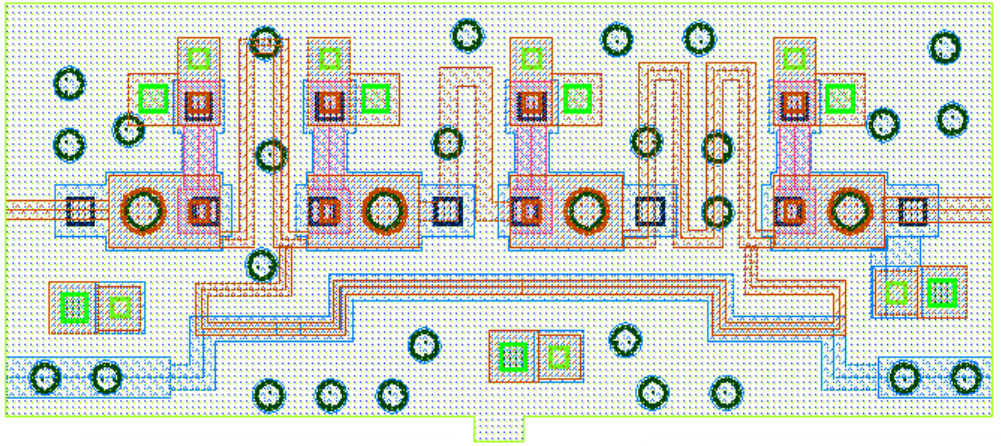
SFQ Circuit Density Limiters: Junctions

- The maximum circuit density is currently determined by the area of resistively shunted Nb/AlO_x-Al/Nb Josephson junctions (RSJ) and inductors
  - *Resistor area:* $A_R \sim (R_s/R_{sq})F^2 + 27F^2$, where F is the minimum feature size
  - *Inductor area:* $A_L = 2F(L/\ell) + 18F^2$, where ℓ is inductance per unit length
- Implementing self-shunted (high-J_c) junctions can increase JJ density by ~ 2× over the current 350-nm technology node with RSJs and by ~4× in 250-nm node
- Technology node with two layers of Josephson junctions has been developed at MIT LL

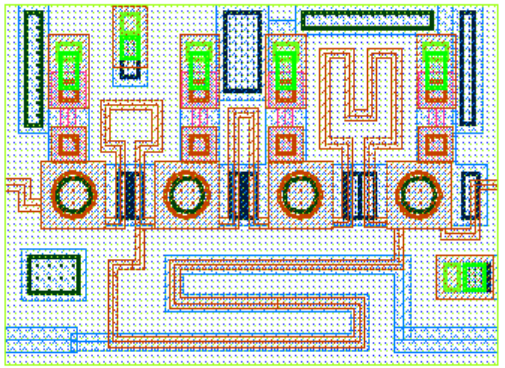


Resistively shunted junction

Shift Register Bit : 17 µm x 40 µm = 680 µm² in Gen 1

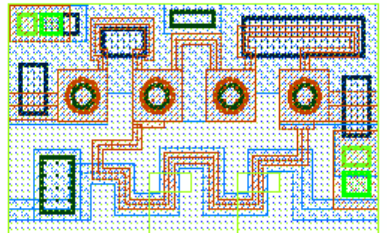


Gen 2



15 µm x 20 µm = 300 µm²

Gen 3

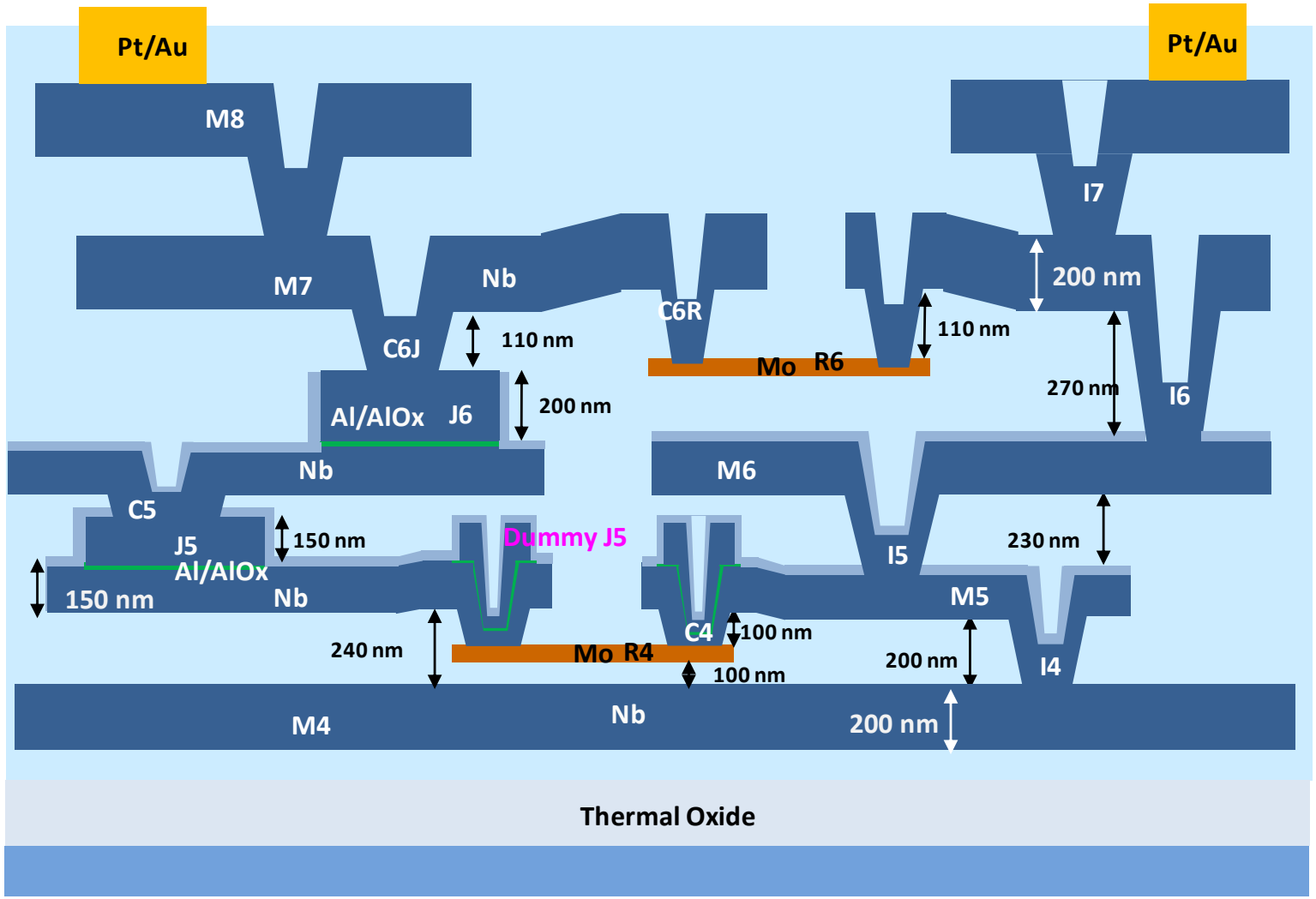


Self-shunted JJs with J_c = 0.5 mA/µm²
10 µm x 15 µm = 150 µm²
Linewidth: 350 nm
Density: 2.7×10⁶ JJ/cm²

MIT LL Process With Two Layers of Junctions

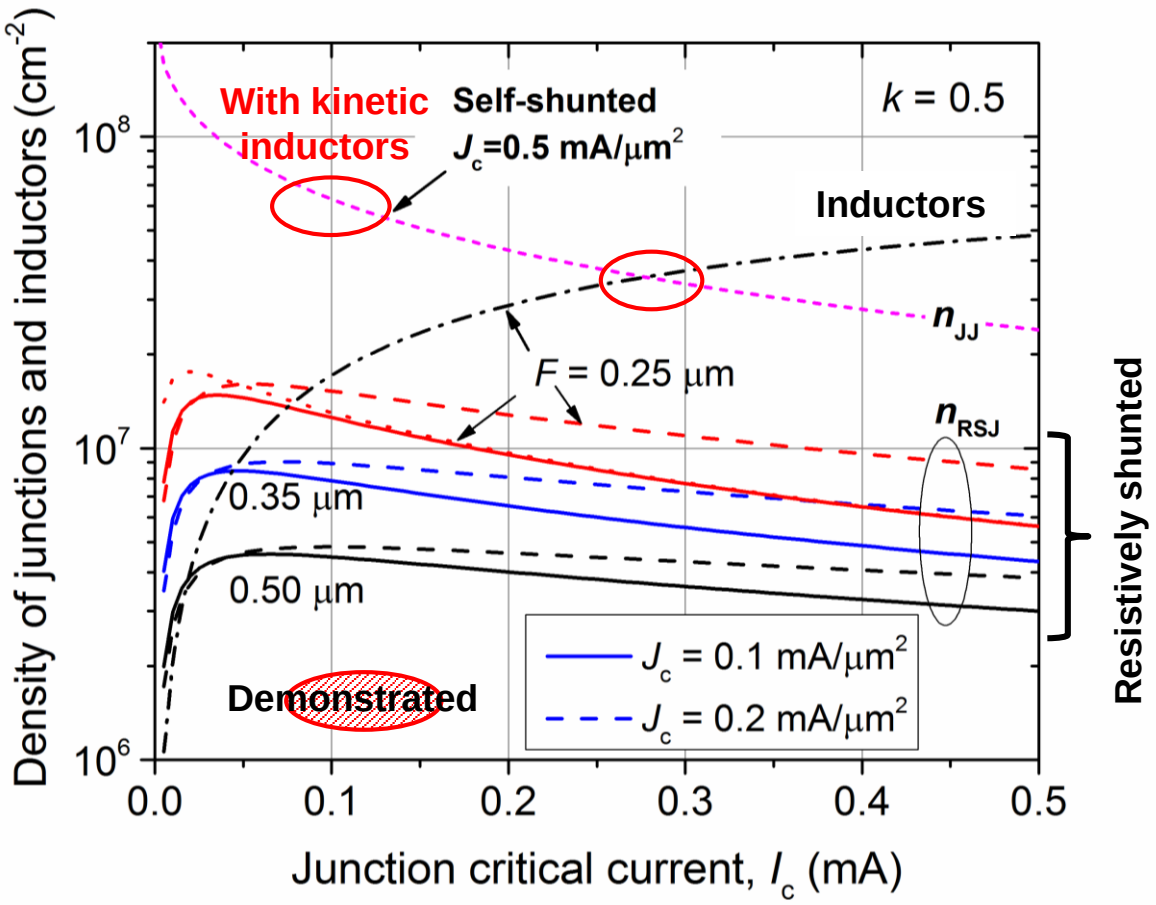
Process SE1

- Two layers of Nb/AlO_x-Al/Nb junctions (J5 and J6)
- Two layers of shunt resistors (R4 and R6): 2 Ω/sq and/or 6 Ω/sq
- Five planarized Nb layers
- First wafer lot completed in Sept. 2017
- Plan to add more Nb layers and bias kinetic inductors
- Provides 2x increase in circuit density



SFQ Circuit Density Limiters: Junctions and Inductors

- Each JJ needs an inductor $L \sim \frac{\beta_L \Phi_0}{2\pi I_c}$, where $\beta_L \sim 2 - 3$ is the cell design parameter
  - Inductor area $A_L = 2F(L/\ell) + 18F^2$, where ℓ is inductance per unit length, $\ell < 1$ pH/μm
  - Max circuit density is achieved when inductor density matches JJ density, $n_L \sim n_{JJ}$
  - Two or three layers of inductors can be used
  - Limits on minimum spacing and # of layers due to cross talk
- With self-shunted JJs, max circuit density becomes limited by the area of cell inductors
- Solution: replace geometrical (magnetic) inductors with low ℓ by compact kinetic inductors with $L_\square \sim 4$ pH/sq
- Implementation of self-shunted JJs and kinetic inductors can increase circuit density by more than 10x over the current 350-nm technology node



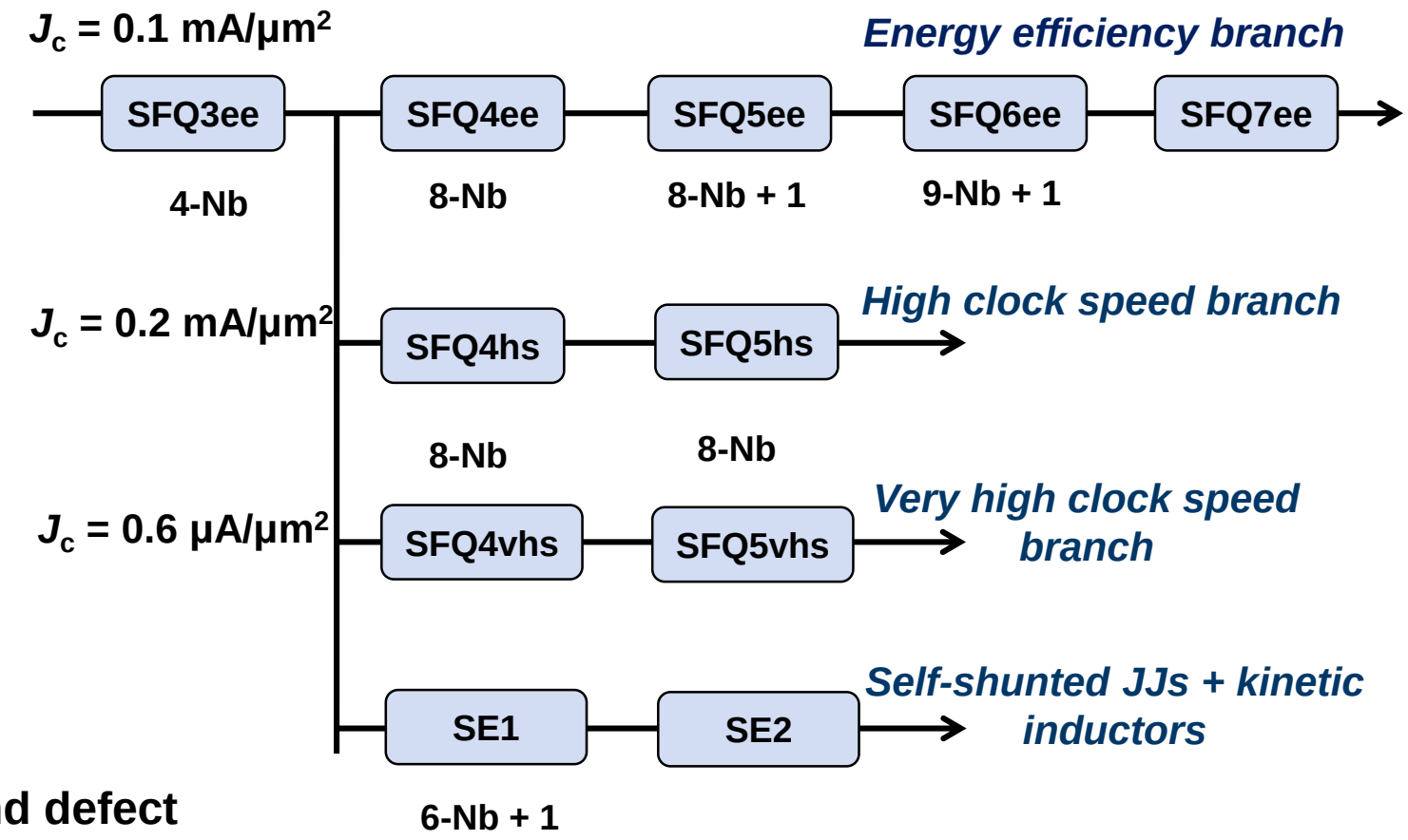
F – minimum feature size

I_c range of JJs used: 0.05 mA to 0.25 mA

Most often used: $I_c \sim 0.125$ mA

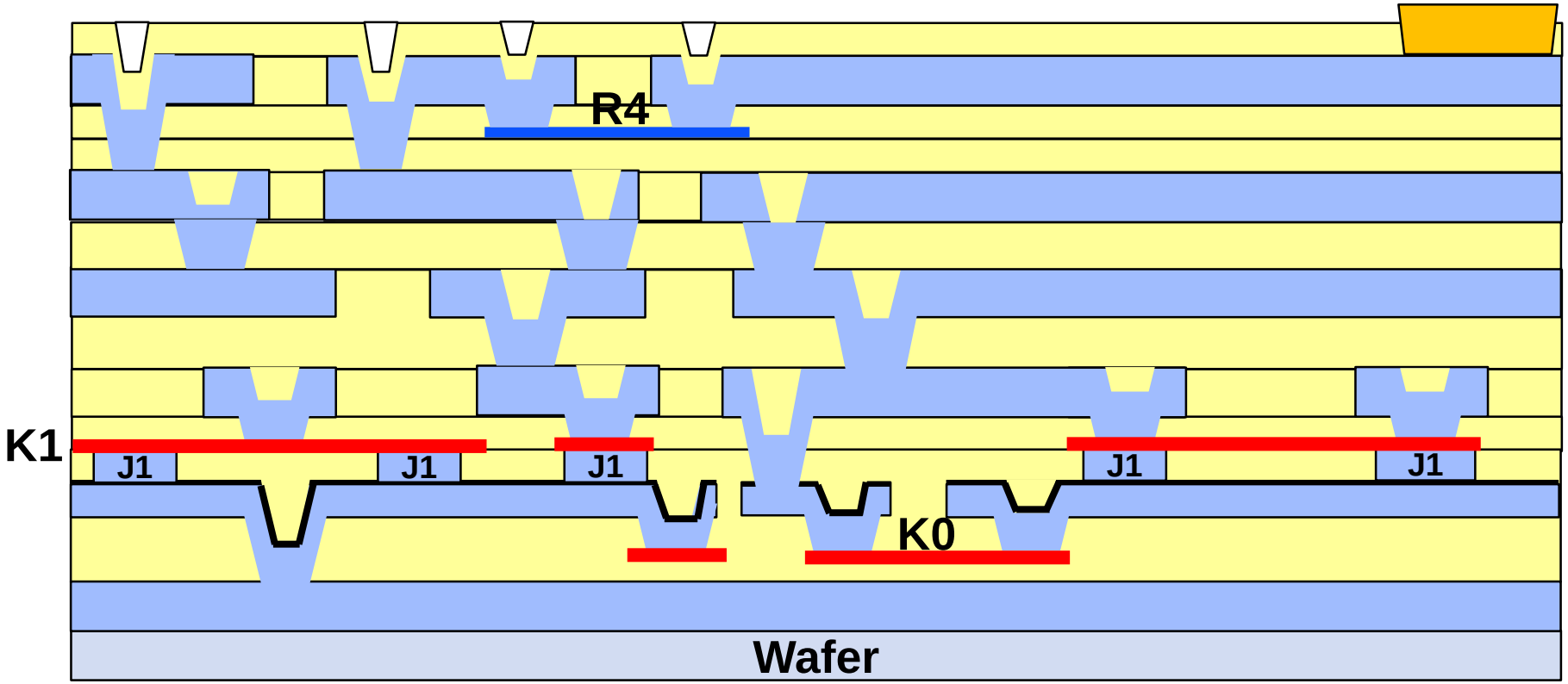
Process Development Directions

- Reduction of the linewidth to 250 nm and below
  - Nb and NbTiN wiring
  - Mo and MoN_x resistors
- Kinetic inductors
  - MoN_x and NbTiN
- Self-shunted high-J_c junctions
  - Nb/AlO_x-Al/Nb
  - Nb/Si:Nb/Nb
- Multiple (two) layers of junctions
- Stud vias and Damascene process
  - Etched Nb pillars
  - PECVD and PEALD: NbN_x, $NbTiN_x$, MoN_x
- Investigation of defects, circuit yield, and defect reduction



Process Cross Section

Process SE2: 1 layer of self-shunted JJs, 1 or 2 layers of kinetic inductors, six Nb layers, 1 layers of resistors



M6 – contact metallization

M5 – Nb layer

R4 – resistor

M4 – Nb layer

M3 – Nb layer

M2 – Nb layer

K1 – kinetic inductor

J1 – self-shunted JJ

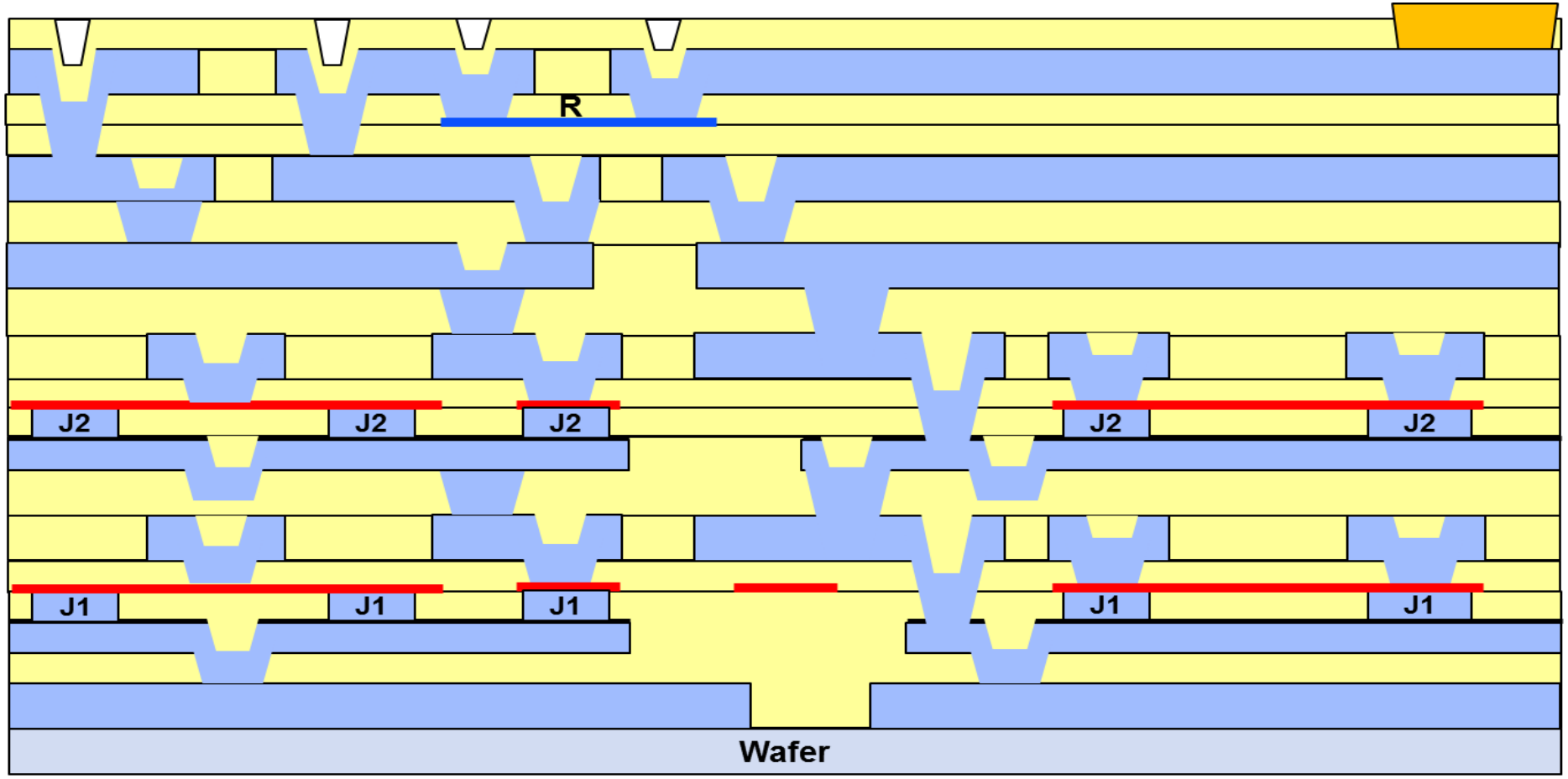
M1 – Nb Base Electrode

K0 – kinetic inductor

M0 – Nb Ground Plane

Target Process Cross Section

2 layer of self-shunted JJs, eight Nb layers, 2 layers of kinetic inductors, 1 layer of resistor (or bias inductors)



M12 – contact metallization
M11 – Nb layer
R – resistor

M10 – Nb layer

M9 – Nb layer

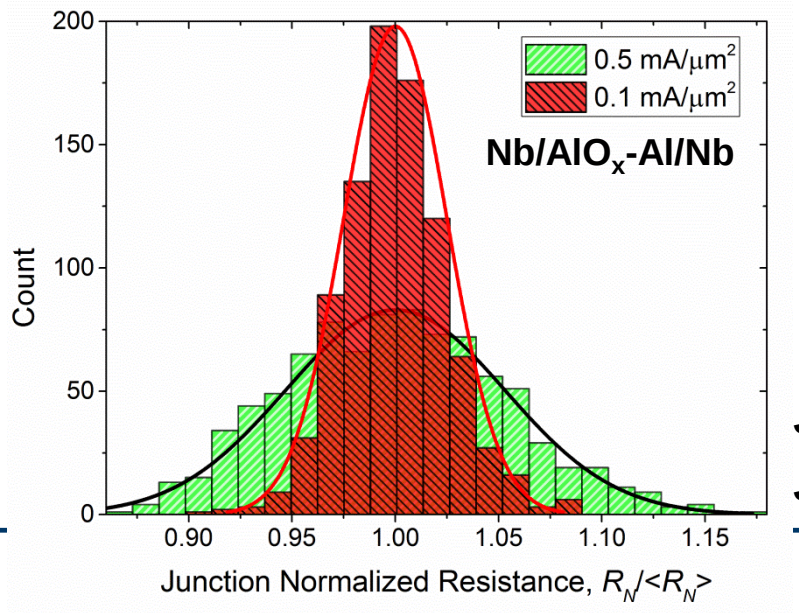
M8 – Nb layer
K2 – kinetic inductor
J7 – self-shunted JJ
M7 – Nb Base Electrode

M6 – Nb layer
K1 – kinetic inductor
J5 – self-shunted JJ
M5 – Nb Base Electrode

M4 – Nb Ground Plane

Self-Shunted High-J_c Junctions

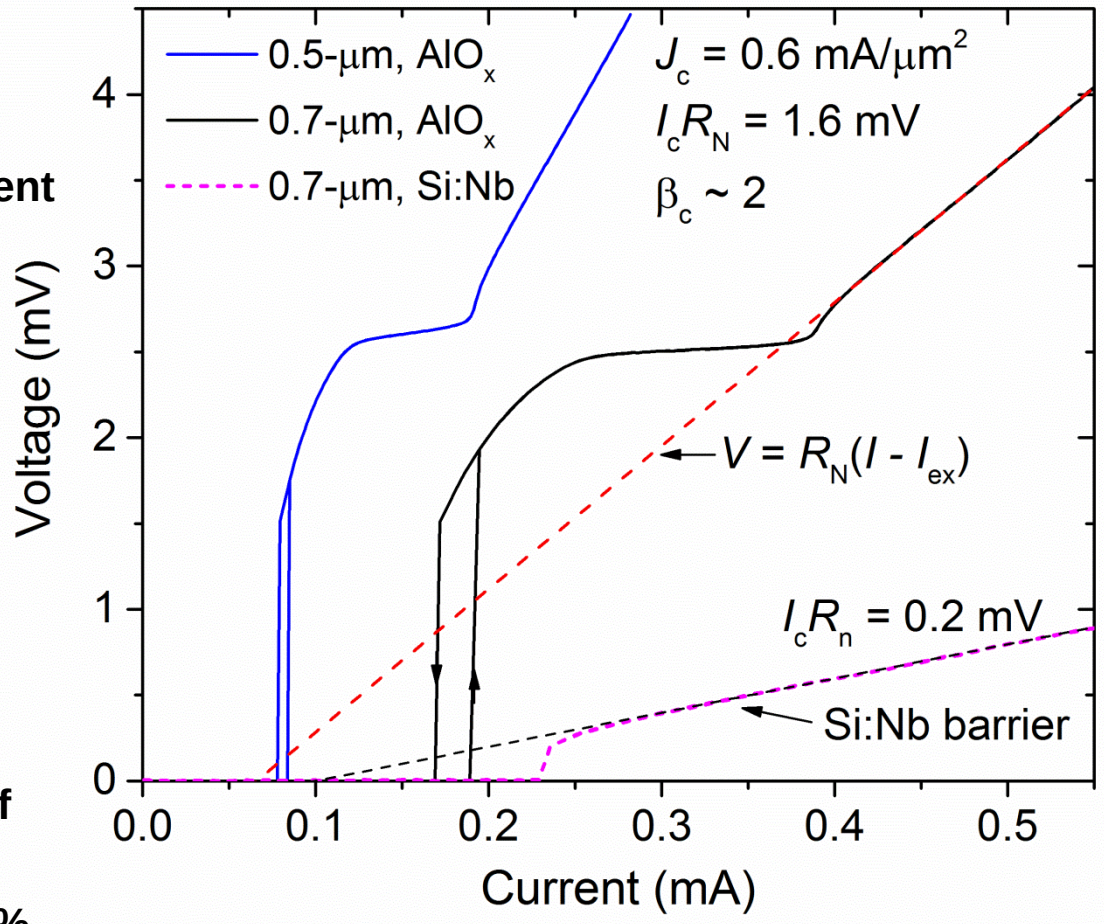
- At $J_c \approx 0.6$ mA/μm², Nb/AlO$_x$-Al/Nb tunnel junctions become self-shunted
  - $V_c \sim 1.6$ mV
  - $\beta_c \sim 2$
  - $1\sigma_{Ic} \sim 5\%$ for 0.5-μm dia JJs ($I_c \approx 85$ μA) – needs improvement
- Self-shunted Nb/Si$_{1-x}$Nb$_x$/Nb junctions, x = 0.1
  - $V_c = 0.2$ mV, a factor of 8 lower max clock frequency
  - $\beta_c \sim 1$
  - No advantages over the tunnel junctions found so far



On-wafer distribution of 0.7-μm JJs

$J_c = 0.1$ mA/μm²; 1σ = 2.3%

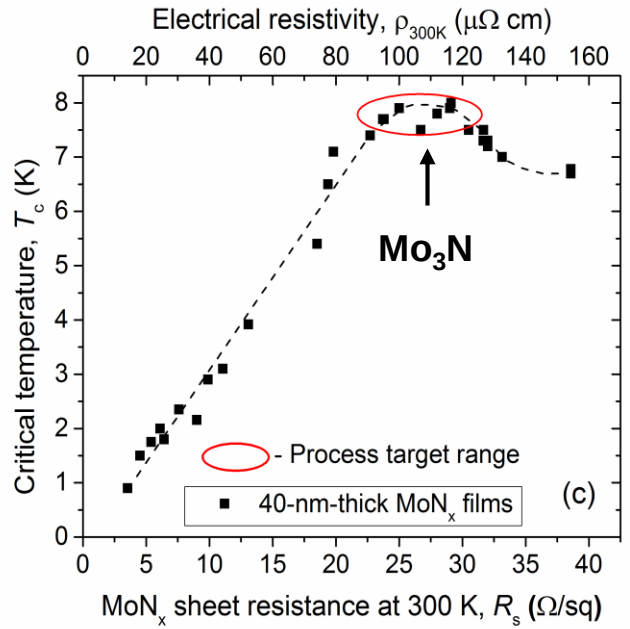
$J_c = 0.5$ mA/μm²; 1σ = 5.3%

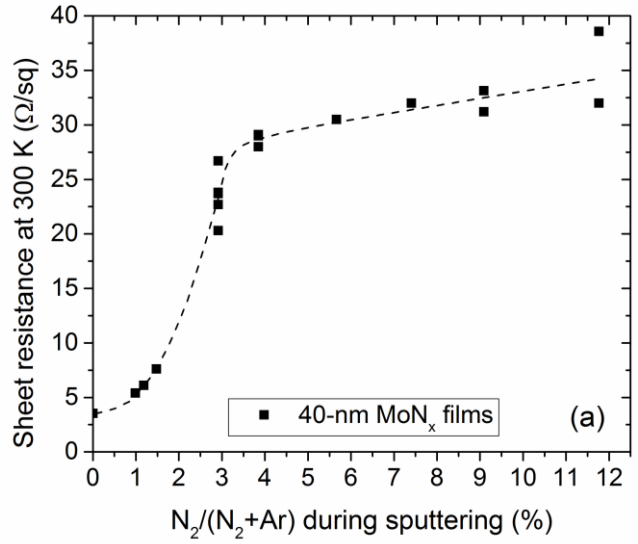


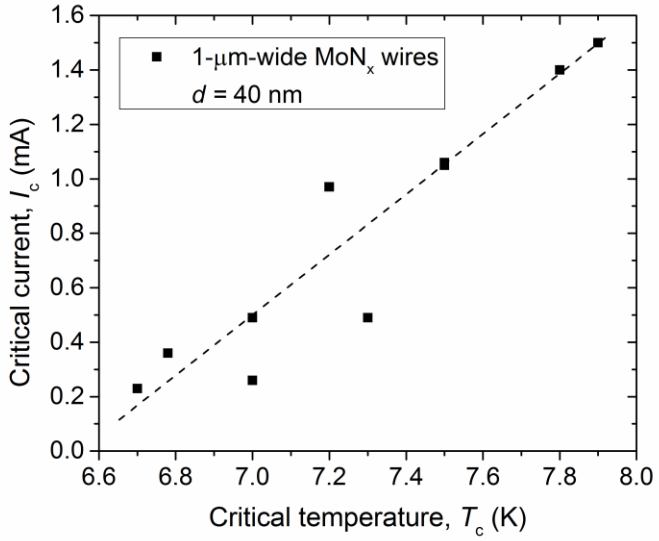
Fabrication and Properties of MoN_x Films

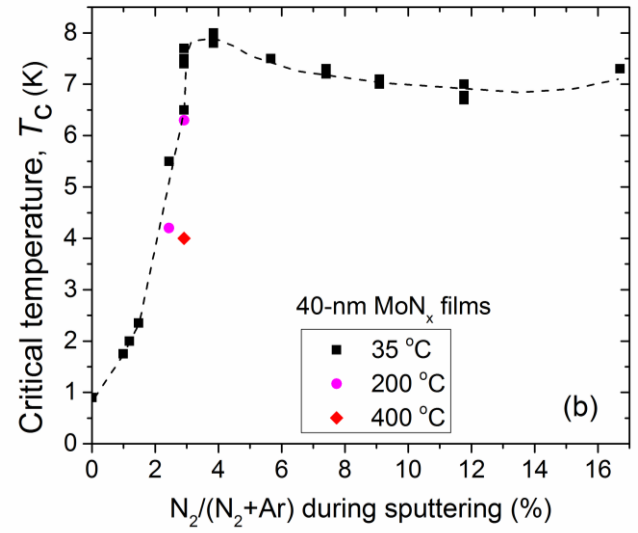
- **Amorphous MoN_x films**
  - **Highest T_c ~ 8 K**
  - **Optimal composition for inductors x ≈ 0.33**
  - **$J_c = 4 \cdot 10^6$ A cm^{-2}**
- **Reactive sputtering of Mo in N_2/Ar**
  - **Room-*T* deposition**
  - **200 mm wafers**
  - **Thickness uniformity 1σ = 2%**
  - **Optimum resistivity 110 μΩ cm**
- **Ti/MoN_x/Ti inductors**
  - **London penetration depth at 4.2 K: 510 nm**
  - **Sheet inductance: 8 pH/sq at 40 nm**
  - **On-wafer uniformity 1σ = 2.7%**
  - **Wafer-to-wafer inductance variation 1σ = 4%**
  - **Kinetic inductor flux storage per unit length:**

$$LI_c \approx 4.4\Phi_0/\mu m$$









London Penetration Depth and Kinetic Inductance of MoN_x Films

Measurement Techniques

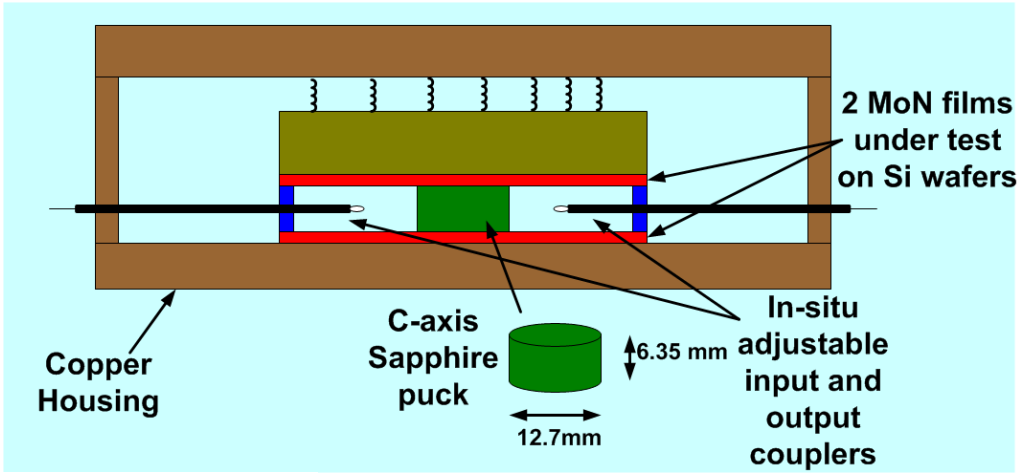
- **Sapphire dielectric resonator technique**
  - $f_r = 9.7$ GHz
  - $Q > 30{,}000$

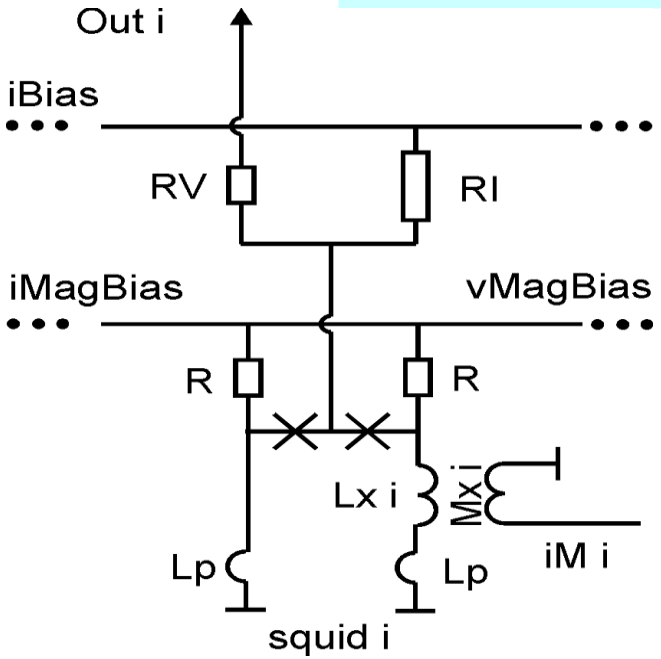
$$f_r(T)/f_r(4.2\text{K}) = 1 - 2g\cdot[\lambda_{eff}(T) - \lambda_{eff}(4.2\text{K})]$$

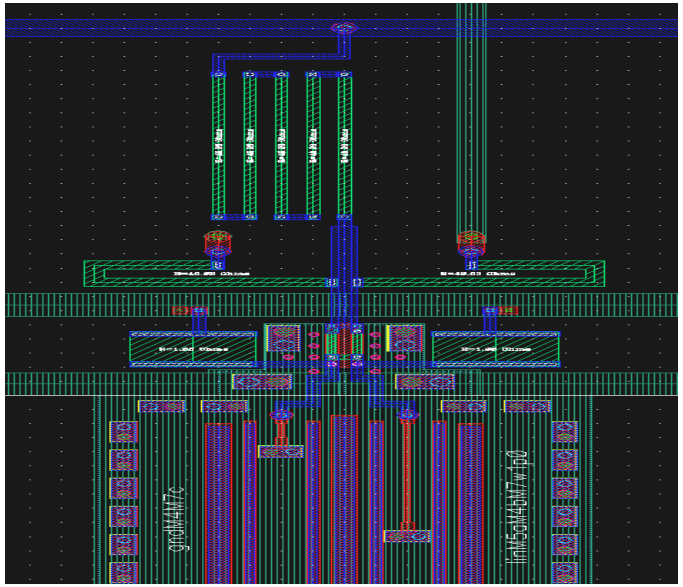
$$\lambda_{eff} = \lambda\coth(d/\lambda)$$

$$\lambda(T) = \lambda_0/[1 - (T/T_c)^4]^{1/2}$$

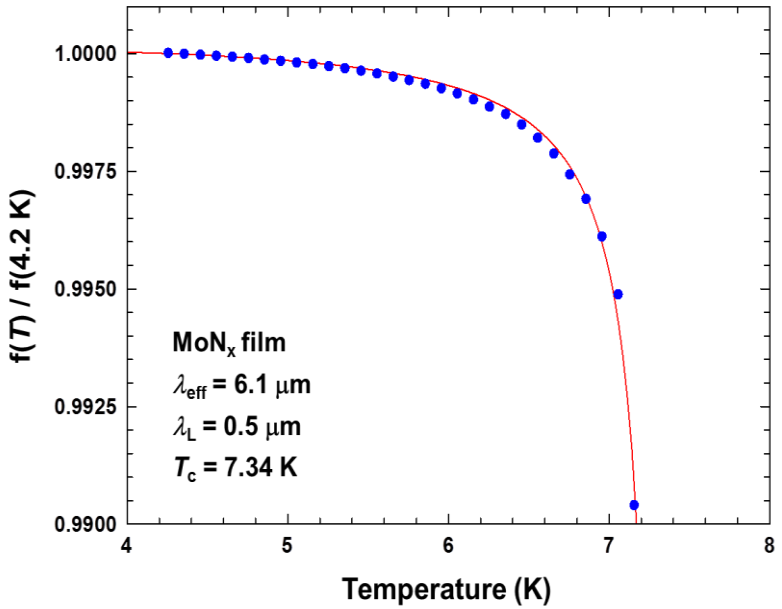
- **dc-SQUIDs with patterned MoN_x inductors**
  - Sheet inductance from the modulation period
  - Inductor widths from 0.5 μm to 2 μm
  - Inverted microstrip and unshielded strips
  - Multiple SQUIDs per chip can be measured

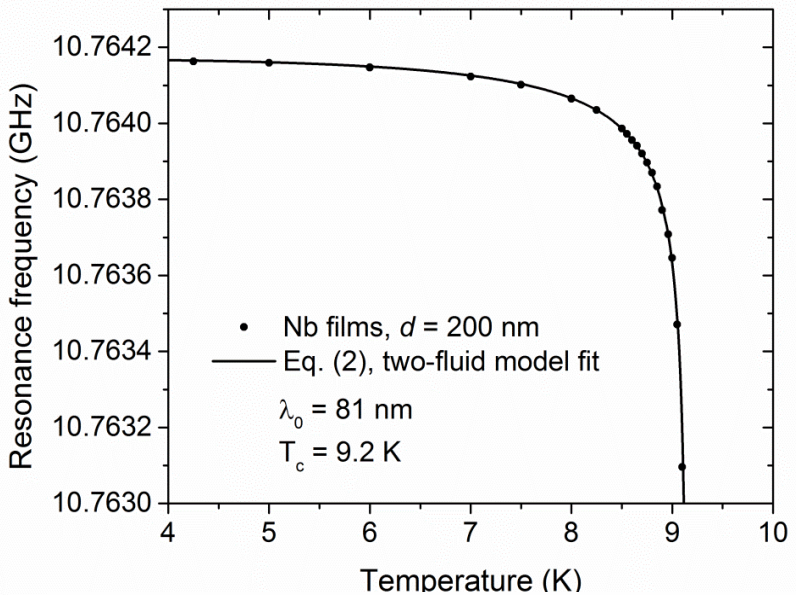


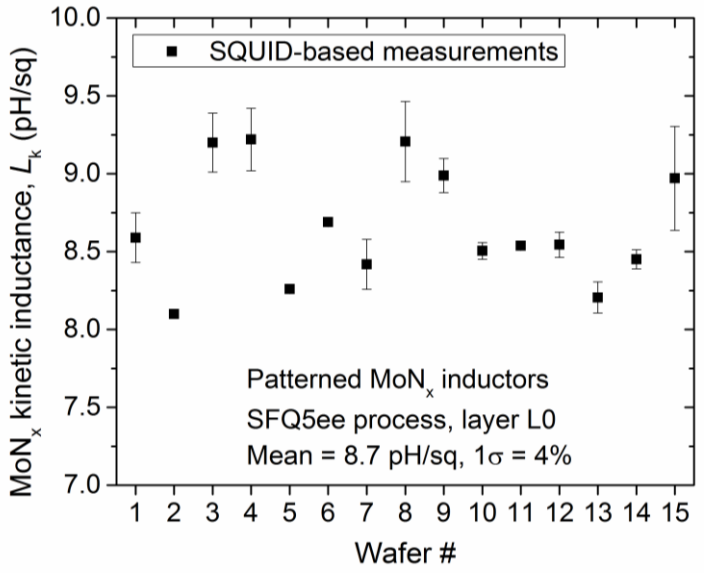




Results on λ_L and Kinetic Inductance of MoN_x Films



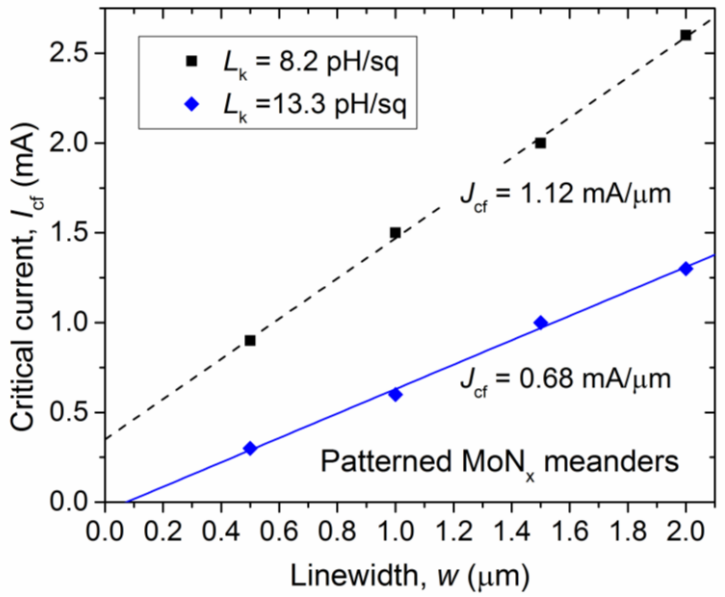


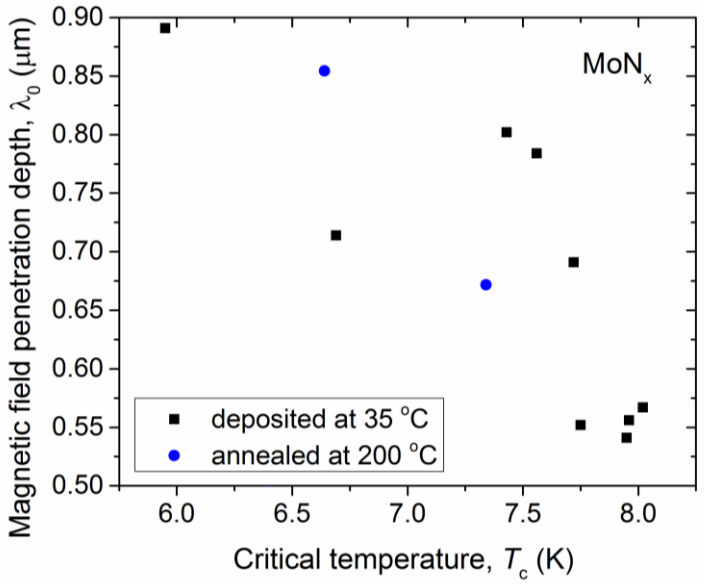


- **Critical current $I_c \sim 1/L_k$**

$$I_{GL}L_k = \Phi_0 w l/(3\sqrt{3}\xi)$$

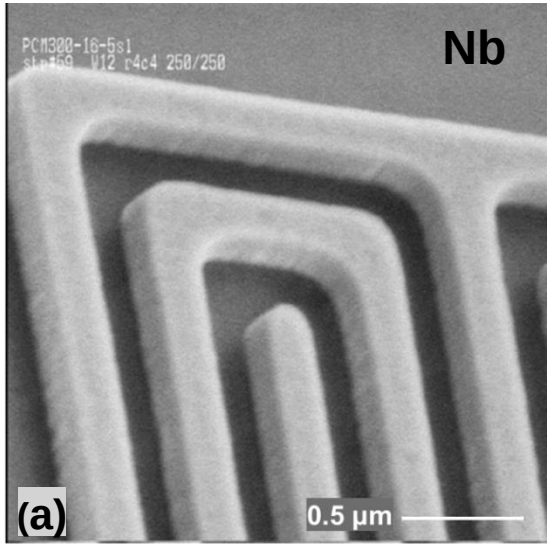
  - **In thin $MoN_{0.33}$ films, $L_k I_c l/w$ product is ≈ 9.1 pH·mA/μm or $4.4\Phi_0$/μm**

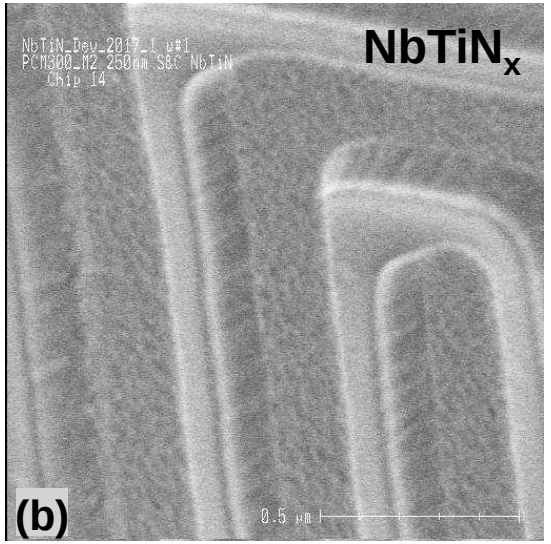




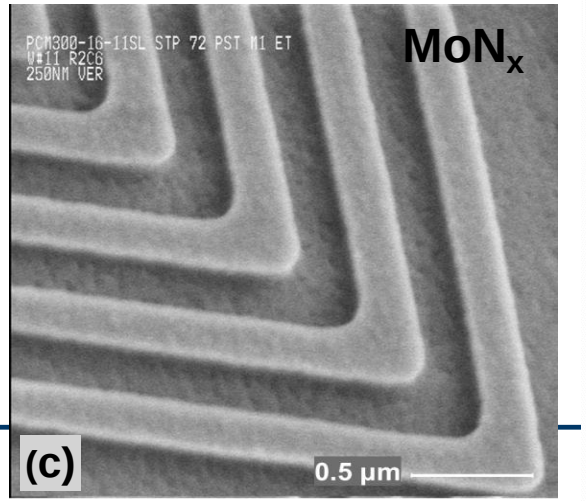
250-nm Nb and NbTiN Inductors and MoN_x Resistors

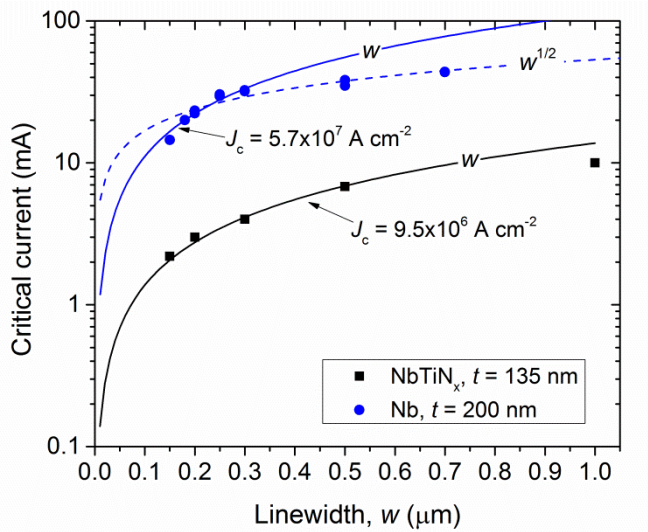
- **250-nm Nb wiring**
  - On-wafer uniformity 1σ = 3.9%
  - Wafer-to-wafer variation 1σ = 4.2%
  - I_c = 25 mA
- **250-nm NbTiN (reactive sputtering)**
  - T_c = 14.5 K
  - $I_c \approx$ 3.5 mA (needs improvement)
  - $J_c = 9.5\times10^6$ A/cm^2 (95 mA/μm^2)
- **250-nm Ti/MoN_x/Ti resistors**
  - Thickness 40 nm for 6 Ω/sq
  - On-wafer uniformity 1σ = 2.7%
  - Wafer-to-wafer variation 1σ = 2.6%
- **PEALD NbTiN for 250-nm via Damascene process**
  - T_c = 9.7 K
  - $J_c = 2\times10^5$ A/cm^2 (needs improvement)





SEM images of the etched features with 250-nm width and 250-nm spacing. Note difference in surface roughness of NbTiN.





Summary

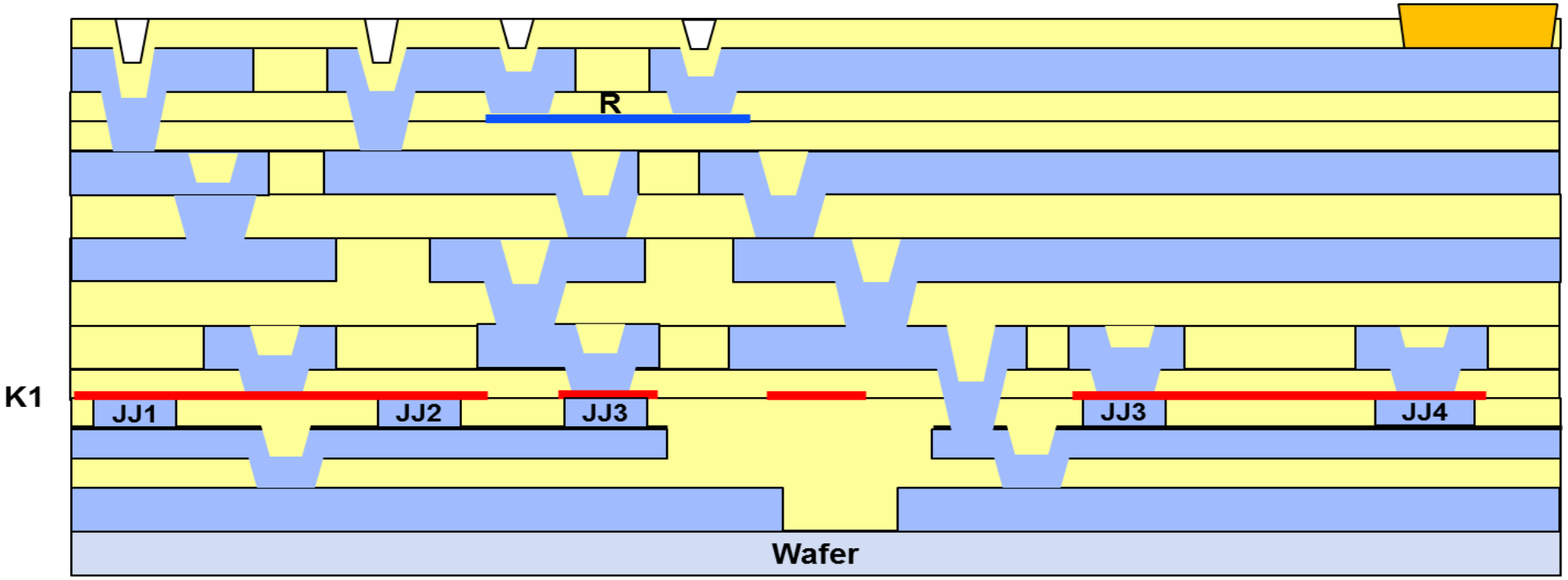
- We have made substantial progress breaking into VLSI and demonstrating SFQ circuits with ~ 1M JJs
- Superconductor electronics fabrication requires further innovations to grow the integration scale
- We have implemented high-J_c self-shunted Nb/AlO_x-Al/Nb junctions (J_c = 0.6-mA/μm^2)
- We have developed and implemented in the fab processes
  - Two layers of Josephson junctions
  - 250-nm Nb wiring
  - MoN_x kinetic inductors
  - 250-nm features Mo and MoN_x resistors
- We continue working on
  - Process with two JJ layers: different J_cs
  - Investigation of Nb:Si barrier junctions
  - Full integration of kinetic inductors into SFQ logic/memory cells
  - CVD-filled interlayer vias
  - Defect reduction and circuit yield improvements

Thank you very much for your attention

Questions?

Process Cross Section (v. 1)

1 layer of self-shunted JJs, six Nb layers, 1 layer of kinetic inductors, 1 layer of resistor (or bias inductors)



M10 – contact metallization
M9 – Nb layer
R – resistor

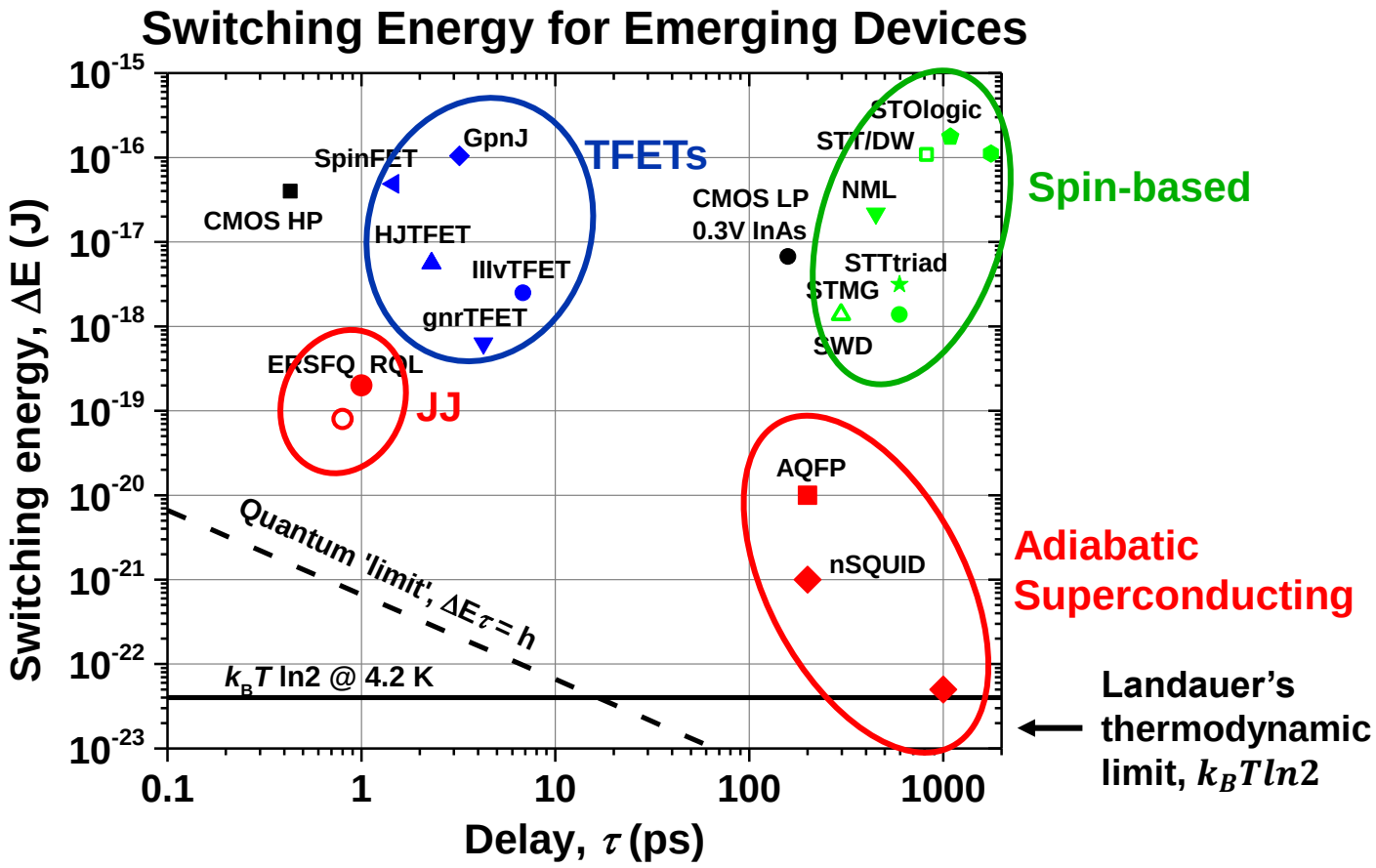
M8 – Nb layer

M7 – Nb layer

M6 – Nb layer
K1 – kinetic inductor
J5 – self-shunted JJ
M5 – Nb Base Electrode

M4 – Nb Ground Plane

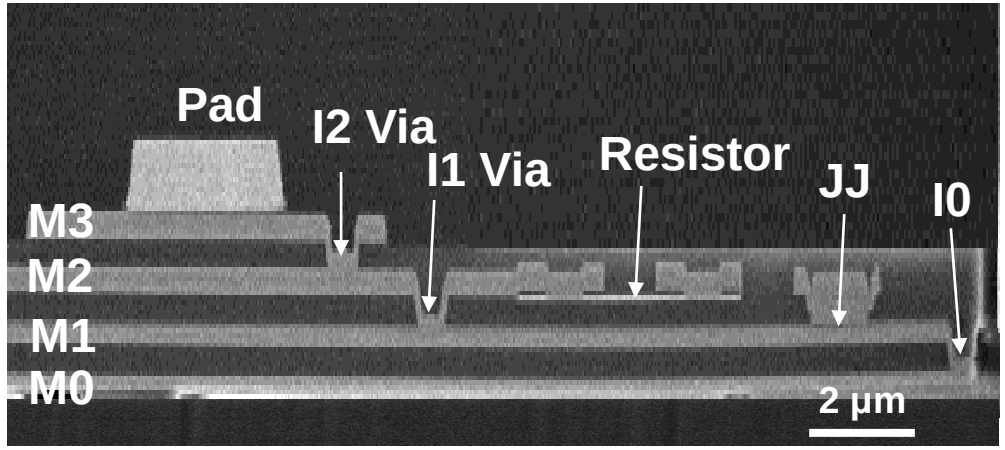
Beyond CMOS Technologies



Superconducting electronics based on Josephson junctions has demonstrated the lowest energy per operation (~ 10^{-22} J), the highest clock speeds (up to 770 GHz), and is more mature than other beyond-CMOS technologies

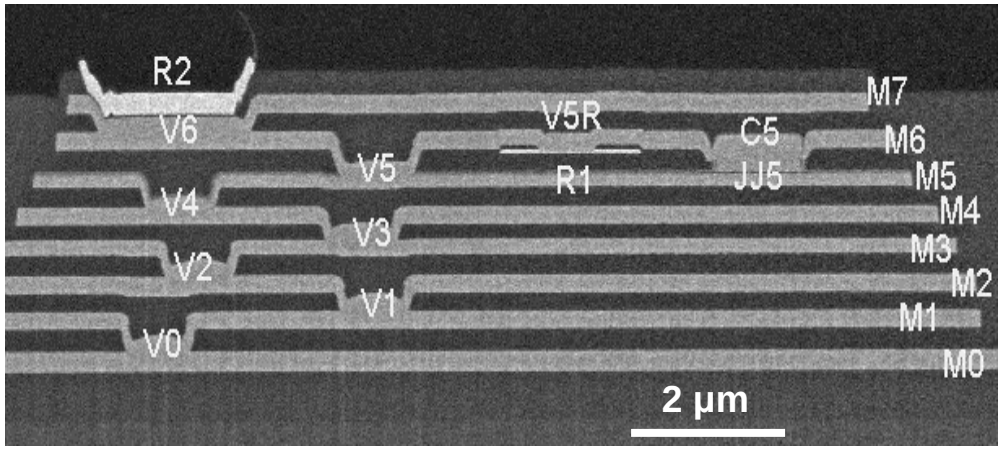
MIT LL Superconducting Electronics Fabrication

4-layer node SFQ3ee, 2012



- Wafer size: 200 mm
- Number of Nb layers: 4
- Resistors: Pt, 2 Ω/sq, lift-off
- Min JJ size: 700 nm
- Min wiring size: 700 nm
- Min spacing: 1000 nm

8-layer node SFQ4ee, 2014



- Wafer size: 200 mm
- Number of Nb layers: 8
- Resistors: Mo, 2 Ω/sq, etched
- Min JJ size: 700 nm
- Min wiring size: 500 nm
- Min spacing: 700 nm