Development of an rf-waveform synthesizer with quantum-based accuracy

EUCAS 2017

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David Olaya, Christine A. Donnelly, Peter Hopkins, Paul Dresselhaus, and Sam Benz

Create quantum-based signal sources

Spanning the entire RF frequency spectrum from 100 kHz to 100 GHz

- Near-perfect signal purity
- Quantum-accurate amplitude (up to 100 mV)
  - Voltage level: 0.2 V at 1 MHz demonstrated by J. Brevik[1]
- Programmable

Customers

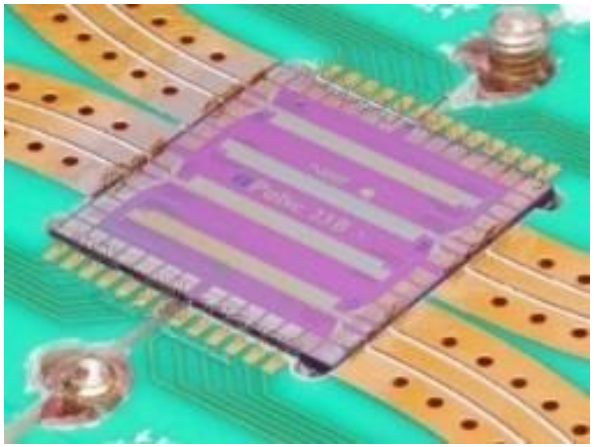
- Metrology labs worldwide
- Wireless communications industry
- RF spectrum users including defense applications

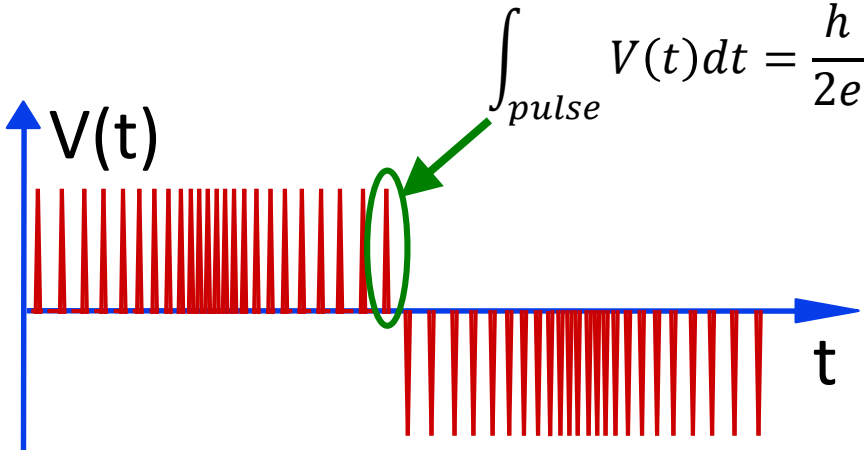
[1] (4EP2-24) Megahertz Waveform Synthesis with the Josephson Arbitrary Waveform Synthesizer

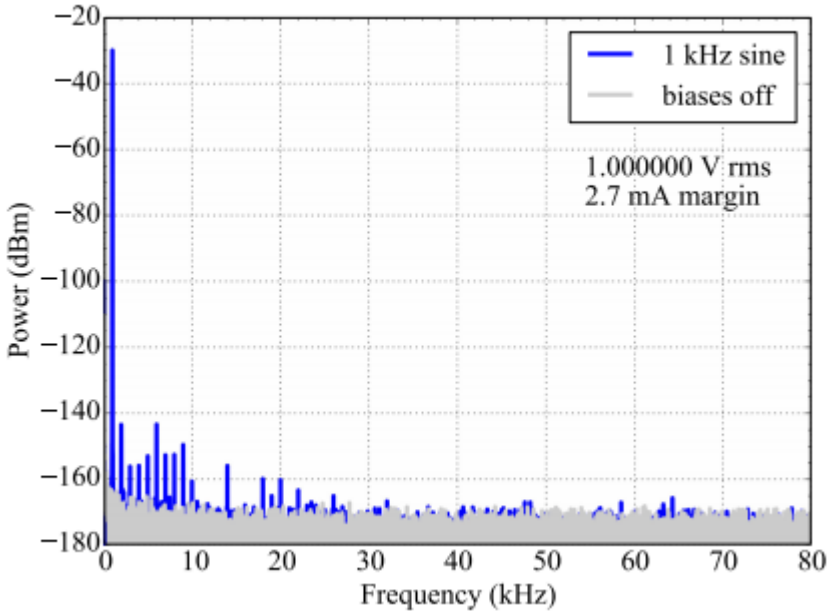
Quantum accurate waveform synthesis

NIST Josephson arbitrary waveform synthesizer (JAWS) with arrays of pulse-driven Josephson Junctions

- 10Hz to 1MHz Frequencies (>1 V)
- PPM accuracy (f<20 kHz)
- Great SFDR performance







(2EO2-07) Quantum Voltage Standard Developments at NIST
S. Benz

NIST

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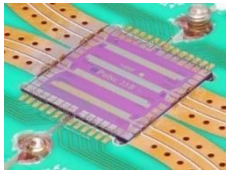

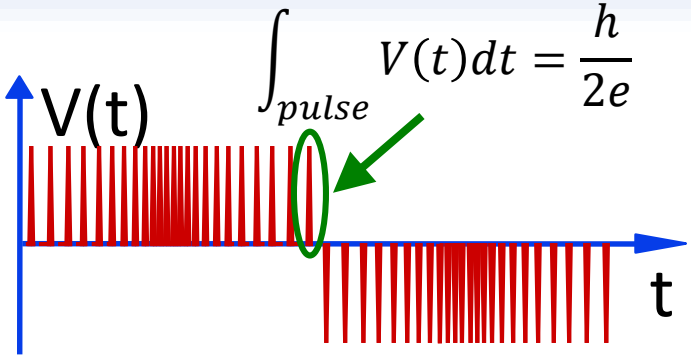

Several suggestions for SFQ-based-DACs

- Frequency modulation of output SFQ pulse train V. K. Semenov, C. Hamilton.
- Switching of multiplication factor in a voltage multiplier. M. Maezawa , F. Hirayama, and M. Suzuki (AIST)
- Use of RSFQ voltage drivers for biasing of large junction arrays. Niemeyer, *et. al.* (PTB)
- Direct Digital Synthesizer (Gigahertz output) O. Mukhanov, *et. al.* (HYPRES)

All suggested implementations imply maximum frequencies in the megahertz!

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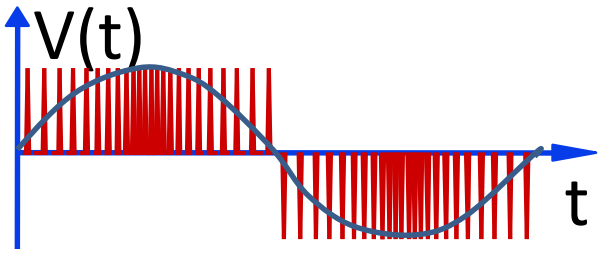
rf Arbitrary Waveform Synthesizer requires fundamental redesign

Goals

- Near-perfect signal purity
- Quantum-accurate amplitude (up to 100 mV)
- Output frequencies at the tens of gigahertz



Challenges

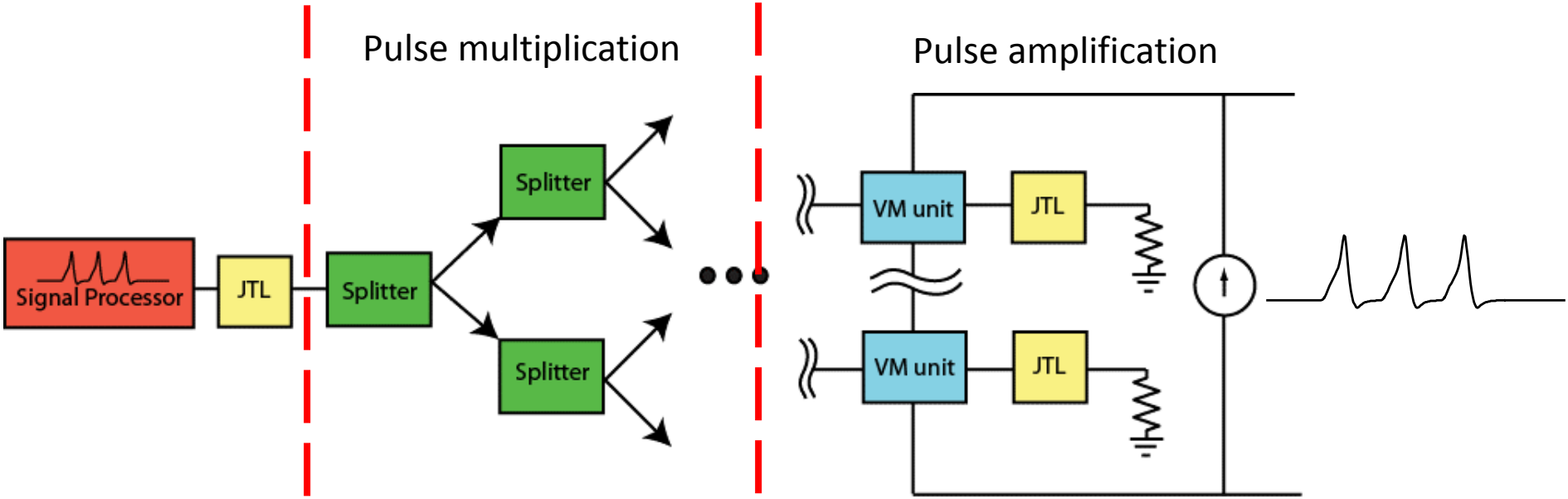
1. **Faster Clocking:** SFQ circuits, higher current density junctions
2. **Signal Purity:** [1] Σ–Δ modulation scheme, Low-pass -> Bandpass
3. **Amplification:** Preserve quantized amplitude, timing, and signal purity
4. **Signal Transmission:** [2] 4K -> 300K, 50 ohms loading
   Collaboration with Communications Technology Laboratory.

[1] (1EP1-10) C. Donnelly
[2] (4EP2-24) J. Brevik

NIST Starting Point

Milestone #1: 1 GHz , 1 mV

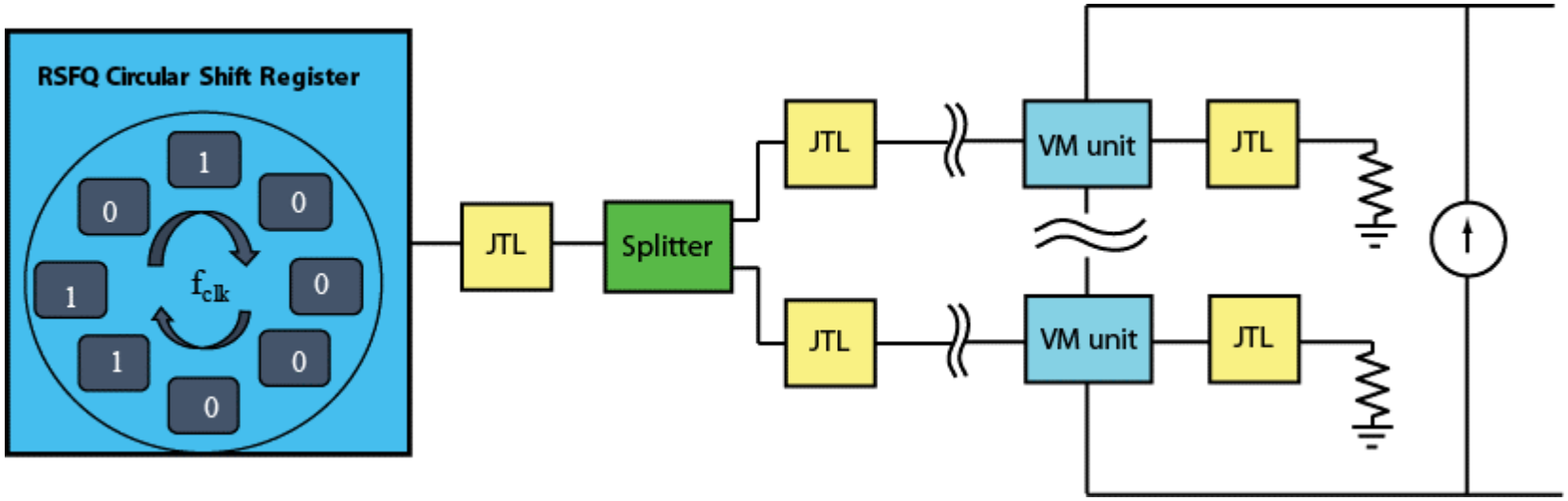
First Step: Δ–Σ SFQ pulse train generation + Voltage Multiplier



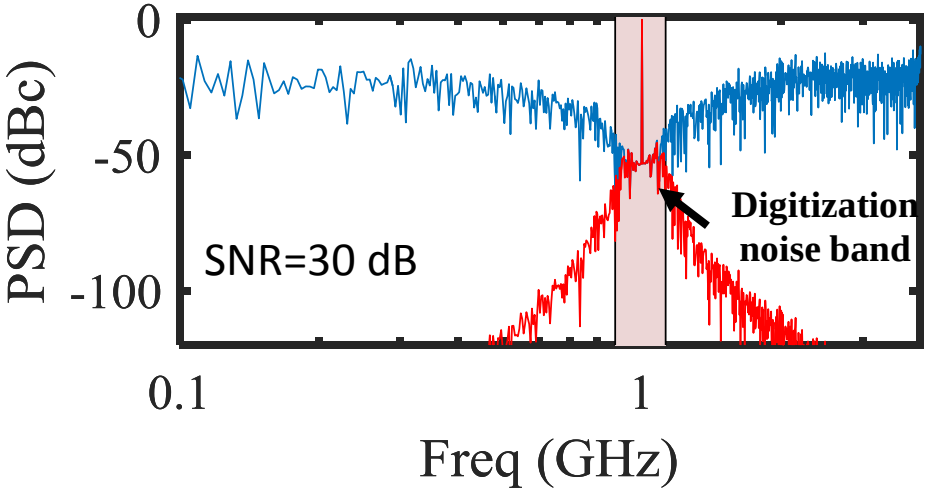
1. Clock speed limit
2. Signal purity, Σ–Δ modulation scheme
3. Quantum-accurate amplification
   - pulse timing/synchronization
4. Signal transmission to 50 ohm load

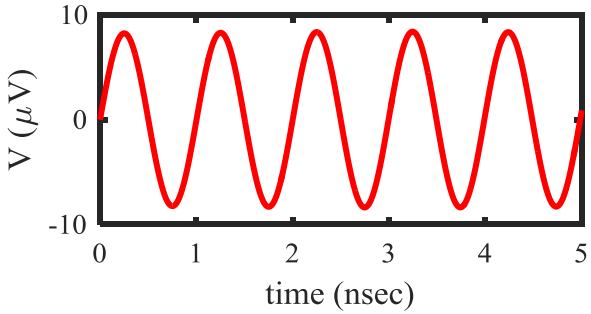
Full Implementation of RSFQ Synthesizer

Plan: for now we will just worry about a unipolar signal loaded into a circular shift-register. Pulse density technique using Σ–Δ modulation



Simulation





Requires gain of 64

Shift register size of 2048 bits
Clocked at 8 GHz
Signal frequency 1 GHz
Noise band 250 MHz

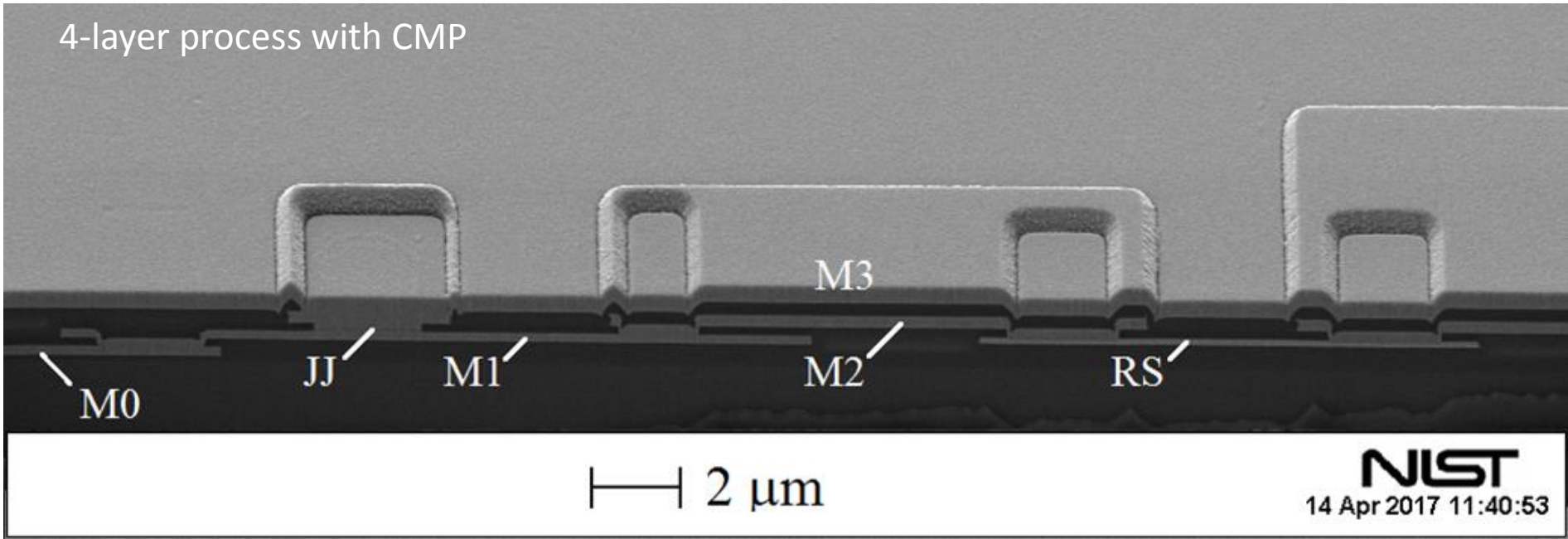
NIST Fabrication Process

NIST cell library using self-shunted Josephson junction: fabrication process includes Nb electrodes with tunable Nb-doped silicon barrier junctions.

Process details

- Nb wiring and ground layers
- Nb-doped Si junction barriers close to metal-insulator transition
- 4 metal layers
- Slightly underdamped junctions (β ~ 1.5)

- Target $I_c R = 250\ \mu\text{V}$
- $J_c = 4.5\ \text{kA/cm}^2$ (capable of doing up to $100\ \text{kA/cm}^2$)



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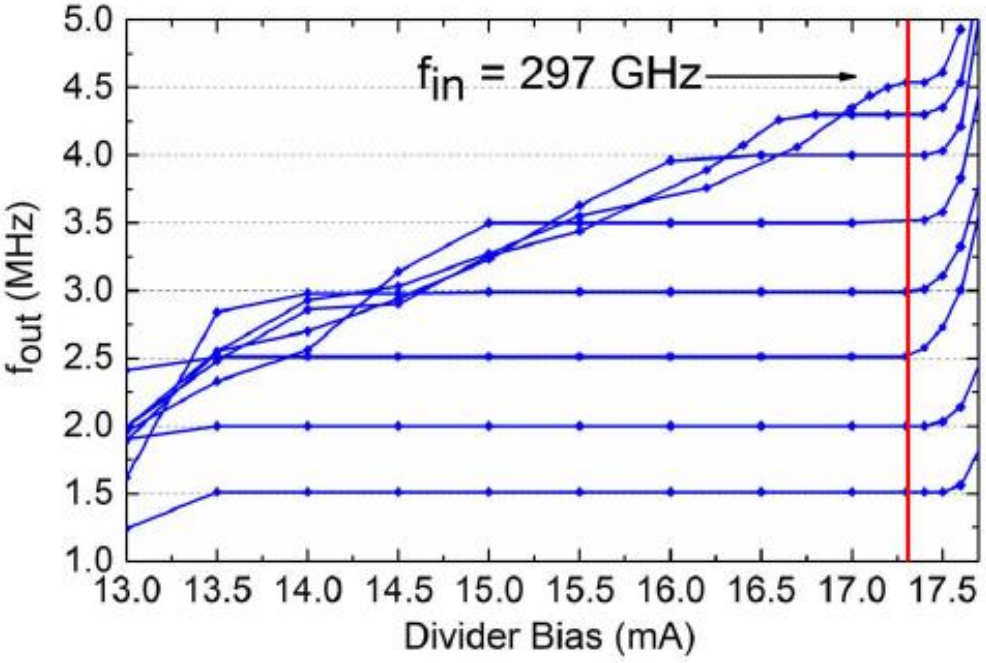
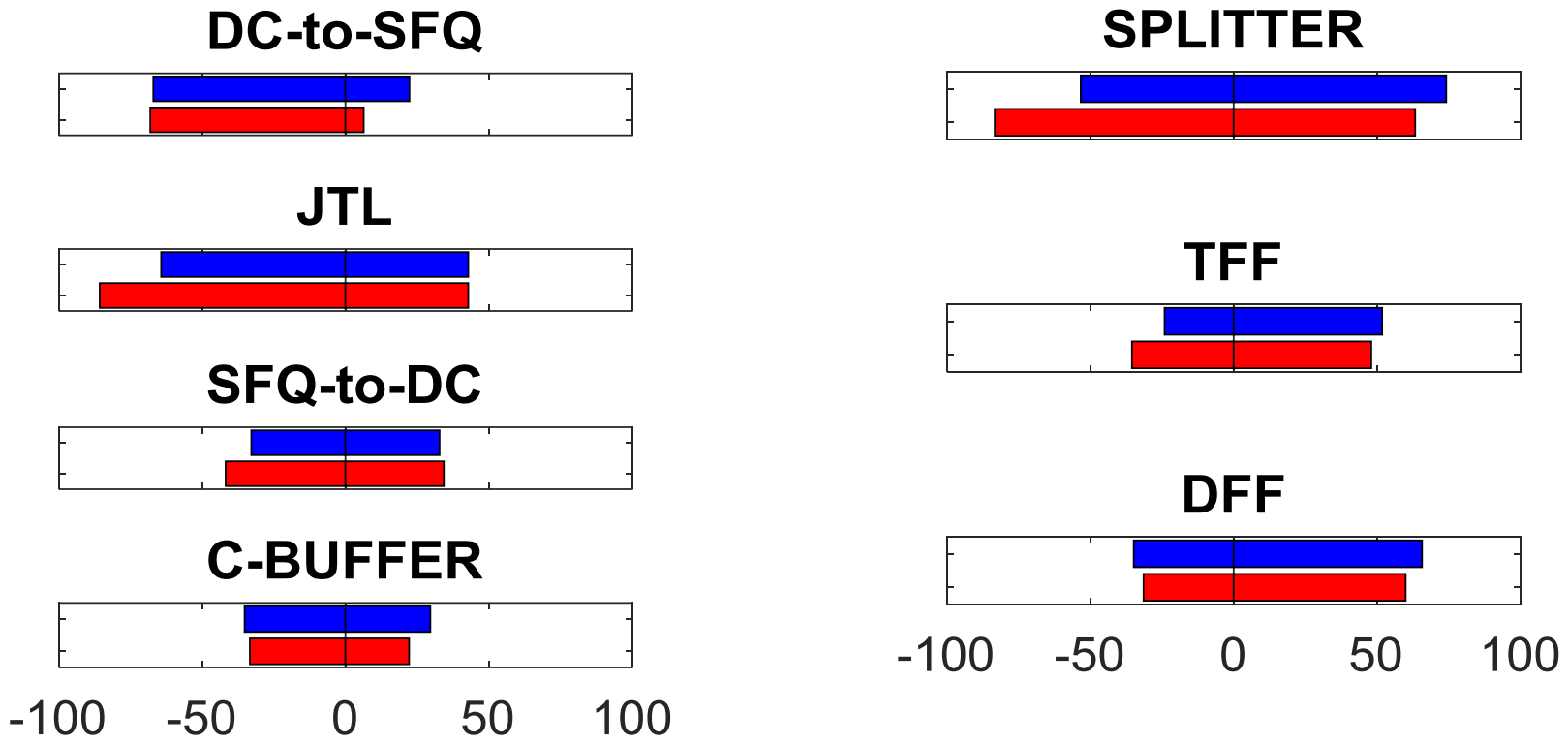


David Olaya, *et al.* "300-GHz Operation of Divider Circuits Using High-Jc $Nb/Nb_xSi_{1-x}/Nb$ Josephson Junctions." IEEE Trans. Appl. Supercond, VOL. 25, NO. 3, JUNE 2015

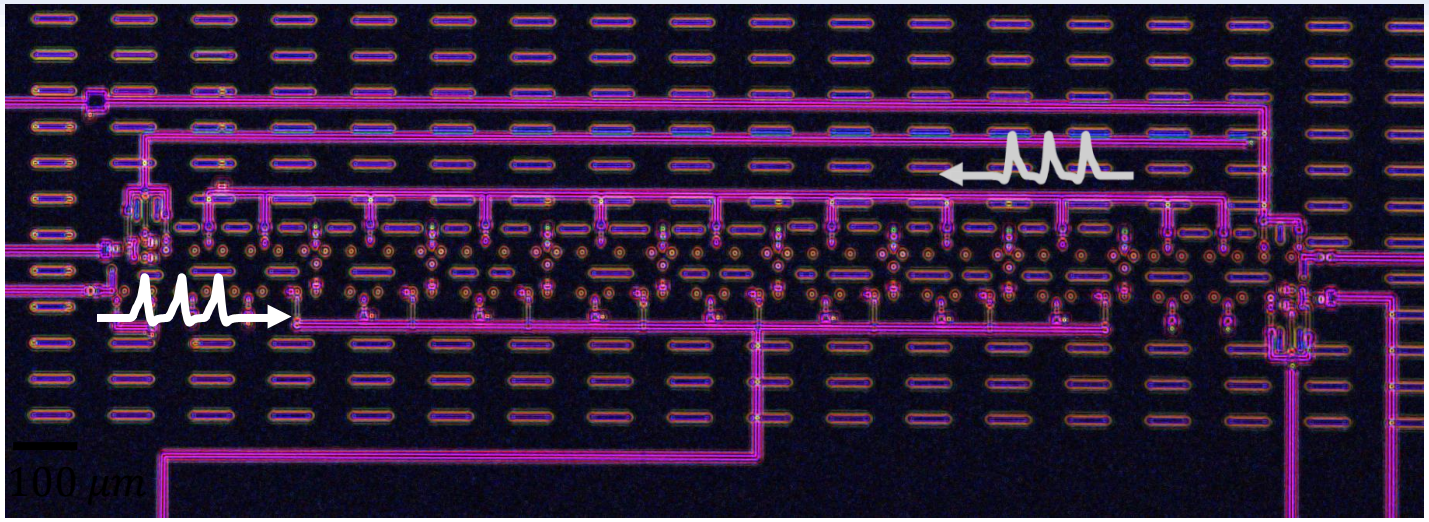
RSFQ circuits for waveform synthesis

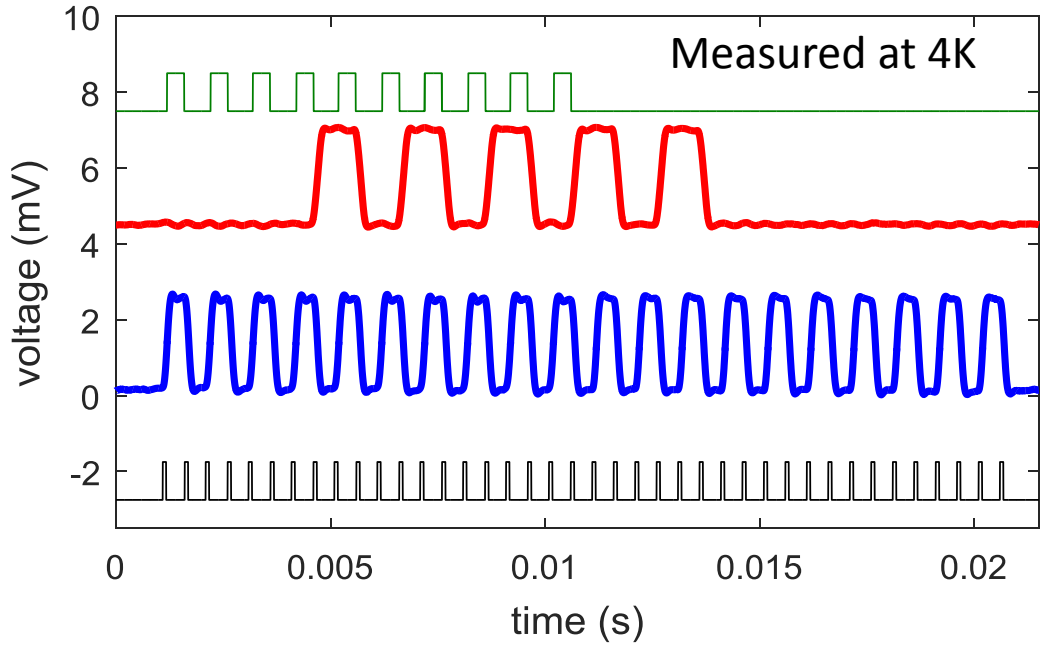
NIST cell library so far:

- *DC-to-SFQ*
- *JTL*
- *SFQ-to-DC*
- *Splitters*
- *Confluence Buffers*
- *T flip-flops*
- *D flip-flops (for shift registers)*
- *Voltage multipliers*



8-bit Shift Register





$|Margins| > \pm 25\%$

Tested at 1 kHz, not expected degradation up to $f = 50\ GHz$

Showing no degradation from single D F-F to an 8-bit SR

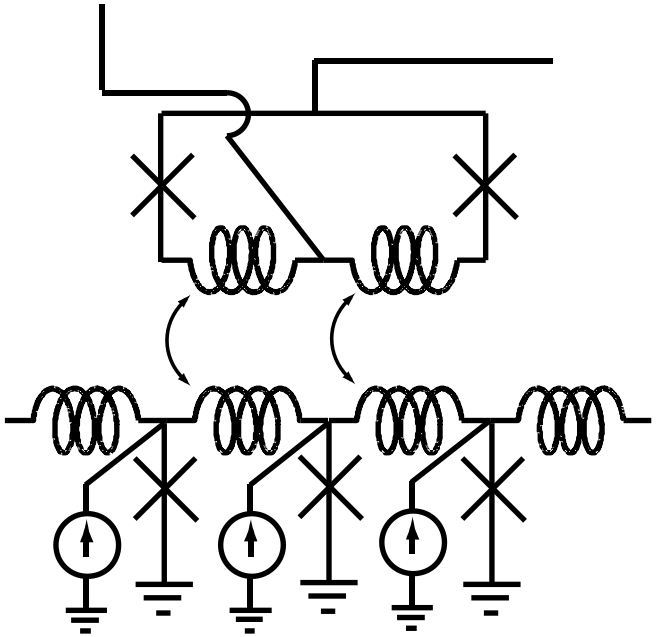
(scaled) Data in

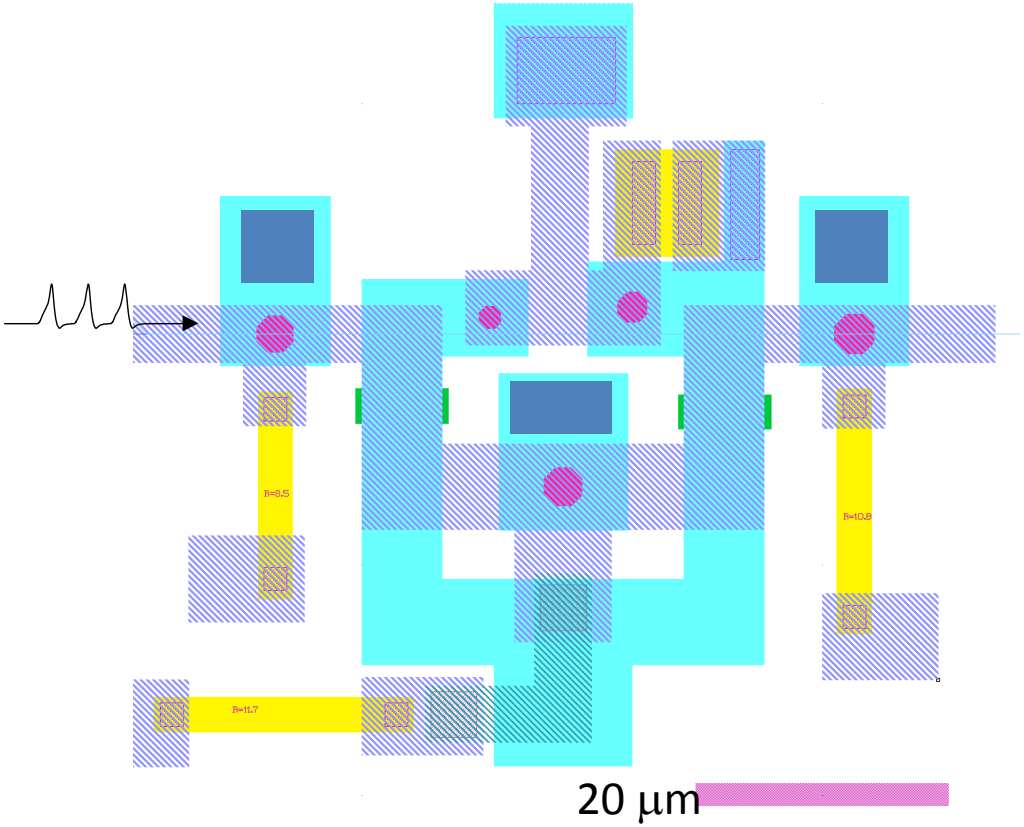
Data out

Clk out

(scaled) Clk in

Voltage multiplier





S. Polonsky and D. Schneider IEEE Transactions on Applied Superconductivity, vol. 7, no. 2 (1997)
F. Hirayama, *et al.* Characteristics of a voltage multiplier for a RSFQ digital-to-analog converter., Superconductor Science and Technology, 15, 4 (2002).

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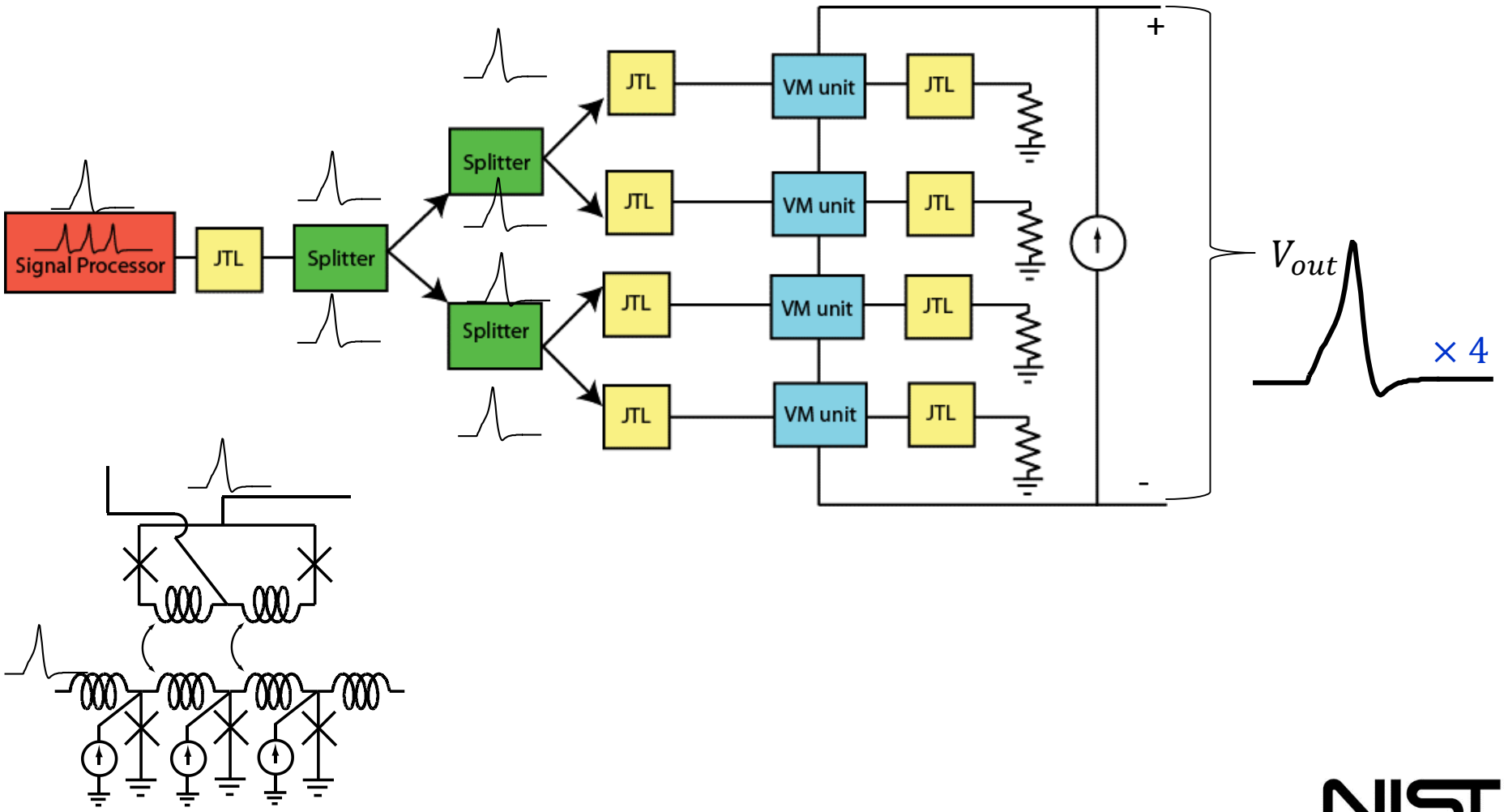
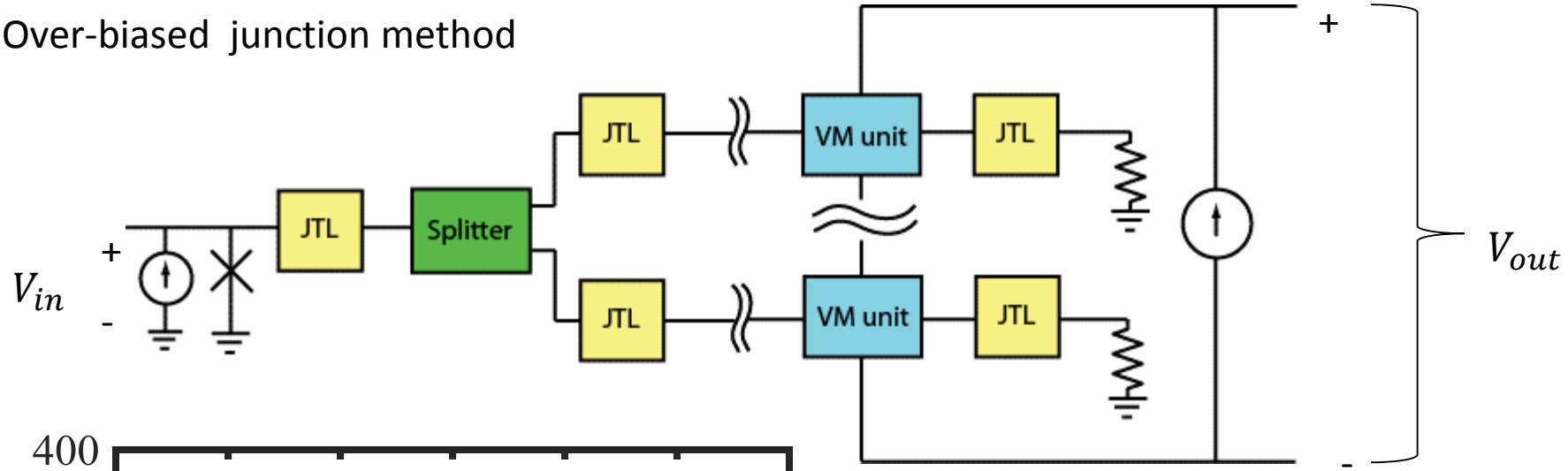
How does the voltage multiplier work?

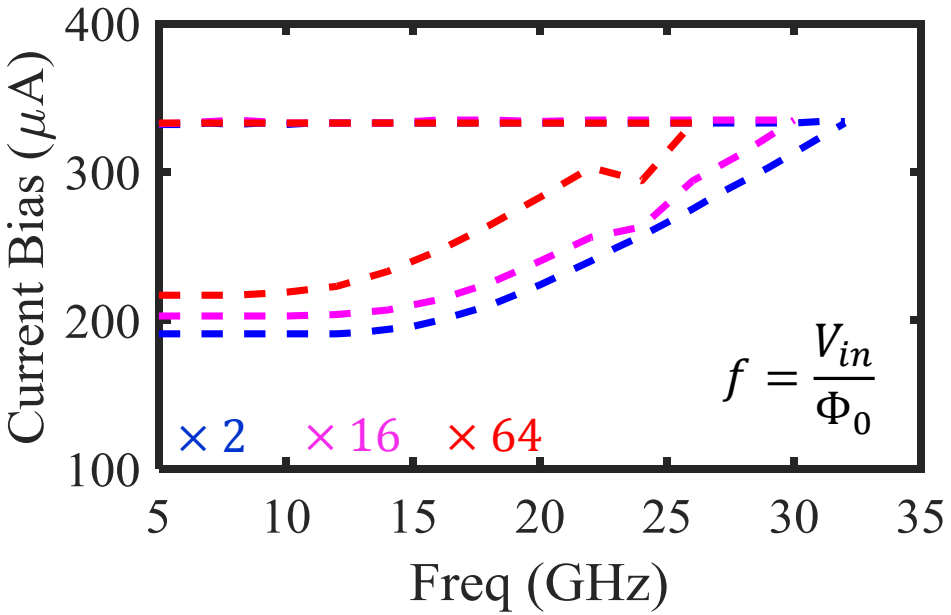


Expected performance of Voltage Multiplier

WRSPICE simulations for margins analysis of circuit

Over-biased junction method





Issues:

- Frequency-limited by $I_c R = 250$ μV
- Margins reduced to $\pm 10\%$ at 20 GHz

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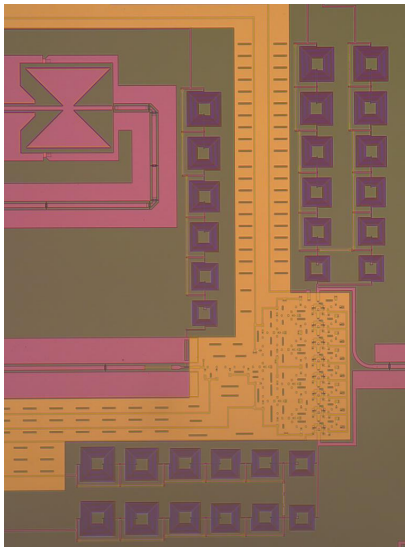
Progress and Future Work

- Building RSFQ infrastructure at NIST: fabricated and characterized basic SFQ circuits
- Fabricating building blocks of our high-frequency synthesizer (shift registers and voltage multipliers)
- Increase intrinsic speed of voltage multipliers
- Understand limitations of finite size circular shift registers
- Fix margin limitations due to 50 Ω impedance loading on voltage multipliers



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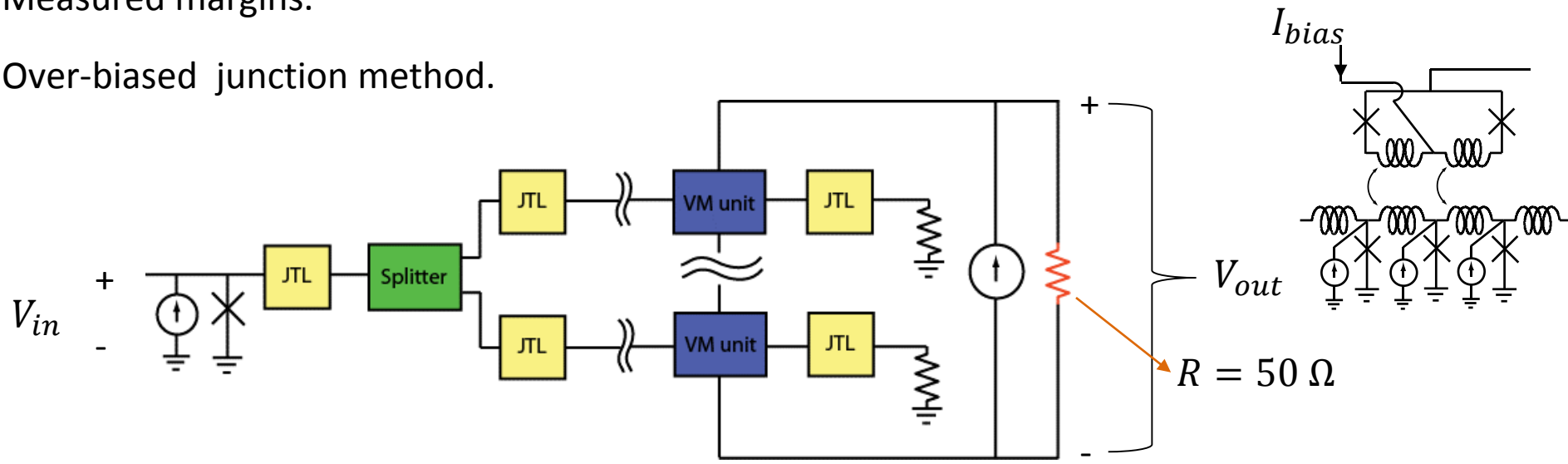
END

Voltage multiplier × 8

Measured margins.

Over-biased junction method.



Data. Still working on it.

Issues:

- Frequency-limited by $I_c R = 115\ \mu V$ due to issues in fabrication
- We have not tested yet the effect of $50\ \Omega$ loading

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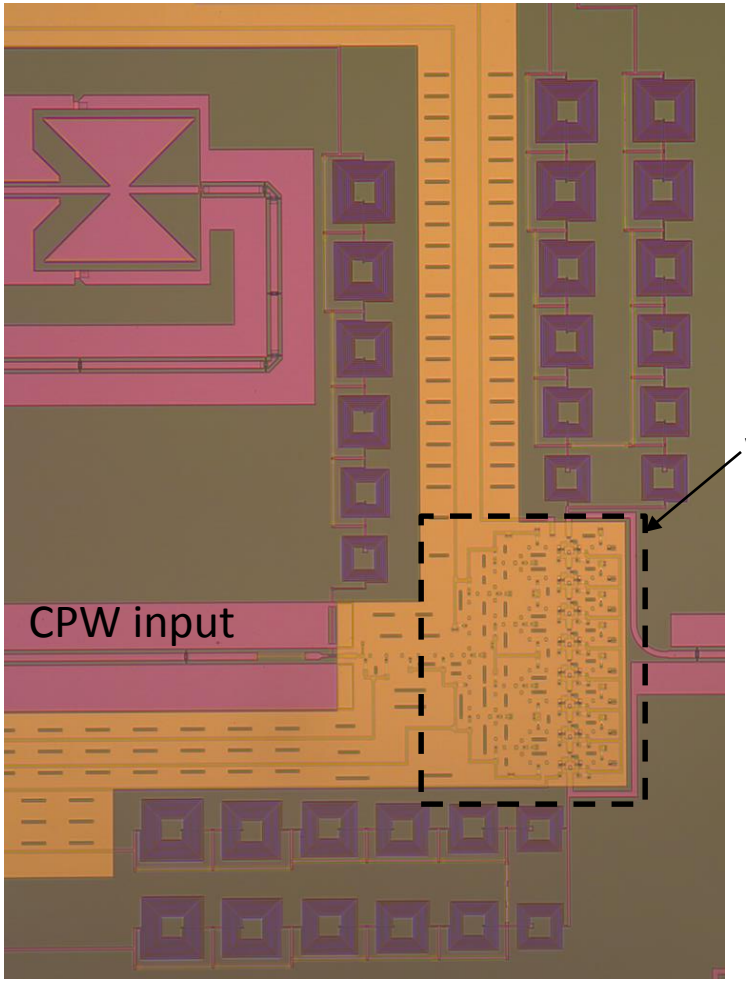
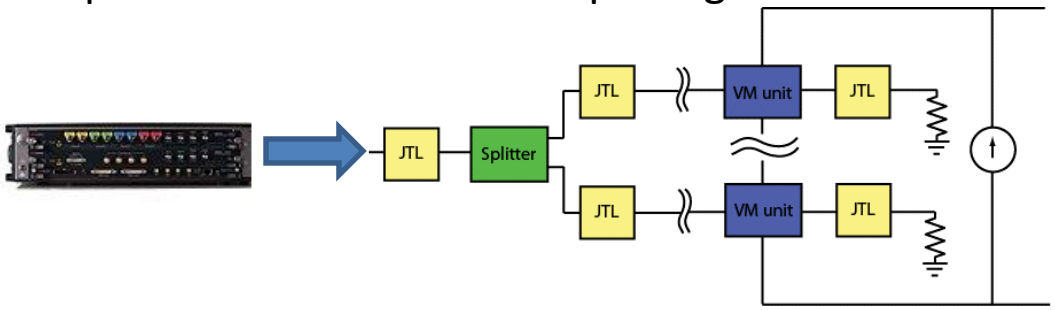
Near-future work

"Low" frequency implementation



Replace it with off-the-shelf pulse generators

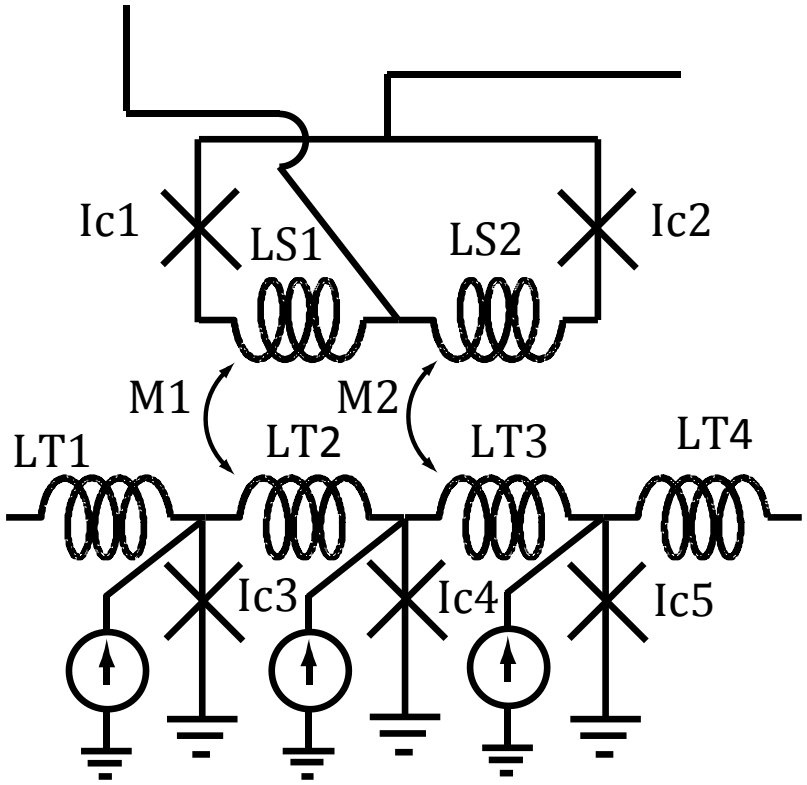


Clocked at 8 GHz
Signal frequency 1 GHz

Voltage multiplier

Voltage multiplier based on inductively-coupled SQUID-stack voltage reproducers.

Name	Value
LT1	1.3 pH
LT2	4.0
LT3	4.0
LT4	1.3
LS1	4.0
LS2	4.0
M1	1.4
M2	1.4
Ic1	240 μA (β= 0.15)
Ic2	135
Ic3	360
Ic4	400
Ic5	420



Polnsky, Schneidr (1997)
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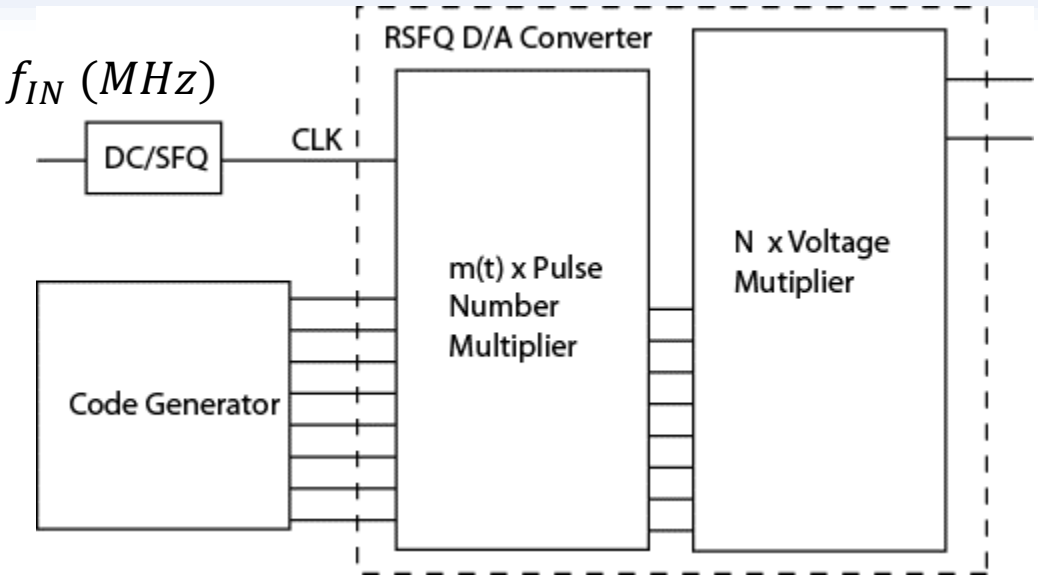
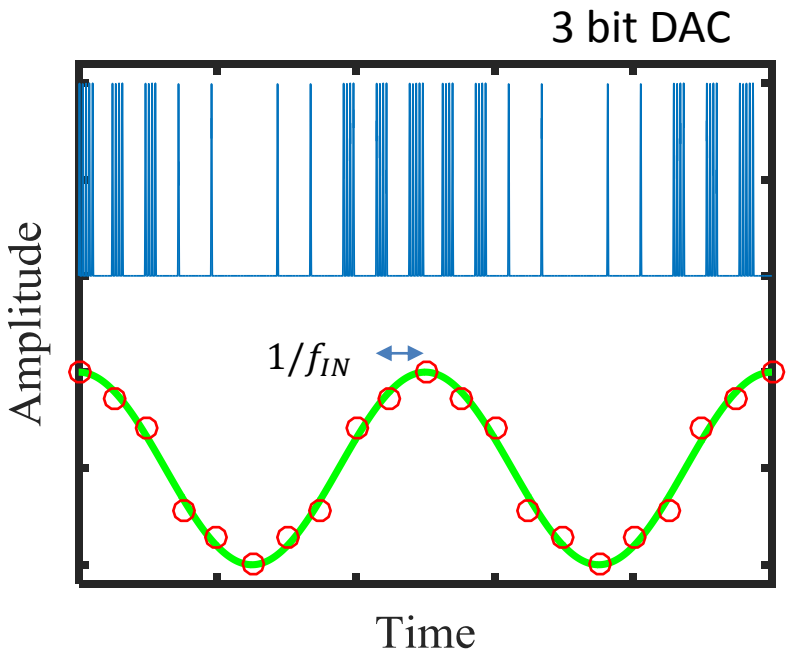
RSFQ circuits for waveform synthesis



$$Vout(t) = \Phi_0 \, N \times m(t) \times f_{IN}$$



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C. Hamilton (NIST).

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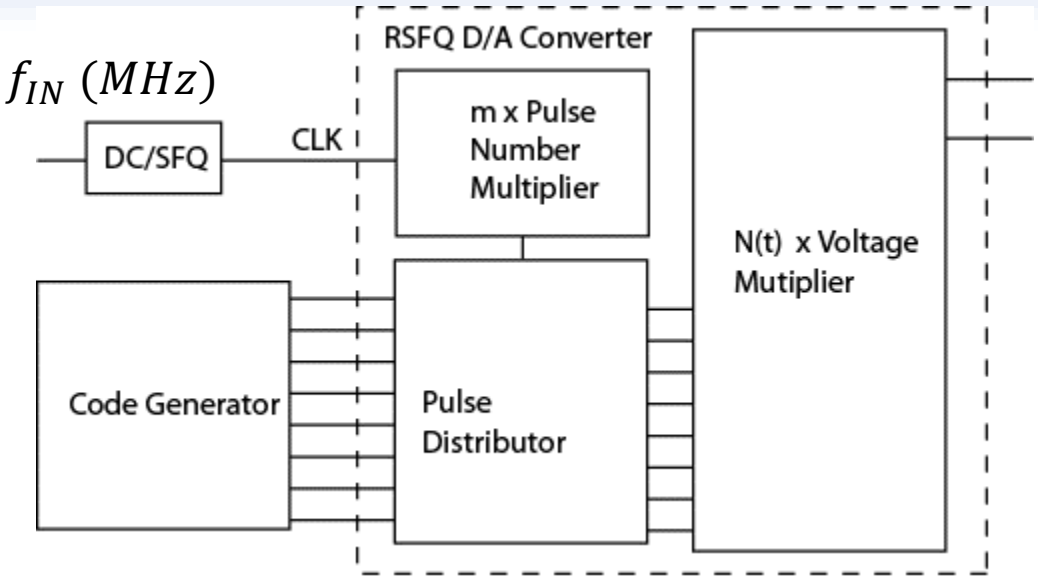

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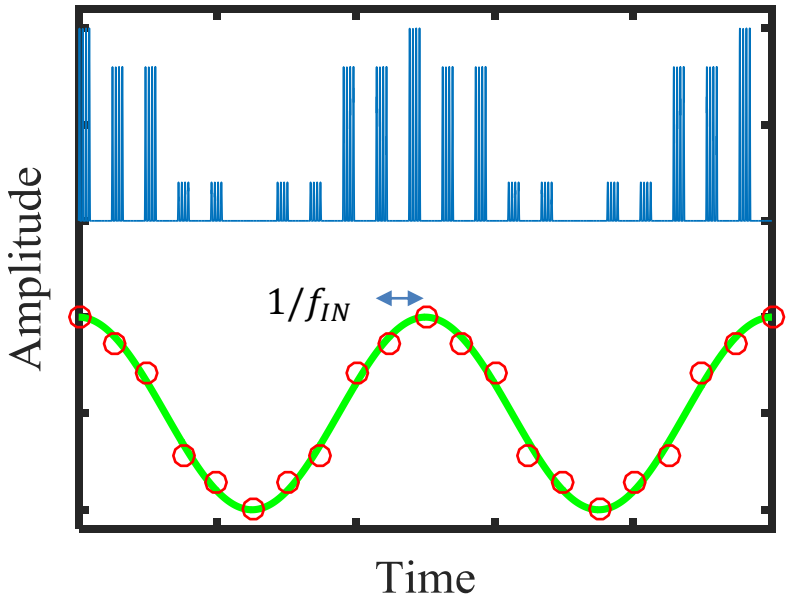
3 bit DAC



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