

A Fast Wire-Routing Method and an Automatic Layout Tool for RSFQ Digital Circuits Considering Wire-Length Matching

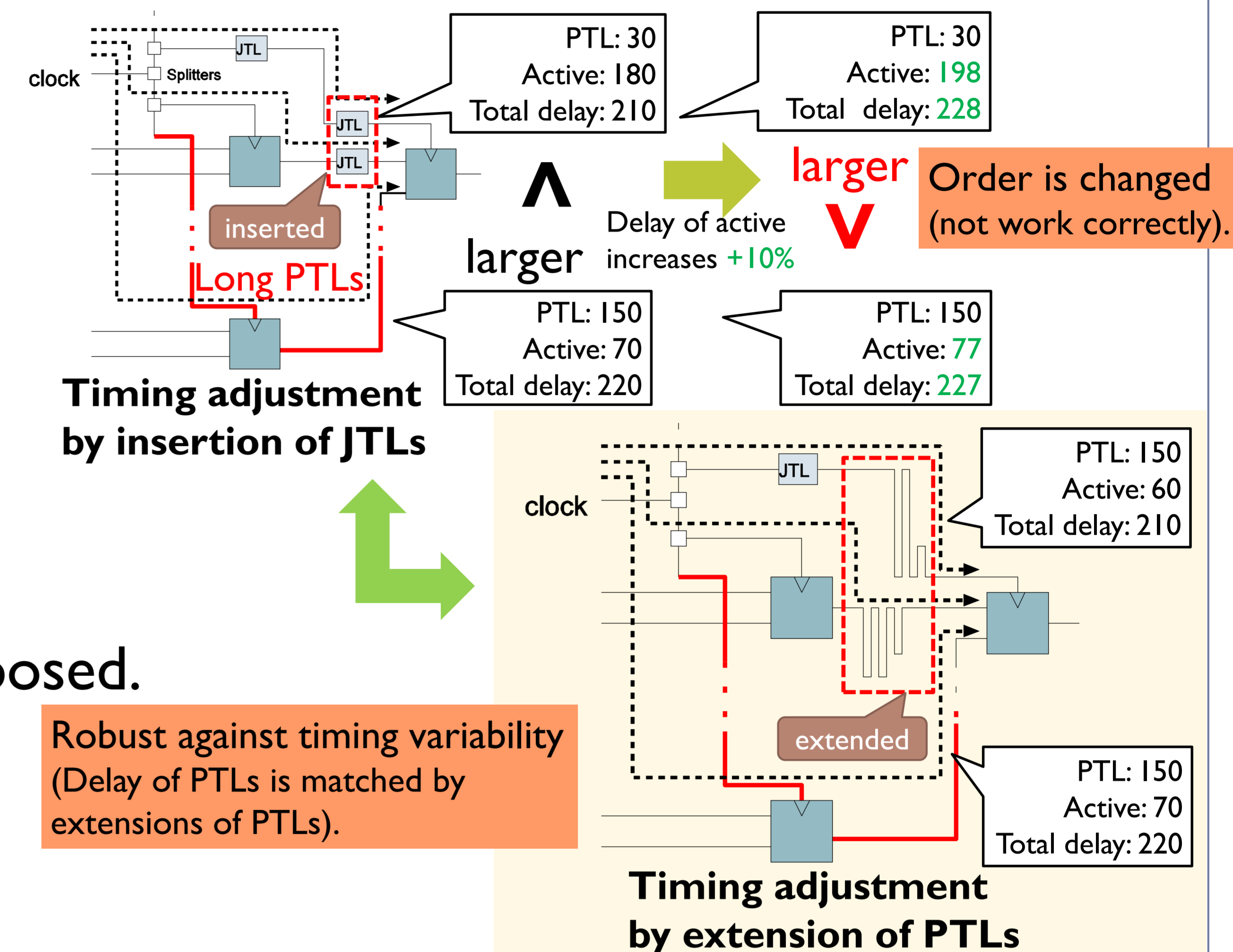
Nobutaka Kito (Chukyo University, Japan), Kazuyoshi Takagi, and Naofumi Takagi (Kyoto University, Japan)

Length-Matching of Passive Transmission Lines (PTLs)

- Timing adjustment is crucial for RSFQ circuits.
 - Order of pulse arrivals at each gate affects logical behavior.
 - Too much delay insertion degrades circuit performance.
- Speed of active/passive devices depends on the bias current differently.
 - Delay of logic gates should be matched by inserting JTLs.
 - Delay of PTLs should be matched by extending PTLs.

• This work

- A routing method for PTLs with wire-length matching is proposed.
 - The set of all PTLs in a channel is optimized as a whole.
- Based on the method, an automatic layout tool is developed.
 - Fast generation of a compact circuit layout is achieved.



A Fast Wire-Routing Method Considering Wire-Length Matching

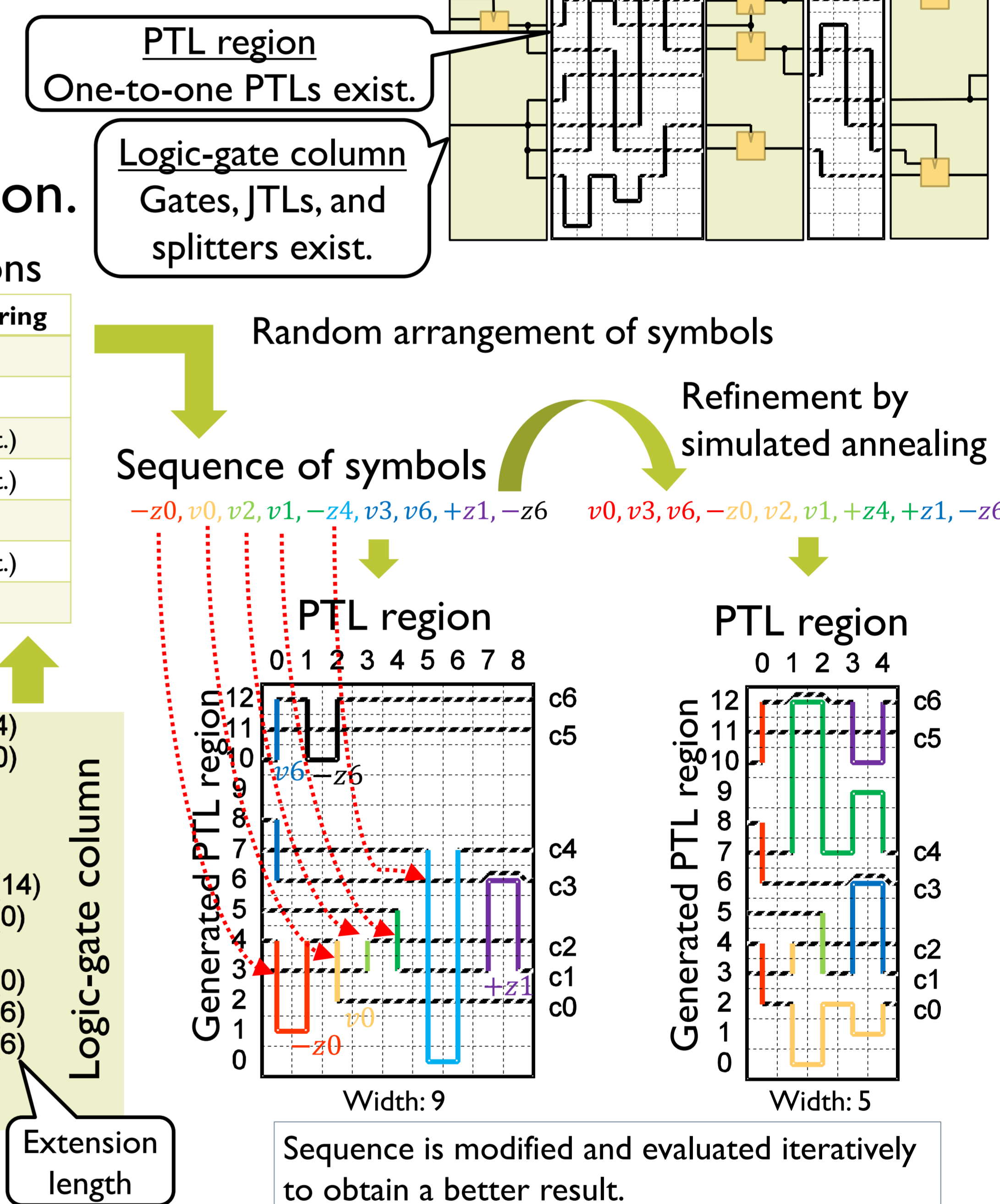
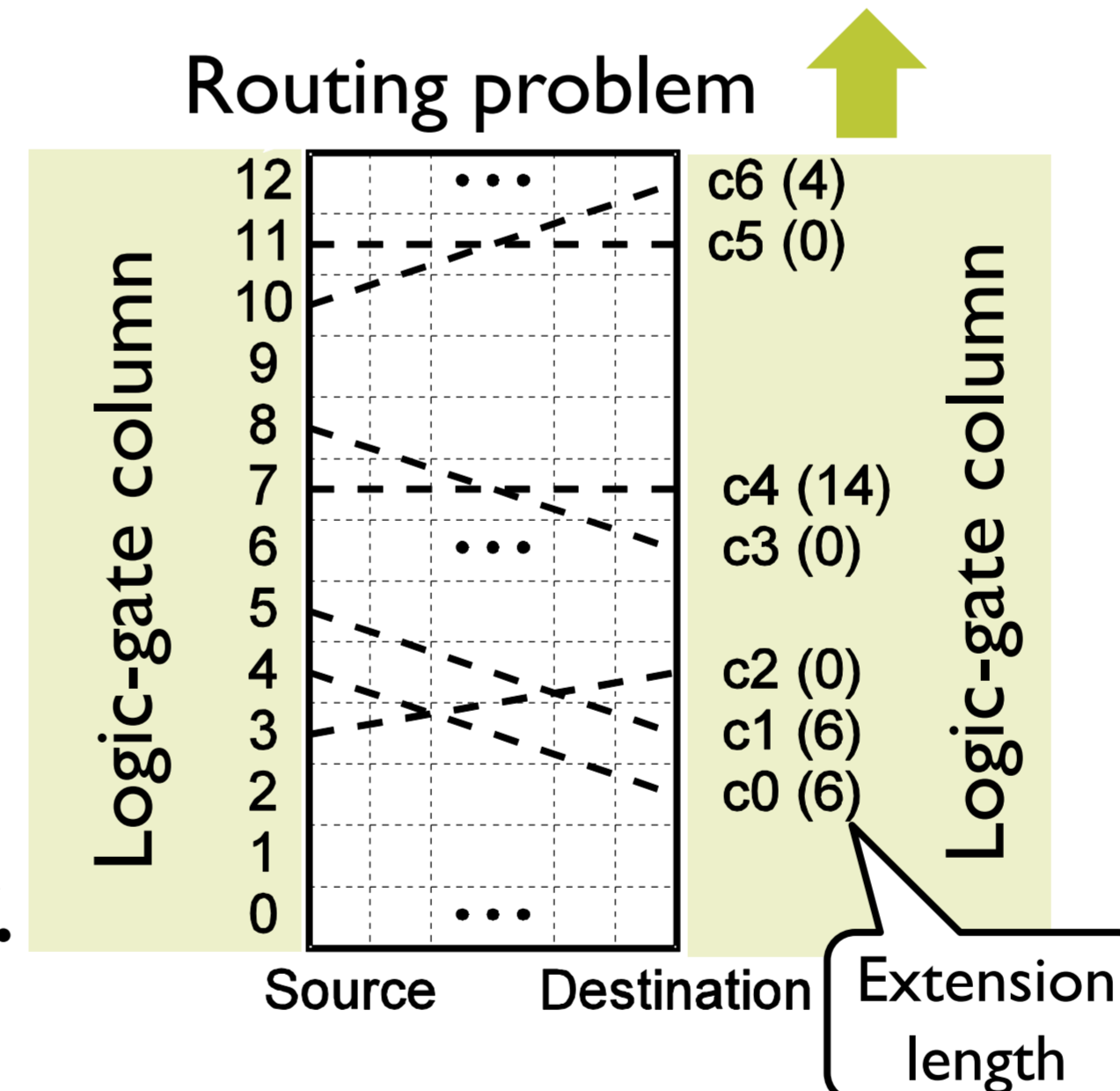
- Wire-routing problem
 - PTL routing regions are reserved between logic-gate columns.
 - Src./dst. positions, and the extension length are given for each connection.

• Proposed method using simulated annealing (SA)

- Each connection is realized by two parts.
 - Vertical segment (symbol v_c)
 - Zigzag wiring for extension (symbol z_c)
 - One of two shapes (upward $+z_c$ or downward $-z_c$) is chosen.
- A set of valid paths is obtained from a sequence of symbols.
 - From the first symbol to the last symbol in order, the corresponding parts are placed on the tracks.
- Sequence of symbols is refined by SA.
 - Two symbols in a sequence are exchanged randomly.
 - PTL regions with small area are found efficiently.

Symbols for connections

	Vertical segment	Zigzag wiring
c0	v_0	z_0
c1	v_1	z_1
c2	v_2	(no ext.)
c3	v_3	(no ext.)
c4	(no segment)	z_4
c5	(no segment)	(no ext.)
c6	v_6	z_6



An Automatic Layout Tool

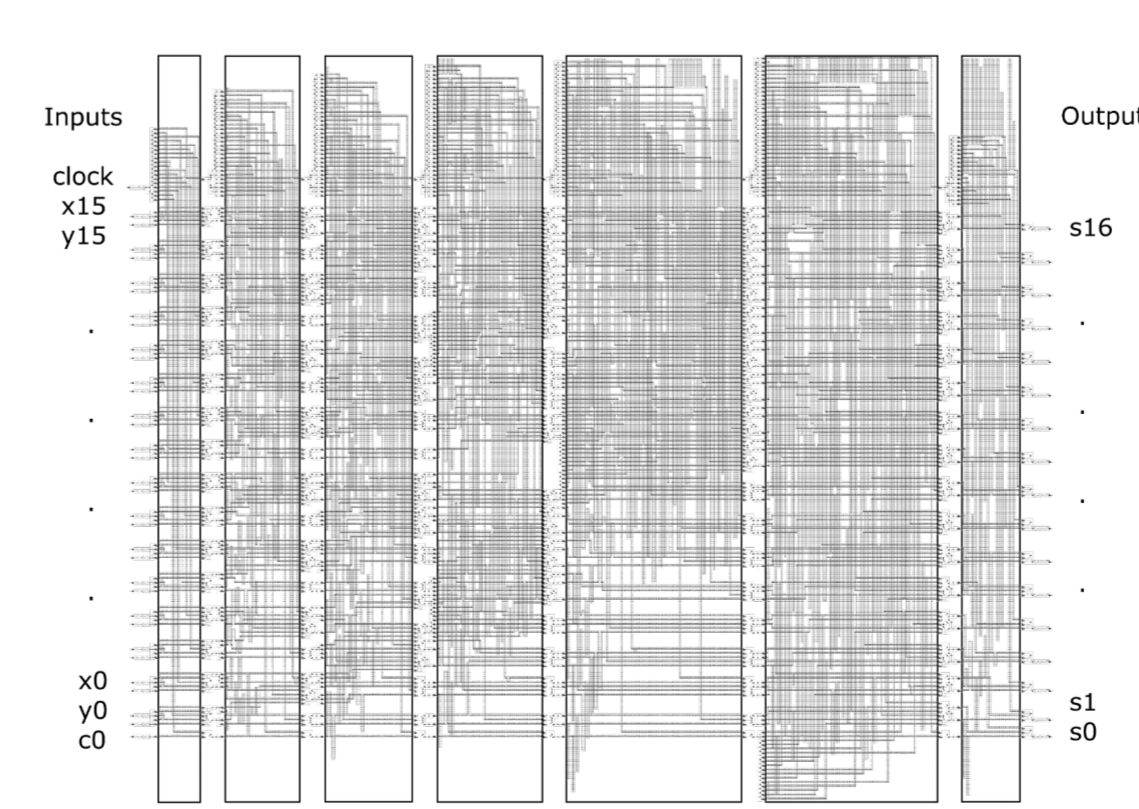
- Design procedure
 - A Design (in HDL) is synthesized into logic netlist.
 - Placer** generates logic-gate columns, and wire-routing problems for all PTL regions.
 - Router** solves wire-routing problems based on the proposed method.

• Placement process

- Gates are grouped into logic-gate columns.
- Splitter trees are generated.
- Positions of gates in columns are determined.
 - Detailed placement is refined by SA.
 - Sum of connection distances and total extension length for length-matching is minimized for reduction of effort in routing phase.

Evaluation

- The router and the layout tool are evaluated using the cell library for AIST ADP2 process



	ILP-based previous	Proposed	Reduction
Wiring area [mm ²]	31.4	27.5	11.2%
Time [s]	Over 10000	336	Over 90%

Routing results of a 16-bit Sklansky adder (The same logic-gate columns are used, and routing are performed with two tools.)

PTL regions with smaller area are obtained in shorter time.

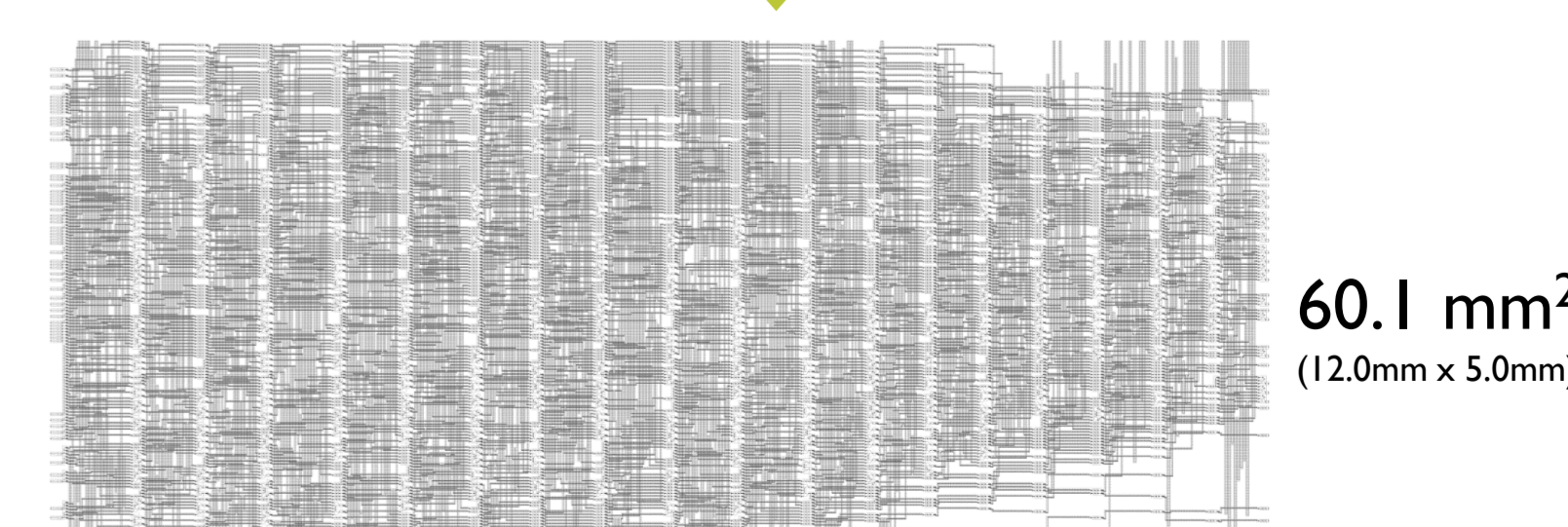
CPU: Xeon E5-1620 v3, OS: Debian Linux

```
module adder32 (a, b, out);
  input [31:0] a;
  input [31:0] b;
  output [31:0] out;

  assign out = a + b;
endmodule
```

Developed layout tool (Runtime: 2727 seconds)

Layout is generated successfully.



Layout of a 32-bit parallel adder generated from a HDL description

It is more compact than a length-matched layout generated without considering length-matching in placement (89.6mm²).