Charge-based superconducting digital logic family using quantum phase-slip junctions

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Abstract

Superconducting electronics are pursued for significantly faster and low energy consuming alternative to CMOS based electronics. Currently, all the superconducting logic circuits are based on Josephson junctions. In this poster, we introduce a new logic family, supported by SPICE simulations and numerical calculations, based on a device called quantum phase-slip junction (QPSJ), which is similar to a Josephson junction. Design methods and example logic gates are presented, along with power-delay comparison to Josephson junction based circuits.

Introduction to QPSJ

A quantum phase-slip junction (QPSJ) is the exact dual superconducting phenomenon to Josephson junction based on charge-flux duality [1].

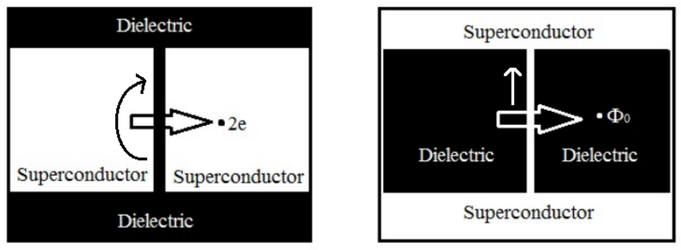

Figure 1: Josephson junction vs. quantum phase-slip junction [2].

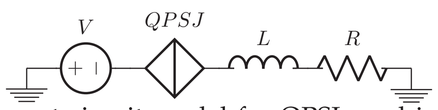

Figure 2: Compact circuit model for QPSJ used in SPICE model development adapted from [1].

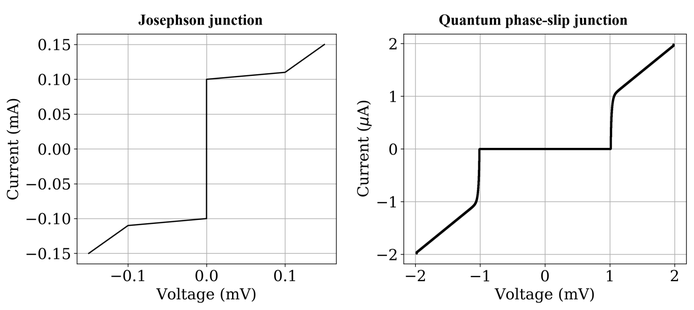

Figure 3: Comparison of simulated I-V characteristics.

Analogous to Josephson junctions, the current through a quantum phase-slip junction is zero, when applied voltage is below its critical voltage V_C.

Logic elements using QPSJs

The charge of Cooper pair $2e$ generated by the QPSJ with a pulse excitation is used as source of information. The presence or absence of charge can be seen as logic levels 1 or 0 respectively. The two different building blocks to develop logic circuits are shown below.

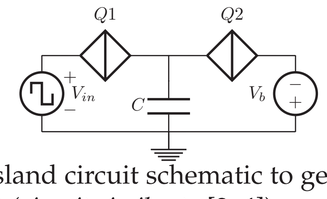

Figure 4: Charge island circuit schematic to generate and/or latch charge $2e$ at node 1 (*circuit similar to* [3, 4]).

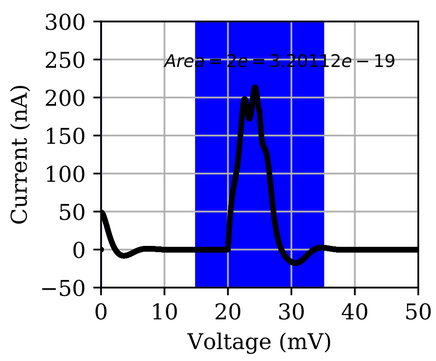

Figure 5: SPICE simulation results of charge island circuit in Fig. 4 generating a current pulse of constant-are representing charge $2e$.

A charge of $2e$ can be trapped on the island *(node 1)* by designing the capacitor to have capacitance $C > 2e/V_C$, where V_C is the critical voltage of the junction.

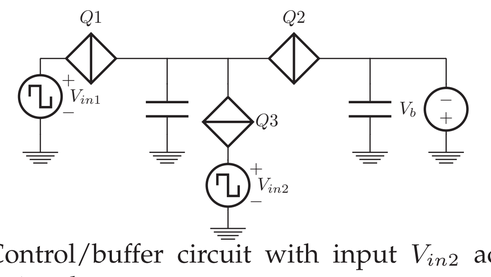

Figure 6: Control/buffer circuit with input V_{in2} acting as enable/control signal.

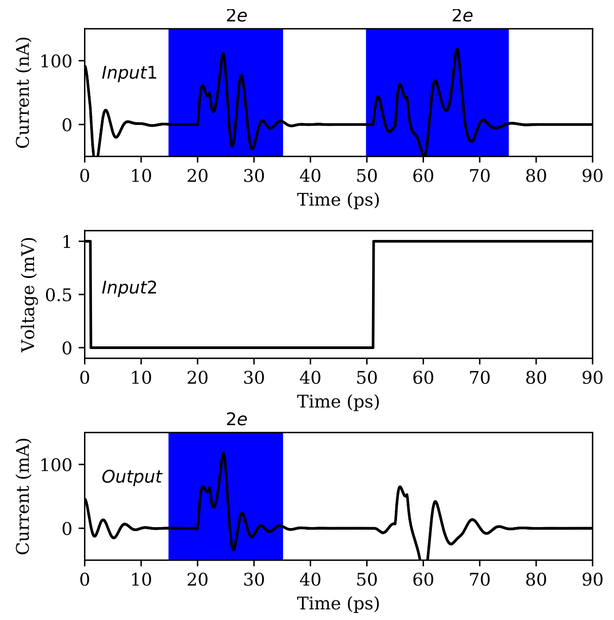

Figure 7: Simulation results of a control gate in Fig. 6, demonstrating the effect of control signal.

A control circuit can be used as a switch to enable/disable the current pulse at the output.

Logic Gate examples

OR gate :

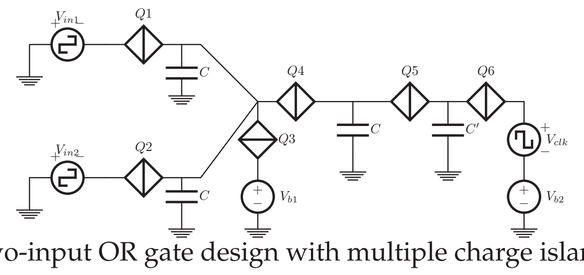

Figure 8: Two-input OR gate design with multiple charge islands in series.

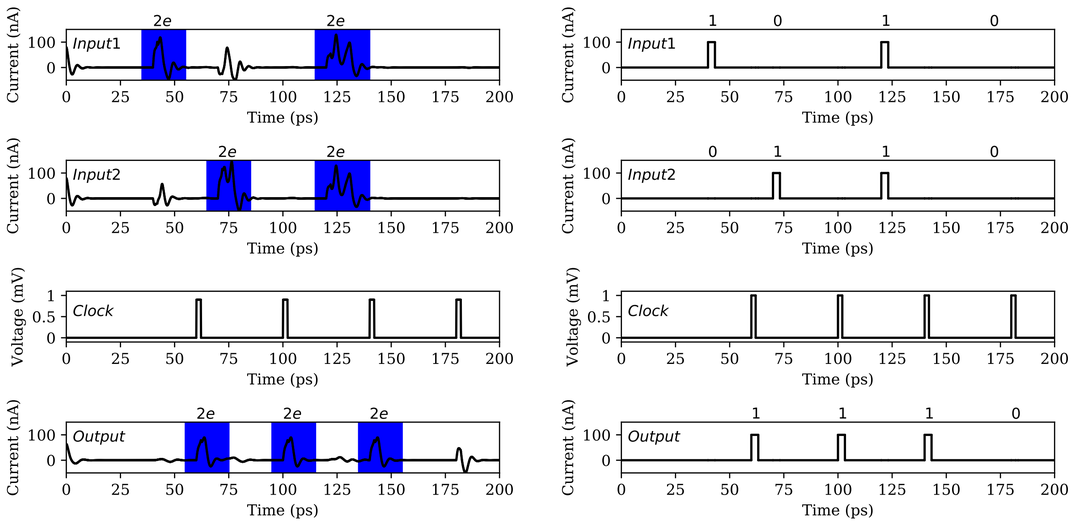

Figure 9: Simulation results of OR gate in Fig. 8 (left). Illustration of OR operation using ideal results (right).

OR gate is built using several charge islands in series, with the island formed by $Q5, Q6$ and C at node 9, trapping the charge.

XOR gate :

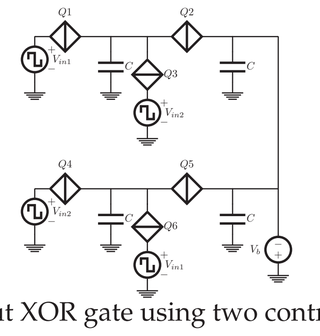

Figure 10: Two input XOR gate using two control gates in parallel.

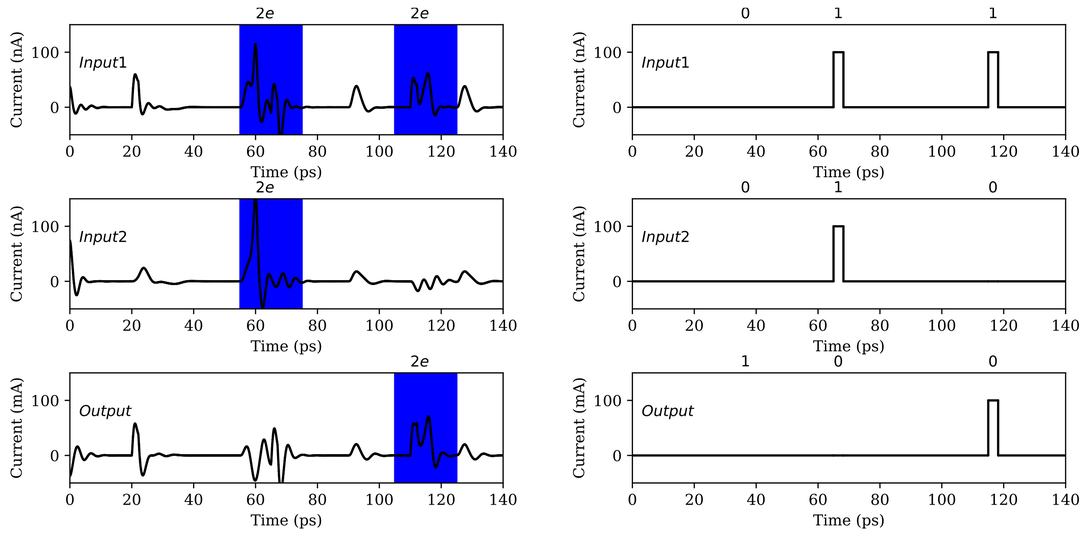

Figure 11: Simulation results of XOR gate in Fig. 10 (left). Illustration of XOR operation using ideal results (right).

XOR gate designed using two control circuits in parallel. This circuit can be modified to obtain inverter, NAND gate etc.

Conclusion

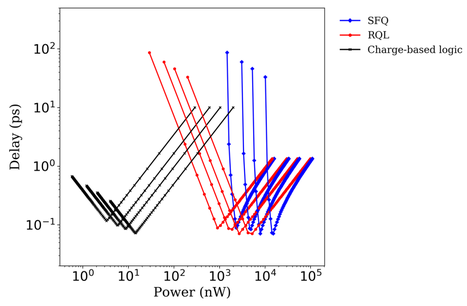

Figure 12: Estimated Power-delay comparison of QPSJ and JJ based logic circuits.

- Significantly lower power consumption (estimated).
- Performance same as Josephson junction based circuits.
- Reduction in design complexity.
- Voltage biased, zero-static power dissipation.
- Challenges exist in practical implementation.

References

[1] JE Mooij and Yu V Nazarov. Superconducting nanowires as quantum phase-slip junctions. *Nature Physics*, 2(3):169–172, 2006.

[2] Oleg Astafiev. Coherent quantum phase-slip. meso12.itp.ac.ru/Meso12$_Talk_Sslides/Astafiev_talk.ppt$, 2012. $[Online; accessed 14 - September - 2017]$.

[3] TT Hongisto and AB Zorin. Single-charge transistor based on the charge-phase duality of a superconducting nanowire circuit. *Physical review letters*, 108(9):097001, 2012.

[4] AM Hriscu and Yu V Nazarov. Coulomb blockade due to quantum phase slips illustrated with devices. *Physical Review B*, 83(17):174511, 2011.