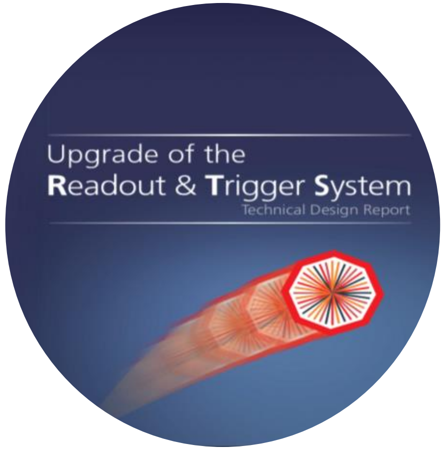
A Large Ion Collider Experiment

ALICE



ALICE trigger upgrade

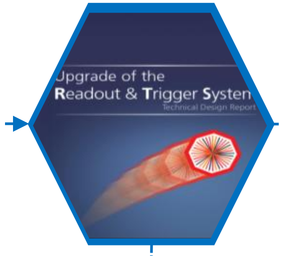
Luis Alberto Pérez Moreno (FCFM - BUAP)

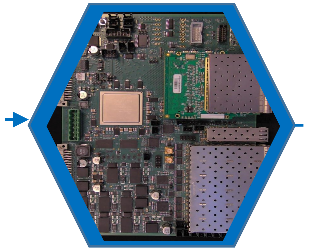
On behalf of the ALICE-CTP group

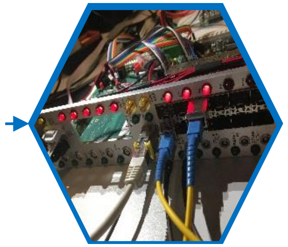
Triggering Discoveries in High Energy Physics II
Puebla –Puebla, México.

February – 1st – 2018

Outline



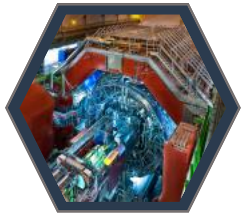




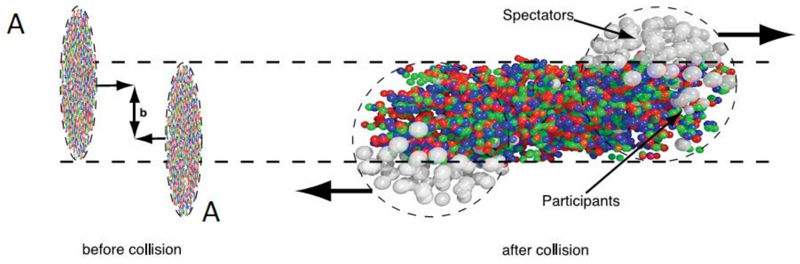
Introduction: ALICE
ALICE – Central Trigger Processor (CTP)
ALICE - CTP requirements for Run 3

Concept of ALICE- CTP system for Run 3
Design of Central Trigger Processor/Local Trigger Unit (CTP/LTU) board
Hardware & Firmware design

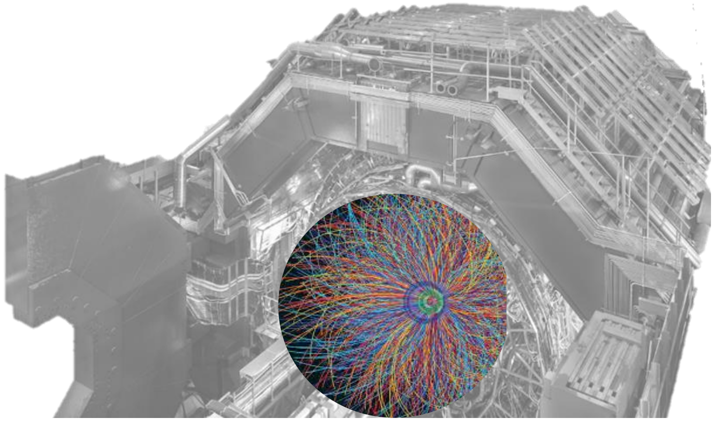
Performance of the CTP/LTU board.
TTC-PON in ALICE-CTP
Downstream Latency
Jitter Map
Bit Error Rate Test (BER)



ALICE is designed to study the physics of strongly interacting matter at extreme conditions of energy density and temperature, and in the particular the properties of the Quark Gluon Plasma (QGP), using nucleus-nucleus (A-A) collisions.



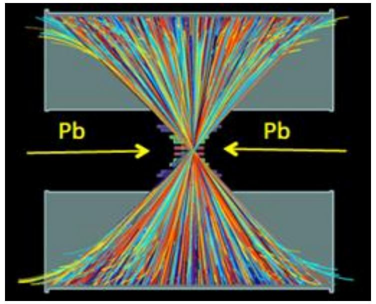
state of matter ~ 10 µs after big bang

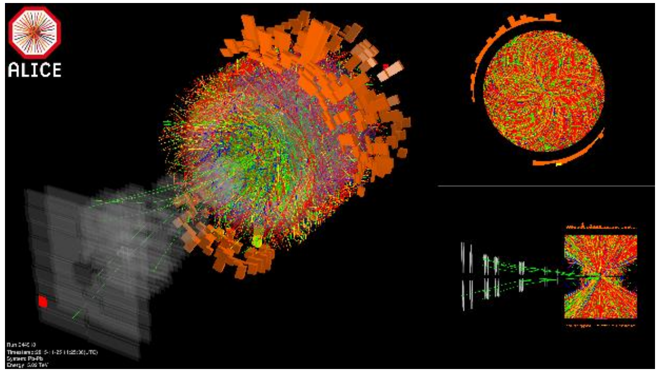


ALICE main goals: to study the properties of the QGP

- Thermodynamics...
- Flow
- Evolution
- Parton interaction with the medium.

Using several probes in a broadd P_T range:
-> heavy-flavor, quarkonia, jets, photons, dileptons, strangeness...



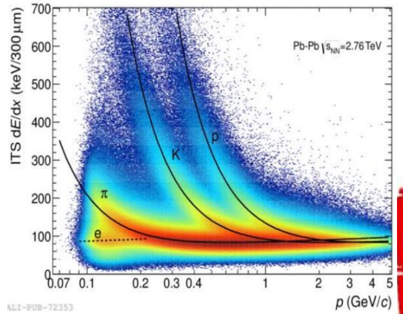


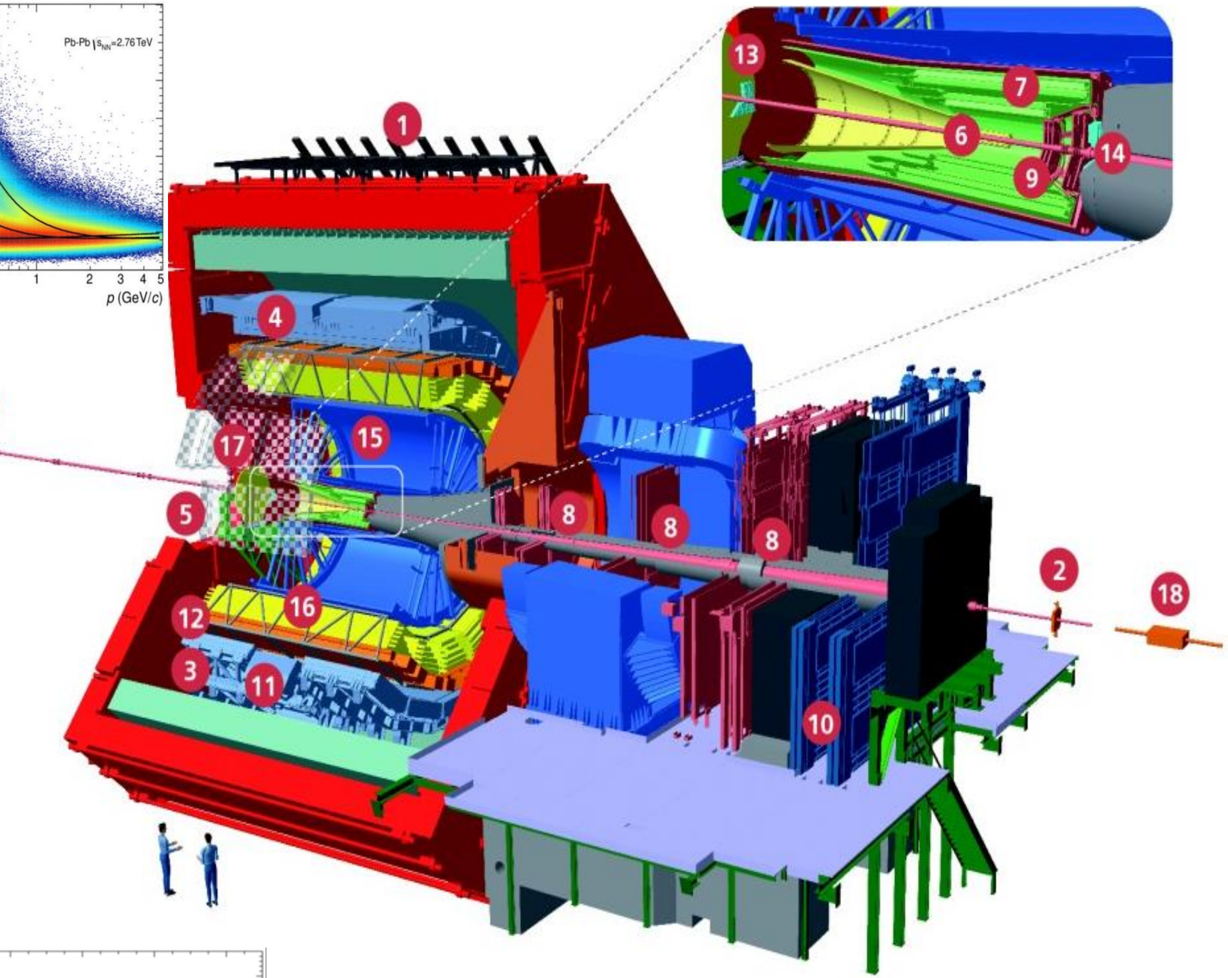
Physics limitations

- Some probes are not fully exploited due to insufficient statistics or large combinational background.

A Large Ion Collider Experiment

ALICE





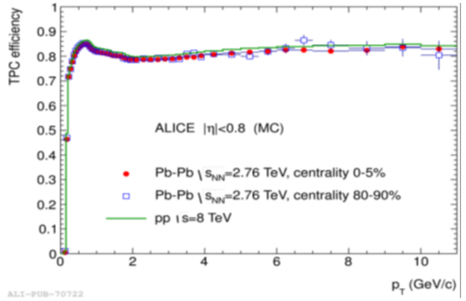
1. **ACORDE** | ALICE Cosmic Rays Detector
2. **AD** | ALICE Diffractive Detector
3. **DCal** | Di-jet Calorimeter
4. **EMCal** | Electromagnetic Calorimeter
5. **HMPID** | High Momentum Particle Identification Detector
6. **ITS-IB** | Inner Tracking System - Inner Barrel
7. **ITS-OB** | Inner Tracking System - Outer Barrel
8. **MCH** | Muon Tracking Chambers
9. **MFT** | Muon Forward Tracker
10. **MID** | Muon Identifier
11. **PHOS / CPV** | Photon Spectrometer
12. **TOF** | Time Of Flight
13. **T0+A** | Tzero + A
14. **T0+C** | Tzero + C
15. **TPC** | Time Projection Chamber
16. **TRD** | Transition Radiation Detector
17. **V0+** | Vzero + Detector
18. **ZDC** | Zero Degree Calorimeter

18 Detectors

Trigger
Tracking
PID
Calorimeters

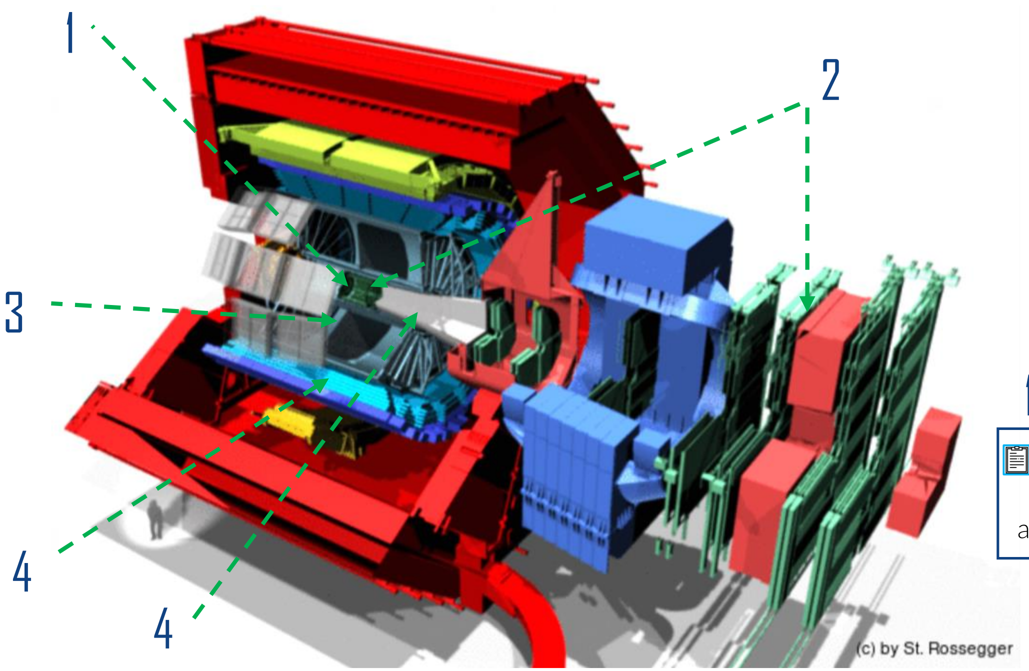
Central Systems Tigger /DAQ

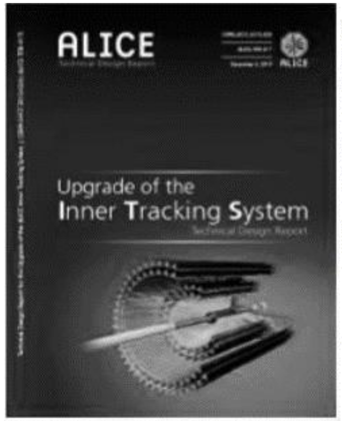
- 4 Trigger Levels (Hardware)
- 8 kHz (Pb-Pb) Collision rate
- 500 Hz (Pb-Pb) Max. Readout rate.



- Designed to cope with very high charged-particle multiplicities
- Excellent tracking and particle identification of charged particles over wide P_T range.

Introduction (Summary of Upgrades)

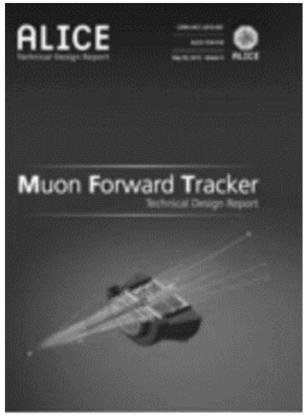




CERN-LHCC-2013-024

1

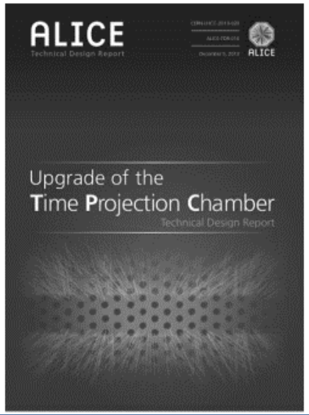
New Inner Tracking System (ITS)
-- Less material ->thinnest tracker at the LCH



CERN-LHCC-2015-021

2

Improved MUON pointing precision
-- new Si tracker
New Muon Arm Readout



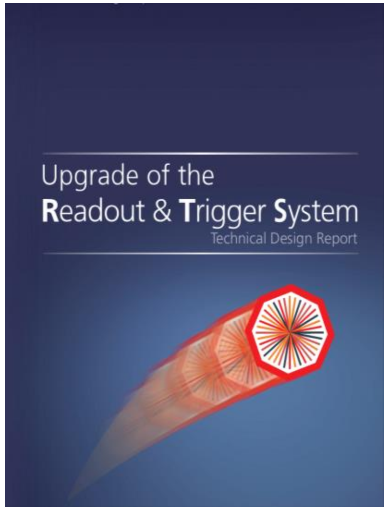
CERN-LHCC-2013-020

3

New GEM technology for readout chambers.
-- Faster readout electronics

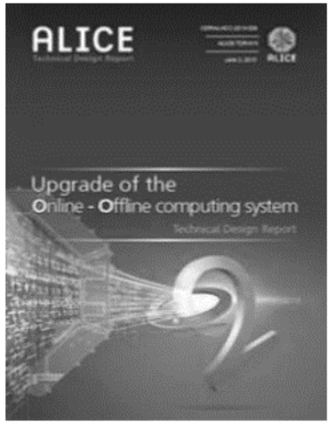
Strategy

-- Improve tracking resolution at low p_T.
-- thinner better resolution.
-- Large statistics (new strategy and trigger system) with high interaction rate.
-- Increase readout rate.
-- Reduce data size
-- Preserve PID capabilities at high rate
-- Speed-up readout of PID detectors



4

New Trigger Detectors (FIT)
TOF, TRD
-> Faster Readout
New Trigger Electronics
(CTP + LTUs)



CERN-LHCC-2015-006

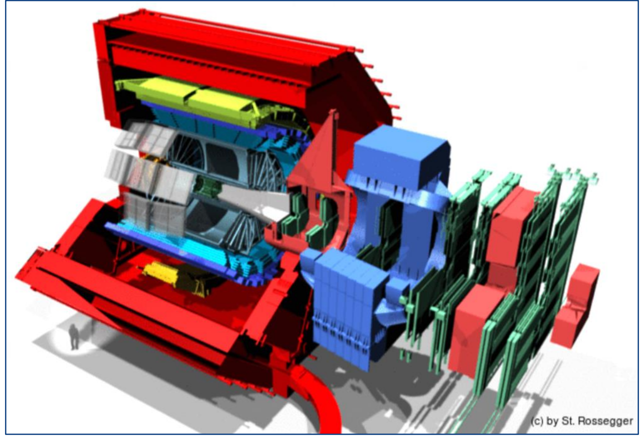
5

Data Acquisition (DAQ)/ High Level Trigger (HLT).
- New Architecture
- Online tracking & data compression

To Summarize:

- Write all Pb-Pb interactions at 50 kHz = (Current system x50 faster)

Design (ALICE architecture for Run 3)



ALICE Run 3

- New ITS (Inner Tracking System)
  - 25 x 10^9 Channels.
  - CTP-FEE direct links .
- New TPC (Time Projection Chamber).
  - Technology GEM.
  - Faster readout electronics.
- Nuevo CTP (Central Trigger Processor)
- New Trigger Electronics (CTP + LTUs)
- Online & Offline (O2) system
  - Online tracking & data compression
- TOF & TRD
  - Faster Readout
- New trigger detector (FIT)

Trigger Contributing Detectors

- Contributions of different types of detectors.
- Trigger latency optimized for every detector.
- Grouping of readout detectors possible.

LTU (Local Trigger Unit)

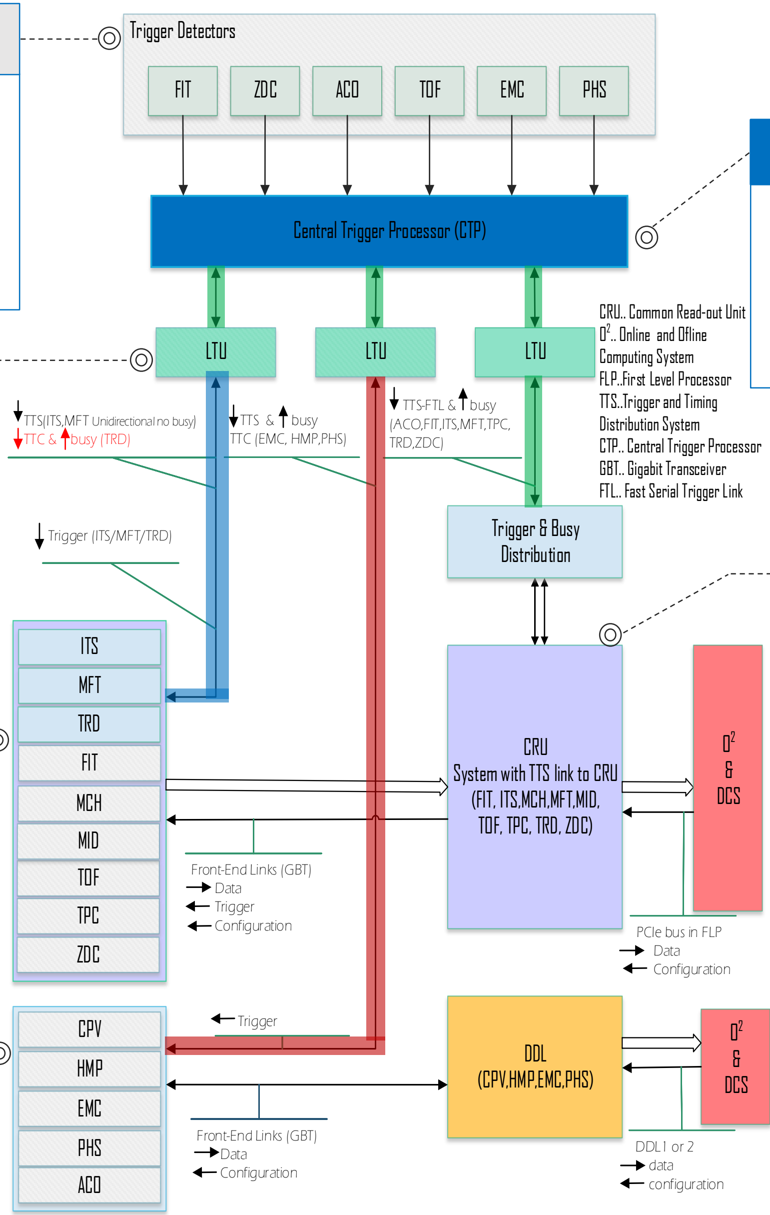
- CTP and detector interface (TTC-PON, GBT, TTC)
- CTP Emulator in standalone mode

Detectors (A, B)

Continuous & triggered read-out

Detectors (C)

Triggered read-out



Block Diagram ALICE – Run 3

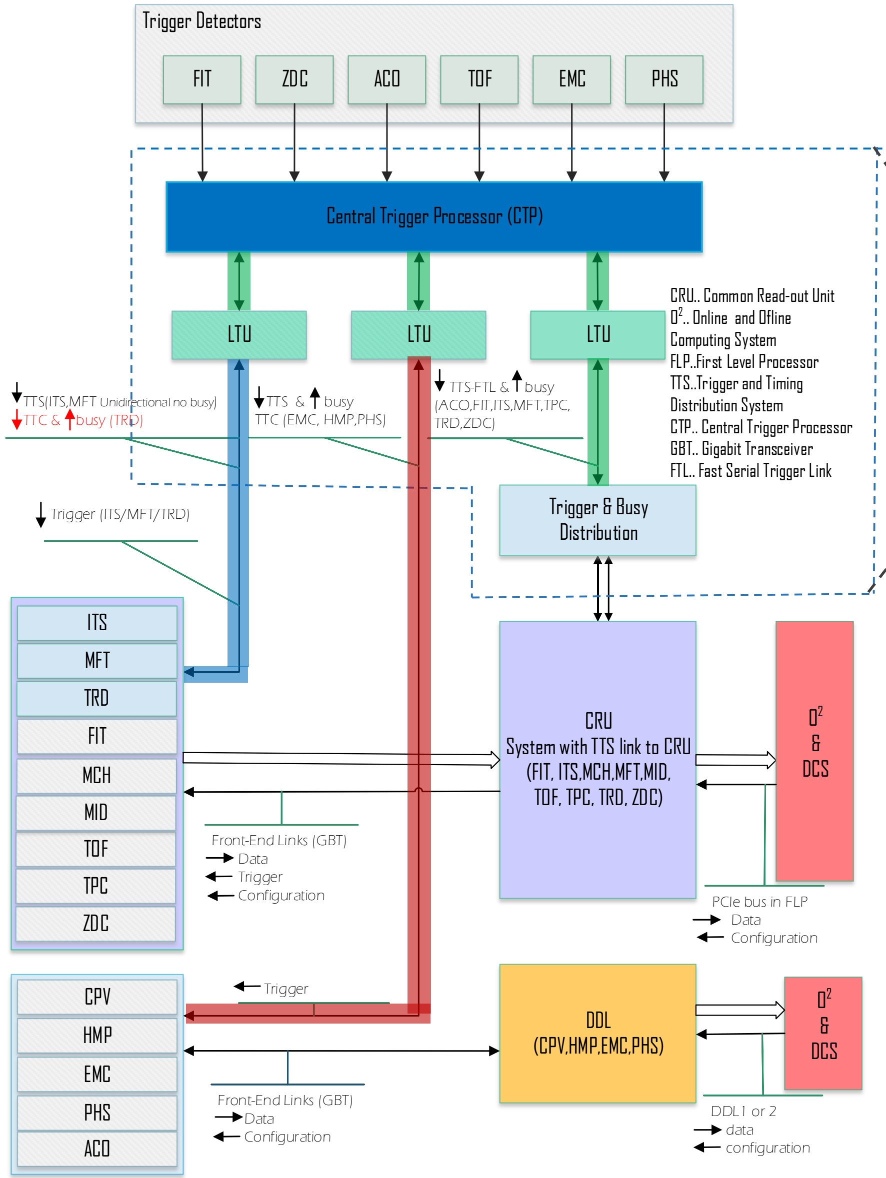
CTP (Central Trigger Processor)

- Receives signals for triggering detectors, make decision and send triggers via LTU to detectors
- Generates software/calibration triggers.

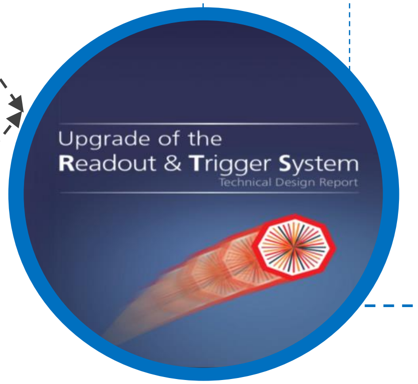
CRU (Common Read Unit)

Interface between on detector electronics, DAQ and CTP (GBT Links)

CTP Requirements for Run 3



Block Diagram ALICE – Run 3



>> Select different physics

>> Different trigger detectors
--- (ACO, FIT, EMC, PHOS, TOF, ZDC).

>> Optimize for different running scenarios

>> Pb-Pb, p-p , p-Pb collisions, with different interaction rates
Pb-Pb: 50 kHz.
p – p: 200 kHz.

>> Optimize use of detectors with

>> Continuous readout.
>> Widely different busy times.
>> Different latency times. (LM, L0, L1)
>> Different Technologies (TTC, GBT, TTC-PON)

>> Special triggers

>> Calibration, Control.

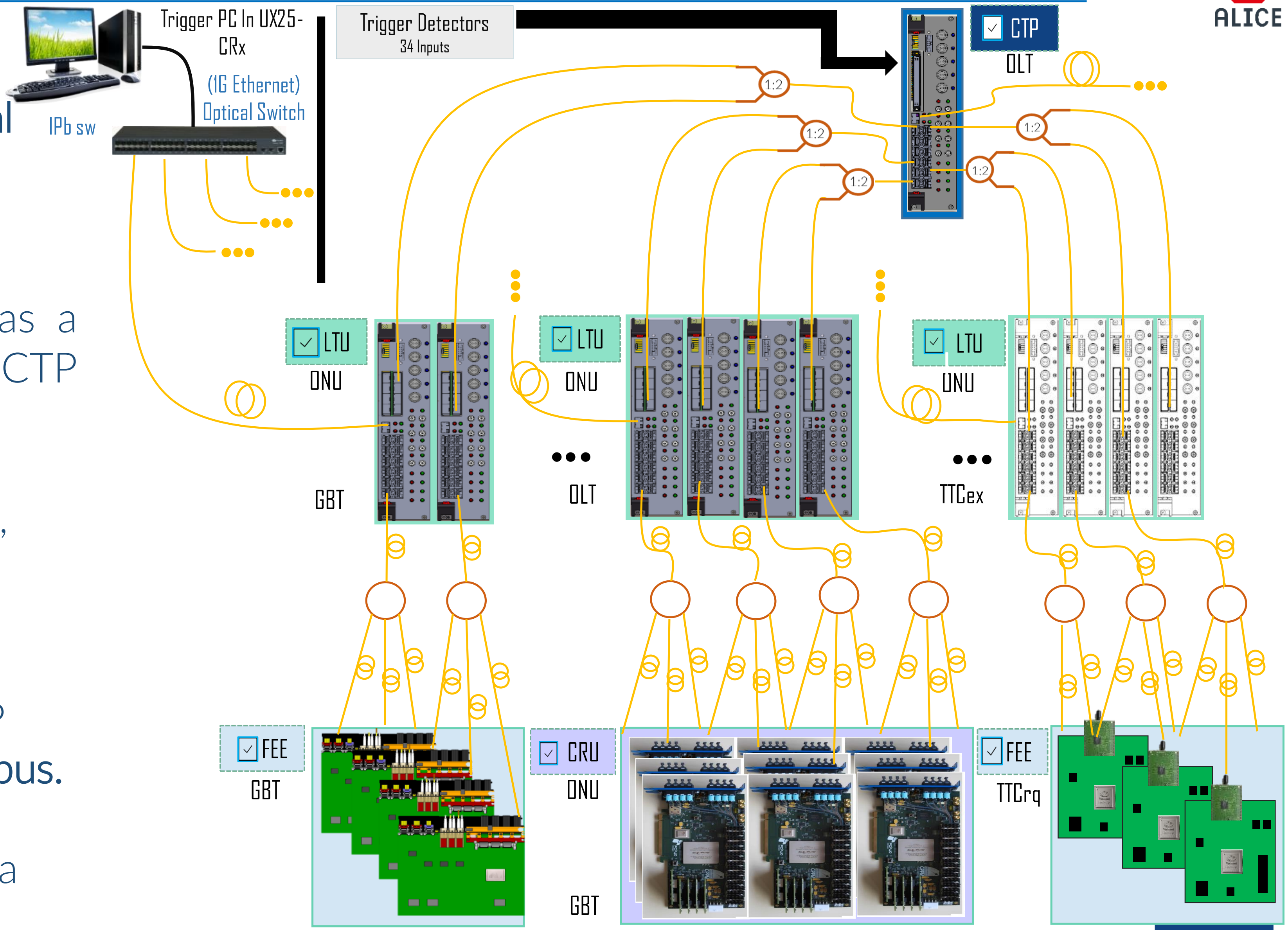
>> BUSY handling

>> Busy propagated with minimal latency.
>> Busy for Upgrade & non Upgrade detectors .

ALICE CTP Requirements

Design Proposal (Concept for New Trigger System)

- The system consists of a **Central Trigger Processor** (CTP) and **Local Trigger Units** (LTUs) as detector interfaces.
- In **Global Run**, the LTU serves as a "transparent link" between the CTP and the FEE of detector.
- In the **Standalone** mode operation, the LTU fully **emulates** the CTP protocol.
- **Monitoring and control** of the CTP and LTU boards are performed **IPbus.**
- The interface of CTP to LTUs is via TTC-PON



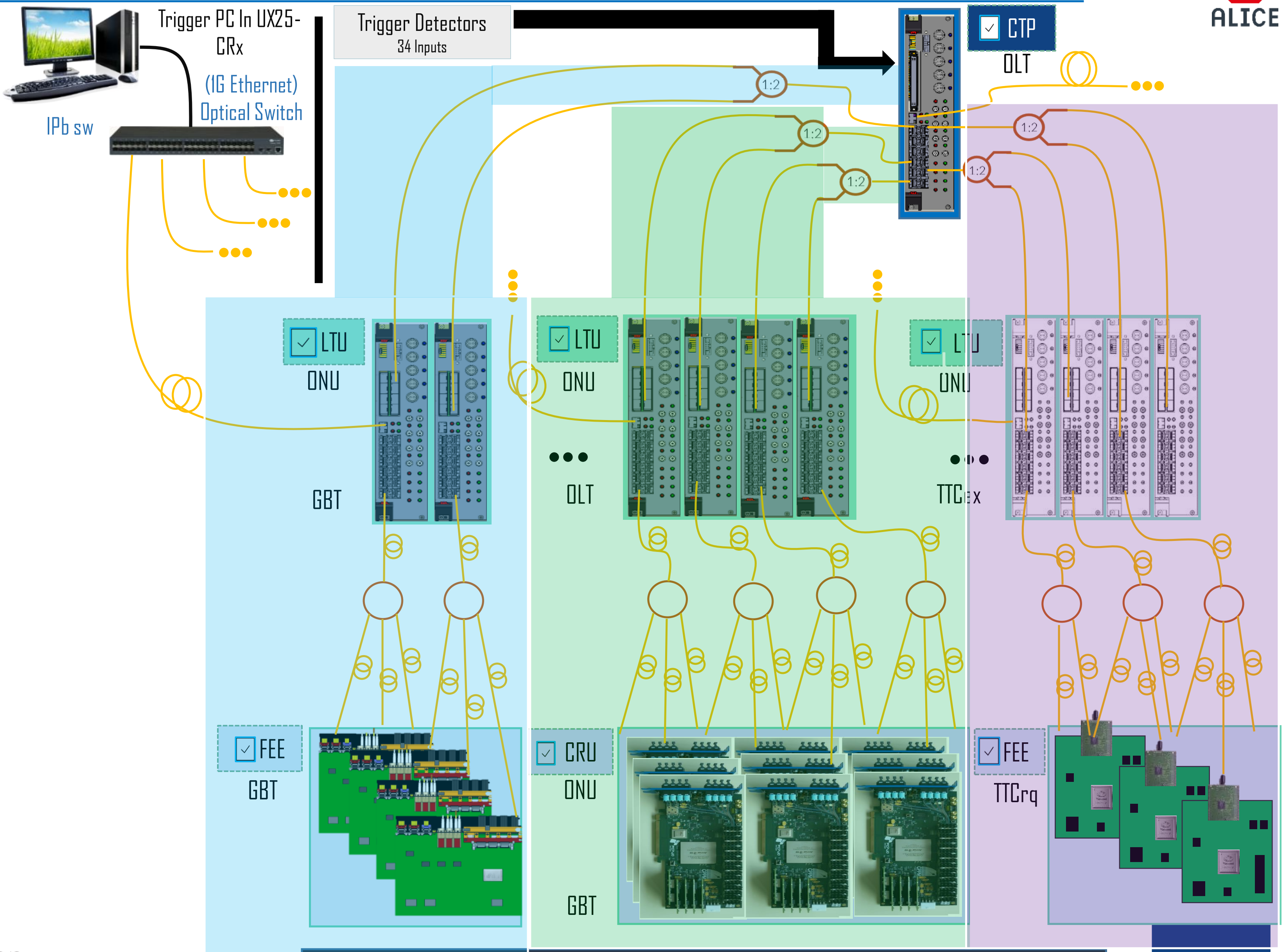
OLT: Optical Line Terminal
ONU: Optical Network Unit

Block Diagram ALICE TTC_PON architecture

Design Proposal (Trigger Protocol)

- **Detectors with CRU:**
  - One trigger over TTC-PON with different latencies.
  - Payload: Event Id (32+12) bits,
  - Trigger Type (32 bits).
- **ITS /MFT**
  - One trigger over GBT.
  - Payload: Event Id (32 + 12) bits.
  - Trigger Type (32 bits).
- **TTC detectors**
  - Max. 2 trigger levels (PHOS).
  - TTC protocol similar to Run2.
- TRD
  - LM trigger to FEE over old TTC
  - One trigger over TTC-PON
  - Payload Event Id (32+12) bits,
  - Trigger Type (32)

For detail see:
https://twiki.cern.ch/twiki/pub/ALICE/EngineeringDesignReview%28June2016%29/CTPLTU18.pdf



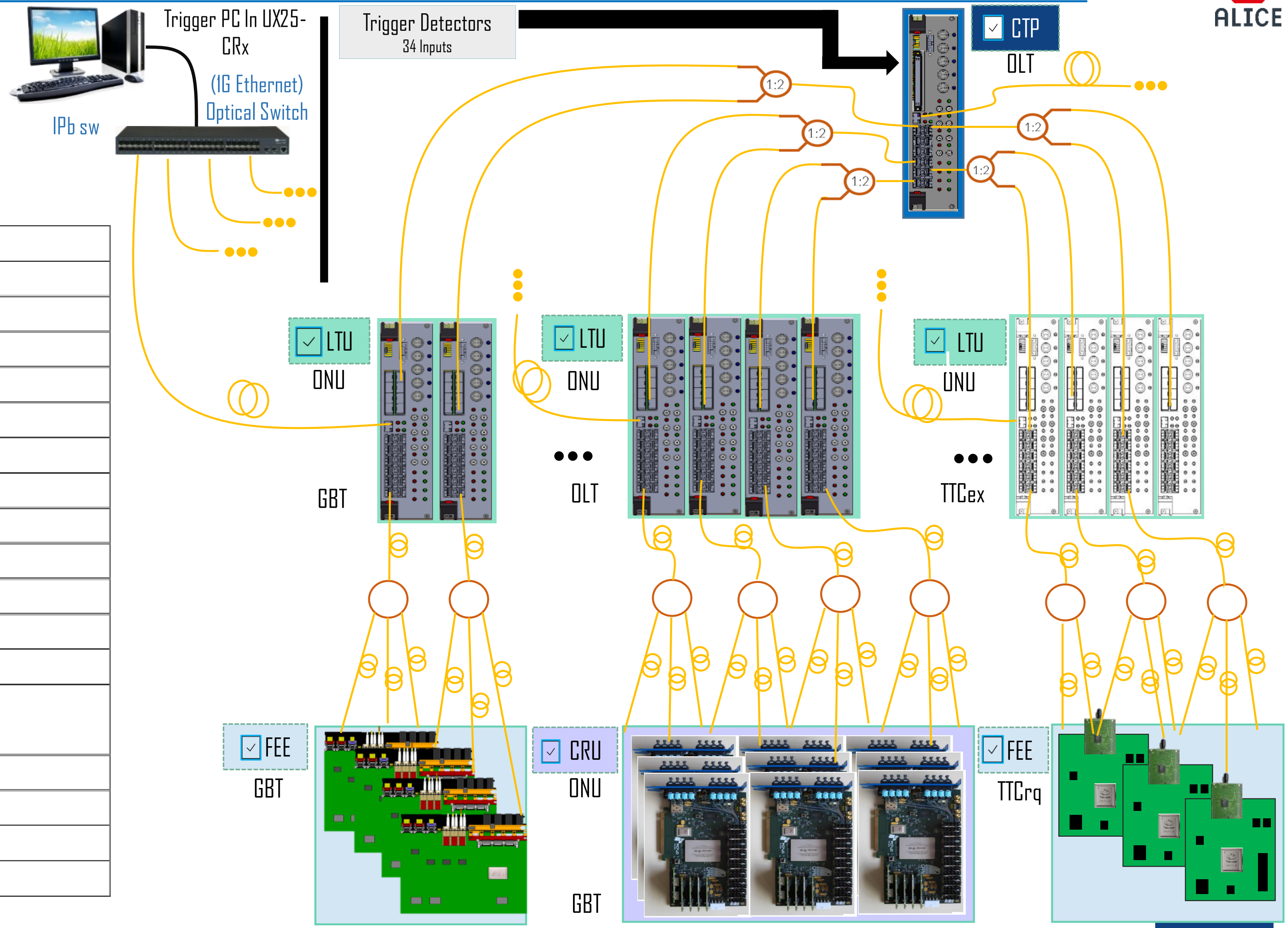
OLT: Optical Line Terminal
ONU: Optical Network Unit

Block Diagram ALICE TTC_PON architecture

Design Proposal (Trigger types)

0	Orbit	Orbit
1	HB	HB
2	HBr	HB reject
3	HBc	Health check
4	Physics	Physics trigger
5	PP	Prepulse
6	Cal	Calibration
7	SOT	Start of Triggered Data
8	EOT	End of Triggered Data
9	SOC	Start of Continuous Data
10	EOC	End of Continuous Data
11	TF	Time Frame delimiter
12	Spare	Not used
⋮	⋮	⋮
28	Spare	Not used
29	SYNC	TPC synchronisation
30	RST	TPC reset
31	TOF	TOF special trigger to signal transferring data from FM to DRM

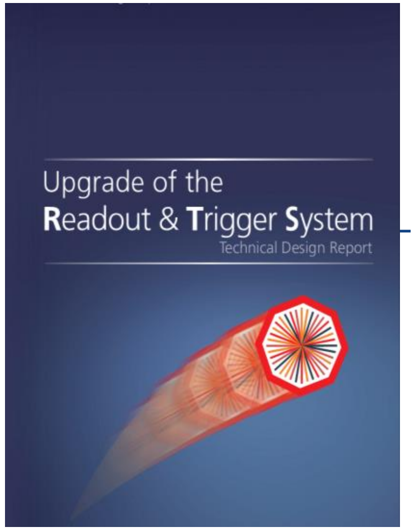
Trigger Types



OLT: Optical Line Terminal
ONU: Optical Network Unit

Block Diagram ALICE TTC_PON architecture

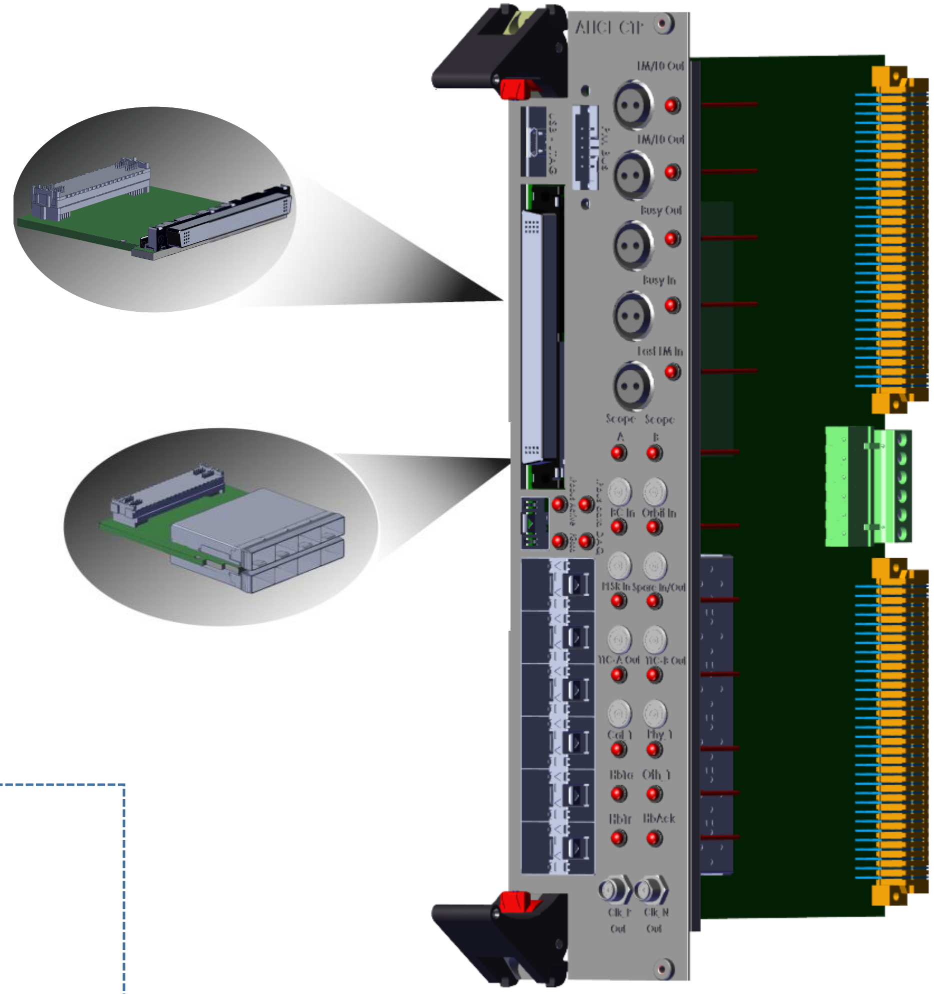
Design



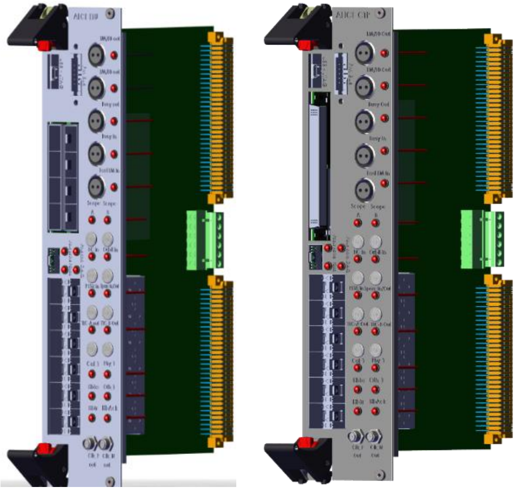
Design
(CTP + LTUs)

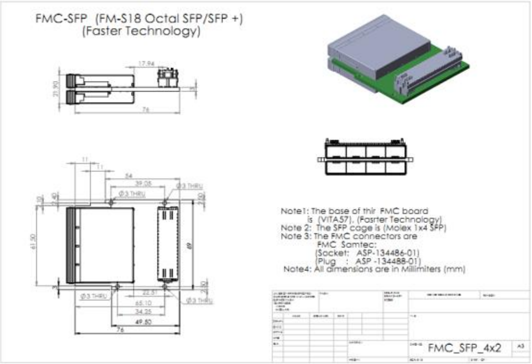
Hardware

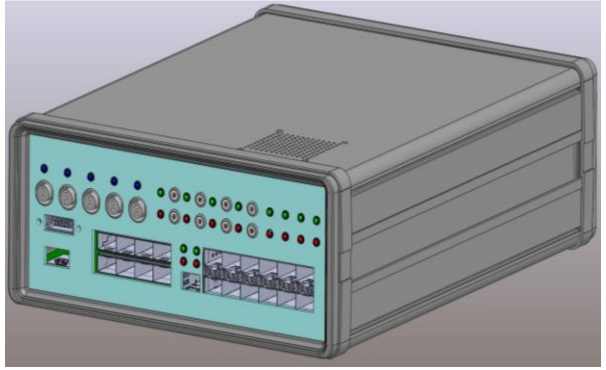
- PCB Design
- Mechanical Drawings
- PCB Simulation

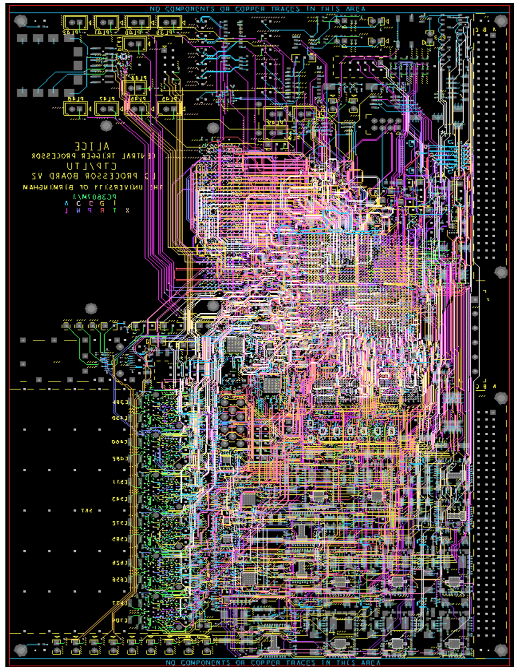


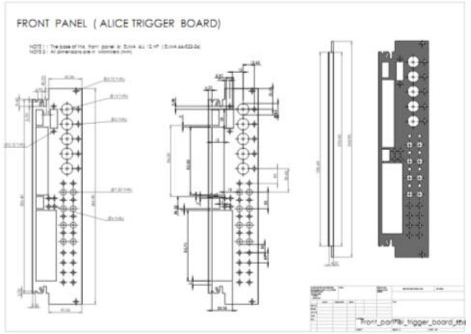
CTP/LTU board (Hardware design in 1 Slide)



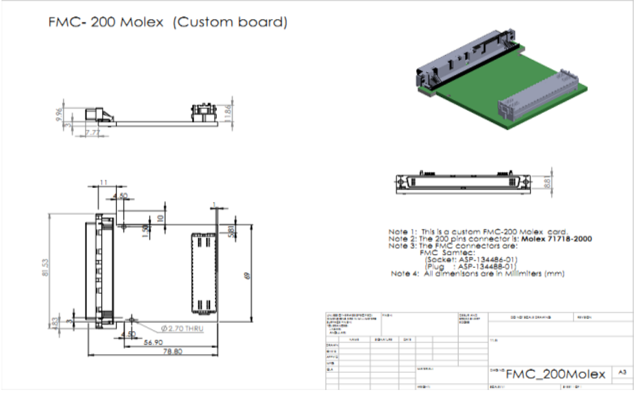


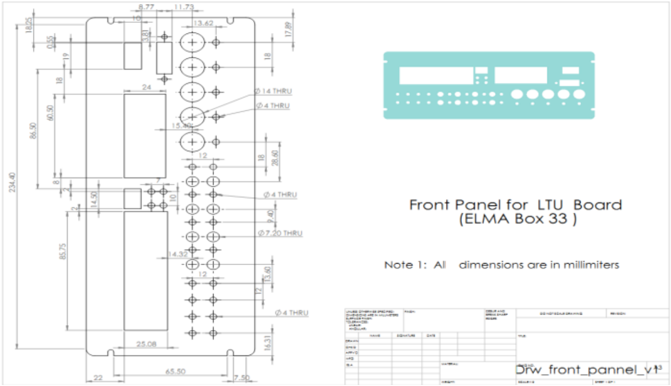


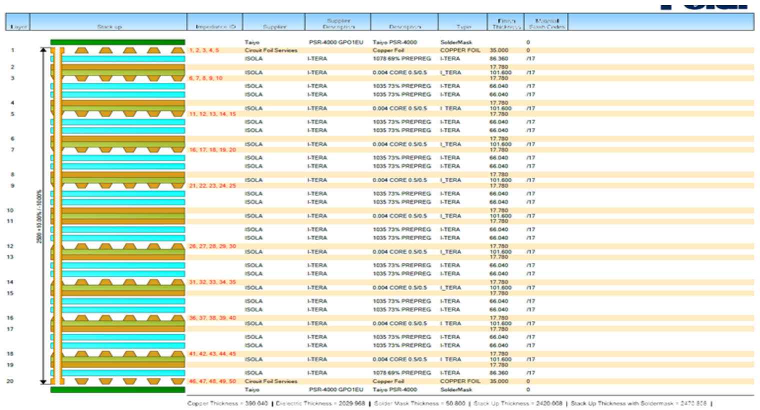




- We are using the new Kintex-Ultrascale FPGA.
- The option to upgrade to an even more powerful Kintex-Ultrascale FPGA is included in the design.
- The design is based around a single universal trigger board (CTP/LTU board).
- Interface between CTP and LTUs is via TTC-PON and optical fan-out unit.
- CTP/LTU board will have a FMC mezzanine card and triple-width front panel
- Will still be based on a VME-type 6u board (VME for power only).
- PCB design
  - 20 Layers (I-TERA MT40 material for high-speed digital multilayer)
  - All clocks have the same length

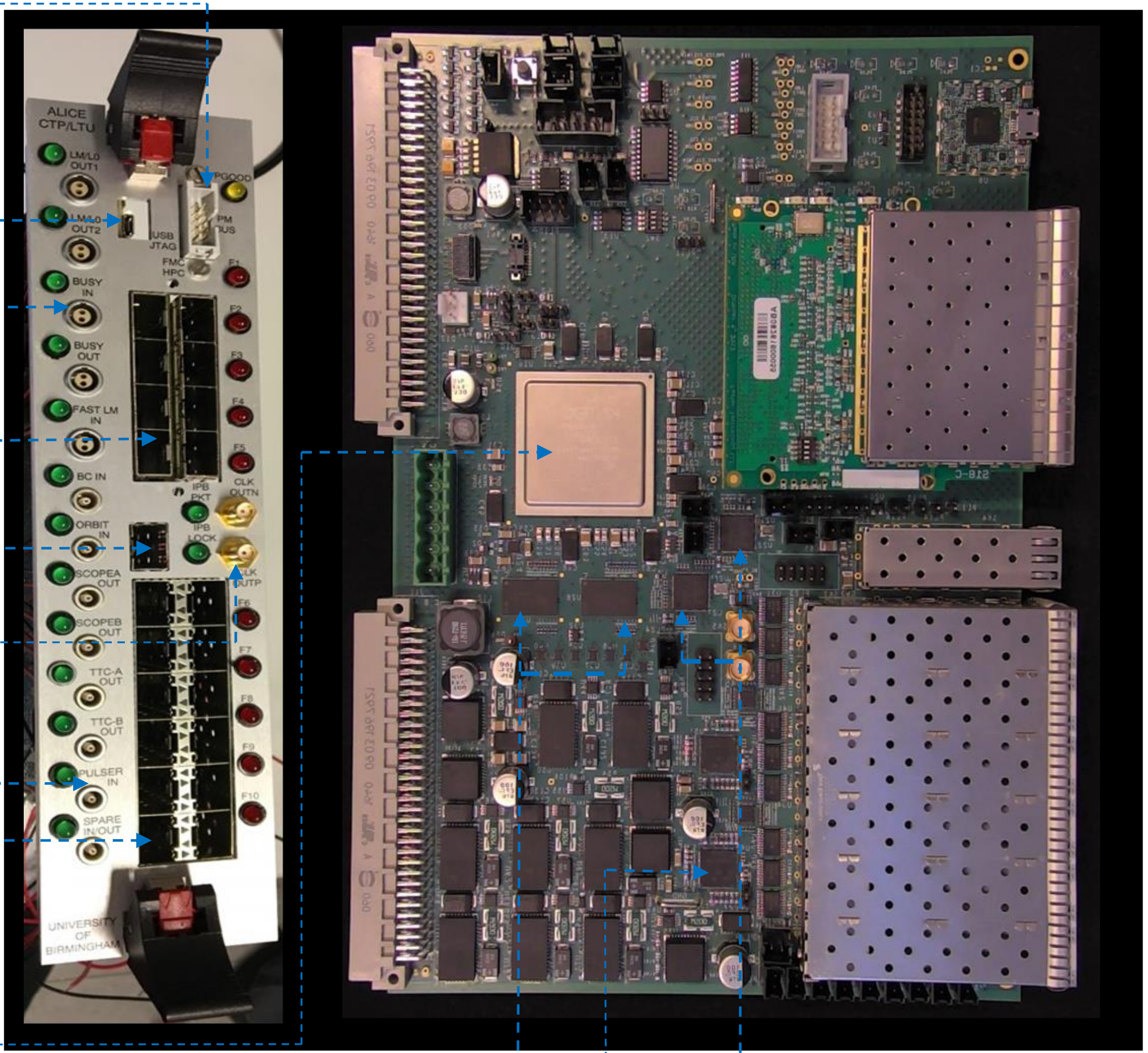






CTP/LTU board

- PM bus connector (Voltage and temperature monitoring).
- USB-JTAG(Programming of FPGA and SPI memory).
- 5 x LVDS LEMO (2x LM/L0 out, BUSY in, BUSY out, Fast LM in).
- FMC board
  LTU mode: FMC S-18 card (optional, GBT, Ethernet)
- SFP+ for IPbus
- Clock Out (LVDs or LVECL, etc...)
- 5 x Lemo 00B (BC in, ORBIT in, Scope A out, Scope B out, TTC-A out, TTC-B out, Pulser in Spare in/out).
- 2x6 SFP +(12 x GBT or 10GPON).
- FPGA Kintex Ultrascale
- 2 DDR4 Memory

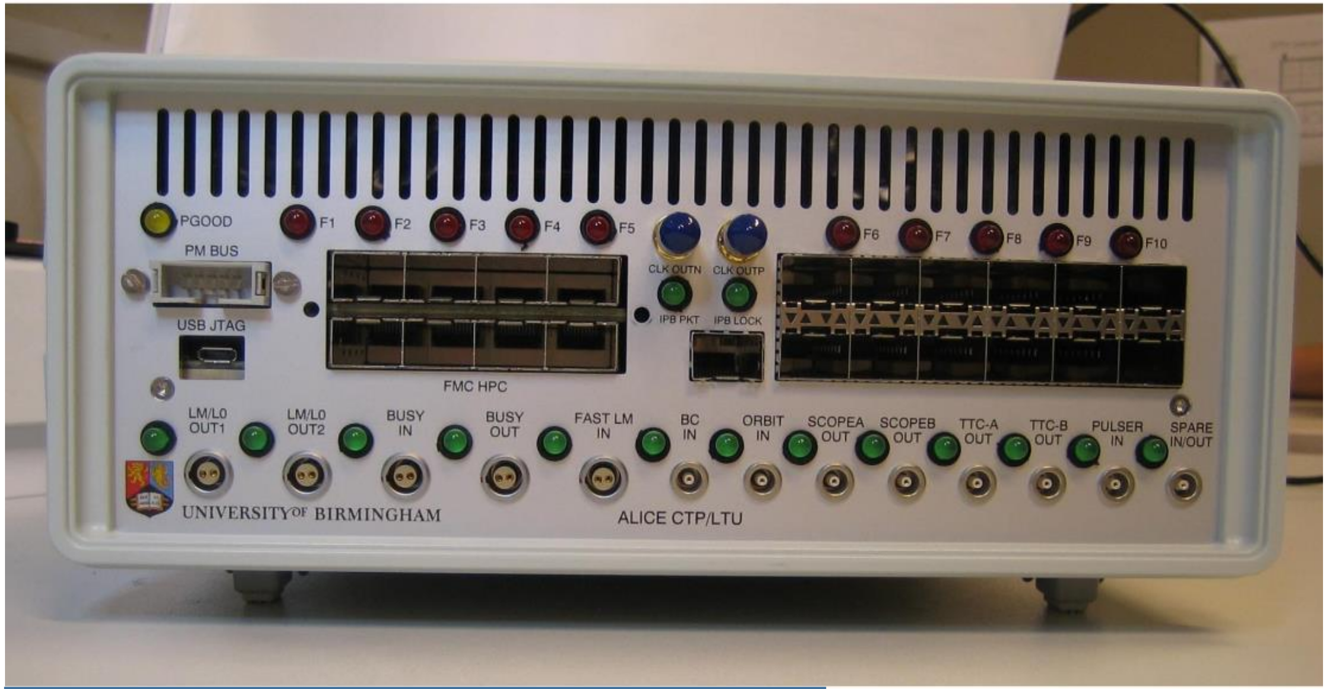


- 2 PLL Si5345
- Power Controller UCD90120A

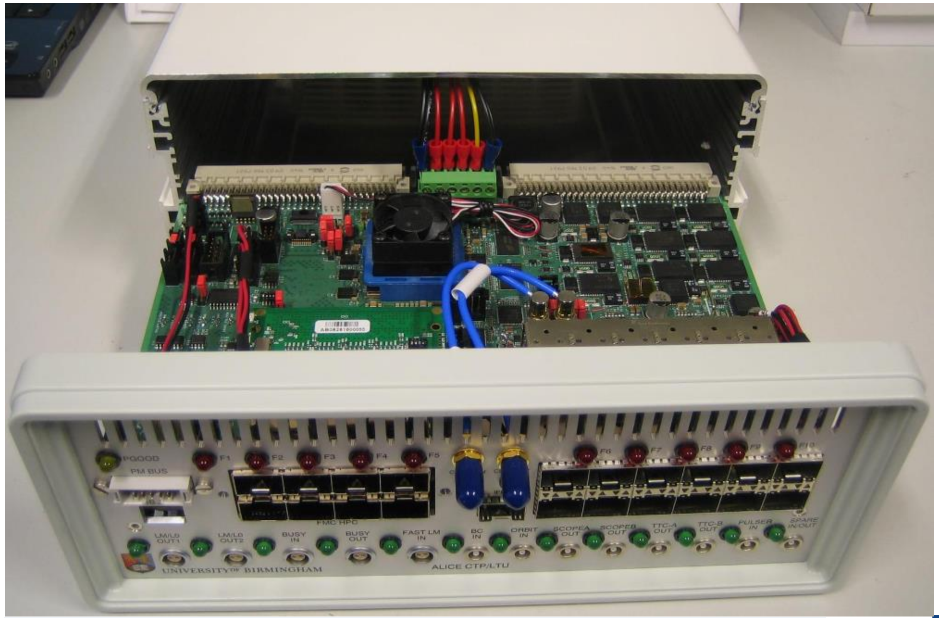
CTP/LTU board (Portable Version)

- LTU board inside standalone box (ELMA Guardbox33).
- Internal power supply + fan for cooling.
- Different version of front panel necessary (ELMA produce it).
- Allows use of LTU in lab without need for VME crate and power supply.

LTU board (ELMAbox) -- Back view

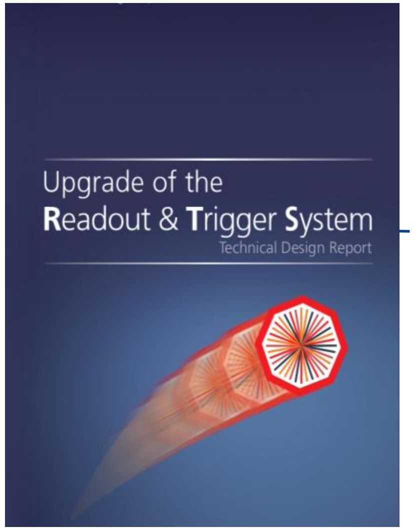


LTU board (ELMAbox) -- Front view



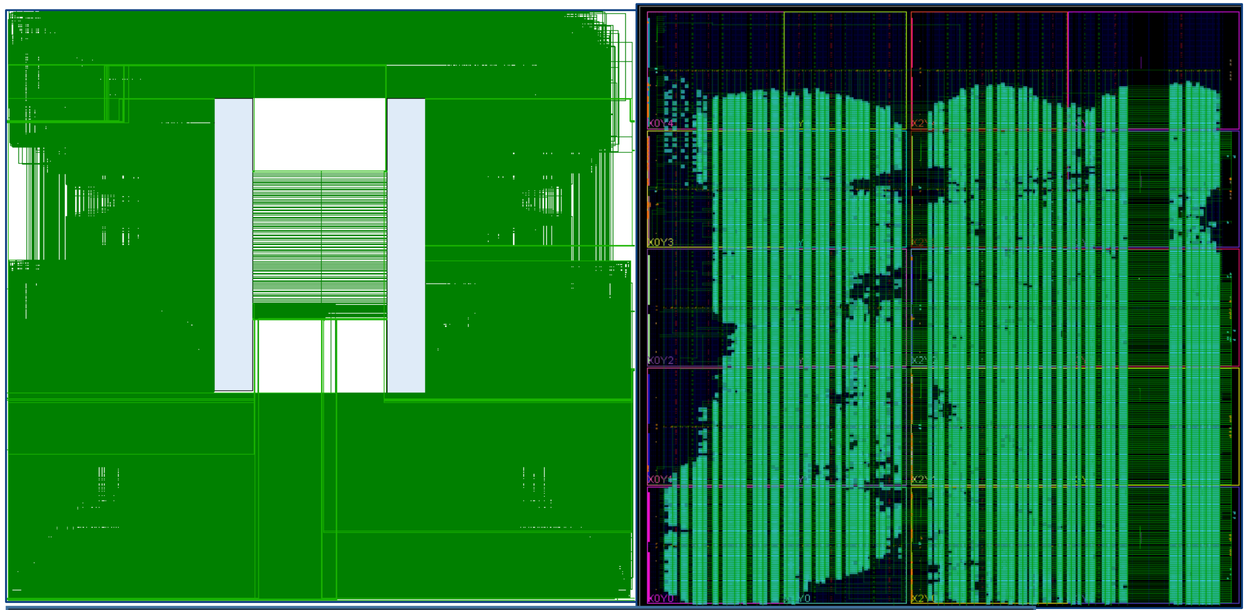
LTU board (ELMAbox) -- Isometric view

Test Logic (IBERT, IPbus, I2C, SPI)
IBERT for FM-S18 Octal SFP/SFP evaluation.



Design
(CTP + LTUs)

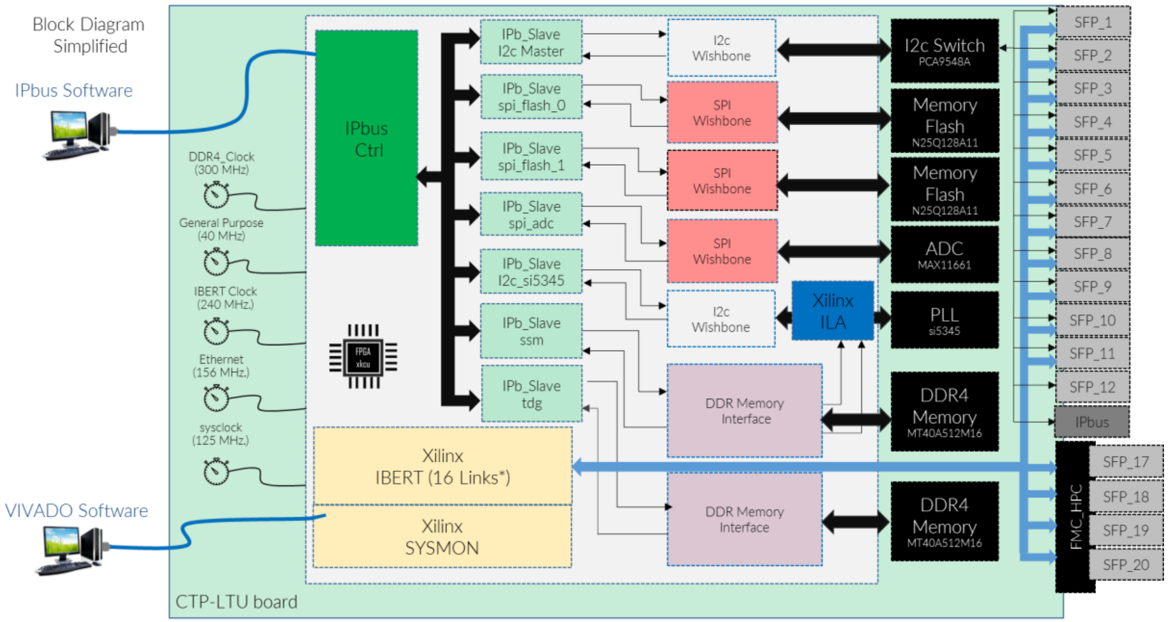
Firmware

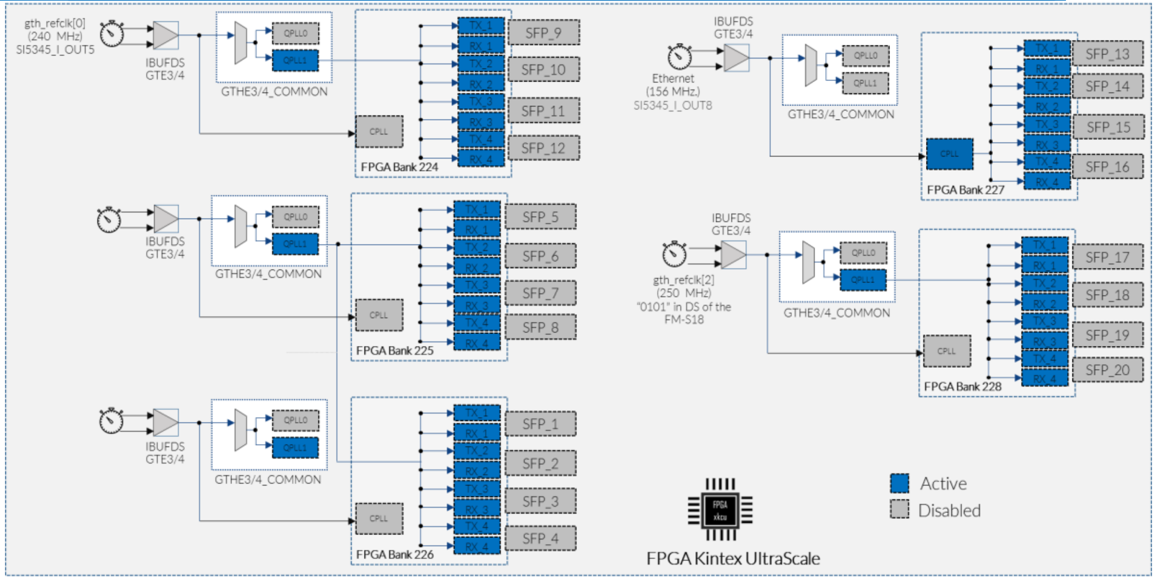


LTU Logic - Schematic and floorplaning

LTU Logic (TTC-PON, GBT, IPbus, DDR4,
Emulator ICAP, I2C, SPI)

Firmware Design for CTP/LTU board (Test Logic)





Test Logic Firmware

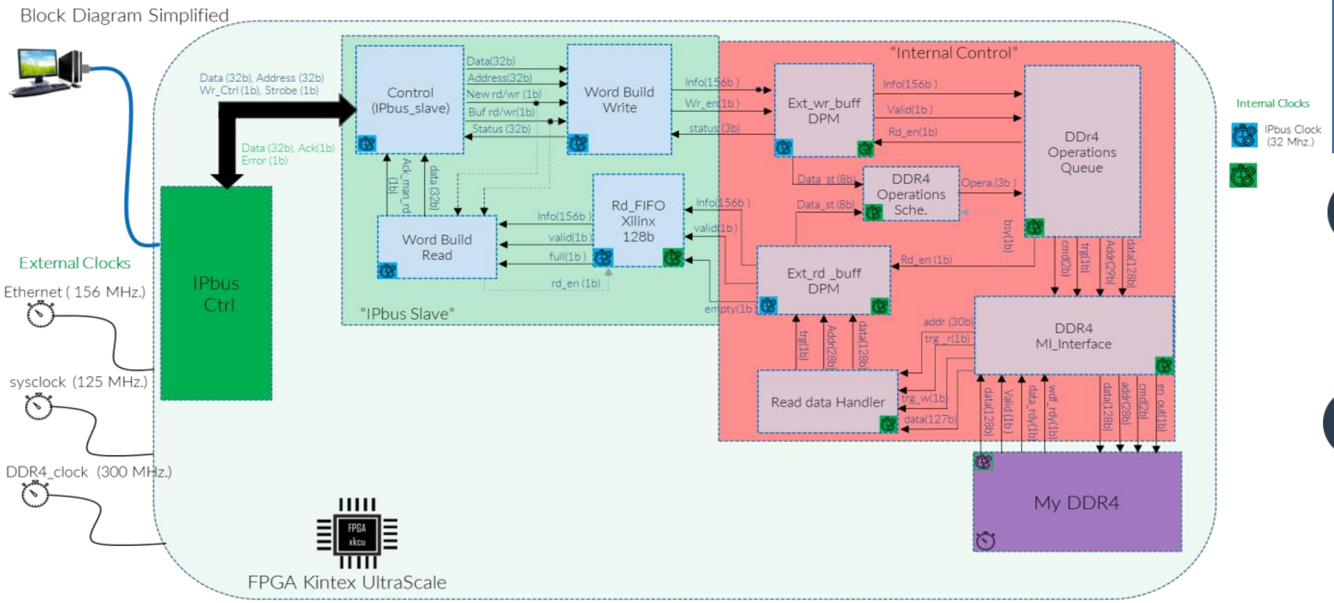
- ✓ 6 IPbus Slaves
- ✓ 2 DDR4
- ✓ 1 I2C ctrl
- ✓ 2 SPI ctrl
- ✓ 1 Gral. Test

IBERT Firmware

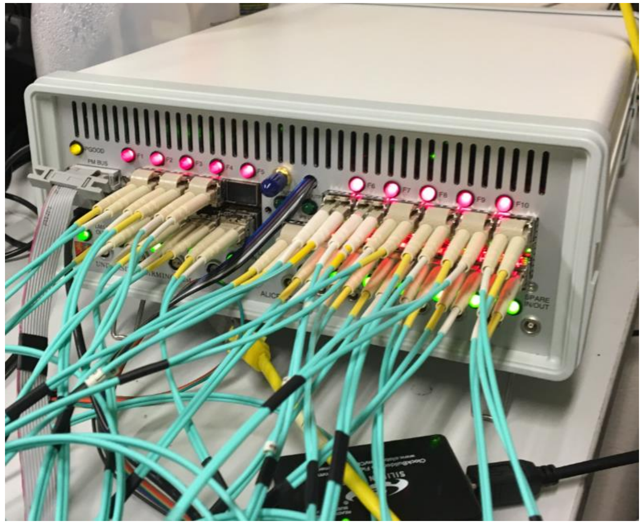
- ✓ 20 BER Test

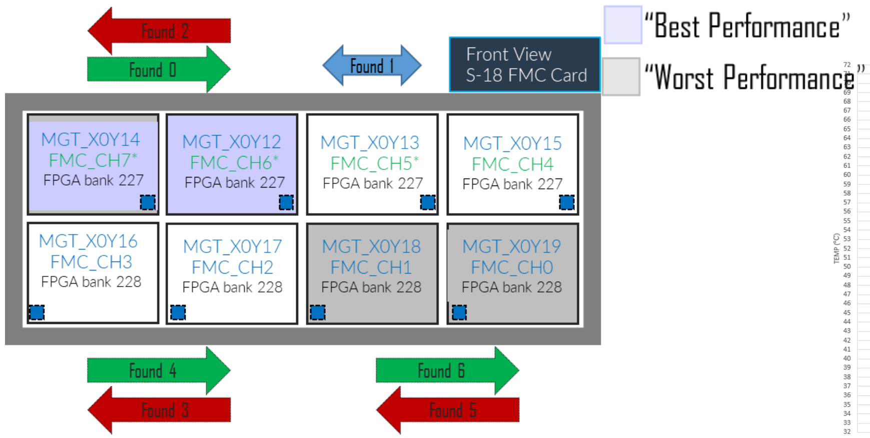
Test Logic + IBERT Firmware

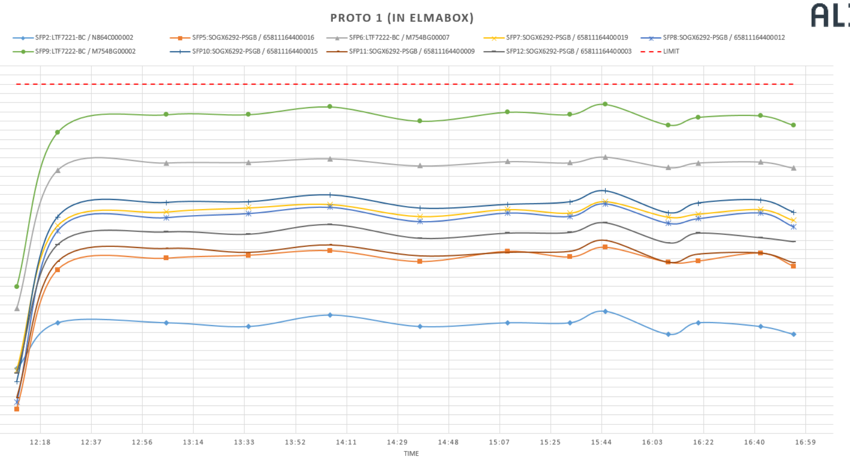
- ✓ 6 IPbus Slaves
- ✓ 2 DDR4
- ✓ 1 I2C ctrl
- ✓ 2 SPI ctrl
- ✓ 1 ICAP
- ✓ 16 BER Test



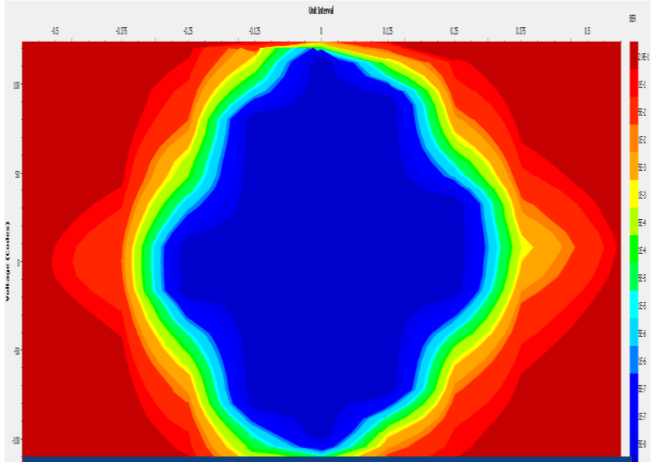
Test Logic Results

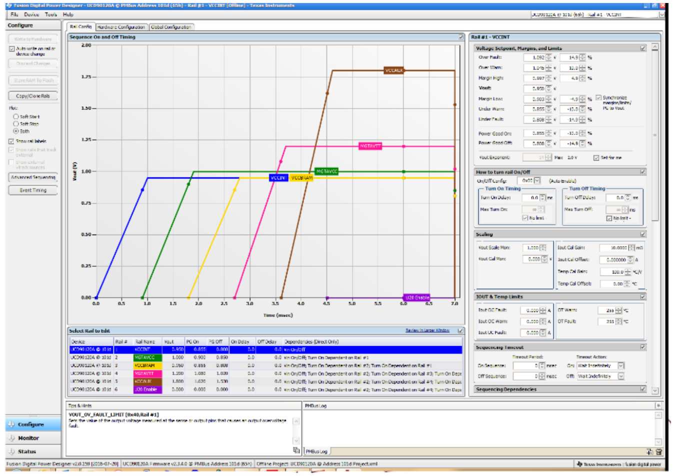


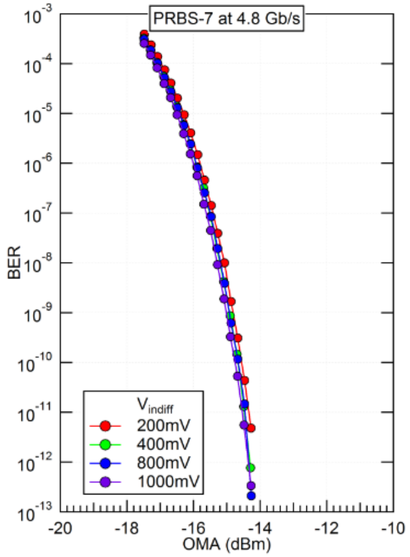


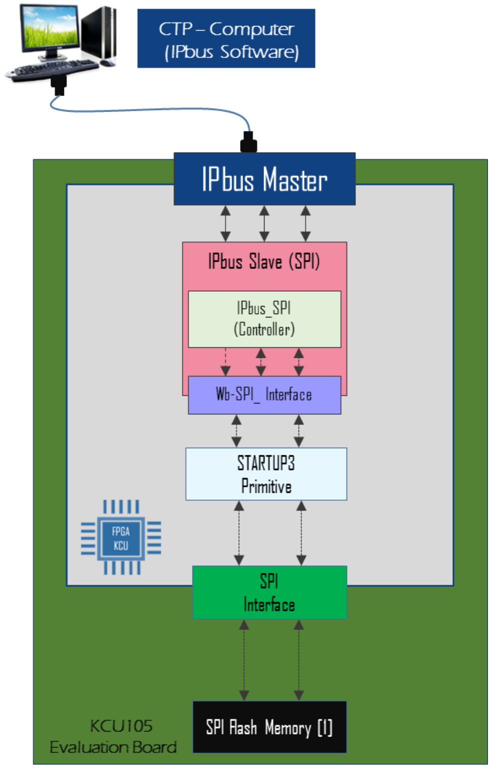


- **Extensive testing** of CTP/LTU board prototype shows **no major problems**.
- Successful PRR at CERN (July 2017)


>> MGT_X0Y09 (Tx_diff_swing = 1080 mV).







DDR4 Memory interface

- The CTP also generates the **Interaction Record** – a list of all bunch-crossing in which the interaction signal has been detected.

- For monitoring and debugging the CTP/LTU board provide a **snapshot memory** – which enable detection of any system inconsistency and identification of possible faults.

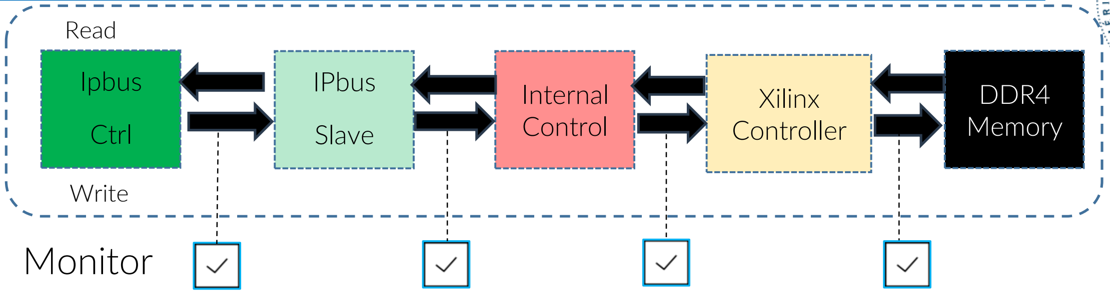
DDR4 Memory Interface – Full Test

In IPbus software

Example:

ssm wrc N blen

- blen → Block Length of each block
  Maximum block size is 0x800
  (software takes care about longer blocks)
- N → Number of the Random blocks
  Randomly written in DDR4 Memory
- wrc → Instruction: Write, Read and Check (pseudo random pattern)
- ssm → Memory Name: 2 in LTU/CTP board
  ssm : SnapShot Memory
  tdg : Trigger Data Generator



Note:

blen	maximum N	
0x800	0x20000	131072 x 2048 =268,435,456 Word/32b
0x100	0x100000	

Snapshot Memory test

```
>ssm  wrc 0x20000 0x800
preparing a random data blok of 2048 words...
DDR kapacity 131072 blocks (1block= 2048 words), last 0 words excluded from the test
N:131072 nfirst:43
write/read/check 0. (block 43 in words:88064)
write/read/check 1000. (block 43043 in words:88152064)
write/read/check 2000. (block 86043 in words:176216064)
write/read/check 3000. (block 129043 in words:264280064)
write/read/check 4000. (block 40971 in words:83908608)
write/read/check 5000. (block 83971 in words:171972608)
write/read/check 6000. (block 126971 in words:260036608)
⋮
write/read/check 126000. (block 44091 in words:90298368)
write/read/check 127000. (block 87091 in words:178362368)
write/read/check 128000. (block 130091 in words:266426368)
write/read/check 129000. (block 42019 in words:86054912)
write/read/check 130000. (block 85019 in words:174118912)
write/read/check 131000. (block 128019 in words:262182912)
Blocks: 131072 of 2048 words, 0.29 MB/sec, checked: 268435456 words, errs:0
```

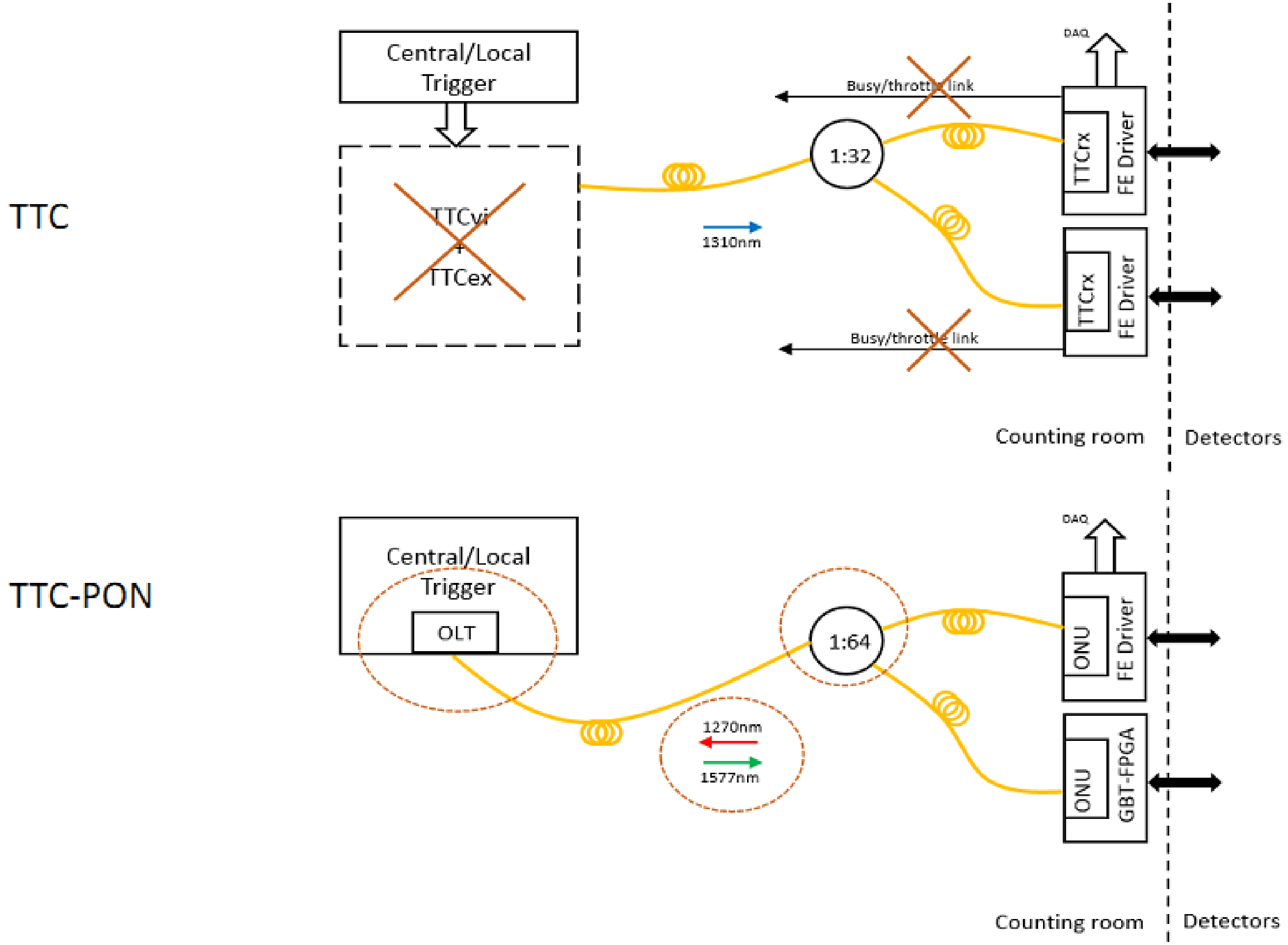
Results: Full test (Write Read and Check) → OK

Trigger Data Generator Memory test

```
>tdg wrc 0x20000 0x800
preparing a random data blok of 2048 words...
DDR kapacity 131072 blocks (1block= 2048 words), last 0 words excluded from the test
N:131072 nfirst:43
write/read/check 0. (block 43 in words:88064)
write/read/check 1000. (block 43043 in words:88152064)
write/read/check 2000. (block 86043 in words:176216064)
write/read/check 3000. (block 129043 in words:264280064)
write/read/check 4000. (block 40971 in words:83908608)
write/read/check 5000. (block 83971 in words:171972608)
write/read/check 6000. (block 126971 in words:260036608)
⋮
write/read/check 126000. (block 44091 in words:90298368)
write/read/check 127000. (block 87091 in words:178362368)
write/read/check 128000. (block 130091 in words:266426368)
write/read/check 129000. (block 42019 in words:86054912)
write/read/check 130000. (block 85019 in words:174118912)
write/read/check 131000. (block 128019 in words:262182912)
Blocks: 131072 of 2048 words, 0.29 MB/sec, checked: 268435456 words, errs:0
```

Results: Full test (Write Read and Check) → OK

The Timing, Trigger and Control (TTC) system is a **crucial** system dedicated to **synchronization** of **experiment electronics** to the **LHC beam**.

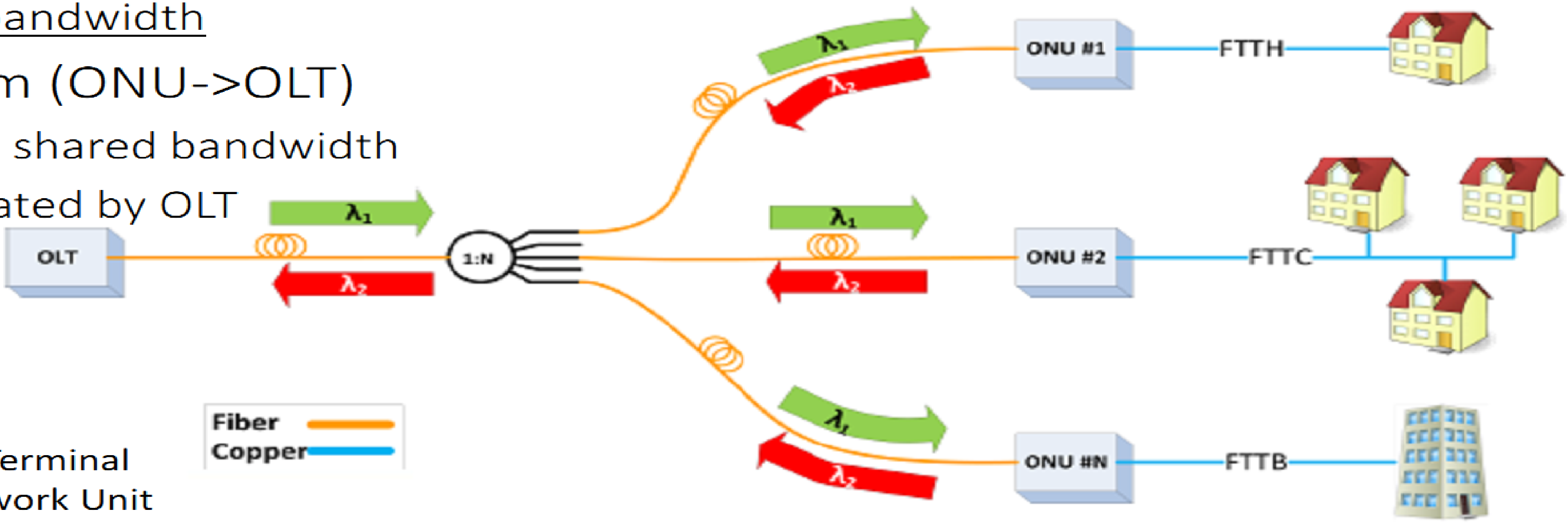


TTCvi : VMEbus interface module
TTCex: Encoder + transmitter
TTCrx: Receiver
FEE : Driver:front.end driver

PON Basics

TTC PON

- PON = Passive Optical Network
  - Used in FTTH
- Point to Multipoint Network (P2M)
  - Bidirectional / WDM: 1 fiber, 2 wavelengths (1 Up, 1 Down)
- Downstream (OLT->ONU)
  - High bandwidth
- Upstream (ONU->OLT)
  - Low & shared bandwidth
  - Arbitrated by OLT

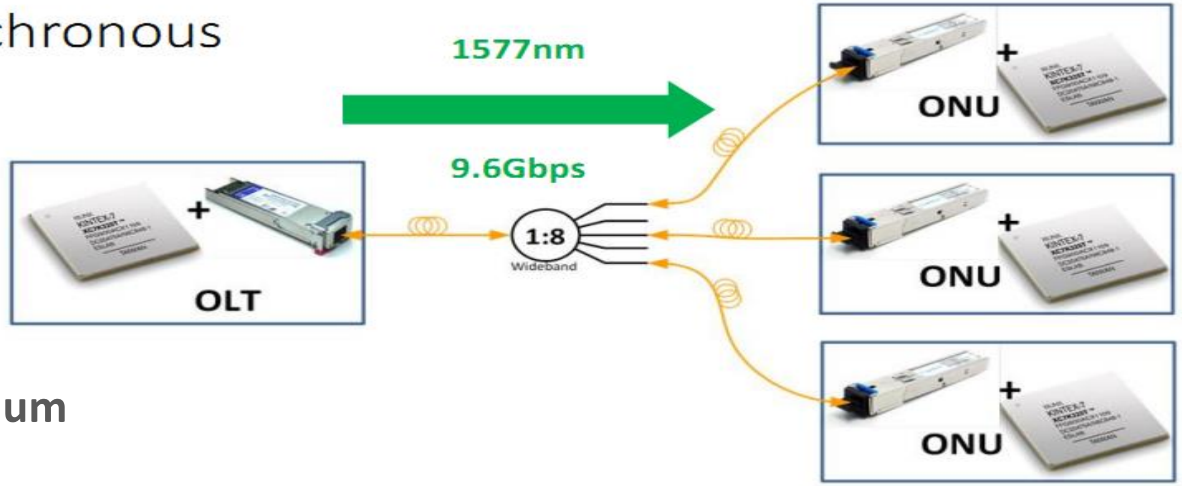


OLT=Optical Line Terminal
ONU=Optical Network Unit

Downstream path

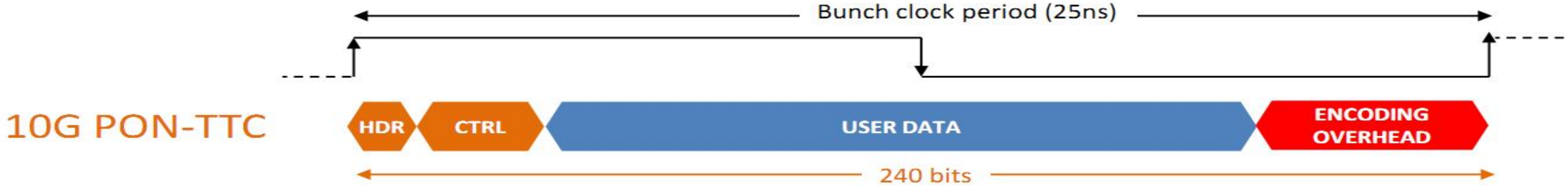
TTC PON

- OLT → ONUs (continuous transmission)
- 9.6Gbps serial link (240 raw bits per BC / 8b header, 24b – control)
- LHC Bunch Clock (BC) synchronous
- Fixed & Low latency
- High bandwidth

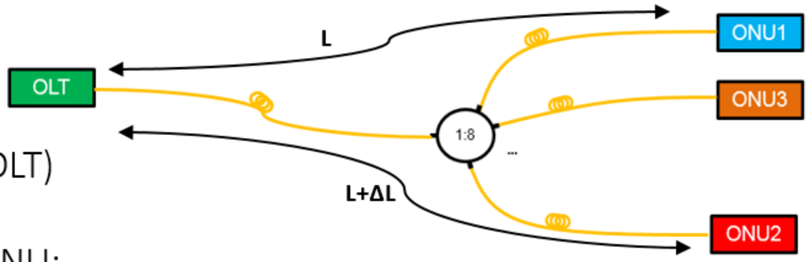


User Field: 20 bytes (160 bits)

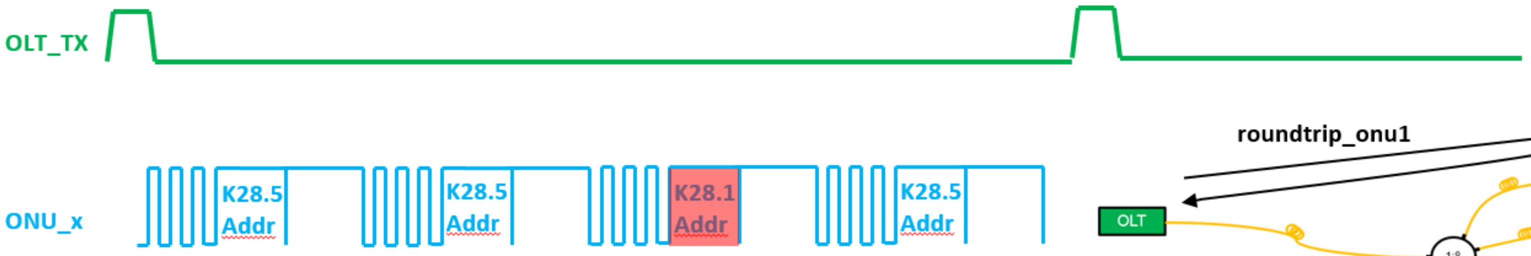
9.6Gbps, **6.4Gbps User Bandwidth maximum**

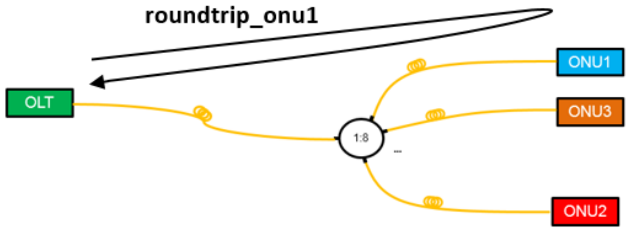


Upstream Challenges



- TDM arbitration – Calibration
  - The procedure is arbitrated by the master (OLT)
  - OLT measures the roundtrip time for each ONU:
    - OLT sends a command: ONU_x enters in calibration_mode / all the others disable transmission
    - When a onu is in calibration_mode, it sends data in a continuous way and acts as a comma-mirror

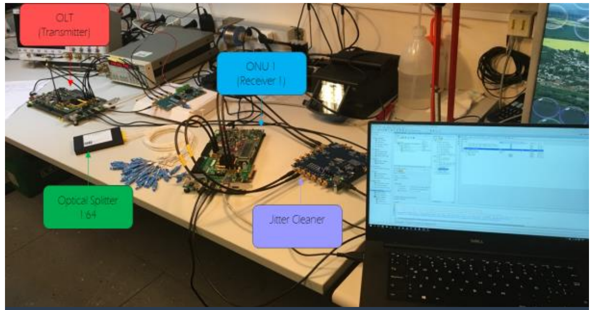




- ONUs → OLT (TDMA)
- 2.4Gb/s line-rate (1270nm)
- Synchronized to downstream
- 8b10b encoded
- Total burst length: 125ns (100ns burst + 25ns gap)

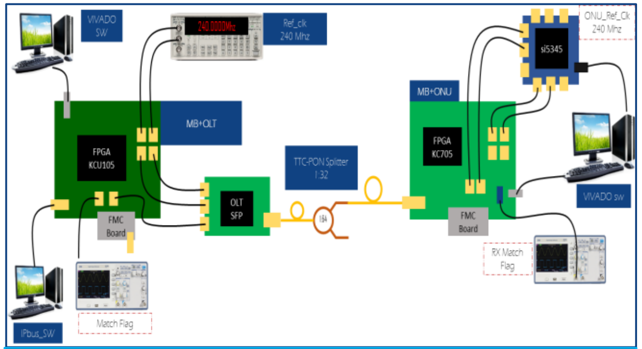
    - ONU_x offset is compensated depending in the measured roundtrip

TTC-PON in ALICE (Evolution)

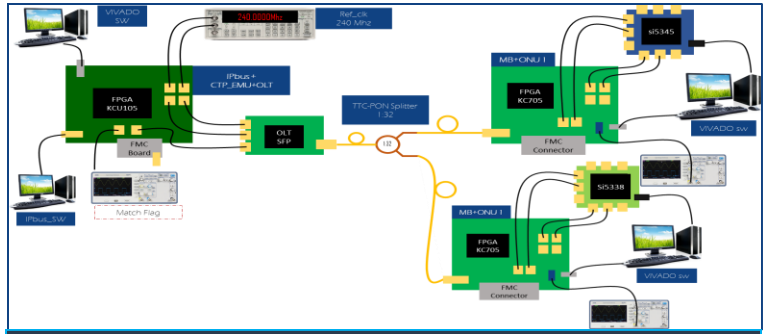


TTC-PON ver_0_0 in KC705
1 OLT. Ctrl/Cfg: Microblaze, SDK
1 ONU. Ctrl/Cfg: Microblaze, SDK
Testability: Counter, PRBS7, PRBS23
Downstream

START

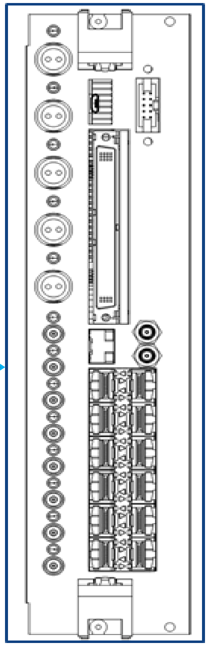


TTC-PON ver_0_1
1 OLT (KCU105). Ctrl/Cfg: IPbus
1 ONU (KC705). Ctrl/Cfg: Microblaze, SDK
Testability: CTP_EMU, Counter, PRBS7, PRBS23 Downstream & Upstream.



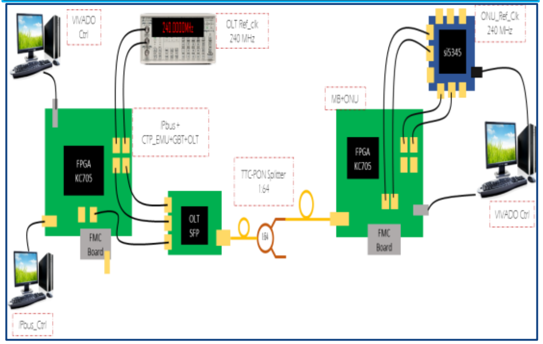
TTC-PON ver_0_3
1 OLT (KCU105) Ctrl/Cfg: IPbus use the FMC_TTC_PON.
2 ONUs (KC705). Ctrl/Cfg: Microblaze, SDK
Testability: CTP_EMU, Counter, PRBS7, PRBS23
Downstream/Upstream
Include calibration process

CTP/LTU board

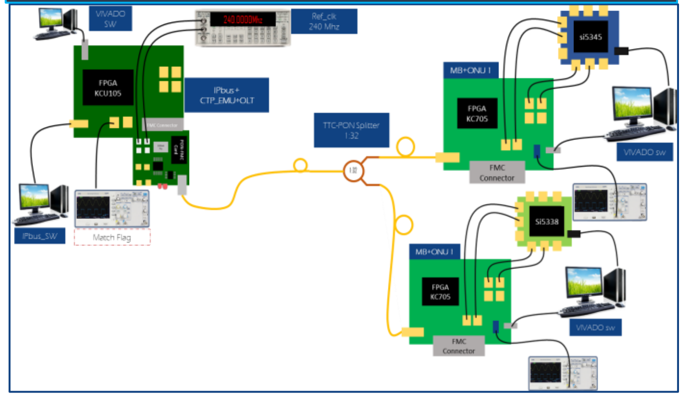


LTU Logic

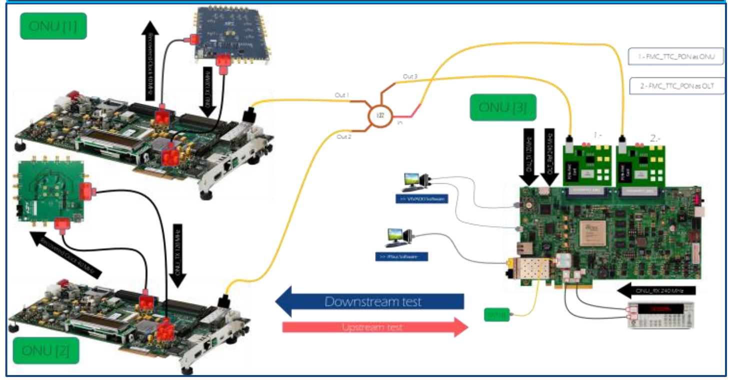
TTC-PON ver_0_1 in KC705
1 OLT. Ctrl/Cfg: IPbus
1 ONU. Ctrl/Cfg: Microblaze, SDK
Testability: CTP_EMU, Counter, PRBS7, PRBS23 Downstream.



TTC-PON ver_0_2
1 OLT (KCU105) Ctrl/Cfg: IPbus
2 ONUs (KC705). Ctrl/Cfg: Microblaze, SDK
Testability: CTP_EMU, Counter, PRBS7, PRBS23, Downstream/Upstream
Include calibration process



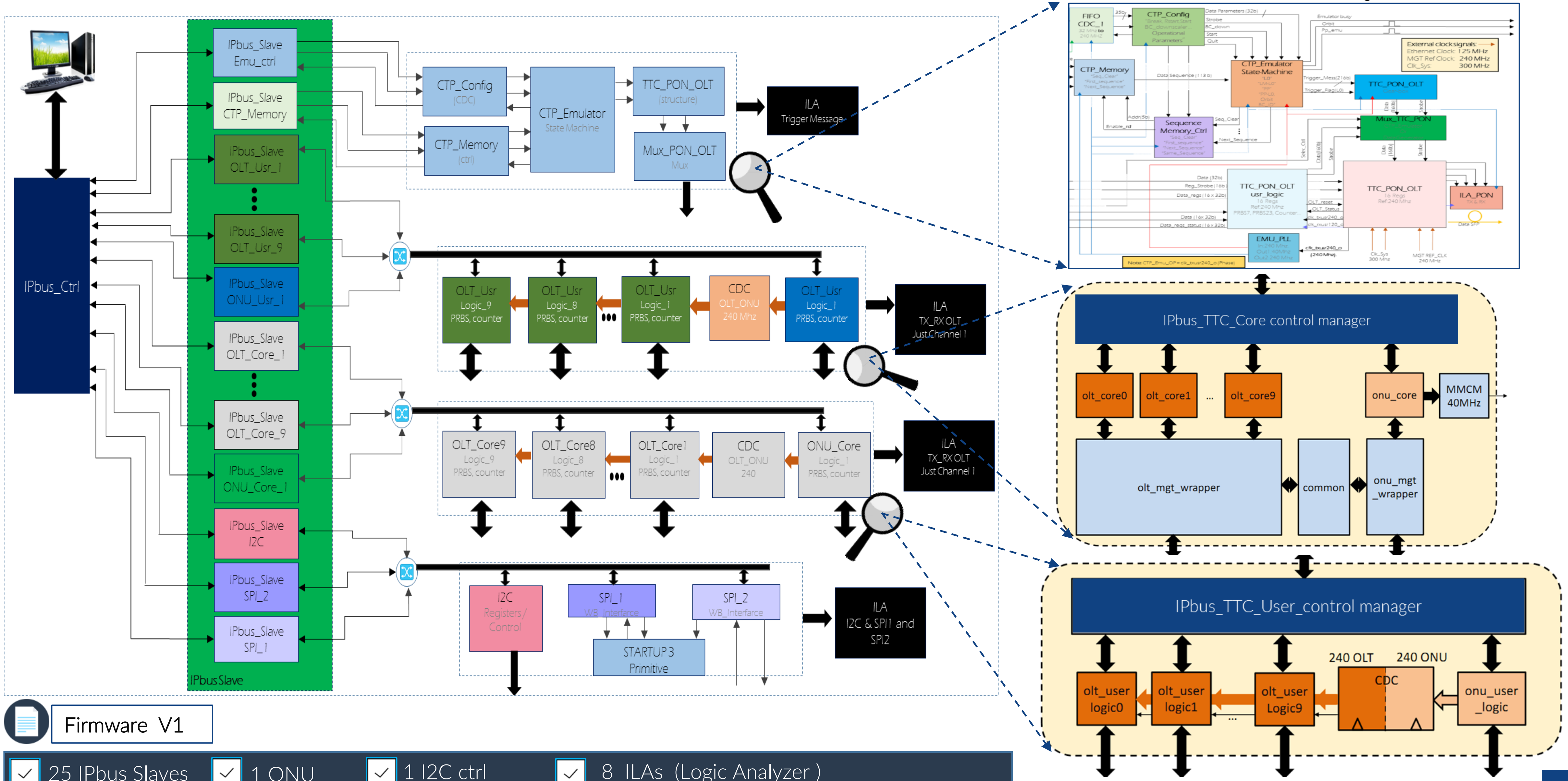
TTC-PON ver_0_4
9 OLT (KCU105) Ctrl/Cfg: IPbus
1 ONU (KCU105) Ctrl/Cfg: Ipbus
2 FMC_TTC_PON (OLT/ONU).
2 ONUs (KC705). Ctrl/Cfg: Microblaze, SDK
Testability: CTP_EMU, Counter, PRBS7, PRBS23
Downstream/Upstream Include calibration process



LTU – Logic (Block-Diagram - Firmware)

A Large Ion Collider Experiment

ALICE



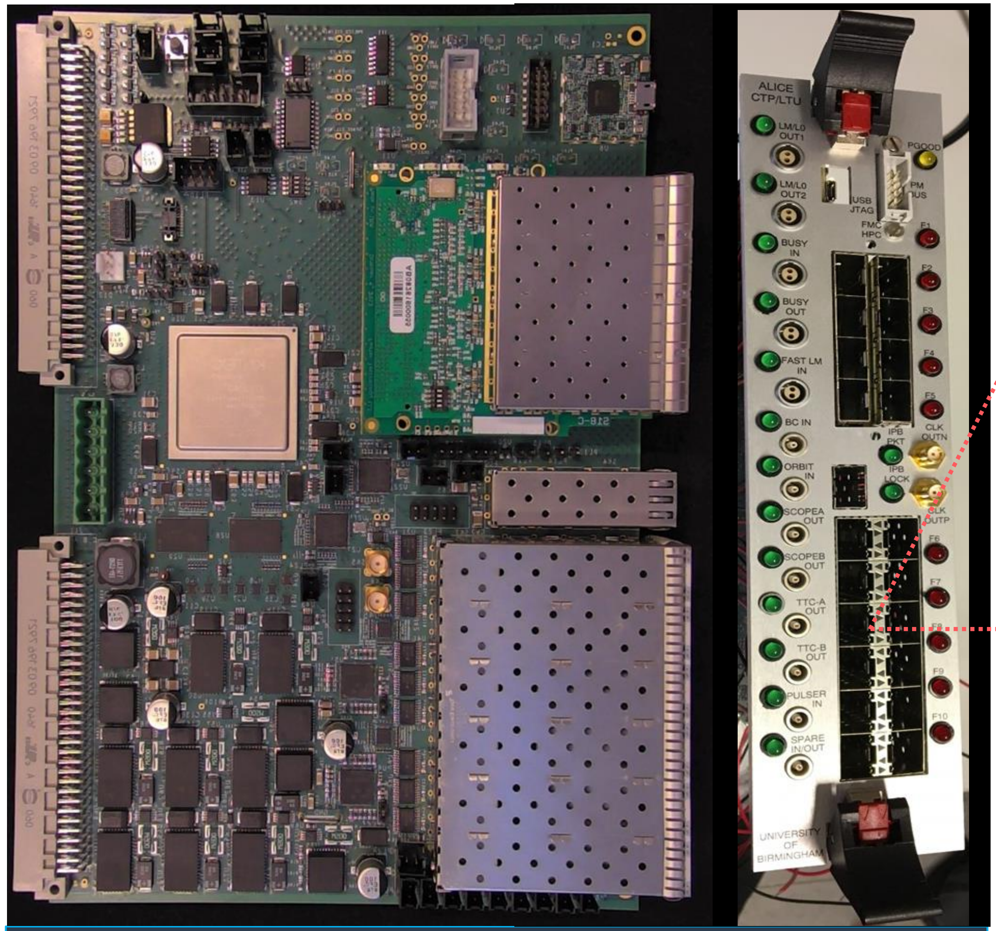
Firmware V1

- ☑ 25 IPbus Slaves
- ☑ 1 ONU
- ☑ 1 I2C ctrl
- ☑ 8 ILAs (Logic Analyzer)
- ☑ 8 OLTs
- ☑ 2 SPI ctrl
- ☑ 1 CTP_ Emulator
- ☑ 1 GBT Link
- ☑ 2 DDR4 Interface

ONU and OLTs distribution in CTP/LTU board

TTC_PON

Encoder Downstream FEC
9 OLTs (200 User bits)
1 ONU (56 User bits)
Control via IPbus



- CTP/LTU board.

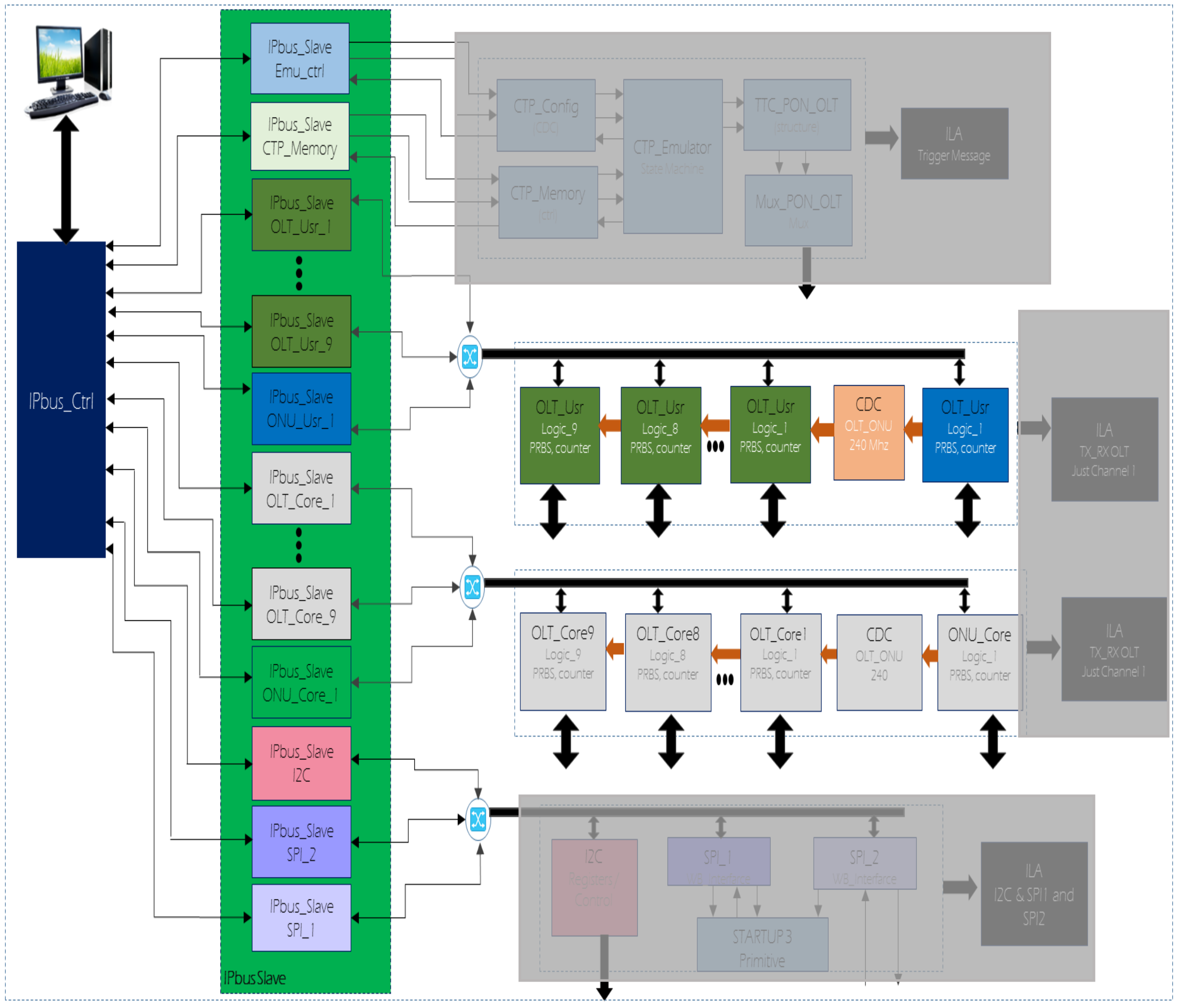
F6 F10

GBT OLT ONU

MGT_X0Y08 SFP 1 FPGA bank 226 I2CMUX45_ch2 OLT 8	MGT_X0Y10 SFP 3 FPGA bank 226 I2CMUX45_ch4 GBT *	MGT_X0Y04 SFP 5 FPGA bank 225 I2CMUX45_ch6 OLT 4	MGT_X0Y06 SFP 7 FPGA bank 225 I2CMUX59_ch2 OLT 6	MGT_X0Y00 SFP 9 FPGA bank 224 I2CMUX59_ch4 OLT 0	MGT_X0Y02 SFP 11 FPGA bank 224 I2CMUX59_ch6 OLT 2
MGT_X0Y09 SFP 2 FPGA bank 226 I2CMUX45_ch3 ONU	MGT_X0Y11 SFP 4 FPGA bank 226 I2CMUX45_ch5	MGT_X0Y05 SFP 6 FPGA bank 225 I2CMUX45_ch7 OLT 5	MGT_X0Y07 SFP 8 FPGA bank 225 I2CMUX59_ch3 OLT 7	MGT_X0Y01 SFP 10 FPGA bank 224 I2CMUX59_ch5 OLT 1	MGT_X0Y03 SFP 12 FPGA bank 224 I2CMUX59_ch7 OLT 3

GBT*: MGT ref clock 120 MHz
Latency Optimized (TX & RX)
GBT Encoder
Control via VIVADO VIO

LTU – Logic (Features of the TTC-PON system)



LTU Firmware V1

- ☑ 25 IPbus Slaves
- ☑ 1 ONU
- ☑ 1 I2C ctrl
- ☑ 8 ILAs (Logic Analyzer)
- ☑ 8 OLTs
- ☑ 2 SPI ctrl
- ☑ 1 CTP_ Emulator
- ☑ 1 GBT Link

Ctrl & cfg. of all OLTs via IPbus

```
>useolt 2
Using OLT 2
>olt
OLT CORE: fy v4, using OLT2.
 0:        HB_PERIOD_25 > 0 0x    ffff:0x       0
 1:         HB_PERIOD_8_3 > 0 0x     fff:0x       0
 2:  SLOW_CTRL_MSG_ONU > 0 0x  ffffff:0x       0
 3:        CAL_ONU_ADDR > 0 0x      ff:0x       0
  :              CAL_ON > 8 0x       1:0x       0
  :            CAL_INIT > 9 0x       1:0x       0
  : ONU_POSITION_LATCH >10 0x       1:0x       0
 4:     BERT_ONU_A_ADDR > 0 0x      ff:0x       0
  :     BERT_ONU_B_ADDR > 8 0x      ff:0x       0
  :          BERT_CLEAR >16 0x       1:0x       0
  :          BERT_LATCH >17 0x       1:0x       0
 5:      BURST_LENGTH-1 > 0 0x      3f:0x       0
  :    SFP_RESET_RX_POS > 6 0x      3f:0x       0
  : SFP_RESET_RX_ENABL >12 0x       1:0x       0
 6: SLOW_CTRL_FROM_ONU > 0 0x  ffffff:0x  b401f6
 7: RONDTRIP_FINE_DELA > 0 0x      7f:0x       0
  : RONDTRIP_COARSDELA > 7 0x    ffff:0x       0
 8:     ERROR_SUM_ONU_A > 0 0x    ffff:0x       0
  :     ERROR_SUM_ONU_B >16 0x    ffff:0x       0
 9:   BERT_LOCKED_ONU_A > 0 0x       1:0x       0
  :   BERT_LOCKED_ONU_B > 1 0x       1:0x       0
  : BERT_FINISHED_ONU_ > 2 0x       1:0x       0
  : BERT_FINISHED_ONU_ > 3 0x       1:0x       0
10:     MGT_TX_POLARITY > 0 0x       1:0x       1
  :     MGT_RX_POLARITY > 1 0x       1:0x       0
OLT USER:
 0:                OLT_CORE_RESET > 0 0x        1:0x       0
 1:                RX_BBERT_CLEAR > 0 0x        1:0x       0
  :                RX_BBERT_LATCH > 1 0x        1:0x       0
  :      RX_BBERT_HEARTBEAT_PERIOD > 2 0x     ffff:0x       0
 2:                SEL_TX_PATTERN > 0 0x        1:0x       0
 3:              OLT_MGT_PLL_LOCK > 0 0x        1:0x       1
  :              OLT_MGT_TX_READY > 1 0x        1:0x       1
  :              OLT_MGT_RX_READY > 2 0x        1:0x       1
 4:         BBERT_ONU_BITSUM(31:0) > 0 0xffffffff:0x       0
 5:        BBERT_ONU_BITSUM(47:32) > 0 0x     ffff:0x       0
 6:       BBERT_ONU_ERRORSUM(31:0) > 0 0xffffffff:0x       0
 7:      BBERT_ONU_ERRORSUM(47:32) > 0 0x     ffff:0x       0
 8:  BBERT_ONU_PACKETLOSSSUM(31:0) > 0 0xffffffff:0x       0
 9: BBERT_ONU_PACKETLOSSSUM(47:32) > 0 0x     ffff:0x       0
10:      BBERT_SELECT_CHANNEL(3:0) > 0 0x        f:0x       0
```

Ctrl & cfg. of the ONU via IPbus

```
>onu
ONU1 CORE:MODE[7..0]:233  HB_PERIOD[31-16]:0  HB_PERIOD[15-0]:29
     SFP_ENA_DEL:9  FINE__OFFSET_TDM:0
USER:
ADD:1  BERT_CLEAR 1[0]:0  BERT_LATCH 1[1]:0
SEL_TX_PAT 2[1-0]:0=PRBS7 TX_INT_MODE 2[2]:0  TX_INJECT_ERR 2[3]:0
3[7-0]:0xfd= RXPLLLOCK TXPLLLOCK RXRDY TXRDY OPER RXLOCKED RX40LOCKED
BITSUM: 2726704256 24   ERRSUM:0 0
```

TTC_PON test Menu (IPbus)

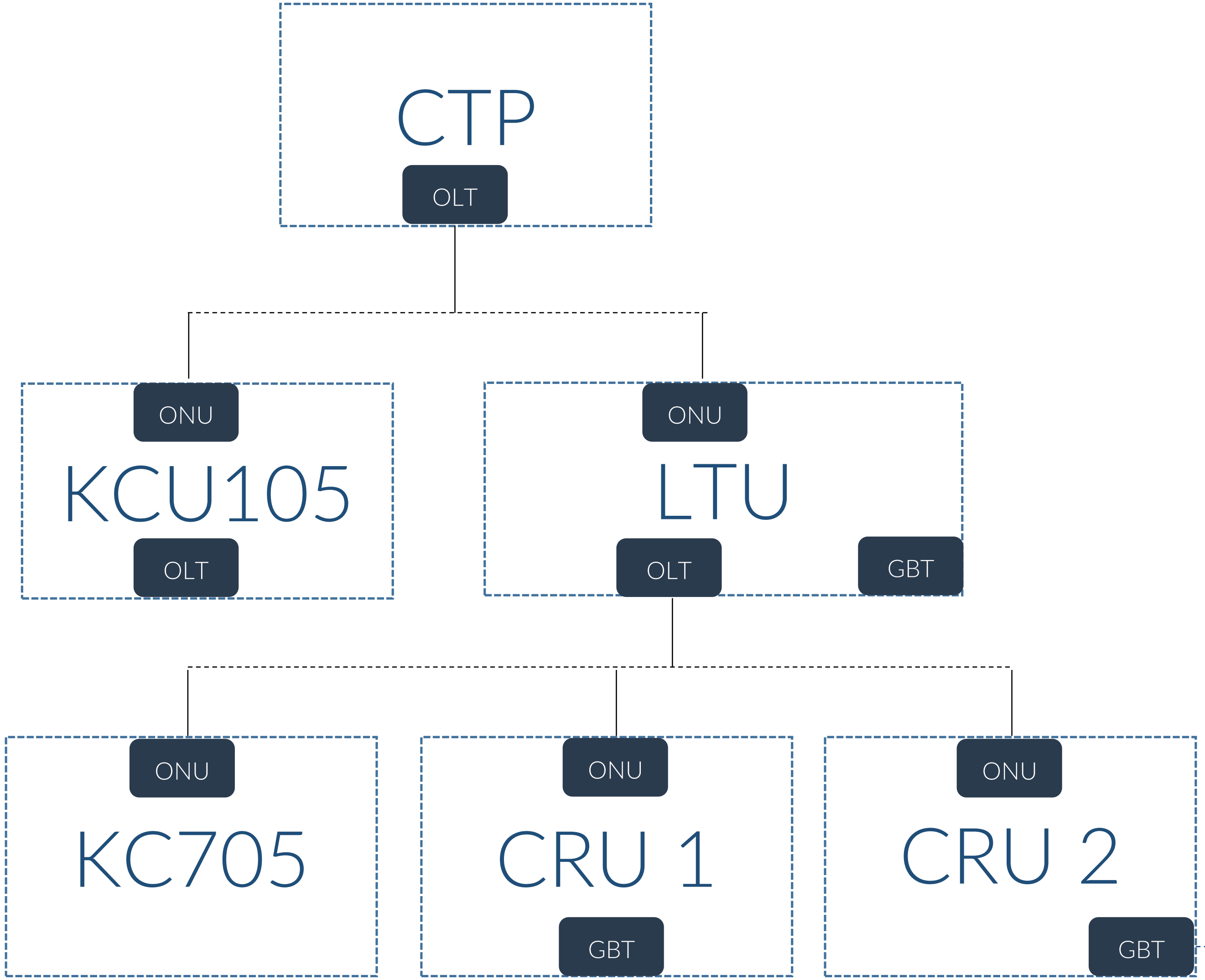
- ☑ Full Calibration.
- ☑ Light Calibration.
- ☑ Network Init.
- ☑ Network Health.
- ☑ Network Presence.
- ☑ BERT Config. (Down/Up)
- ☑ BERT Read. (Down/Up)
- ☑ Downstream Latency
- ☑ Status ONU
- ☑ Status OLT
- ☑ Toggling (TX & RX)
- ☑ OLT Reset loop

ONU_Ref_clock via IPbus (IPbus to I2C)

```
>dev si5345

si5345 loadpll [fn]     -init Si534x + read LOS/LOL bits
    checkpll [fn]     -read+compare with expected values
                       fn -data file to be loaded from file ~/WORK/fn
    losl              -check Loss of Signal/Lock bits
    phases            -read+show 4 deviders N[0..3]_DELAY
    fphase            -find phase good of ONU
    sphase N          -set phase N (0..127)
    hwreset           -reset (i.e. falling edge 1->0 on Si5344 pin PLL_RST)
    rreg page addr
    nreg page addr    NEW WAY!
                      -page for rreg/nreg: c -> use current page!
    wreg page addr value
```

Experimental Setup



Test Procedure

1.- TTC_PON calibration

2.- Downstream Latency
CTP to LTU+GBT (Loopback)

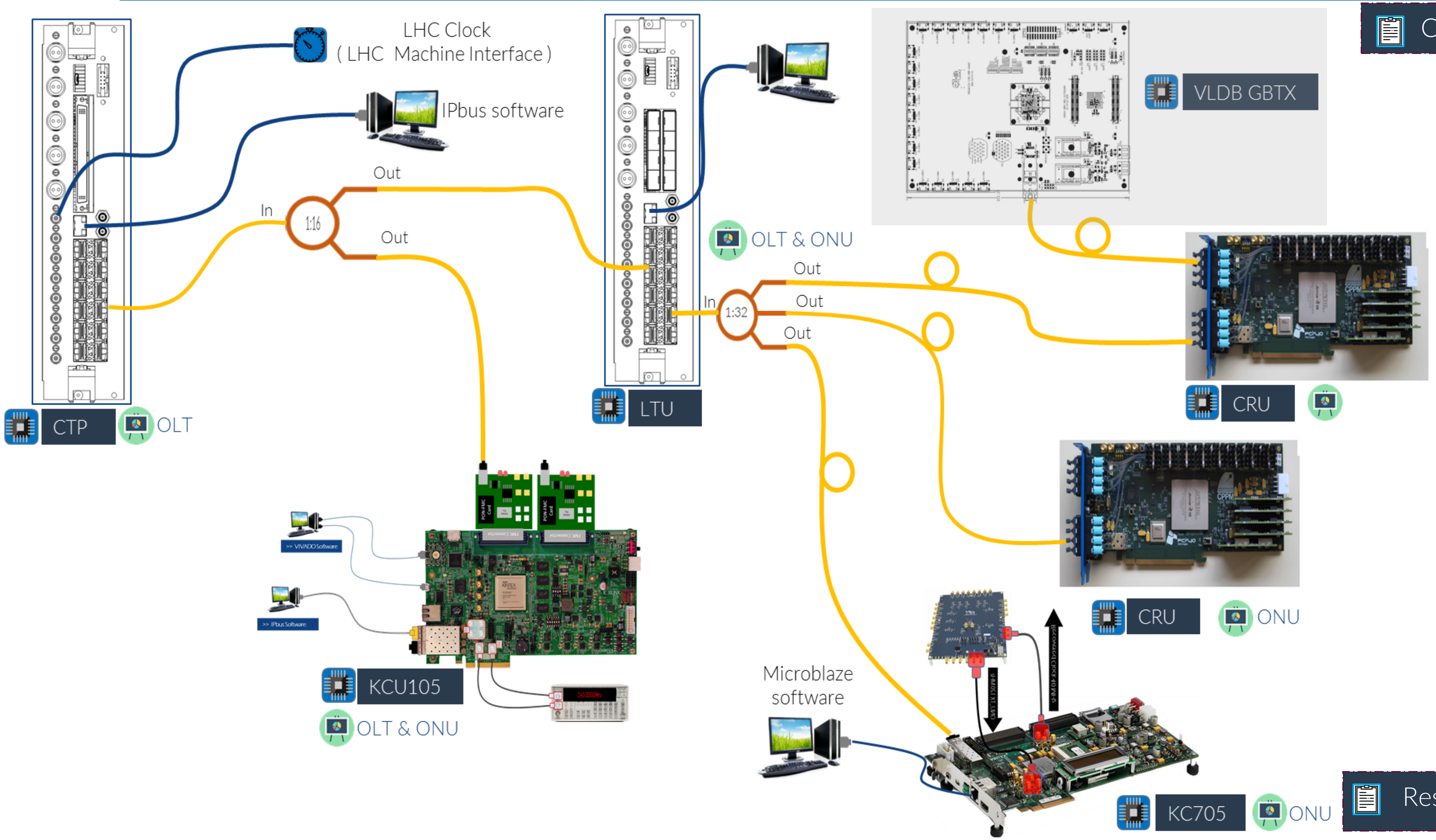
3.- TTC_PON BERT
Standalone (No LHC clock)

4.- Clock Jitter Map
CTP + LTU + CRU + VLDB

5.- Downstream Latency
CTP + LTU + CRU + VLDB

6.- BERT (Full chain in ALICE)
CTP + LTU + CRU + VLDB

Experimental Setup (Calibration process)



Calibration Process (LTU to 2 CRUs and 1 KC705)

```
- ttc_pon - INFO: OLT trying to detect ONU ADDR 1...
- ttc_pon - INFO: ONU 1 detected in trial number 1
- ttc_pon - INFO: OLT trying to detect ONU ADDR 3...
- ttc_pon - INFO: ONU 3 detected in trial number 1
- ttc_pon - INFO: OLT trying to detect ONU ADDR 4...
- ttc_pon - INFO: ONU 4 detected in trial number 1
- ttc_pon - INFO: Started SFP RX reset positioning ...
- ttc_pon - INFO: Ideal position found at:25
- ttc_pon - INFO: Started SFP enable delay positioning for ONU 1
- ttc_pon - INFO: Ideal position found at:8
- ttc_pon - INFO: Started SFP enable delay positioning for ONU 3
- ttc_pon - INFO: Ideal position found at:13
- ttc_pon - INFO: Started SFP enable delay positioning for ONU 4
- ttc_pon - INFO: Ideal position found at:13
- ttc_pon - INFO: Starting Offset calculation ...
- ttc_pon - INFO: Starting PRBS analysis ...
- ttc_pon - INFO: ONU 1 - ERRORS:0 - PRBS_LOCKED:1
- ttc_pon - INFO: ONU 3 - ERRORS:0 - PRBS_LOCKED:1
- ttc_pon - INFO: ONU 4 - ERRORS:0 - PRBS_LOCKED:1
- ttc_pon - INFO: Full calibration done
- ttc_pon - INFO: Time elapsed: 0.399101018906 s
```

KC705

CRUs

Result OLT Config:

[trigger@alictpserverlab WORK]$ more proto_X_olt_config.csv

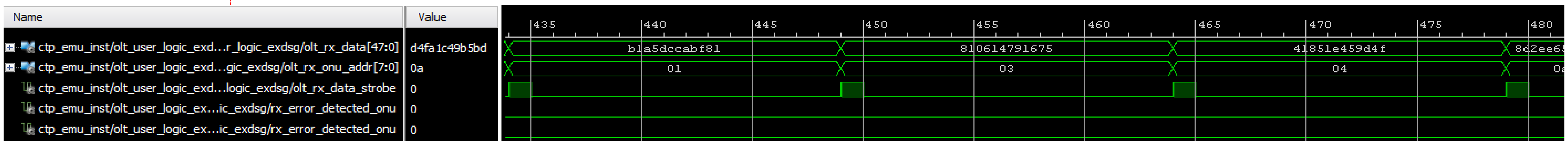
olt_reg_addr,	olt_reg_value
0,	20
1,	60
2,	2156810
3,	266
4,	2564
5,	5725
6,	10766913
7,	5700
8,	0
9,	15
10,	1
11,	0
12,	0
13,	0
14,	0
15,	0

Result ONU Config:

[trigger@alictpserverlab WORK]$ more proto_X_onu_config.csv

onu_addr,	detected,	nb_onu_system,	coarse_roundtrip,	fine_roundtrip,	coarse_offset,	fine_offset,	sfp_en_delay,	prbs7_errors,	prbs7_locked
1,	1,	4,	48,	44,	0,	0,	8,	0,	1
3,	1,	4,	60,	36,	6,	2,	13,	0,	1
4,	1,	4,	60,	36,	36,	2,	13,	0,	1

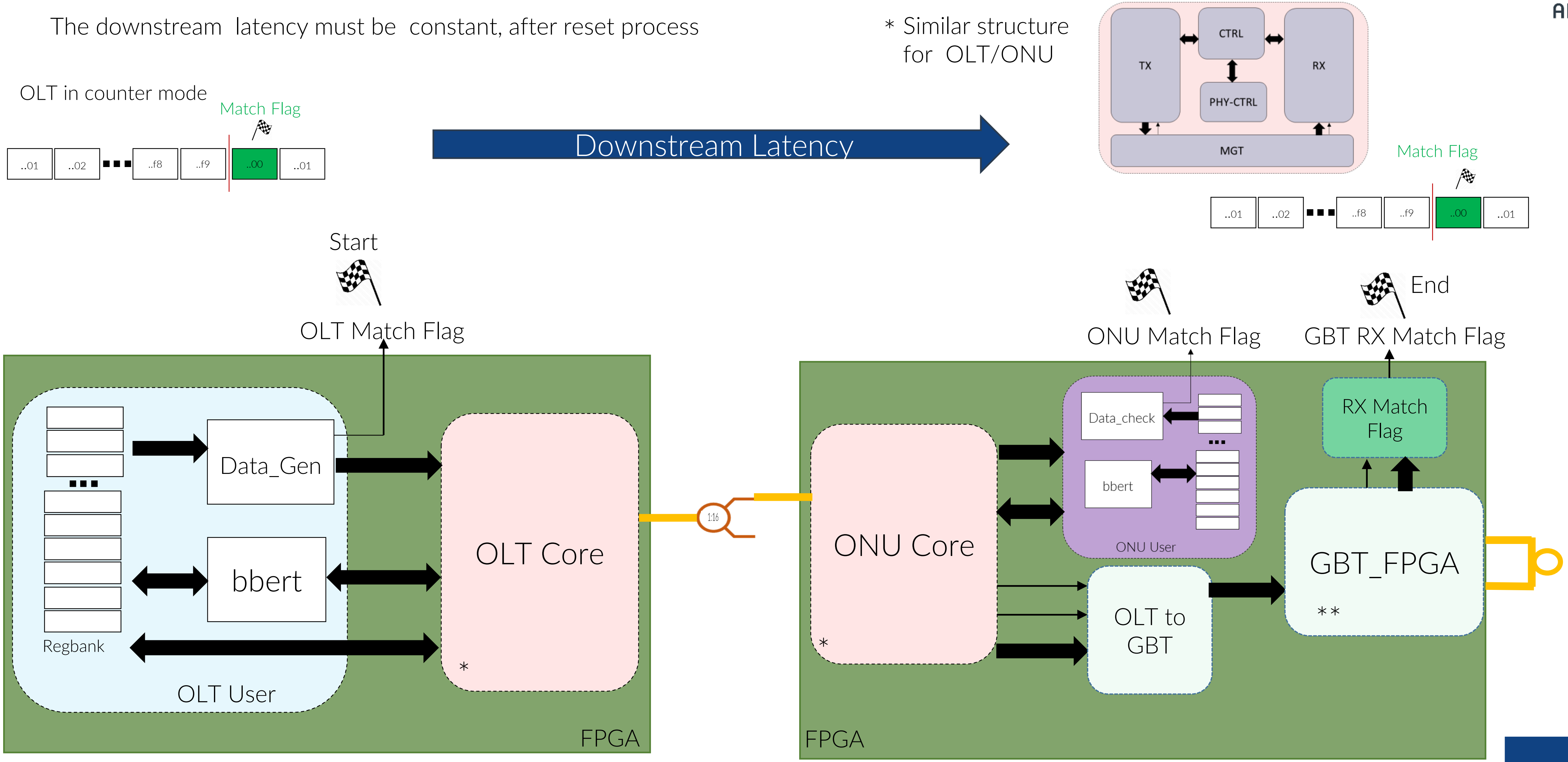
LTU(OLT_RX)(ILA) After calibration.



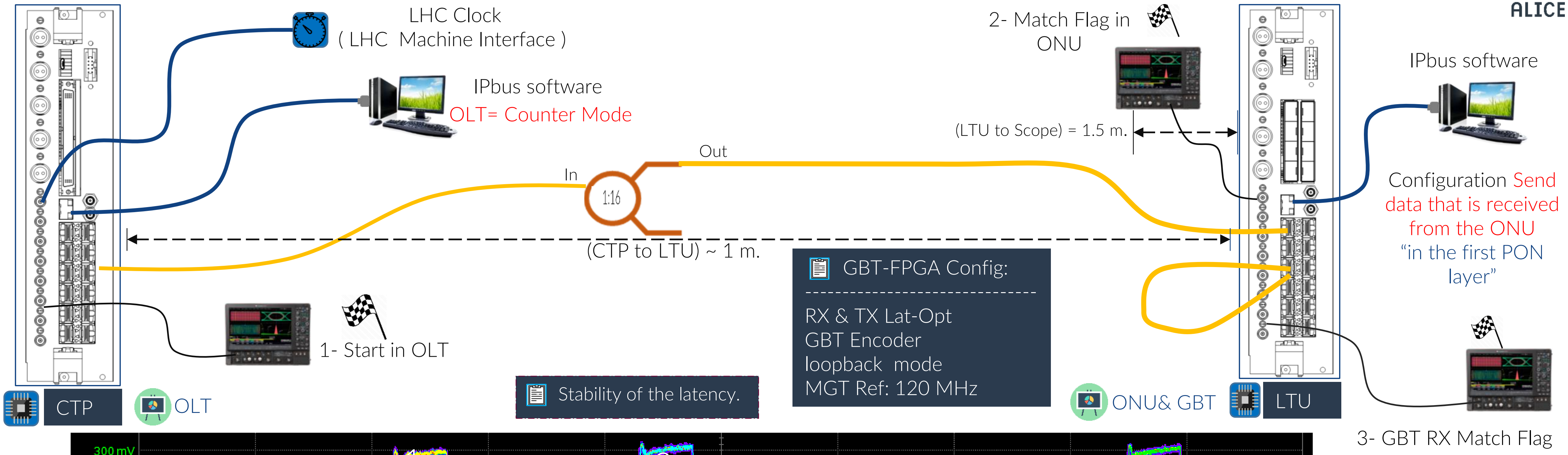
GBT Downstream

The downstream latency must be constant, after reset process

* Similar structure for OLT/ONU



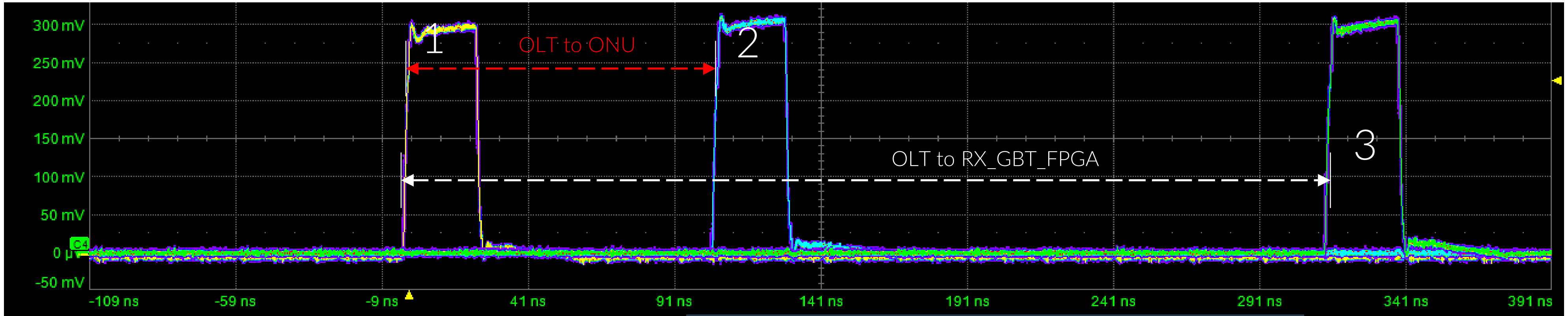
Experimental Setup (GBT Downstream Latency after several resets)



GBT-FPGA Config:

RX & TX Lat-Opt
GBT Encoder
loopback mode
MGT Ref: 120 MHz

Stability of the latency.



Measure	P1:ddelay(C1...	P2:ddelay(C1...	P3:ddelay(C3...	P4:---	P11:---	P12:---
value	105.6532 ns	315.2006 ns	209.5475 ns			
mean	105.64855 ns	315.19806 ns	209.54951 ns			
min	105.5409 ns	315.1306 ns	209.4496 ns			
max	105.7435 ns	315.2623 ns	209.6713 ns			
sdev	35.97 ps	20.24 ps	37.18 ps			
num	1.248e+3	1.248e+3	1.248e+3			
status	✓	✓	✓			

1-2 ~ 106 ns (- 4 ns of cables) ~ 102 ns
1-3 ~ 317 ns (-10ns of cables) ~ 307 ns

Reset in CTP_OLT (~ 200 times)

Experimental Setup (LTU standalone)

A Large Ion Collider Experiment

ALICE

```
>pd_r a
ONU1 bits: 754012544 14716 errs: 0 0 errs/bits: 0.000e+00
ONU10 bits: 694566528 14717 errs: 0 0 errs/bits: 0.000e+00
```

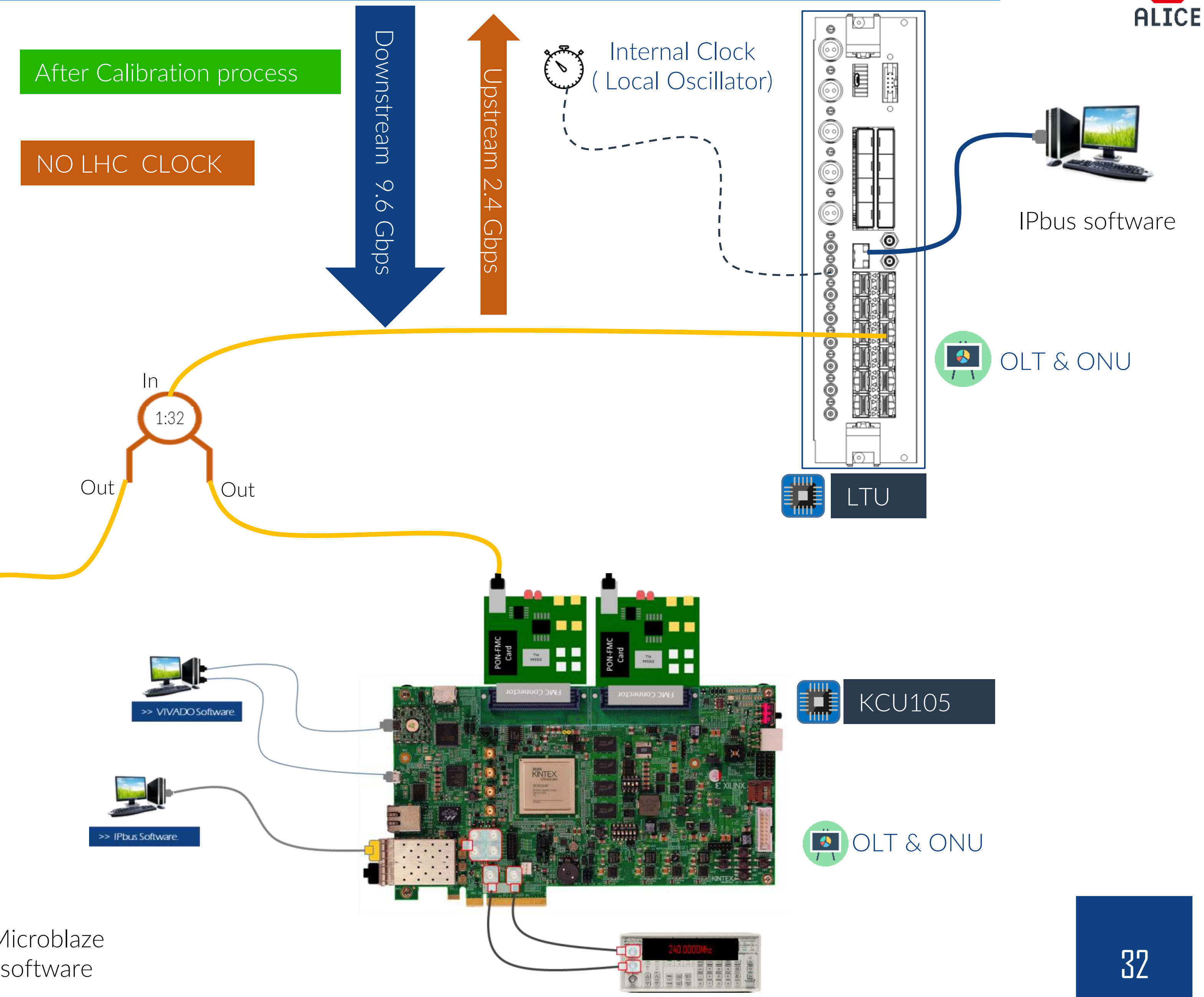
BERT Downstream (LTU to 2 ONUs). No Errors

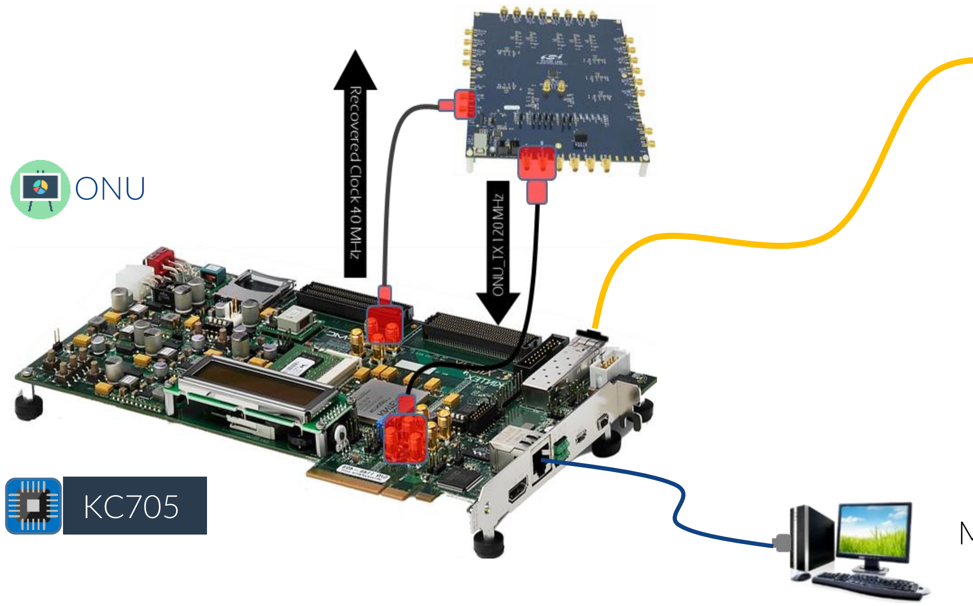
```
>pu_r
reading upstream BBERT for ONU10
ONU10 bits: 256780752 435 errs: 0 0 errs/bits: 0.000e+00
```

BERT Upstream (ONUs to LTU). No Errors

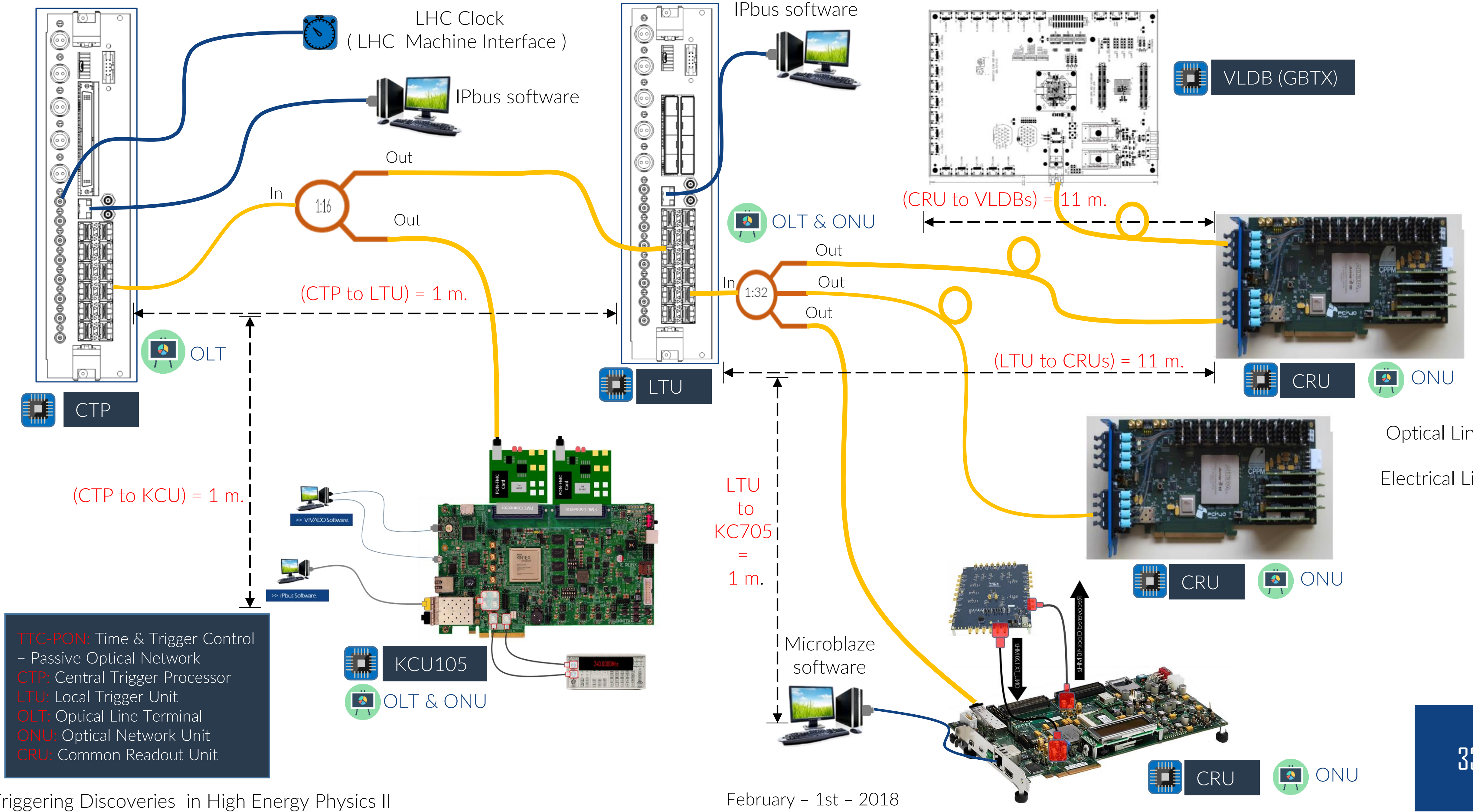
BER_Downstream ~ 10^{-14}

BER_Upstream ~ 10^{-13}



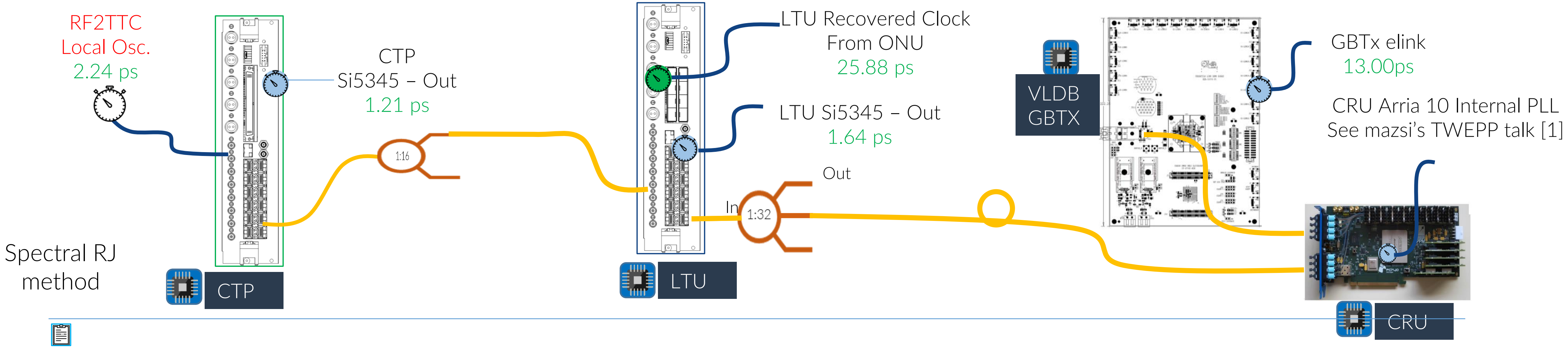


Experimental Setup (CTP-CRU)



TTC-PON: Time & Trigger Control – Passive Optical Network
CTP: Central Trigger Processor
LTU: Local Trigger Unit
OLT: Optical Line Terminal
ONU: Optical Network Unit
CRU: Common Readout Unit

The CTP + CRU distribute the LHC clock to all detectors and requirements are very strict.



Clock quality mainly depends on last PLL in a chain but other PLLs can contributes with noise:

	Tj (BER-12)	Rj	Dj	Pj
RF2TTC local osc.	149.42 ps	2.24 ps	117.54 ps	72.04 ps
CTP Si5345 out	62.14 ps	1.21 ps	44.94 ps	21.88 ps
LTU recovered clk from ONU	438.36 ps	25.88 ps	69.23 ps	137.44 ps
LTU Si5345 out	42.10 ps	1.64 ps	18.78 ps	19.75 ps
CRU Aria10 internal PLL				
GBTx elink0	298.95 ps	13.00 ps	113.53 ps	101.91 ps

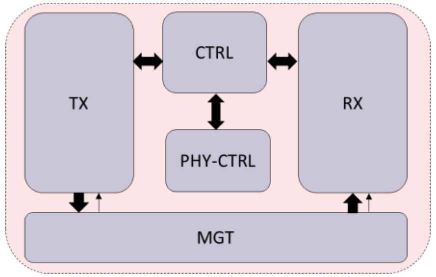
[1] https://indico.cern.ch/event/608587/contributions/2614130/attachments/1522045/2378235/20170912-twepp2017-alice-cruclk-v8.pdf
[2] https://indico.cern.ch/event/646273/contributions/2624915/attachments/1491002/2317610/CTPLTU_board_tests_PRR11072017.pdf

TTC_PON Downstream

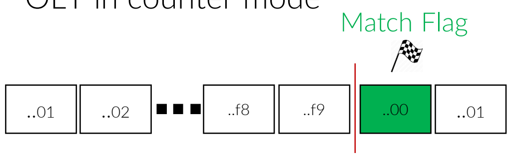
ALICE

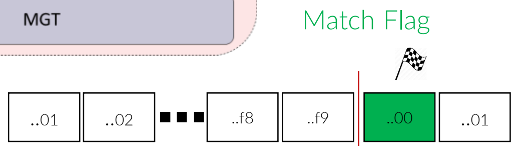
The downstream latency must be constant, after reset process

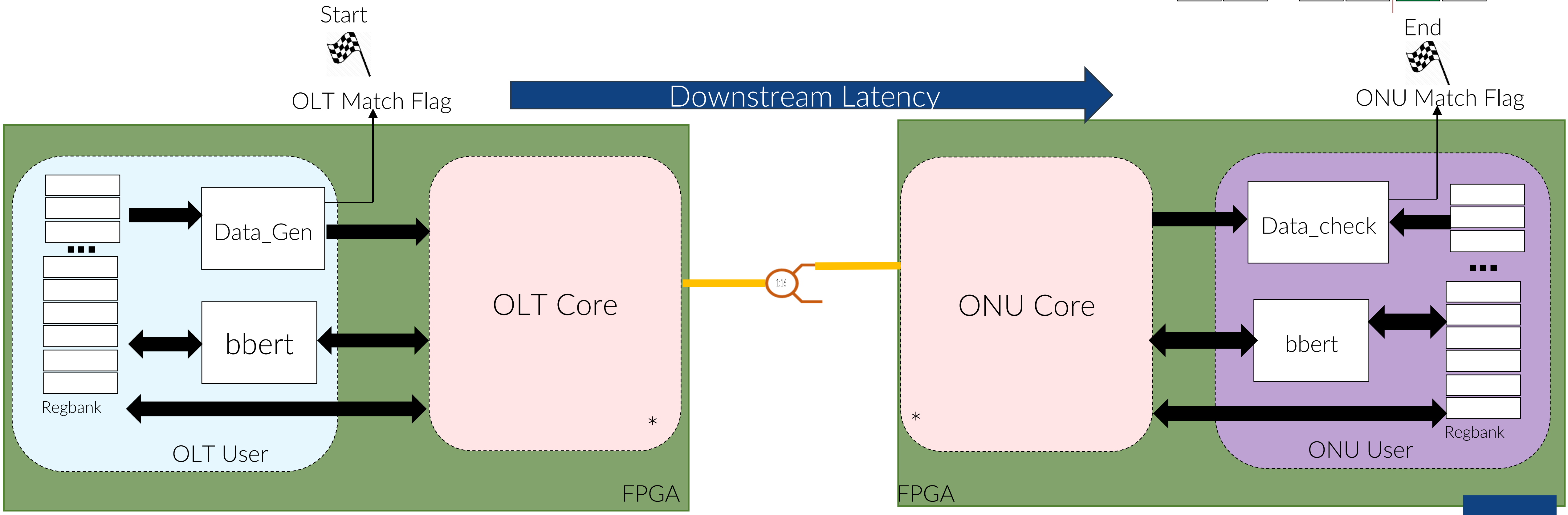
* Similar structure for OLT/ONU



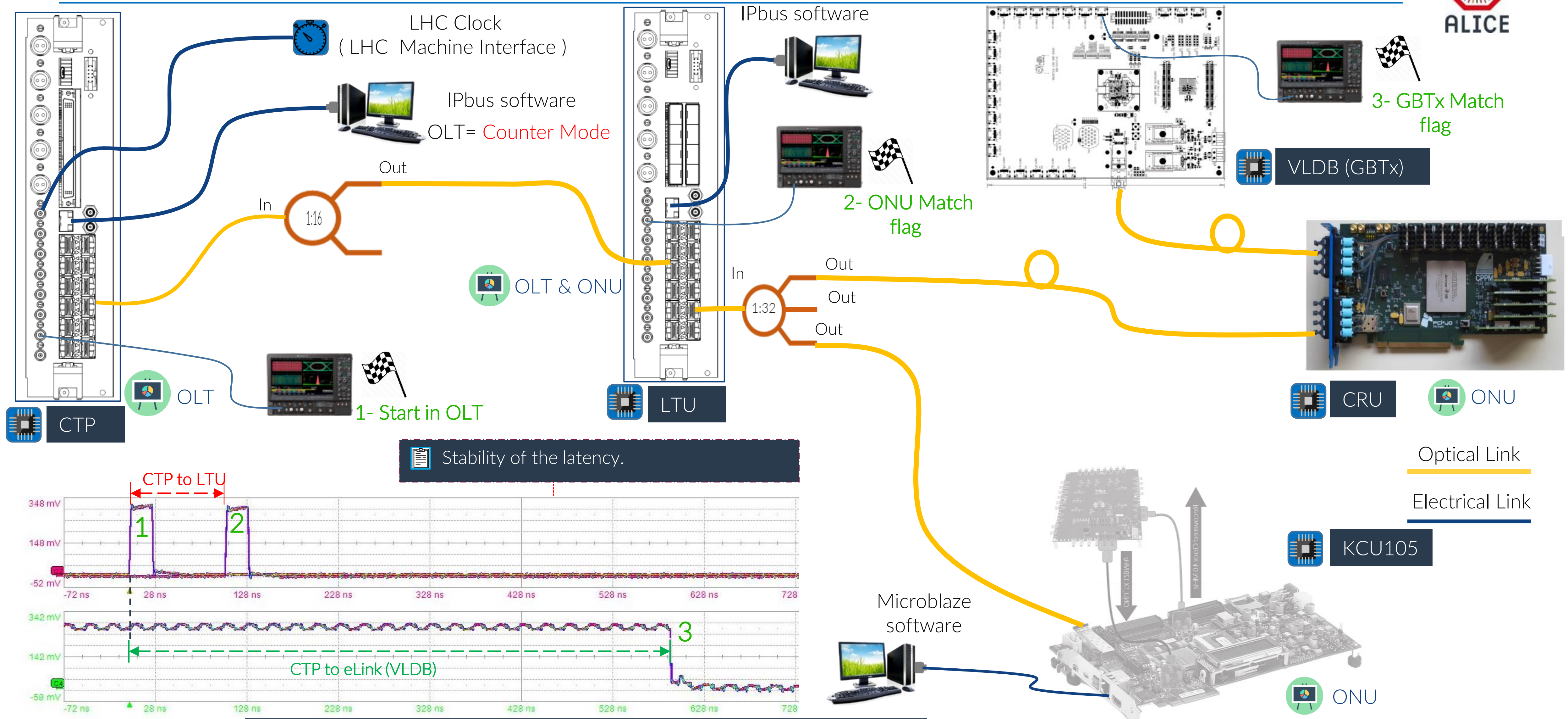
OLT in counter mode







Experimental Setup (Consistency of Downstream Latency)



Measure	P1:ddelay(C1...	P2:dt@lv(C1,...
value	104.9253 ns	590.9007 ns
mean	104.88820 ns	590.88456 ns
min	104.7619 ns	590.7905 ns
max	105.0308 ns	590.9988 ns
sdev	46.28 ps	30.98 ps
num	5.706e+3	5.706e+3
status	✓	✓

1-2 ~ 105 ns (- 3 ns of cables) ~ 102 ns

1-3 ~ 590 ns (-120 ns of cables – CTP to LTU) ~ 365 ns (CRU + VLDB)

After several resets in CTP_OLT, LTU_OLT

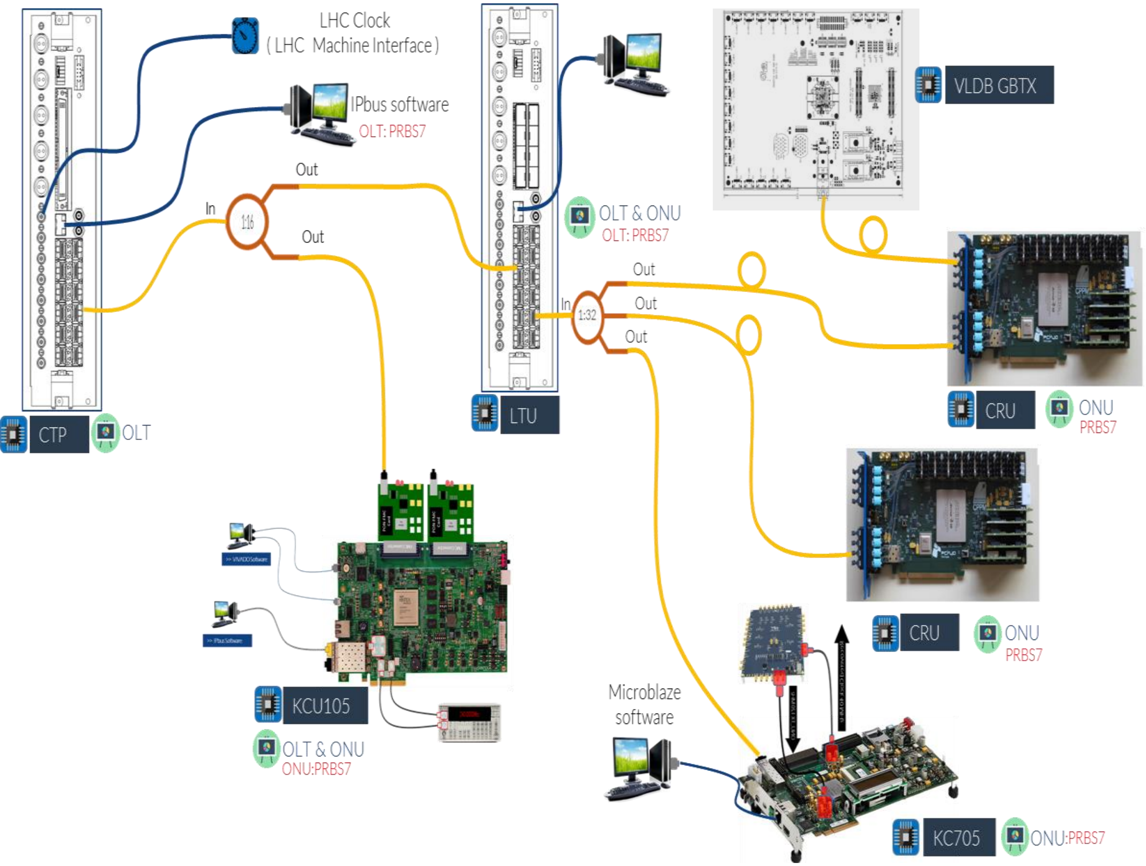
Experimental Setup (Bit Error Rate Test Results)

CTP

Upstream 2.4 Gbps

Downstream 9.6 Gbps

LTU & KCU



LTU

Downstream 9.6 Gbps

Upstream 2.4 Gbps

CRUs

BERT Upstream (CRUs to LTU). No Errors >22 hrs

CRU1

```
>pu_r
reading upstream BBERT for ONU3
ONU3 bits: 1058966656 2564 errs: 0 0 errs/bits: 0.000e+00
>
```

CRU2

```
>pu_r
reading upstream BBERT for ONU4
ONU4 bits: 3927776048 2656 errs: 0 0 errs/bits: 0.000e+00
```

BER_Downstream ~ 10^{-15}

BER_Upstream ~ 10^{-14}

BERT Downstream (LTU & 2CRUs). No Errors > 22hrs

CRU1

0x022a0010	0xf32bd060	4079734880
0x022a0014	0x0000e6eb	59115
0x022a0018	0x00000000	0
0x022a001c	0x00000000	0

CRU2

0x022a0010	0x9bbb9d60	2612764000
0x022a0014	0x0000ef78	61304
0x022a0018	0x00000000	0
0x022a001c	0x00000000	0

Summary

- Prototype CTP/LTU **boards produced and tested successfully**
- We tested the TTC-PON system on the CTP/LTU board.
  - First version of the LTU firmware well advanced (DDR4, ICAP, Emulator, TTC-PON, GBT,IPbus)
- The consistency of the downstream latency between CTP-LTU-CRU-VLDB tested.
  - Downstream Latency CTP-LTU ~ 102 ns
  - Downstream Latency CTP-LTU-GBT(loopback) ~ 307 ns
  - Downstream Latency of the full chain ~ 590 ns
- BER between LTU-CRU tested.
  - BER downstream ~ 10^{-15}
  - BER upstream ~ 10^{-14}
- Measured of the clock jitter for ALICE-TTC PON system

Thank you !!

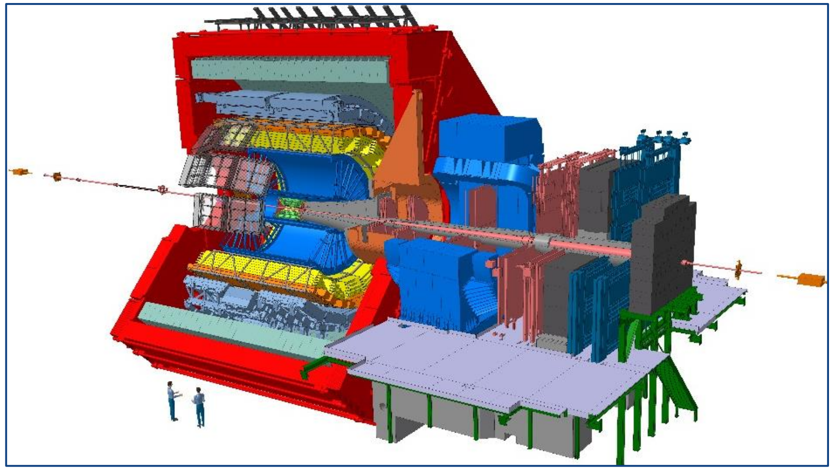
ALICE Central Tigger Processor (Upgrade)

Backup!!

ALICE Central Tigger Processor (Upgrade)

Backup!!

Introduction (ALICE Upgrade)

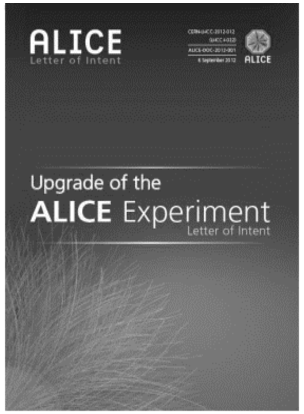


U P G R A D E

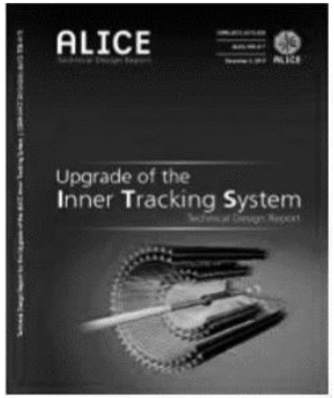
Physics goals for ALICE upgrade ...

High Precision measurements :
- HF mesons and baryons
- Charmonium states
- Di-leptons from QGP radiation and low-mass vector messons

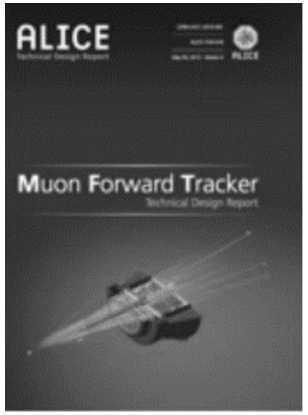
Low p_T
High precision
Central and
forward



CERN-LHCC-2012-012



CERN-LHCC-2013-024



CERN-LHCC-2015-021

Upgrade Strategy

-- Improve tracking resolution at low p_T.
-- thinner more resolution.
-- Large statistics (new strategy and trigger system) with high interaction rate.
-- Increase readout rate.
-- Reduce data size
-- Preserve PID capabilities at high rate
-- Speed-up readout of PID detectors

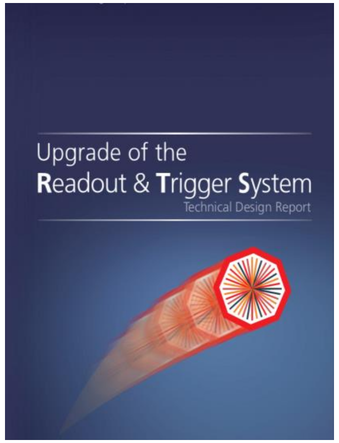
ALICE after LS2

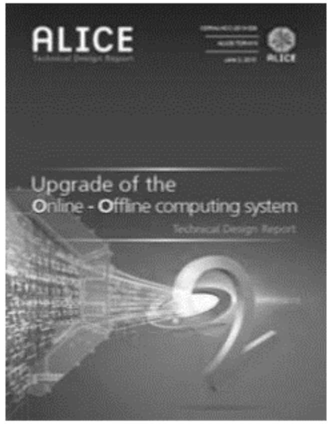
-- Pb-Pb recorded luminosity: ≥ 10 nb^{-1} → 8×10^{10} events.

-- pp(@ 5.5 Tev) recorded luminosity ≥ $6pb^{-1}$ → 1.4×10^{11} events

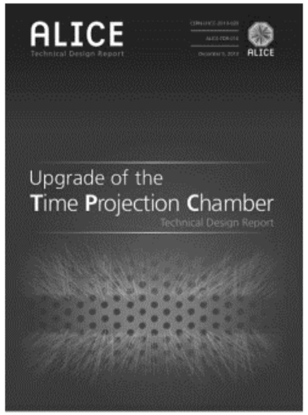
-- Triggered physics: gain factor 10

-- Minimum bias physics: gain a factor 100





CERN-LHCC-2015-006

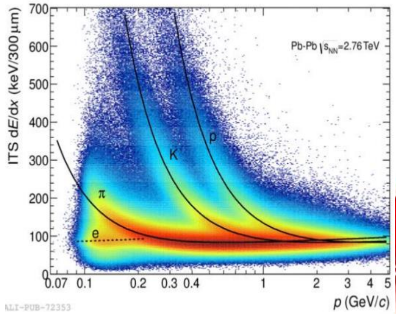


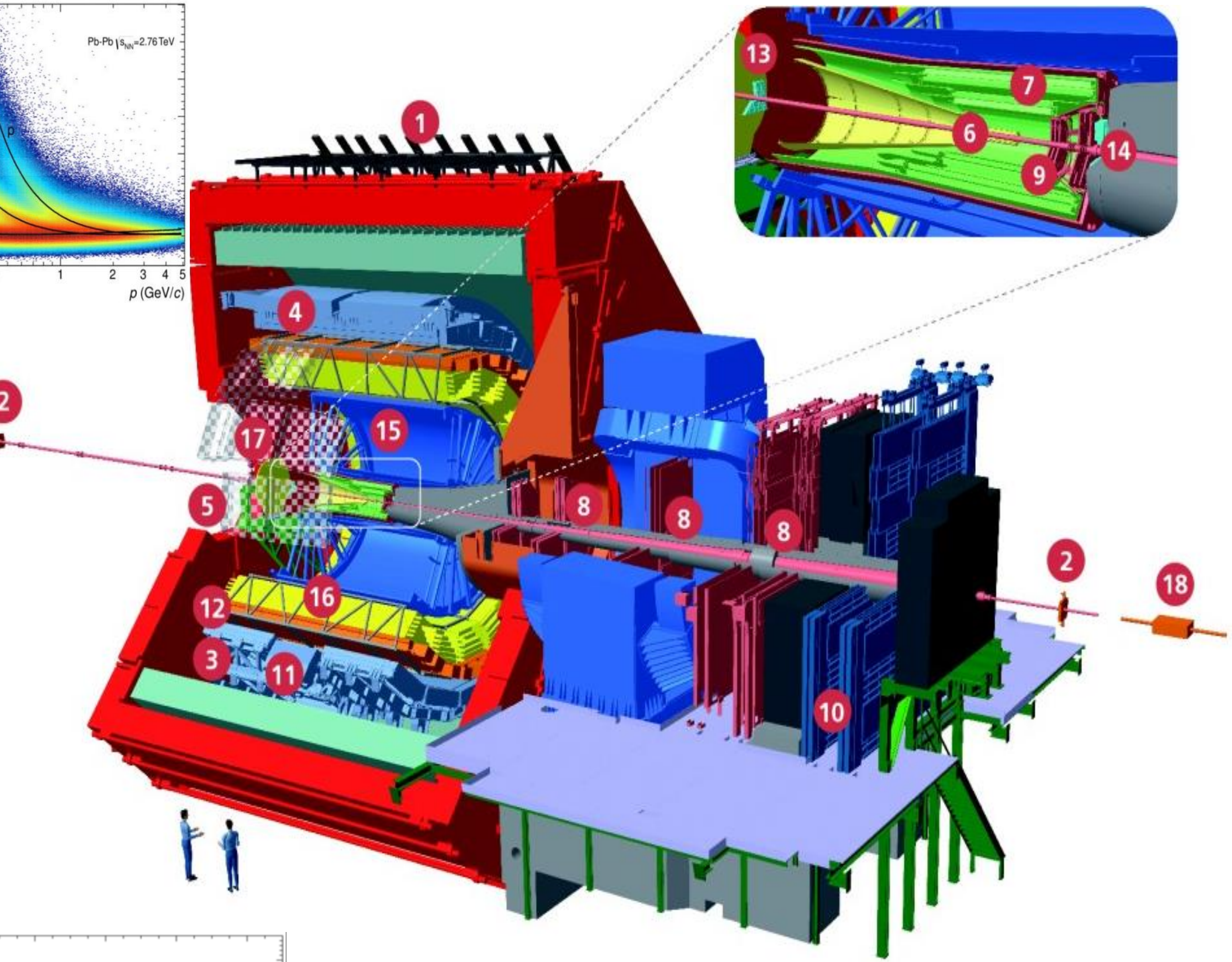
CERN-LHCC-2013-020

To Summarize:

- Write all Pb-Pb interactions at 50 kHz...

Introduction (ALICE present detector layout)





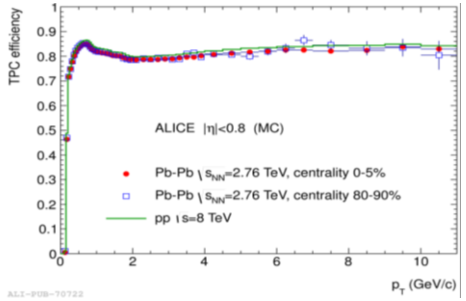
1 **ACORDE** | ALICE Cosmic Rays Detector
2 **AD** | ALICE Diffractive Detector
3 **DCal** | Di-jet Calorimeter
4 **EMCal** | Electromagnetic Calorimeter
5 **HMPID** | High Momentum Particle Identification Detector
6 **ITS-IB** | Inner Tracking System - Inner Barrel
7 **ITS-OB** | Inner Tracking System - Outer Barrel
8 **MCH** | Muon Tracking Chambers
9 **MFT** | Muon Forward Tracker
10 **MID** | Muon Identifier
11 **PHOS / CPV** | Photon Spectrometer
12 **TOF** | Time Of Flight
13 **T0+A** | Tzero + A
14 **T0+C** | Tzero + C
15 **TPC** | Time Projection Chamber
16 **TRD** | Transition Radiation Detector
17 **V0+** | Vzero + Detector
18 **ZDC** | Zero Degree Calorimeter

19 Detectors

Trigger
Tracking
PID
Calorimeters

Central Systems Tigger /DAQ

- 4 Trigger Levels (Hardware)
- 8 kHz (Pb-Pb) Collision rate
- 500 Hz (Pb-Pb) Max. Readout rate.

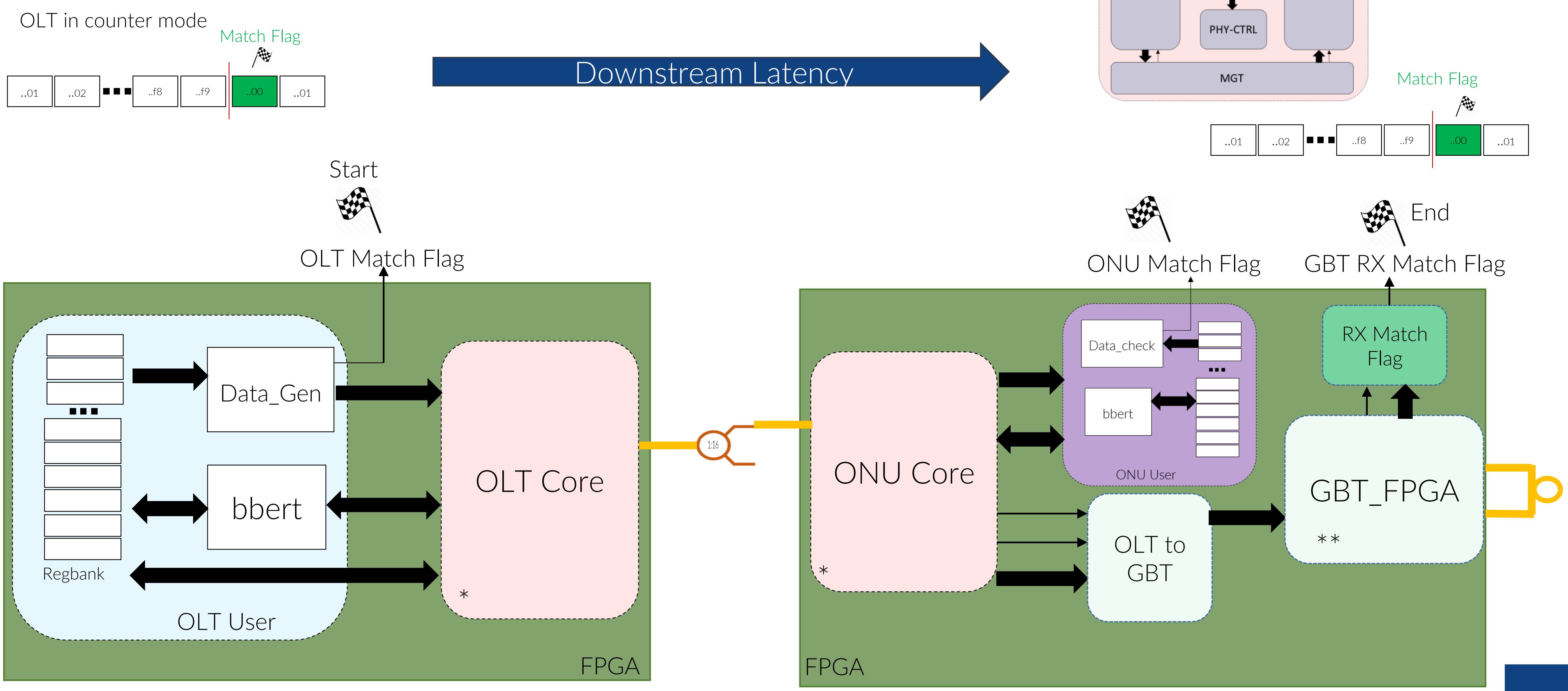


- Designed to cope with very high charged particle multiplicities
- Excellent tracking and particle identification of charged particles over wide P_T range.

GBT Downstream

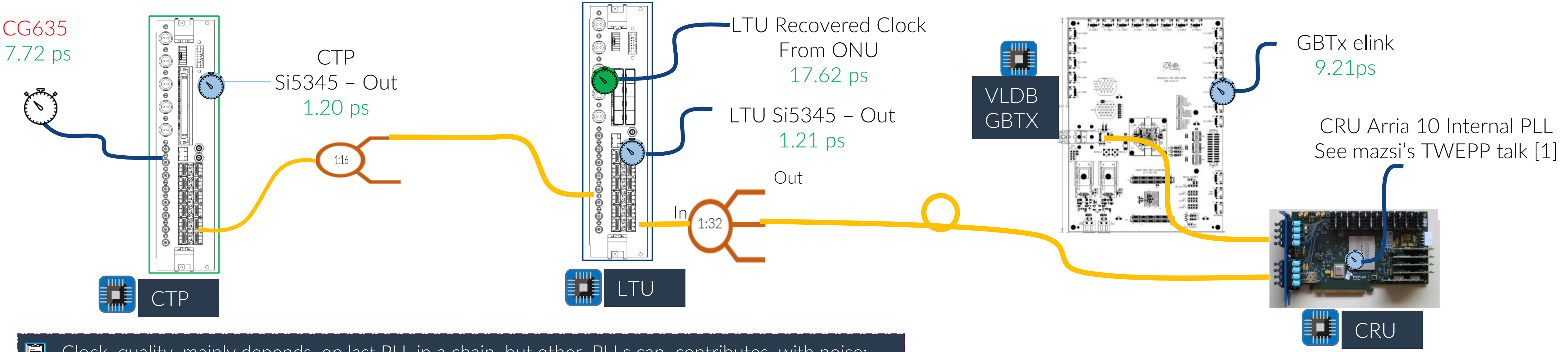
The downstream latency must be constant, after reset process

* Similar structure for OLT/ONU



Clock Jitter summary

Spectral RJ method



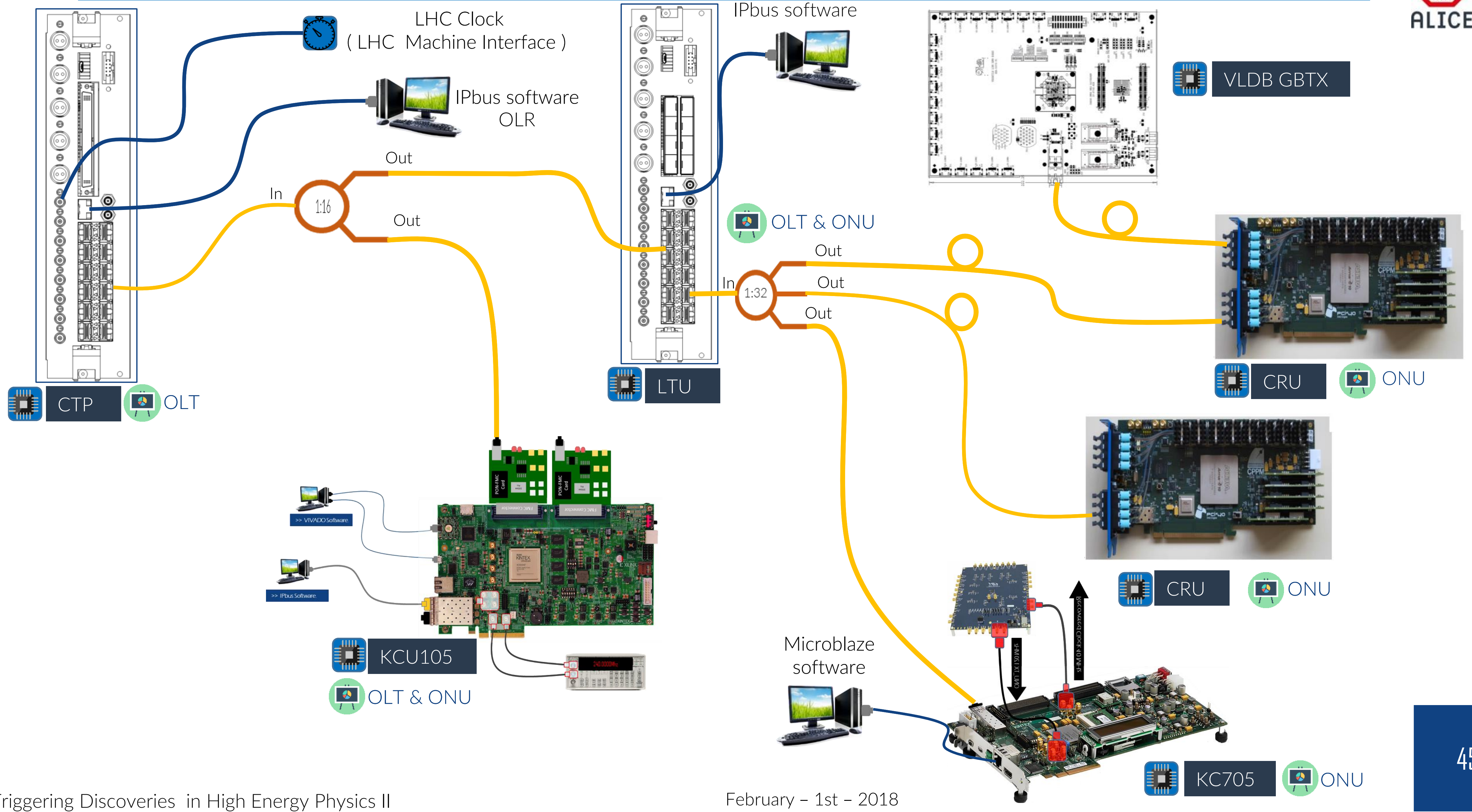
Clock quality mainly depends on last PLL in a chain but other PLLs can contributes with noise:

	Tj (BER-12)	Rj	Dj	Pj
CG635	110.02 ps	7.72 ps	91 fs	7.40 ps
CTP Si5345 out	17.21 ps	1.20 ps	163 fs	1.93 ps
LTU recovered clk from ONU	340.09 ps	17.62 ps	88.85 ps	134.52 ps
LTU Si5345 out	17.42 ps	1.21 ps	181 fs	2.54 ps
CRU Aria10 internal PLL				
GBTx elink0	144.99 ps	9.21 ps	13.67 ps	31.95 ps

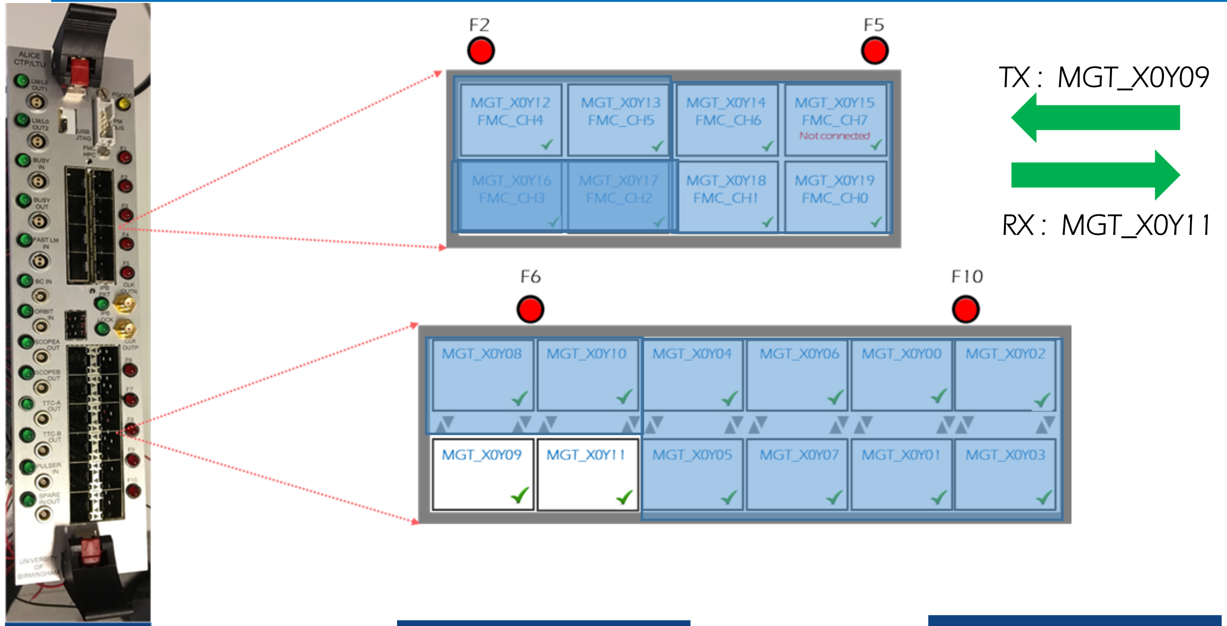
See Marian's presentation for more details [2]

[1] https://indico.cern.ch/event/608587/contributions/2614130/attachments/1522045/2378235/20170912-twepp2017-alice-cruclk-v8.pdf
[2] https://indico.cern.ch/event/646273/contributions/2624915/attachments/1491002/2317610/CTPLTU_board_tests_PRR11072017.pdf

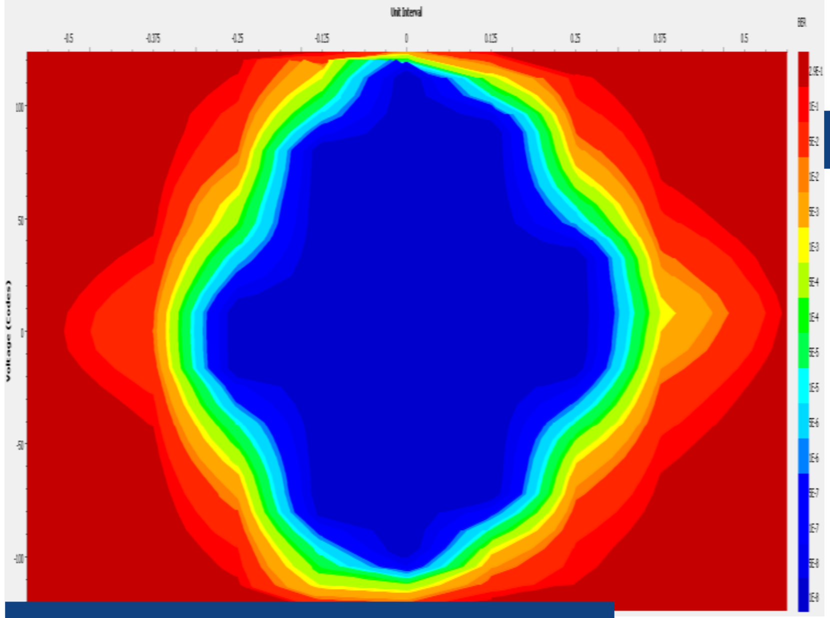
Experimental Setup (CTP-CRU)



GTH Channels (10 Gbps = 10G ethernet)

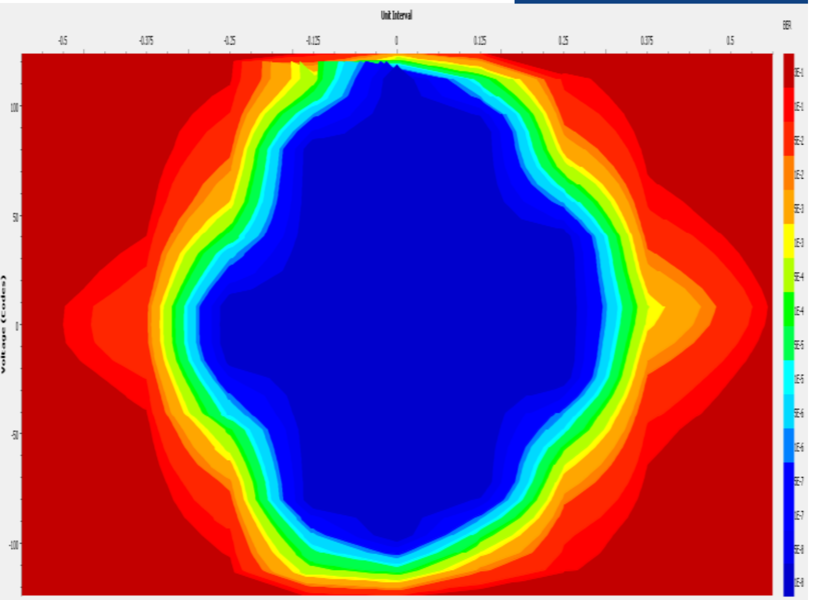


>> CTP/LTU Board



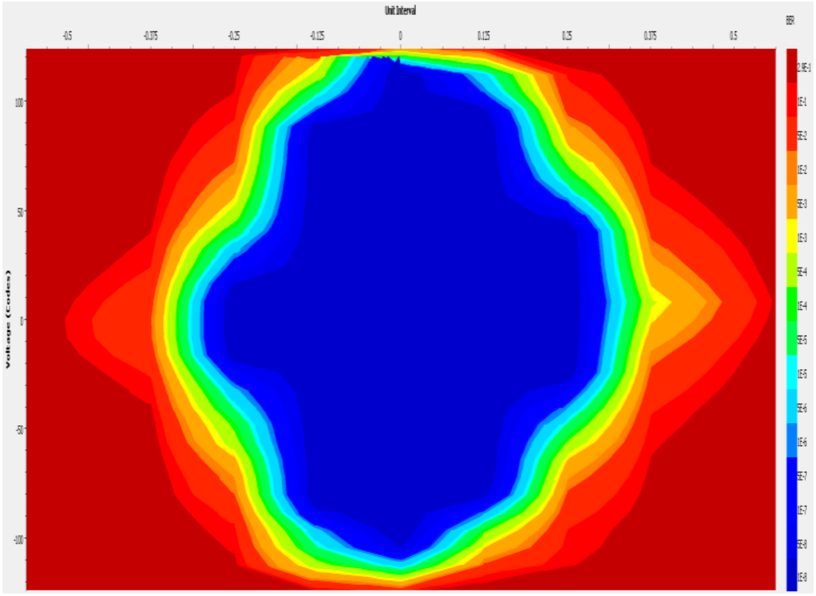
>> MGT_X0Y09 (Tx_diff_swing = 1080 mV).

>> Open Area = 4736



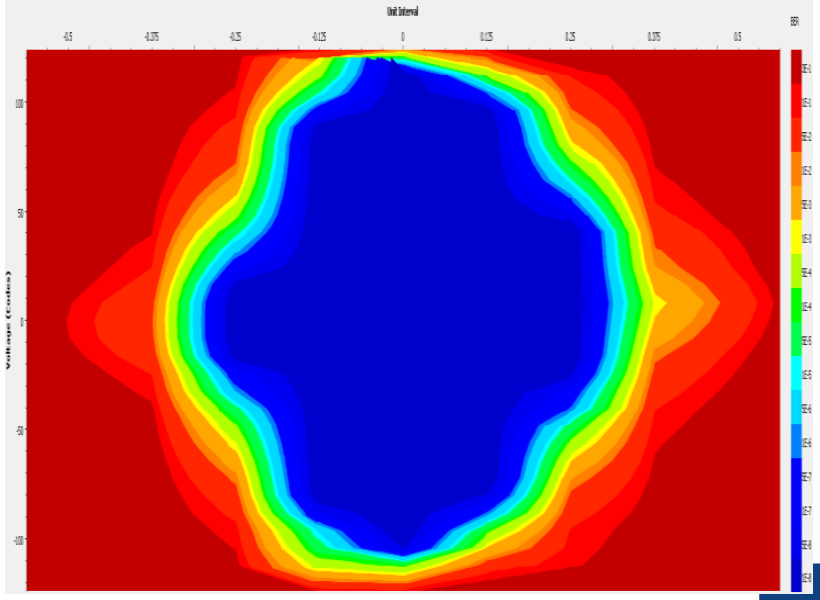
>> MGT_X0Y09 (Tx_diff_swing = 840 mV).

>> Open Area = 4928



>> MGT_X0Y09 (Tx_diff_swing = 660 mV).

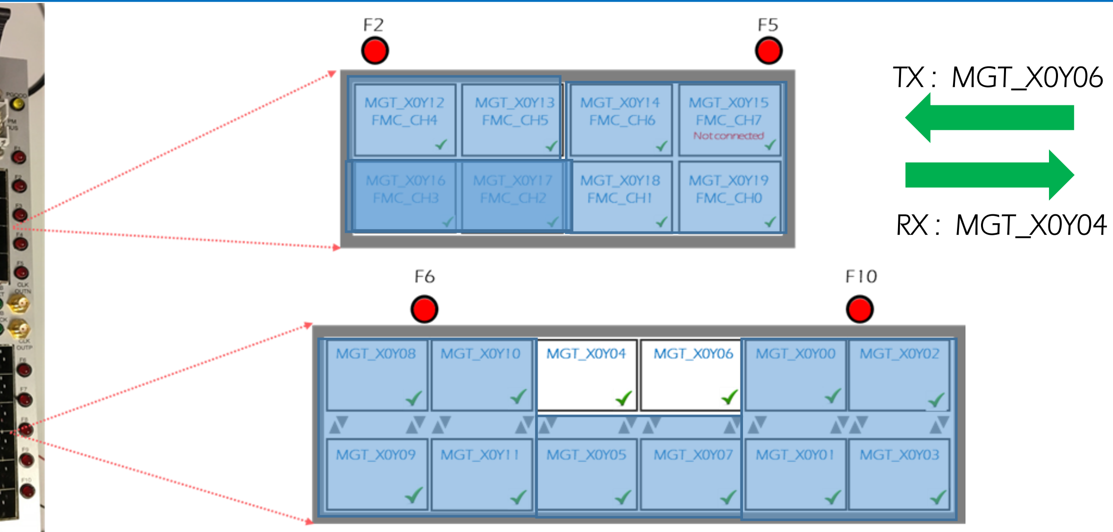
>> Open Area = 4992

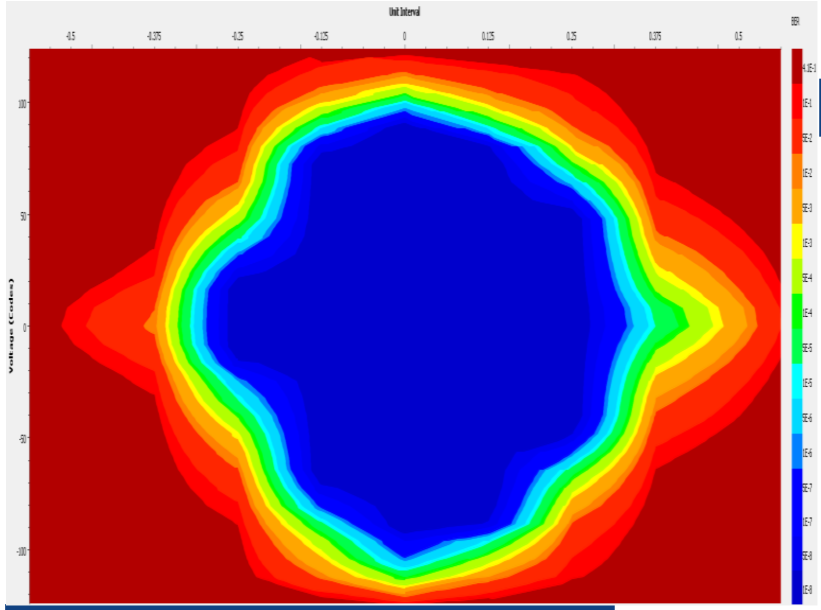


>> MGT_X0Y09 (Tx_diff_swing = 390 mV).

>> Open Area = 5056

>> CTP/LTU Board





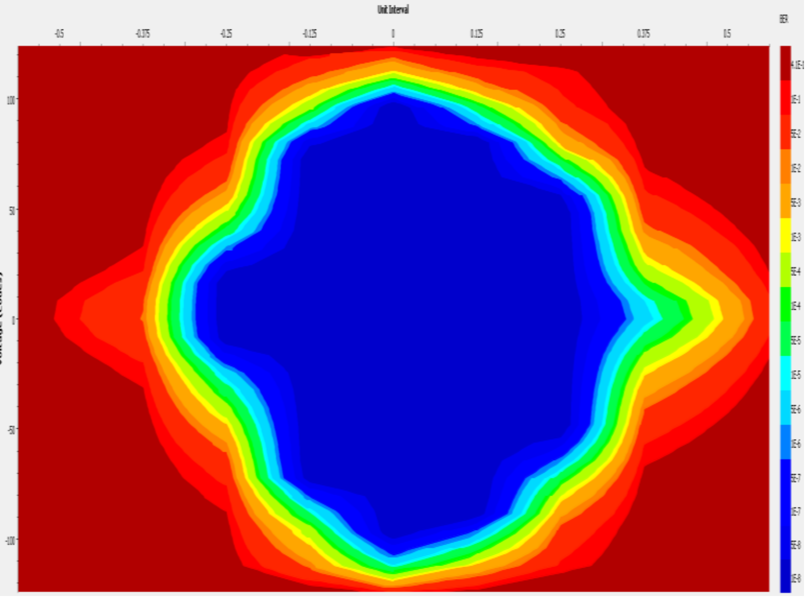
>> Open Area = 4736

>> MGT_X0Y06 (Tx_diff_swing = 1080 mV).

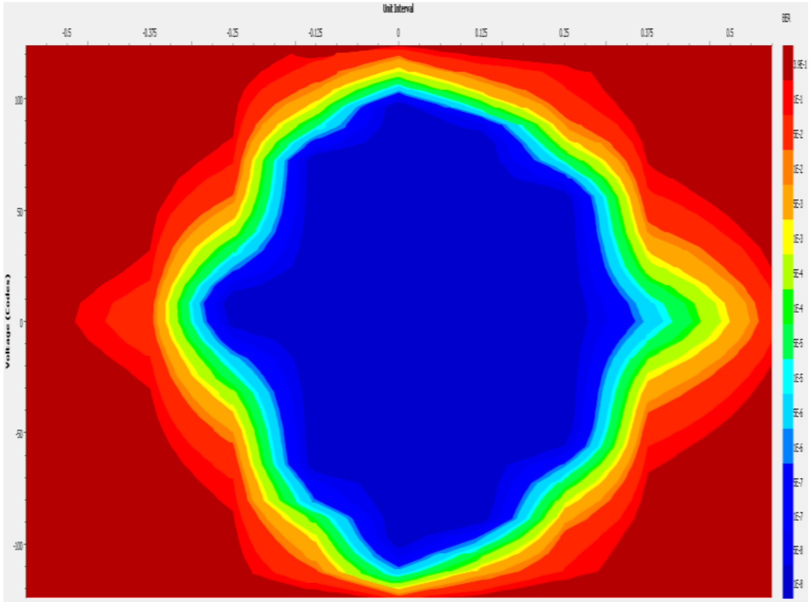
>> Open Area = 5056

>> Open Area = 4800

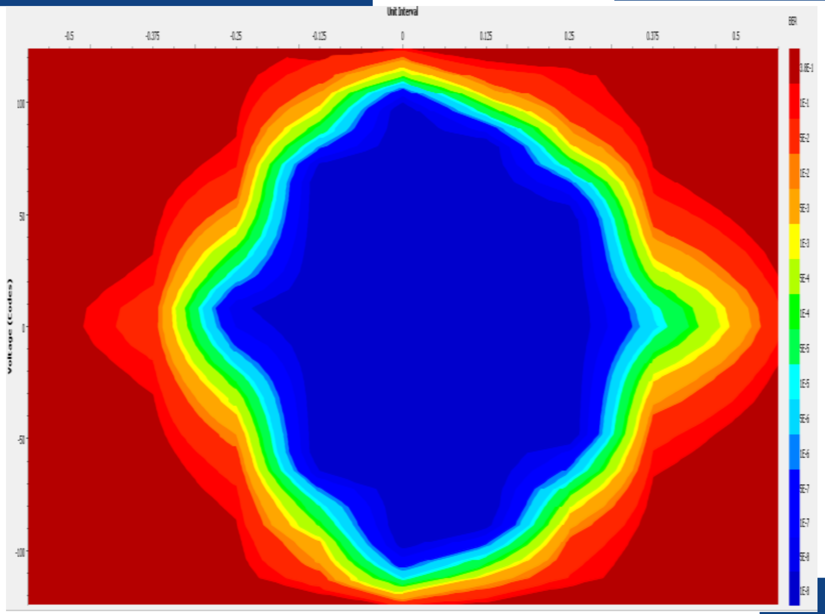
>> Open Area = 4608



>> MGT_X0Y06 (Tx_diff_swing = 840 mV).



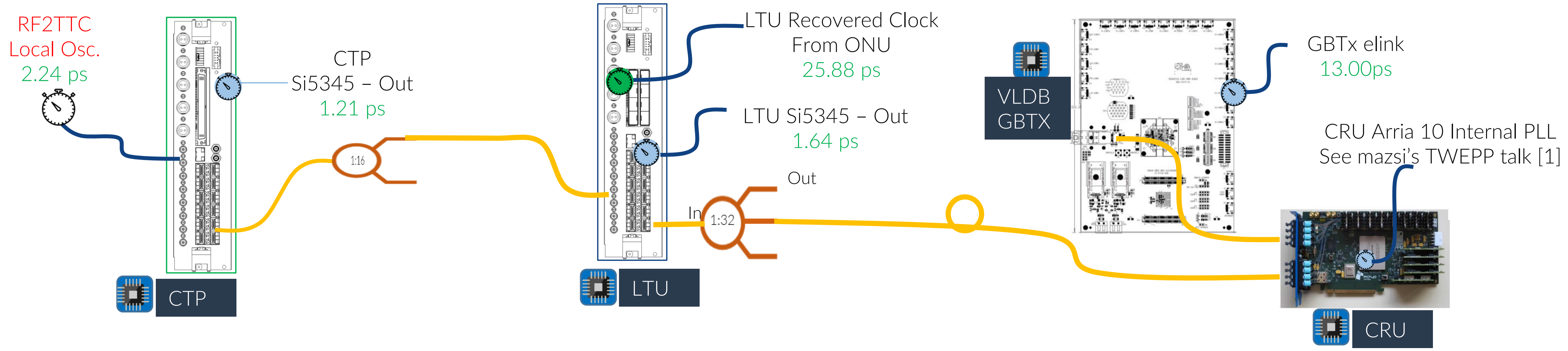
>> MGT_X0Y13 (Tx_diff_swing = 660 mV).

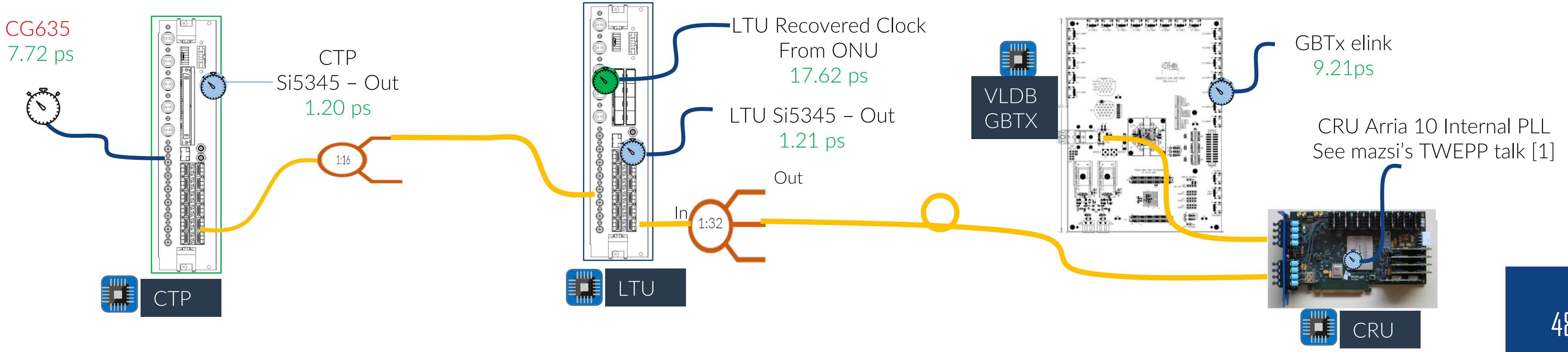


>> MGT_X0Y13 (Tx_diff_swing = 390 mV).

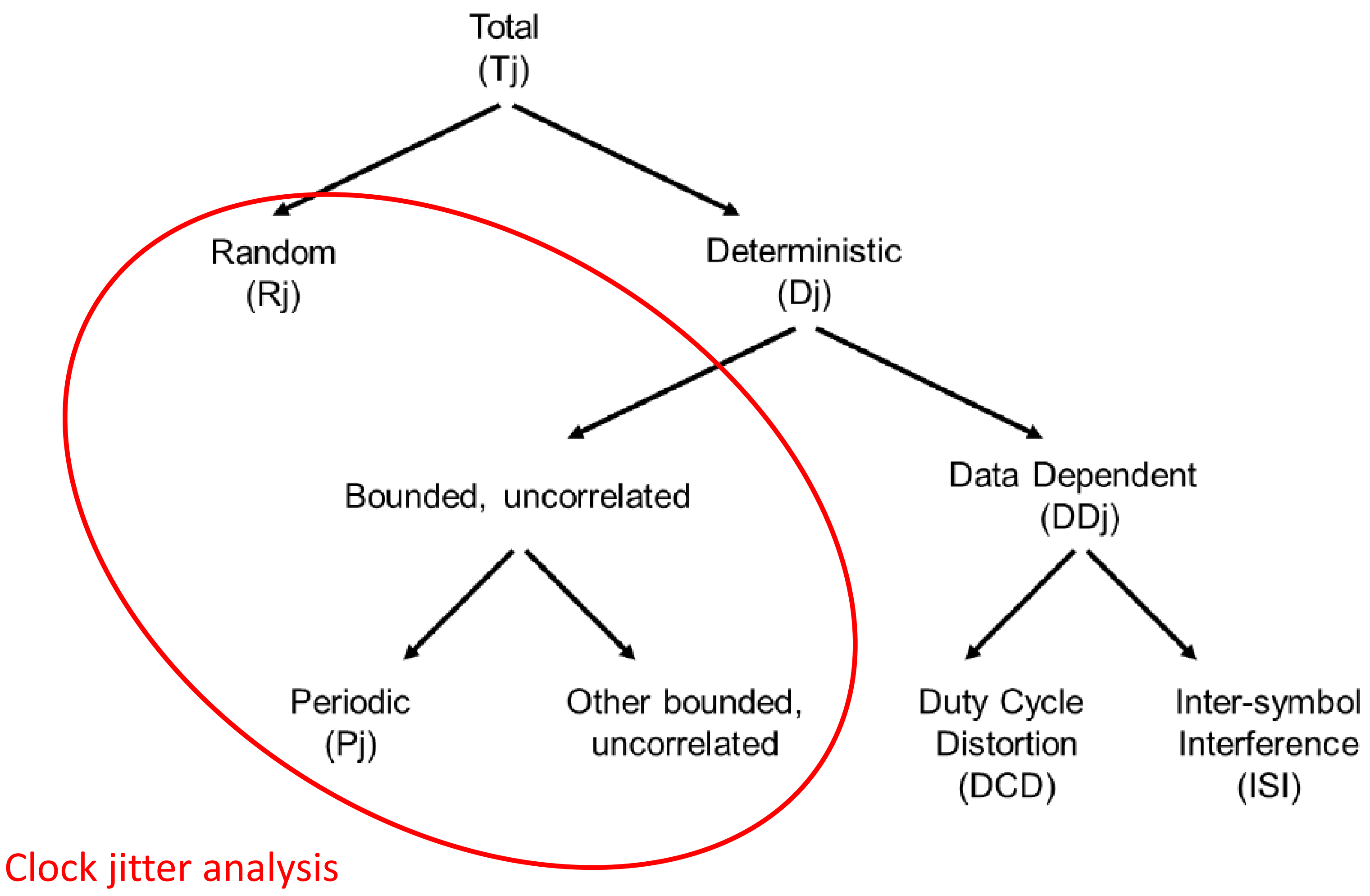
Clock Jitter summary

Spectral RJ method





Jitter categories

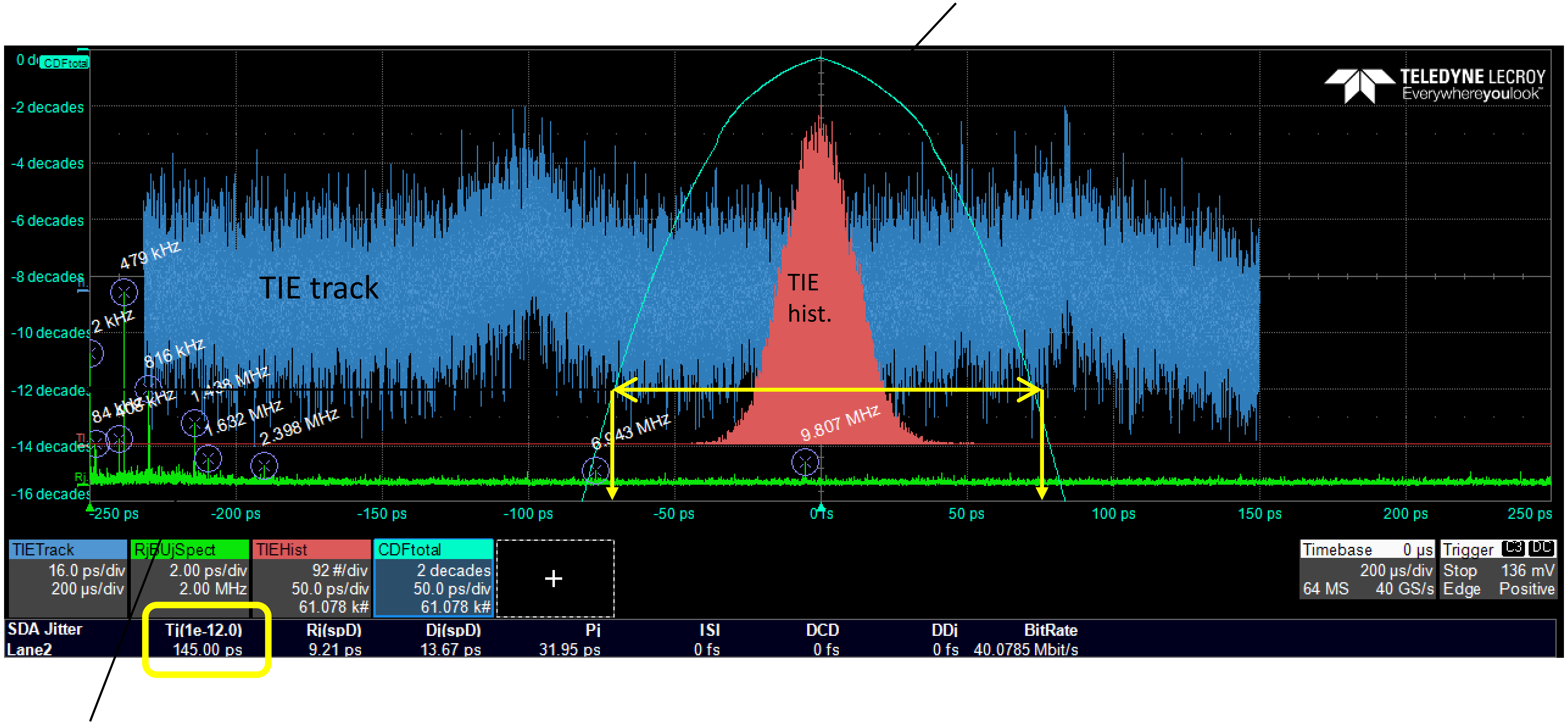


What type of jitter each component is most likely to generate

- The character of the reference clock is reproduced in the clock recovery circuit at the receiver
- The reference clock generates primarily RJ from the thermal noise of the oscillator, PJ from spurious sideband resonances of the oscillator
- The transmitter contributes to RJ from thermal effects and PJ from pickup of EMI
- The receiver generates RJ from shot noise. PJ and, another category called Bounded Uncorrelated Jitter (BUJ) can be introduced through the EMI of other circuit elements. BUJ is the repository for other types of bounded jitter. The best example of BUJ is generated by crosstalk from neighbouring signals.

- Ref…[http://www.keysight.com/upload/cmc_upload/All/Clock_Jitter_Analysis_2008.pdf?&cc=FR&lc=fre]

Explanation of BER-12 for Total Jitter (GBTx elink0)



Comparison of methods

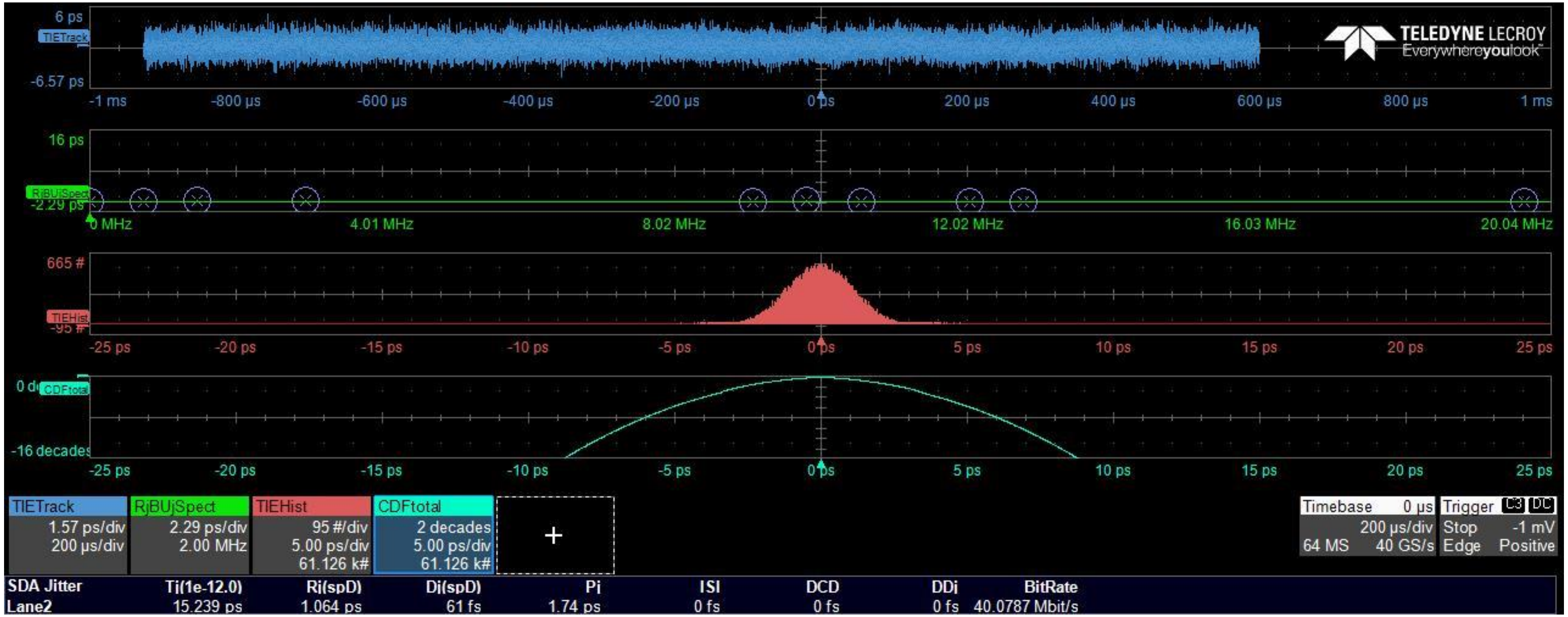
Special background may cause that spectral estimate of gauss σ fails, => Compare available methods:

- Spectral Rj method (spD)
- Spectral Rj+Dj CDF fit (sp)
- NQ-scale method (nonspectral) (NQM)

❑Example of measurement on LTU Si5345 out

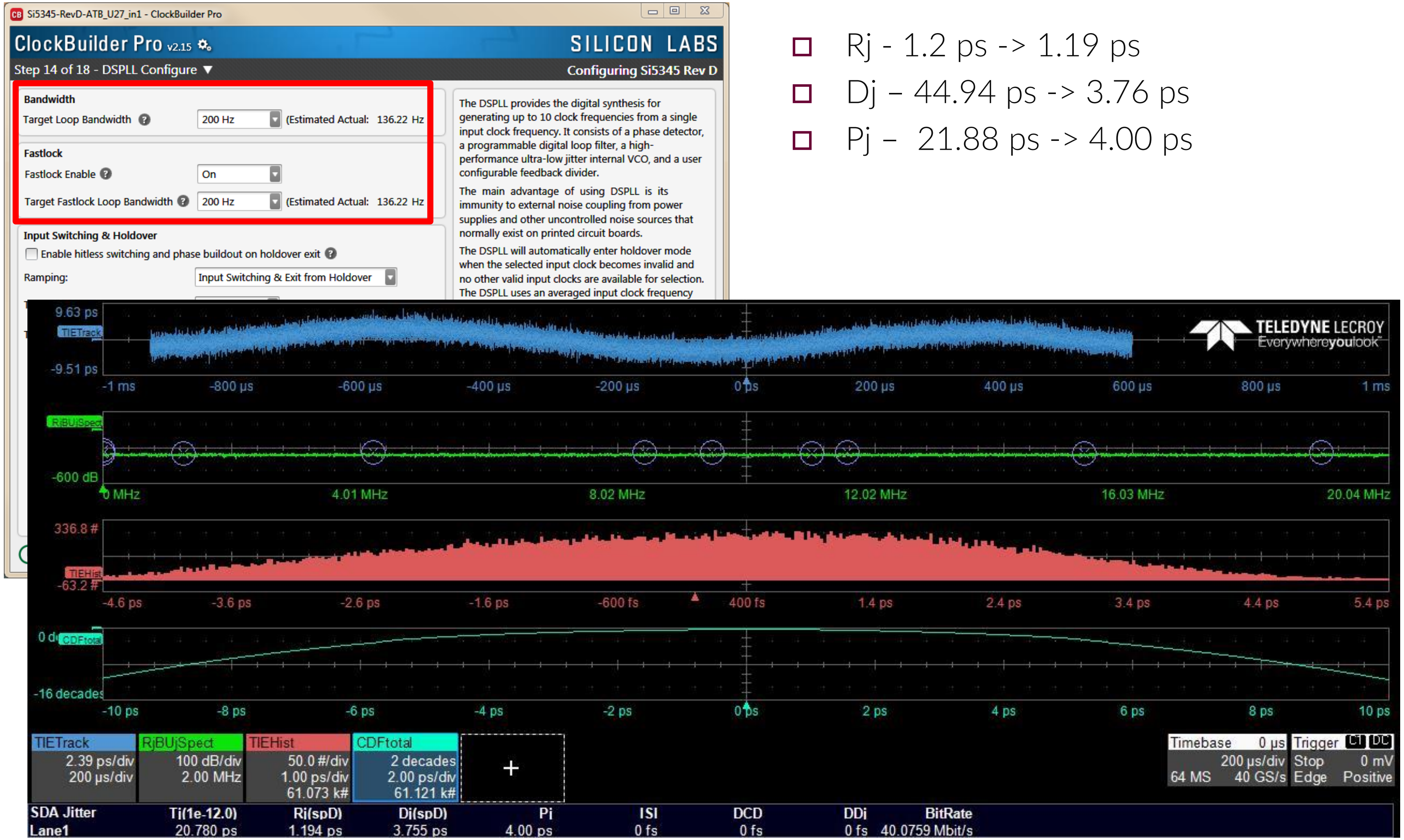
Jitter	spD	sp	nq	nq/spD
Ti(10^{-12}) [ps]	36.657	36.657	40.365	1.10
Rj [ps]	1.177	1.191	1.493	1.27
Dj [ps]	19.878	19.671	19.071	0.96
Pj[ps]	12.42	12.43	-	

Jitter on free-running Si5345 (second one) which emulates LHC clock for LTU in the lab

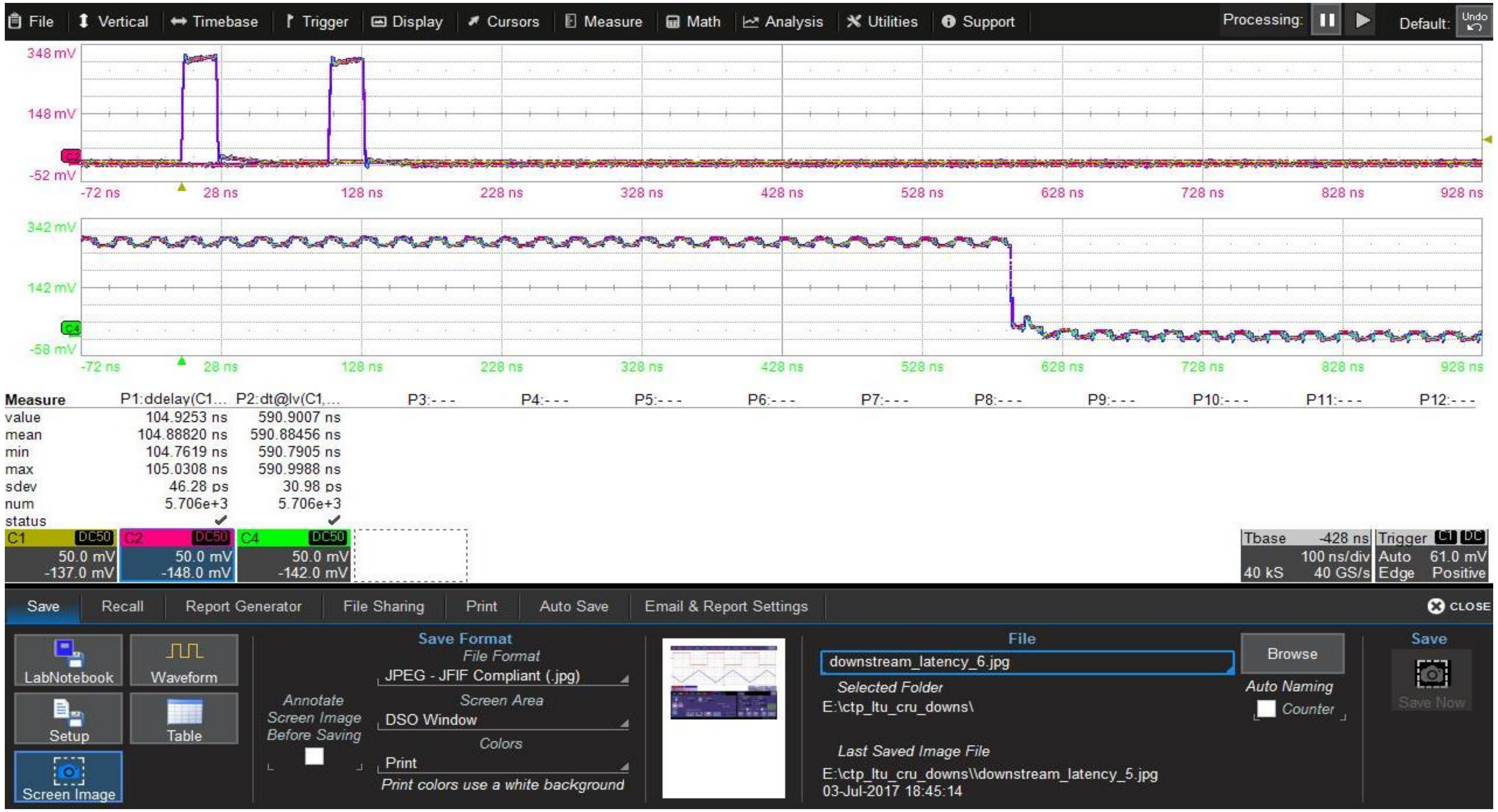


If no clock present on input of Si5345 => it generates free running clock 40.0785 MHz

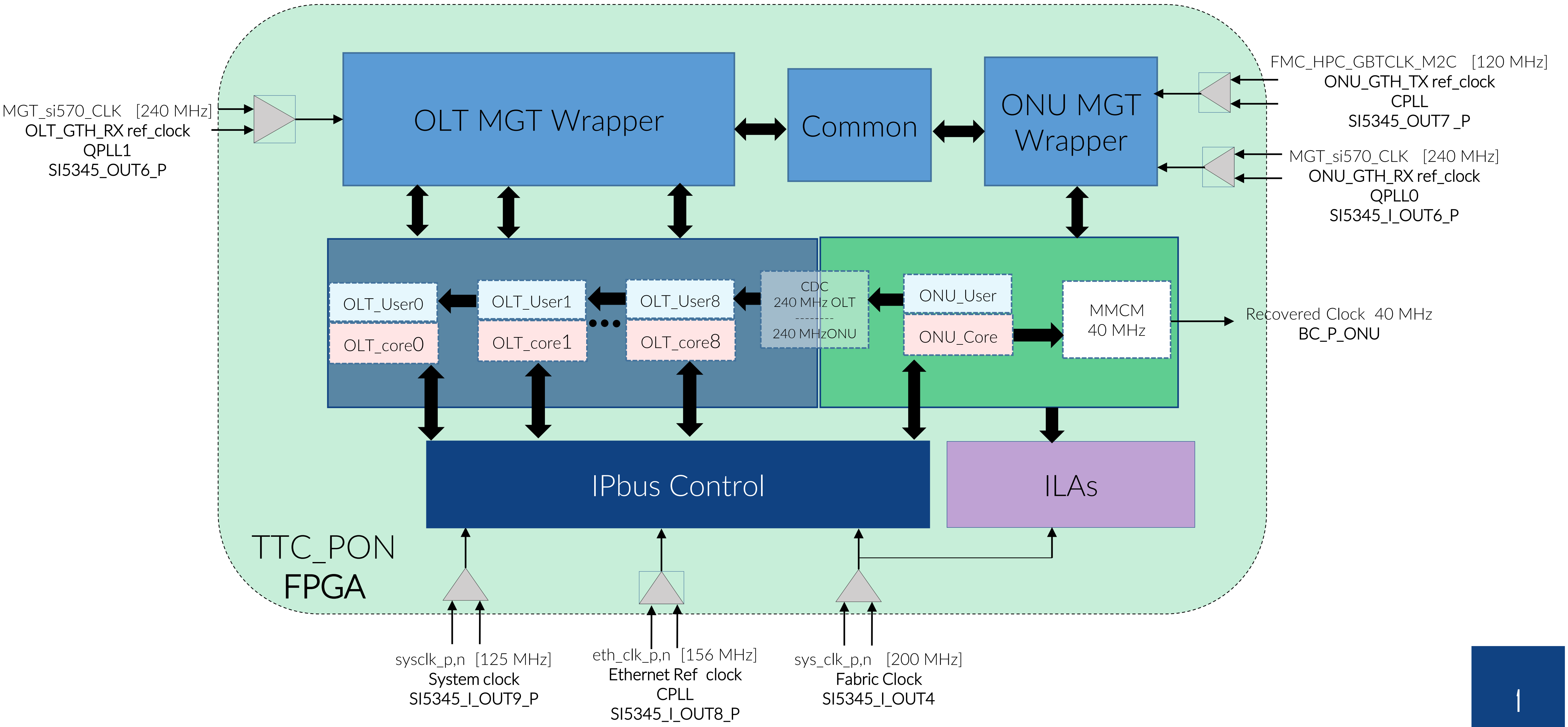
Si5345 bandwidth 718 Hz -> 136 Hz



- Rj - 1.2 ps -> 1.19 ps
- Dj – 44.94 ps -> 3.76 ps
- Pj – 21.88 ps -> 4.00 ps

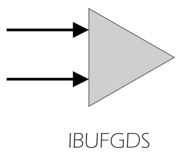

File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Support
Processing:
Default:
348 mV
148 mV
-52 mV
-72 ns 28 ns 128 ns 228 ns 328 ns 428 ns 528 ns 628 ns 728 ns 828 ns 928 ns
342 mV
142 mV
-58 mV
Measure P1:ddelay(C1... P2:dt@lv(C1,... P3:- - - P4:- - - P5:- - - P6:- - - P7:- - - P8:- - - P9:- - - P10:- - - P11:- - - P12:- - -
value 104.9253 ns 590.9007 ns
mean 104.88820 ns 590.88456 ns
min 104.7619 ns 590.7905 ns
max 105.0308 ns 590.9988 ns
sdev 46.28 ps 30.98 ps
num 5.706e+3 5.706e+3
status
C1 DC50 50.0 mV -137.0 mV
C2 DC50 50.0 mV -148.0 mV
C4 DC50 50.0 mV -142.0 mV
Tbase -428 ns 100 ns/div 40 kS 40 GS/s
Trigger C1 DC Auto 61.0 mV Edge Positive
Save Recall Report Generator File Sharing Print Auto Save Email & Report Settings
CLOSE
LabNotebook Waveform Setup Table Screen Image
Save Format
File Format
JPEG - JFIF Compliant (.jpg)
Annotate Screen Image Before Saving
Screen Area
DSO Window
Colors
Print
Print colors use a white background
File
downstream_latency_6.jpg
Browse
Selected Folder
E:\ctp_ltu_cru_downs\
Auto Naming
Counter
Last Saved Image File
E:\ctp_ltu_cru_downs\\downstream_latency_5.jpg
03-Jul-2017 18:45:14
Save
Save Now

Clock Scheme of the TTC_PON Multilink in “Proto_X”



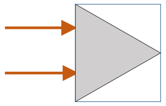
Clock Scheme of GBT_FPGA

* GBT_FPGA Simplified Block Diagram



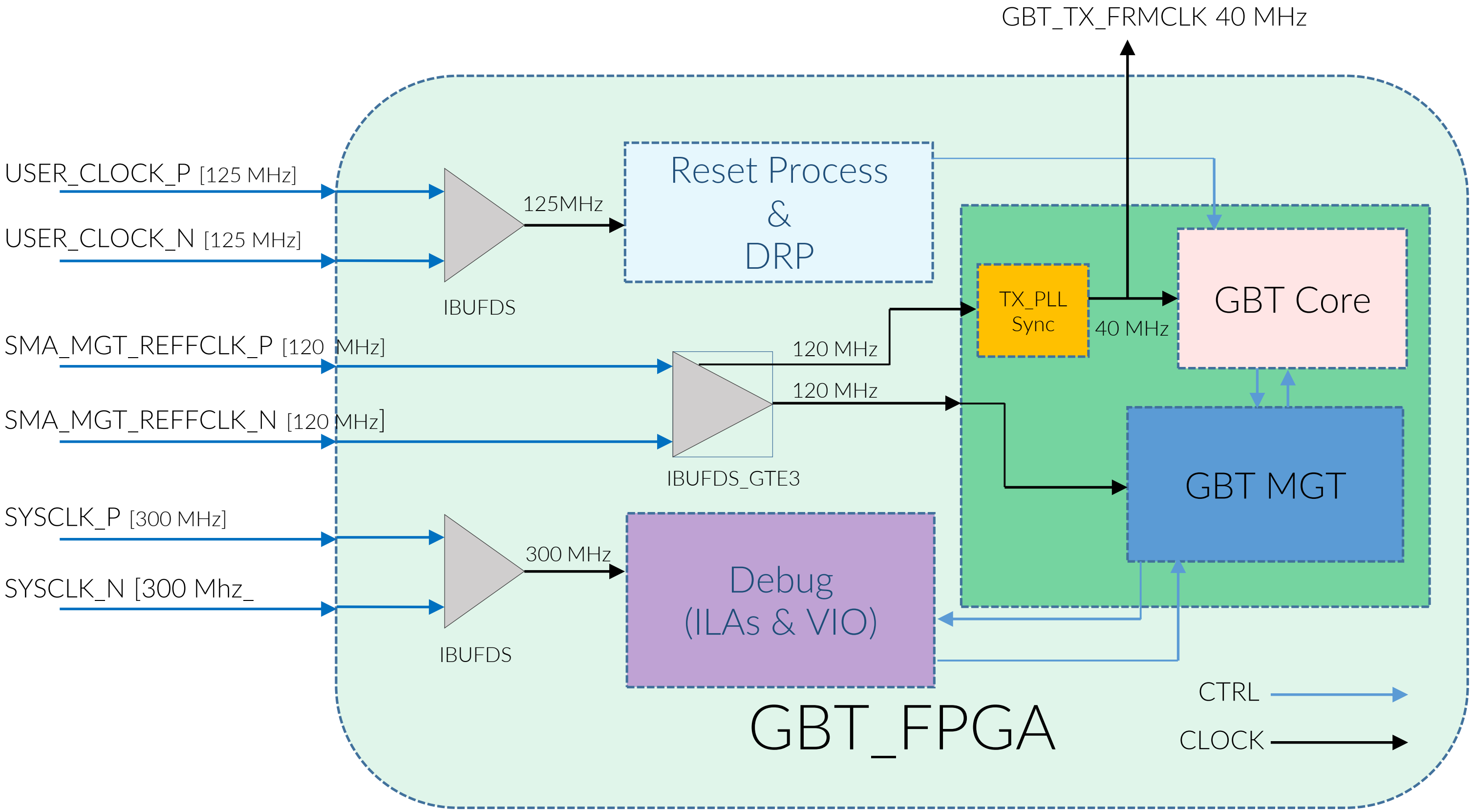
Xilinx Documentation
ug471

- IBUFGDS is used when an differential input buffer is used as a clock input

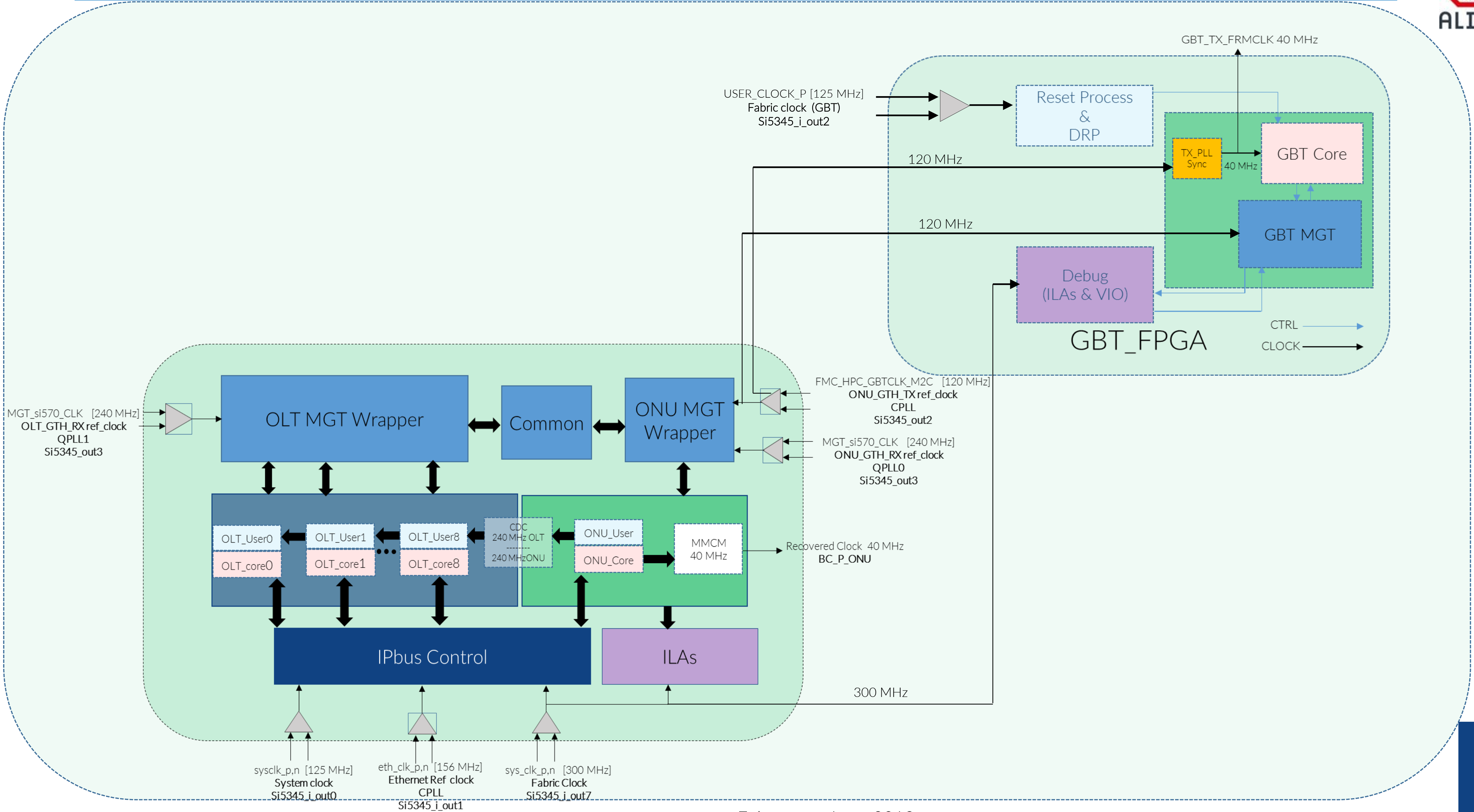


Xilinx Documentation
ug576

The reference clock is instantiated in software with the IBUFDS_GTE3 software primitive in UltraScale FPGA



Clock Scheme of the TTC_PON Multilink in “Proto_X”



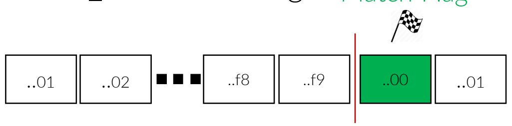
GBT-FPGA Downstream latency

The downstream latency must be constant, after reset process

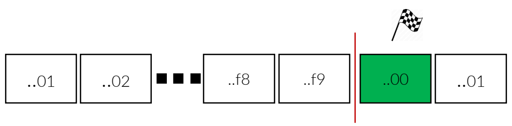
* GBT_FPGA Structure

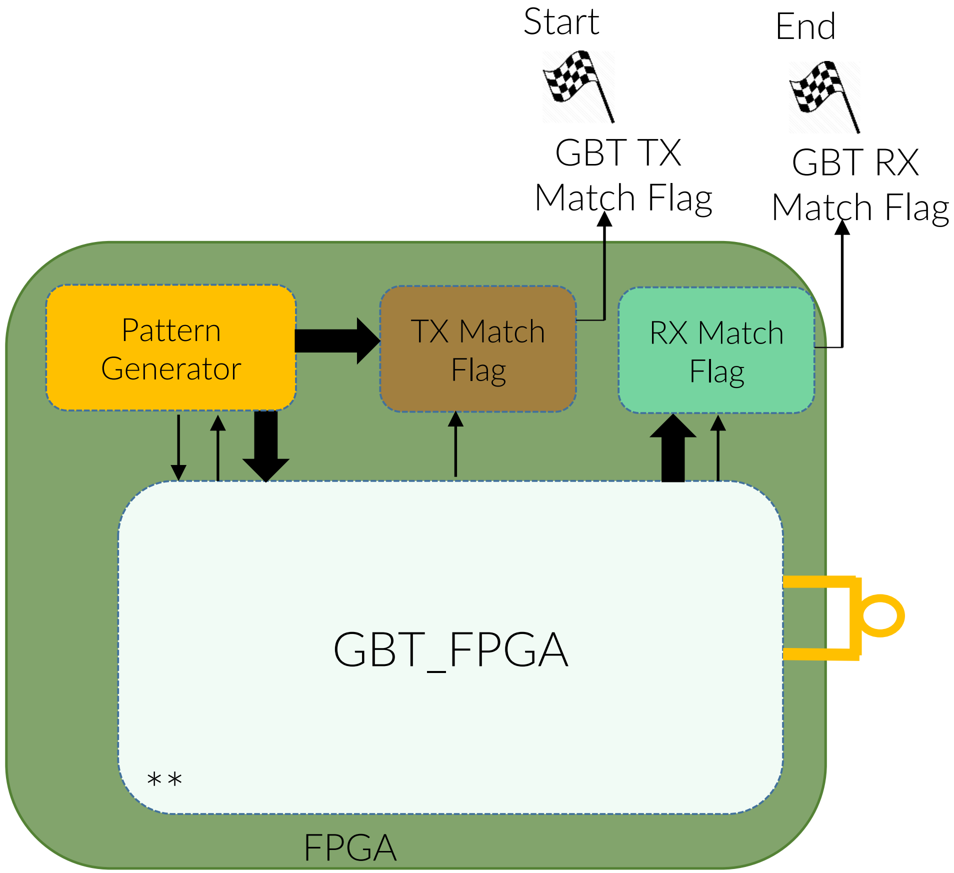
Downstream Latency

GBT in counter mode
GBT_TX Match Flag



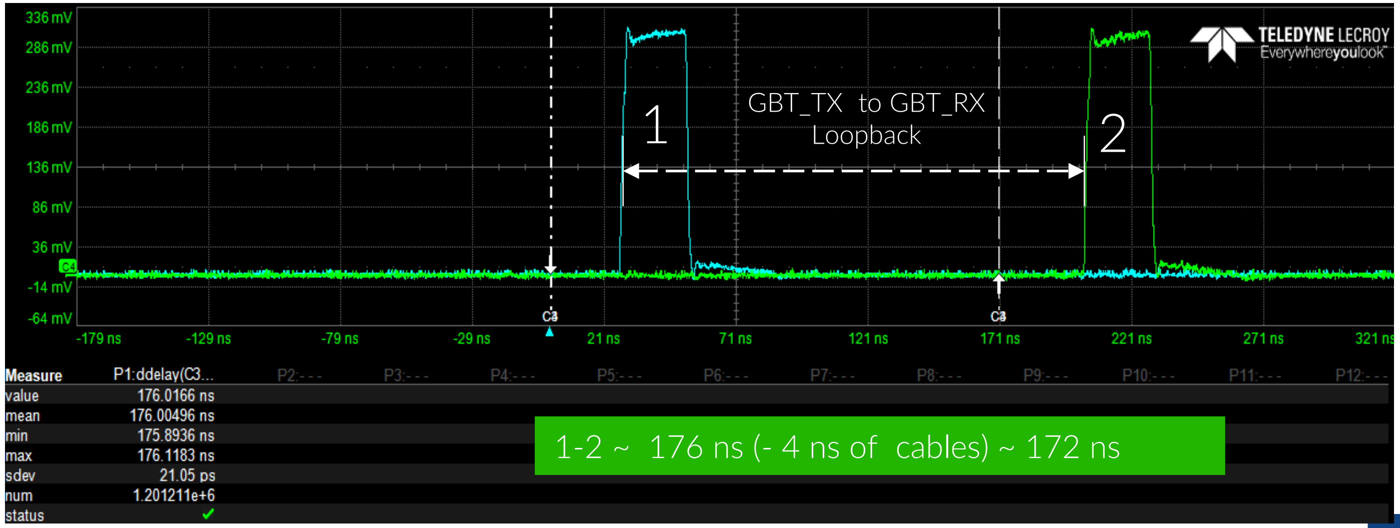
GBT_RX Match Flag





GBT-FPGA Config:

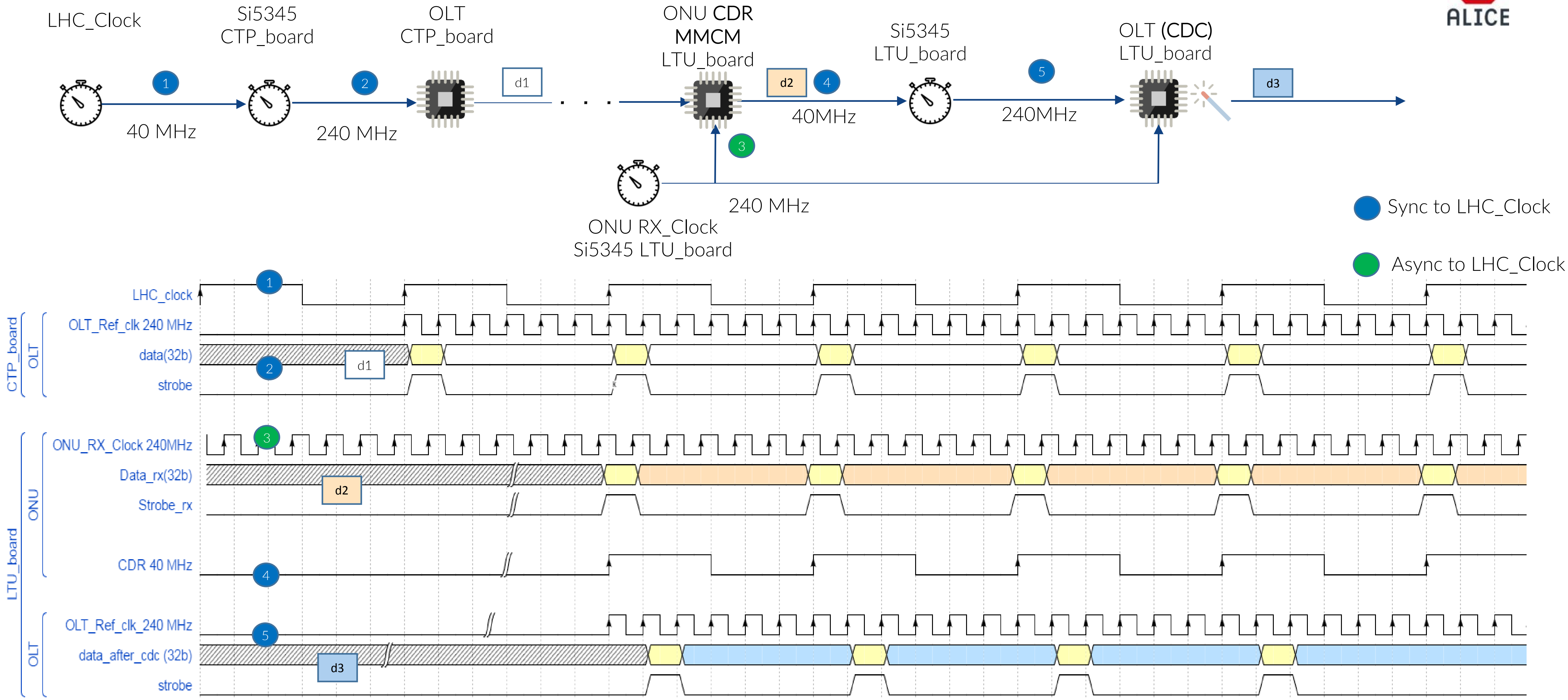
RX & TX Lat-Opt
GBT Encoder
loopback mode
MGT Ref: 120 MHz



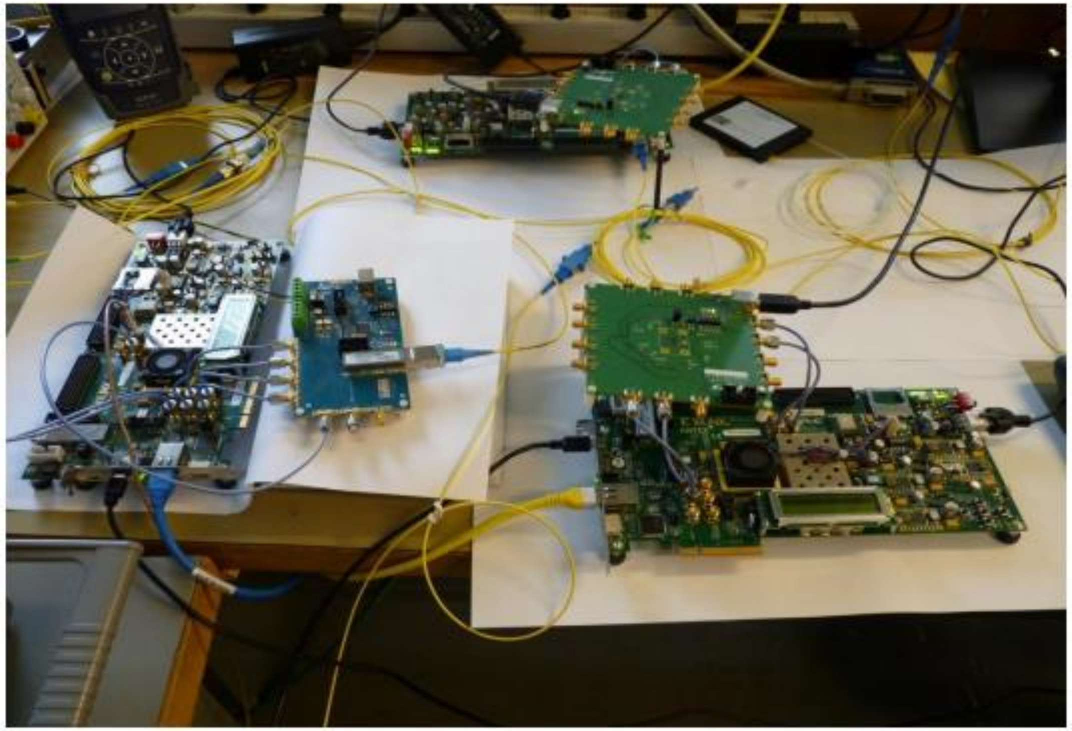
1-2 ~ 176 ns (- 4 ns of cables) ~ 172 ns

TTC-PON-- Clock scheme

ALICE



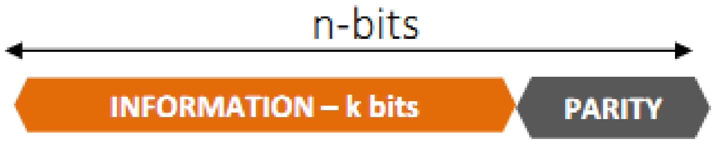
- OLT
  - 1 PON OLT device (SFP+ or XFP package)
  - 1 FPGA
    - Deployed on Kintex7, Kintex Ultrascale
  - 1 BC synchronous reference clock (240MHz) for the transceiver



- Optical Network
  - Single mode fibers
  - Passive wideband splitter

- ONU
  - 1 PON ONU device (SFP+)
  - 1 FPGA
    - Deployed on Kintex7, Kintex Ultrascale, Arria10
  - 1 PLL for Upstream Reference clock (120MHz)
    - Si5344

- Binary BCH codes are good for correcting random errors with a relatively low complexity [5]
  - Systematic encoding: BCH(n,k)



  - Four shortened-BCH codes were evaluated:
    - BCH(40,34)
    - BCH(80,73)
    - BCH(120,113)
    - BCH(120,106)

  BCH(40,34), BCH(80,73), BCH(120,113): Single-error correcting

  BCH(120,106): Double-error correcting

  - Main Figures of merit:
    - Efficiency (k/n)
    - Coding gain
    - Latency
    - Timing
    - Complexity (area)

- Scrambling: signal randomizer
  - Self-synchronous scrambling: no sync. overhead but error multiplication…

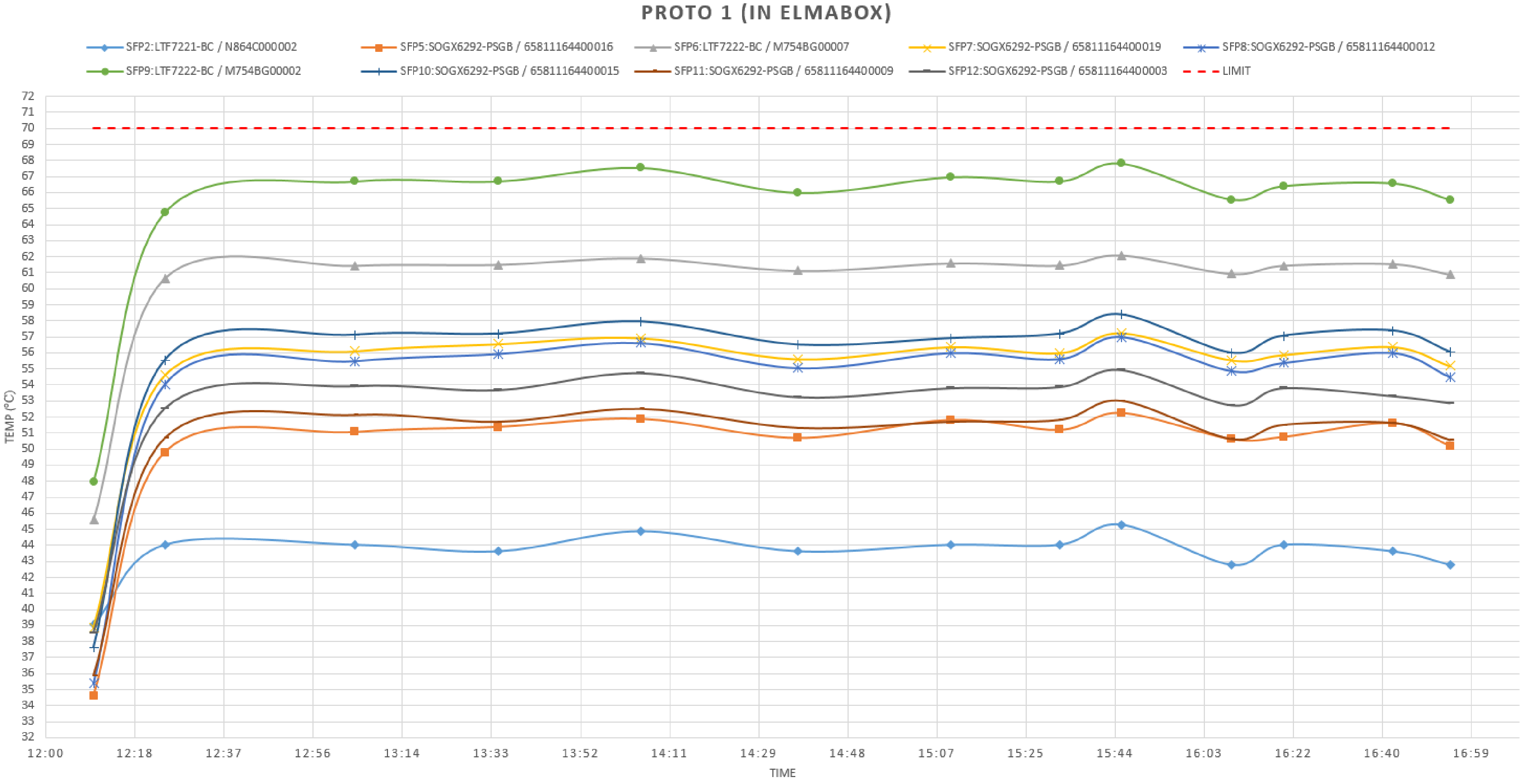
2. Block Error *Correction* Codes:

A. Hamming linear block error correcting codes.
B. BCH (Bose-Chaudhuri-Hocquenghem) cyclic block codes.
C. Reed-Solomon cyclic block codes.
D. Turbo Product Codes (TCP).

- This class of codes is a remarkable generalization of the Hamming code for multiple-error correction.
- We only consider binary BCH codes in this lecture note. Non-binary BCH codes such as Reed-Solomon codes will be discussed in next lecture note.
- For any positive integers $m \geq 3$ and $t < 2^{m-1}$, there exists a binary BCH code with the following parameters:

Block length:	$n = 2^m - 1$
Number of parity-check digits:	$n - k \leq mt$
Minimum distance:	$d_{min} \geq 2t + 1.$

Temperature test for OLTs and ONU (ELMA box, room temperature ~ 20°C)



DDR4 Memory Interface -- Clock scheme

Block Diagram Simplified