

# NA62 Trigger and Data Acquisition system

Dario soldi on behalf on NA62 collaboration



## WHY ARE WE TALKING ABOUT NA62?

- $\blacksquare$  NA62 aims to measure the ultra-rare decay K+ -> $\pi^+\nu\nu$ 
  - The Standard model expectation is: BR(πvv) = 8.4 x 10<sup>-11</sup>
- very intense hadron beam particle rate
  - close to a GHz upstream
  - more than 13 MHz of particles downstream
- good time resolution at level-0;
- a fast, selective trigger and data acquisition system;
- minimization of data-collection dead times and maximization of its efficiency and reliability rank high among the required features.





## GENERAL NA62 TRIGGER OVERVIEW

- 3 trigger levels:
  - hardware level: level-0 trigger
  - software level on partial data: level-1 trigger
  - software level on complete event: level-2 trigger
  - Level 0 trigger:
    - No collisions but continuous stream of data:
      - An Event is defined by in-time local conditions of different detectors.
      - Requires a seed detector to define a reference time.





# The NA62 Experiment

Ideas are everywhere, but the knowledge is rare Thomas Sowell



- Fixed Target experiment: 75 GeV secondary beam (6% kaons);
- High intensity beam: ~750 MHz;
- Signal: 1 beam track, 1 charged track, nothing else;
- Kinematics: O(10<sup>4</sup>) background suppression;
- Downstream  $\pi/\mu/e$  separation;
- 10<sup>7</sup> muon suppression, mainly from K  $\rightarrow \mu v$ ;
- 10<sup>7</sup> photon (mainly from  $K^+ \rightarrow \pi^+\pi^0$ ) suppression;
- Sub ns time resolution.



...and many others

Pr

6

0.16 0.14

0.12 0.1 0.08

0.06 0.04

180 200

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80 70 60



- 3 stations of Silicon pixel detectors inside an achromat;
- Time :  $\sigma \approx 130$  ps per station;
- Direction:  $\sigma_{dx,dy} \approx 0.016$  mrad, Momentum:  $\Delta P/P < 0.4\%$ ;



#### Straw Spectormeter:

- 4 straw chambers in vacuum;
- Each chamber measuring 4 coordinates (views);
- High accuracy: 130 µm/view;
- Straws participate to level-1 trigger selection. **RICH:**
- Cherenkov detector filled with Neon;
- 70 ps of time resolution.
- Used in the level-0 trigger as time reference.
- GPU-level-0 trigger implementation under study Dario Soldi - NA62 Trigger and Data Acquisition

NA48 CHOD

- Plastic scintillator hodoscope;
- ~200 ps time resolution;
- Used in level-0 trigger as control trigger;
   CHOD:
- Plastic tile scintillator;
- <1 ns time resolution;
- Decay topology detection;
- Used in level-0 trigger;



#### Large Angle Vetoes (LAV):

- 8.5 50 mrad
- 12 stations along the vacuum tank;
- LAV12 can be used in level-0 trigger to veto photons;
- LAVs participate at the level-1 trigger selection.

#### Small Angle Vetoes (SAV): very small angle <1 mrad;

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#### Liquid Krypton Calorimeter (LKr):

- Electromagnetic calorimeter
- photon veto coverage 1÷8.5 mrad;
- LKr is used in level-0 trigger to veto photons, mostly from  $\pi^0$ s.



#### MUV1/MUV2: Hadronic Calorimeters;

- Readout with LKr electronics;
- Can be used in level-0 as hadron trigger to complete the LKrelectromagnetic calorimeter information;

#### MUV3: Muon Veto

- Placed after an iron wall;
- Rate: ~ 14 MHz muons.
- Used in level-0 trigger to veto muons;

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# NA62 Data acquisition system

If we have data, let's look at data. If all we have are opinions, let's go with mine. Jim Barksdale

#### THE NA62 DATA ACQUISITION SYSTEM

- □ Fixed target experiment: **bursts** ~3 seconds long;
- Some detectors send raw data (primitives) to the level-0 trigger processor LOTP;
  - Primitives are generated from TEL62 read out boards.
- L0 trigger is generated after a **maximum latency of 1 ms**;
- All detectors except Calorimeters and GTK respond to L0;
- Calorimeters and GTK send data after L1 request;
- □ L2 trigger run over the complete event information.





## PRIMITIVES

Primitives encapsulated in ethernet standard UDP payload: 270 m of detector length requires switches to connect different read-out boards. Easy to debug.

- Data Format: 32 bit.
- Primitive ID : encodes the detector information (Energy, multiplicity, position);
- □ Timestamp : 25 ns precision time of the raw data;
- □ Fine Time : additional time information with a precision up to 100 ps.



## **TEL62 - A COMMON READOUT**





□ Allow to read **data and** generate trigger **primitives**; □ Upgrade of LHCb TELL1;

Hosts TDC Boards: custom mezzanine equipped with 4 High Performance Time to Digital Converter chips with 100 ps LSB precision.

□ 4 FPGAs (PP) are connected to TDC Boards and to 2-GByte DDR2 memory buffers, storing the data during the LO trigger latency.

- The central FPGA (SL): connected with each PP through two 32-bit data buses reserved for data and L0 trigger primitive flow.
- □ The data and L0 trigger primitives from all PP are linked, **possibly zero suppressed** and encapsulated on the SL, where **aggregation with data from other** TEL62 boards can also take place.

Data from several events are packed together, stored in a Quad Data Rate (QDR) SRAM, and finally sent to the output board.

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# LO - Trigger Generators

**Tank**: So what do you need? Besides a miracle? **Neo**: Guns. Lots of guns! Matrix

## What we need:

- Charged Track Topology, Multiplicity and Time
  - CHOD hodoscope
  - RICH
- Energy
  - Calorimeters
- Vetoes
  - Calorimeters
  - LAVs
  - Muon Veto (MUV3)
- Minimum Bias Trigger: NA48-CHOD
- R&D: RICH GPU Trigger Generator

stable latency

#### CHOD - MUV3 LO TRIGGER GENERATORS

- **MUV3** is used in L0 trigger to tag muons;
  - 14 MHz of muon rate;
- CHOD is used to tag any charged particle;
  - identify different **topologies**;



- TDC hits are read from the PP-FPGA, arranged and time-ordered to the level of 25 ns;
- ♦ TDC hits are sent to one of 64 tile modules;
- Tile modules contains 2 buffers used to store hits from the two channels of the same tile, plus a coincidence module that compares absolute hit times;
- If hits are within coincidence time window they are combined into a **tight candidate**, otherwise the earlier hit is converted to a **loose candidate**, while the later one remains in the buffer;
- ♦ An output module transfers candidates to the SL-FPGA in frames of 6.4us;
- ♦ A sorting module contains two sets of 64 sorting buffer FIFOs;
- ♦ Candidates in consecutive frames are sent alternately to the first or second buffer set
- each buffer stores hits related to a **100 ns time interval**, with earliest hits in the first and latest hits in the last buffer.
- Once all candidates from a frame have been written, they are passed to the clustering modules.

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#### CHOD - MUV3 LO TRIGGER GENERATORS

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- A cluster is characterized by:
  - the cluster seed time (T) being the time of the candidate that created the cluster;
  - **the summed time-difference (DT)** between the merged candidates and the cluster seed time;
  - the number of candidates (N) merged into the cluster;
  - Four flags to record which quadrants the merged candidates are assigned to.

Candidates are read, compared to the cluster seed time If the their time is within a matching time window around the seed time, they are merged into the cluster. Otherwise the candidate is converted into a new cluster;

Clusters are converted to trigger primitives labeled with an absolute primitive time **PT = T + DT/N** 

#### CHOD - MUV3 PERFORMANCES



#### **RICH-NA48 CHOD LO TRIGGER PERFORMANCES**



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## THE NA62 LKr ELECTROMAGNETIC CALORIMETER

Radiation Length: 27 X0;

read out channels: 13248

□  $\sigma_{E}/E$  (GeV): 0.032/ $\sqrt{E}$  + 0.09/E + 0.0042; □  $\sigma_{x,y}/x,y$  (cm): 0.42/ $\sqrt{E}$  + 0.06; □  $\sigma_{t}/t$  (ns) : 2.5/ $\sqrt{E}$ ;

□ Photon veto in the angular decay region 1-8.5 mrad

- $\Box$  mostly due to  $K^+ \rightarrow \Box^+ \Box^0$  decays
- $\square$  for E $\square$  < 35 GeV 80% of the photons are in the Lkr acceptance
- □ Inefficiency <  $10^{-5}$  for E□ > 10 GeV



## CALORIMETER READOUT MODULES (CREAMS)



## THE LKr TRIGGER PROCESSOR



- **Pixel-based trigger processor** with 4x4 calorimeter cell tiles (Super-Cells)
- Identifies em clusters and prepares a time-ordered list (time, position and energy) for the LO Trigger Processor.
  - □ Front-End boards (28): **peaks in time** indipendently searched in each vertical slice: digital constand fraction discriminator + linear interpolator for fine timing.
  - Merger boards (7): peaks close in space and time merged and assigned to the same electromagnetic cluster.

#### THE LKr TRIGGER PROCESSOR



MaxClsPrimDeltaXYPosition



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Time Offset for all supercells, corrected







#### ONLINE TIME-ALIGNMENT AND MONITOR



- 7 mirroring switches to duplicate trigger-primitive streams going from the detectors to the LOTP;
   monitor and alignment of incoming primitives.
- check beam quality;

#### Primitive Timing wrt RICH: Run 7906 Burst 129





## LEVEL ZERO TRIGGER PROCESSOR



- □ UDPs sent in frames with a period of 6.4 us;
- □ Unsorted primitives form 7 different sources received by LOTP:
  - □ first alignment at UDP frames;
  - ☐ fine alignment of primitives using time addressed rams;
- In time primitives compared with pre-selected masks using an associative memory;
- □ Triggers sent in phase with the 40 MHz clock;
- Triggers are sent after a programmable latency (up to 1 ms).

LOTP Design values:	
Sources	7
Inputs	10 MHz
Outputs	1 MHz
Masks	16
Latency	< 1 ms
Dead Time	75 ns

## LEVEL ZERO TRIGGER PROCESSOR IN 2016

#### L0 Trigger Rate<sub>2016</sub> $\sim$ 435kHz





## RICH-GPU TRIGGER PROCESSOR

The measure of a man is what he does with power Plato

## RICH-GPU TRIGGER PROCESSOR

**GPUs** provide a huge computing power on a single device, thus allowing to take complex decisions with a significantly high speed capable to match valid event rates.

GOAL: RICH-Ring reconstruction directly on GPU. Very clean tag/veto system at level-0

Problems to be investigated:

Are GPUs fast enough to take trigger decision at tens of MHz events rate?
 Is the latency along the whole data path (Detectors -> GPU -> Trigger) stable enough for usage in synchronous trigger systems?



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## LATENCY: MAIN PROBLEM OF GPU COMPUTING



- Data coming from the detectors are received from the Network Interface Card
- Data must be moved/copied between Host and Device
- Latency fluctuations due to OS

- **NaNet** is an FPGA-based PCIe NIC with real-time data transport architecture
- Allows direct data exchange over the PCIe bus with no CPU involvement
- Zero copy I/O
- Perform preprocessing on data stream on the NIC

#### GPU HARDWARE ENVIRONMENT



NaNet design implemented on an ALTERA Stratix V FPGA dev board (Terasic DE5-NET)

- PCle x8 Gen2
- 4 SFP+ ports (four 10GbE 10GBASE-KR)
- GPUDirect RDMA capability
- UDP protocol offload
- Real-time stream processing on the FPGA:
  - Decompression and Merging of events
  - Arranging data for optimal GPU memory access (data alignment)

Results can be directly injected from GPU memory into the network

## GPU ALGORITHM

- □ XY plane divided into a grid
- A histogram is created with distances from these points and hits of the physics event
- Rings are identified looking at distance bins whose contents exceed a threshold value
- □ **Pros**: naturally mapped on the GPU threads grid
- Cons: local memory limited, performances depending on number of events/hits
- $\diamond$  Trackless
- ♦ Multi-rings
- $\diamond$  Fast
- $\diamond$  Low latency
- Accurate





#### **GPU RESULTS**



Pascal P100 makes the ring reconstruction latency on GPU compatible with the experiment requirements.

Tests at the experiment are ongoing.



# High Level Triggers

They say they have you on tape, pulling the trigger! Prison Break – Seasion 1 – Episode 16



HLTs are running online on 30 PCs.

L1 algorithms selects data using the information coming from:

- KTAG  $\rightarrow$  incoming particles has to match with a Kaon;
- LAVs  $\rightarrow$  events with photons at large angle are veto;
- STRAWs  $\rightarrow$  cut on topology and momentum of the tracks;



#### Kaon TAGger



**\_**\_\_

8

all\_L0

6

beam tracks

minimum KTAG multiplicity

- Reduces of a factor 2.5 the L0 rate;
- Reduces of a factor 10 the beam halo traks;

3

efficiency

1

0.8

0.6

0.4

0.2

0

**P** 

omulti-tracks

#### Large Angle Vetos And Straws

#### LAVs

- **Hit-multiplicity cut** in the twelve LAV stations
- reduction of  $K^+ \rightarrow \pi^+\pi^0$  background by identifying photons at large angles.
- **Trigger efficiency** on a single-track event > 95%
- Data reduction ~20%



#### STRAWs

- Hough transform to define a track
  - Position of vertex
  - closest distance of approach to the beam axis
- Crude momentum evaluation
- Trigger efficiency on signal > 99%
- Data reduction ~40%





# Conclusions

Si finis bonus est, totum bonum erit. Gestae Romanorum

#### CONCLUSIONS

- The NA62 TDAQ system is quite peculiar with respect to other collider trigger systems:
- The timing resolution appears fundamental already at the level-0 trigger in order to reject the high background.
- All the systems involved in the trigger have a level-0 time-resolution < 2.5 ns.
- □ NA62 is able to digest ~14 MHz of decay-products reducing them at 1 MHz after level-0 and 100 KHz after level-1 triggers.
- Monitoring systems allow reproducing the trigger conditions offline, giving the possibility of data-driven trigger simulations.
- GPU level-0 trigger system is under development.
- NA62 is triggering its πvv events, analysis is going on to make them emerging from the data.

# **THANK YOU** for your **ATTENTION!**



# SPARES

additional material

#### RICH-NA48 CHOD L0 TRIGGER GENERATORS

- > produce time-clusters of hits belonging to the same event.
- > provide **precise time reference** (100 ps time resolution) and hit count.
- > No geometrical or detector-specific information is used.
- □ A Data Converter reads TDC data and converts them in the trigger processor format.
- A Data Merger in the SL mergers the clusters coming from 4 PP-FPGAs at a rate of 1 word per clock cycle.
- □ The data merger is purely combinatorial
- □ This module can handle a 1024–16=1008 words per 6.4us frame

#### Anomalous instantaneous high rate are absorbed in dedicated buffers

An Average Calculator module computes the weighted mean of the clusters' times with a 8-bit FPGA-embedded divider.

It calculates the new cluster as:

```
Seed<sub>new</sub> = Seed<sub>old</sub> + SUM<sub>old</sub>/N<sub>old</sub>
N<sub>new</sub> = N<sub>old</sub>
SUM<sub>new</sub> = 0
```

A Primitive Builder formats the incoming data in the standard NA62 format, computes the ID for each primitive and sends it to the standard assembler module and then to the LOTP. Dario Soldi - NA62 Trigger and Data Acquisition 1 - Feb - 18

#### TO CORRECTION FOR THE ONLINE LKR TIME CALCULATION

Calo T0 Map



#### NOT ONLY $K^+ \rightarrow \pi^+ \vee \vee$



+ Pedestals before and in burst + LKr calibrations at the end of beam extraction.

#### HIGH INTENSITY BEAM



Rate after target: ~800 MHz;

Rate of Kaons: ~50 MHz (6%) =  $5 \times 10^7$  Kaon/s;

burst/year: #days (100) x 24 h x 60 min x 3 burst/min:  $4 \times 10^5$ ;

Kaon decays/year:  $3 \operatorname{seconds} x 4 \times 10^5 \operatorname{burst/year} x 5 \times 10^7 \operatorname{Kaon/s} = 5 \times 10^{13}$ ;

Decays in fiducial region: 10%;

Decay in the detector acceptance: 10%;

Total Kaon decay collected/year: =  $5 \times 10^{11}$ ;

In one year of data taking we expect: 40 K<sup>+</sup> ->  $\pi^+$ vv if standard model BR;



- Models with a CKM-like structure of flavour interactions (e.g. MFV);
- Models with new flavour and CP- violating interactions in which either left or right handed currents fully dominate (e.g. Z or Z' FCNC scenarios);
- More specifics NP models like Randall-Sundrum;

#### EFFECTIVE SPILL LENGTH

To calculate the rates, the effective length of the spill is required:

Rates calculated using  
the Effective Spill  
Length:  
$$T_{eff} = \frac{\left[\int_0^T F(t)dt\right]^2}{\int_0^T F(t)^2 dt}$$
F(t): beam current as a  
function of time,  
approximated with the  
number of primitives.  
**Best value: 3.8 s.**

## CLOCK AND TIMING DISTRIBUTION





#### TTC The TTC (Timing and Trigger Control) system encodes on the same single-mode optical fibre

- Clock.
- synchronous triggers pulses.
- Start of Burst (SOB).
- End of Burst (EOB).
- CHOKE/ERROR triggers (asynch).

#### Local Trigger Unit (LTU)

- Receive trigger from the L0 Trigger Processor.
- Encode triggers and send to detector TTCex.
- Receive CHOKE/ERROR signals from detector and propagate it to LOTP.

#### DETECTORS IN 2016 DATA TAKING

#### CHOD

*Primitive*: Coincidence between two slabs *ID*: multiplicity and quadrants

#### RICH

Primitive: Time clusters ID: Hit multiplicity

#### LAV12

Primitive: Coincidence between high and low threshold crossingID: Hit multiplicity (possible cut on ToT)

#### MUV3

*Primitive*: Coincidence between the 2 PMTs coupled to the same tile *ID*: Position, Multiplicity.

#### **New CHOD**

Primitive: Coincidence between the 2 PMTs coupled to the same padID: Multiplicity, topology of the event;

**LKr** (LKr, MUV1-2, IRC/SAC) *Primitive and ID*: Energy threshold, number of clusters









#### HARDWARE

Terasic DE4 board powered by the Stratix® IV GX FPGA;

- 4 Gigabit Ethernet links.
- 2 HSMC.
- USB mini-b.
- USB blaster.
- 2 40-pin connectors.
- SMA in/out.

Two mezzanines with 2 GE ethernet links;

Daughter card with TTCex component;

Lemo adaptor for LKr Calibration Signals.

Located in the Electronic Room, environment without radiation.

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LEMO adaptor for LKr calibration signals



## RICH LO PRIMITIVE GENERATION SCHEME



