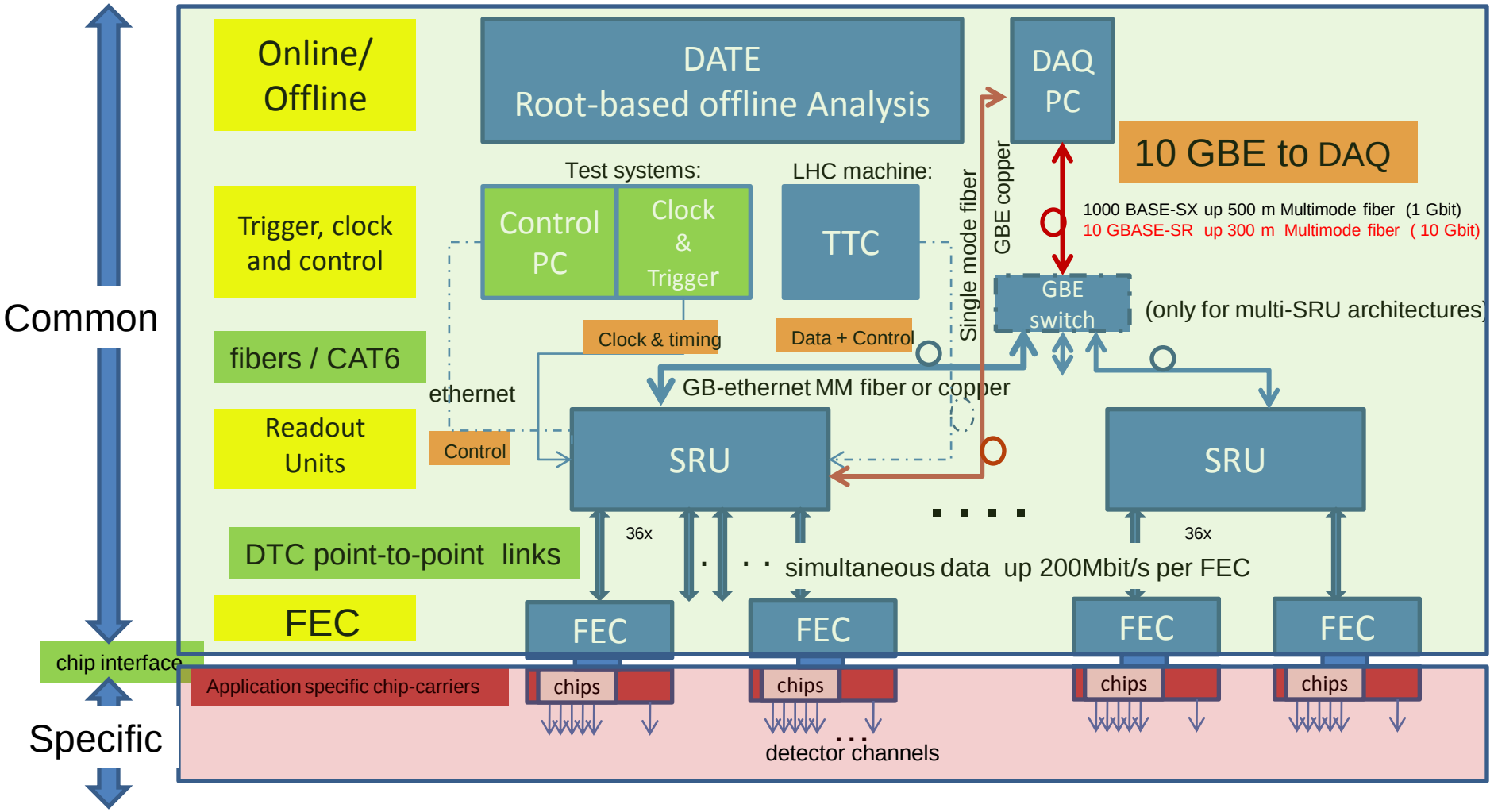
Status of the RD51 Scalable Readout System (SRS)

common for: gas & solidstate & photon - detectors

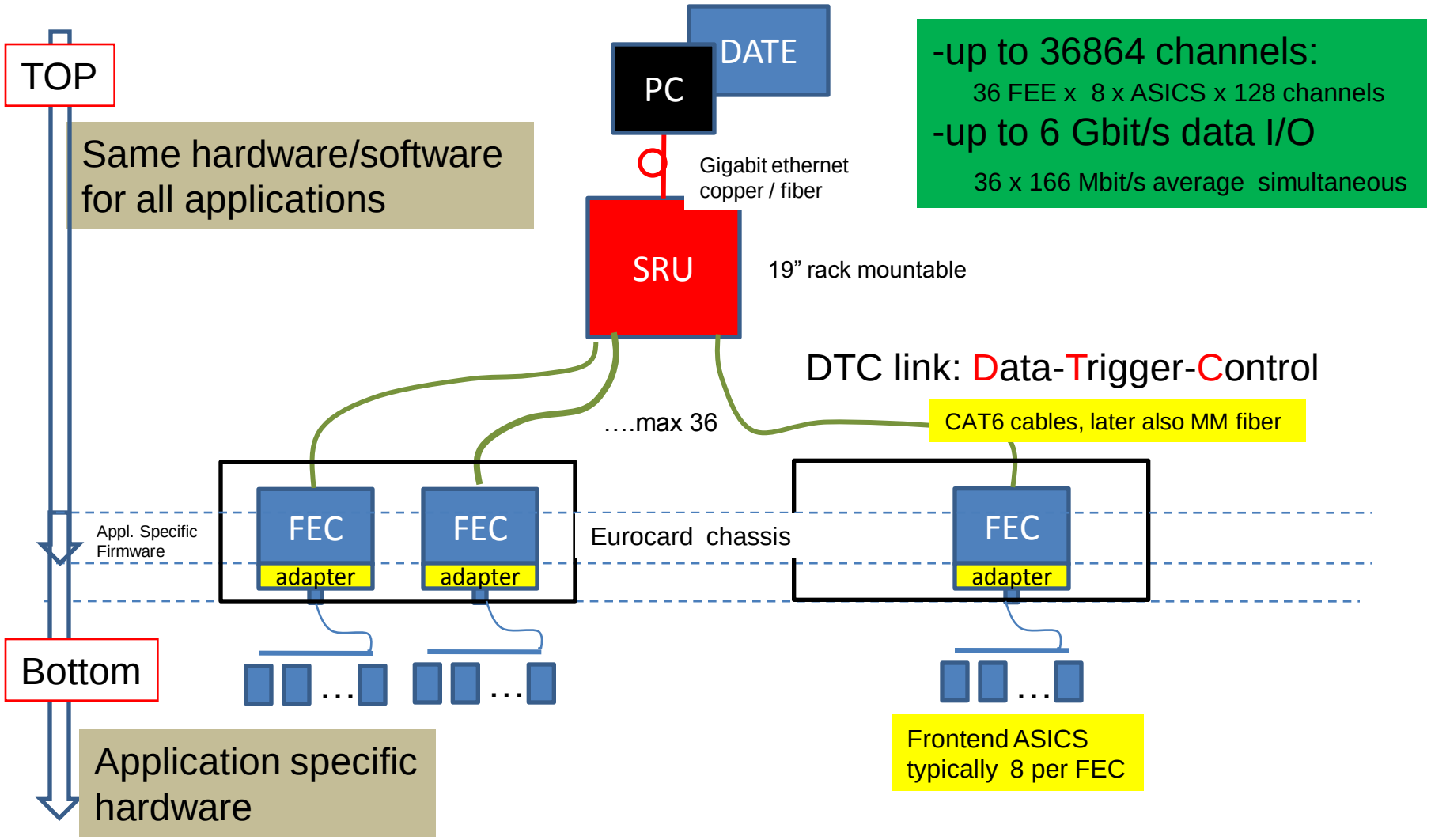
See previous talks:

April 2009 (CERN) proposal
July 2009 (Creta) approval
September 2009 (CERN Miniweek) work status

SRS proposal revisited:



First target 2009: single SRU system 1Gbit



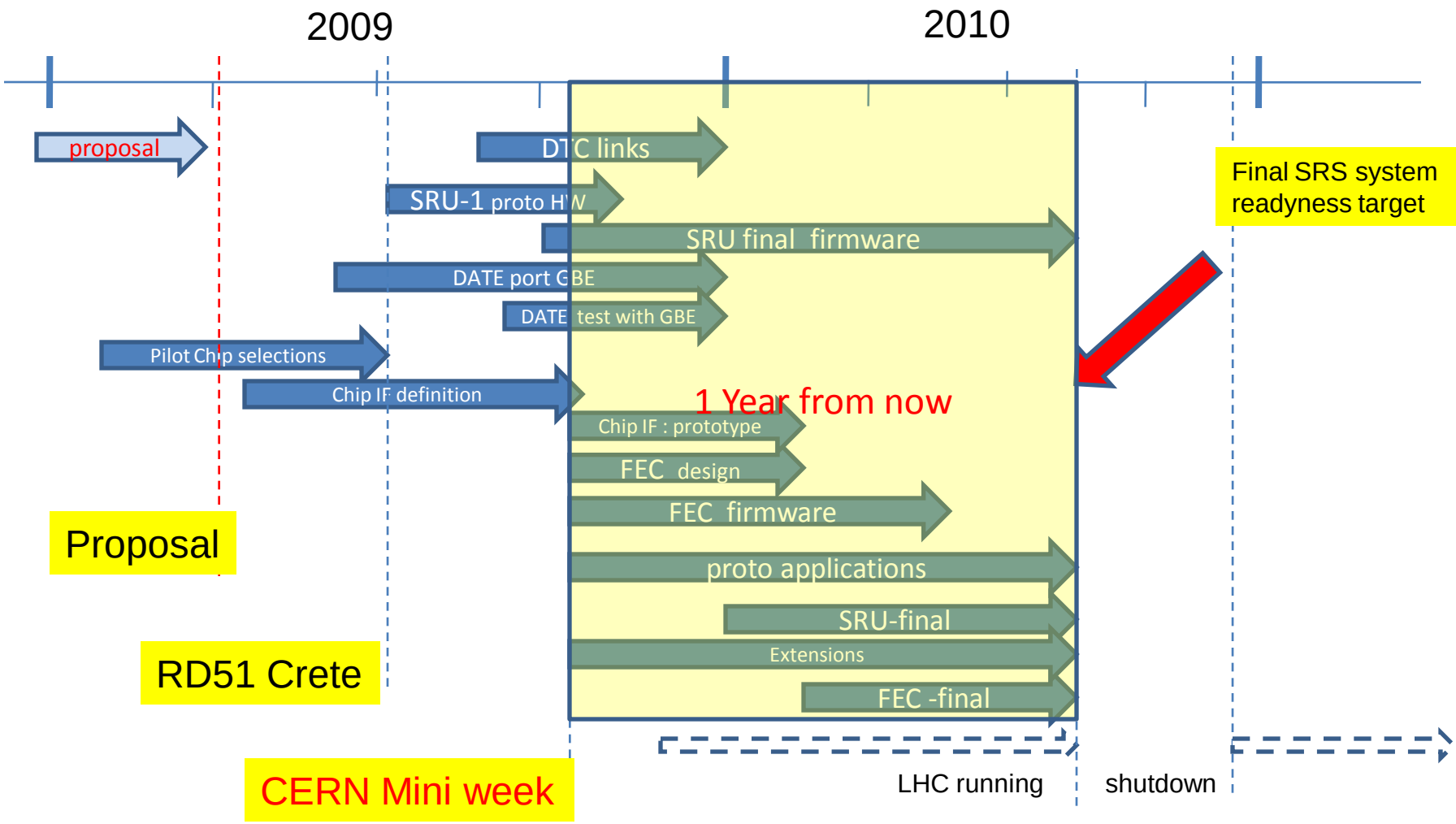
What happened since July (Crete)

- Frontend interface for readout chips finalized for approval and ready to go
- System extensions added to the frontend concept
- CERN Fellow (Sorin Martoiu , thesis on readout systems) joined (see talk)
- First version of SRU board layout finalized, PCB production pending
- First success with porting of DATE software to Gigabit Ethernet (see talk)
- DTC (Data Trigger Control) link protocol ready for test at CCNU/ Wuhan
- Declaration of interest from 2 more teams (to be confimed)
- First targeted chip adapters cover: APV25, Timepix, After, Altro
- First targeted extensions: APD / SiPM programmable bias, 1 ns light pulser
- Extensions under consideration: GBT and Triggerless system adapter
- PCIe x16 general purpose extension added

SRS characteristics

- Links instead of buses: more reliable, longer distance, more bandwidth
- Scalable: small system= few links 1SRU, large system= N links to N/36 SRUs
- Merge 3 streams : single DTC link (Data, Trigger, Control) copper or fiber
- Chip frontend exchangeable: keep the common readout system
- Cheap & standard: frontend card chassis, cables, fibers, network
  = Eurocard format, CAT6 cable or 850 nm MM fiber, (10)Gigabit Ethernet
- DAQ system: robust, user-friendly and supported: Alice / DATE
- Scalable RO architectures: consisit of few HW units: SRU and FEC+ adapter
- Chip interfaces and Extensions based on 2 type of adapter cards A and B
- A cards for chips, B cards for extensions (LED pulsers, programble HV etc)
- Extensions possible: 1.) GBT radhard fiber for new frontend ASICs
  2.) PCIe application chips (images and video) 3.) triggerless systems

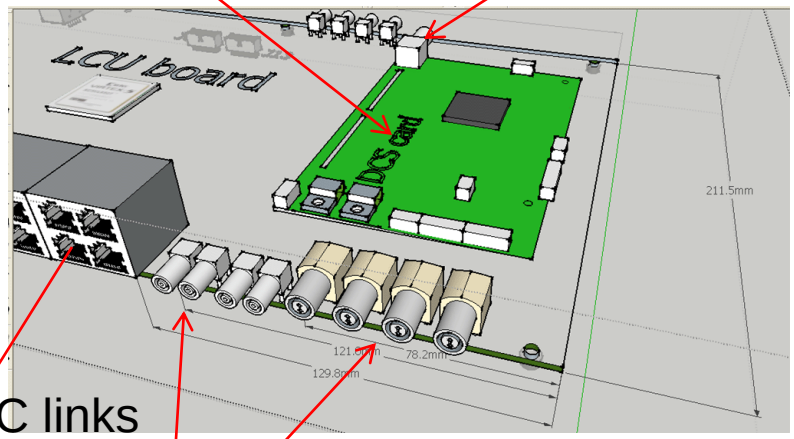
updated project timing

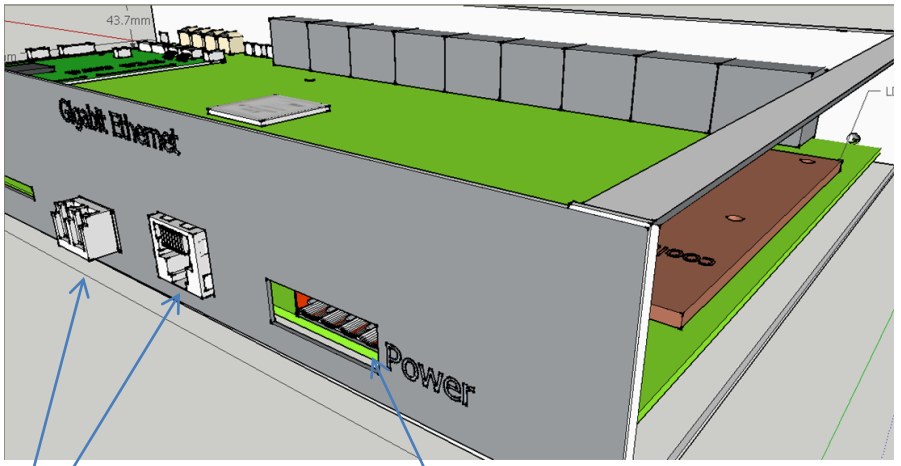


SRU connectivity

Networked
slow controls subsystem

LHC: TTC optical input





DTC links
→ FEC

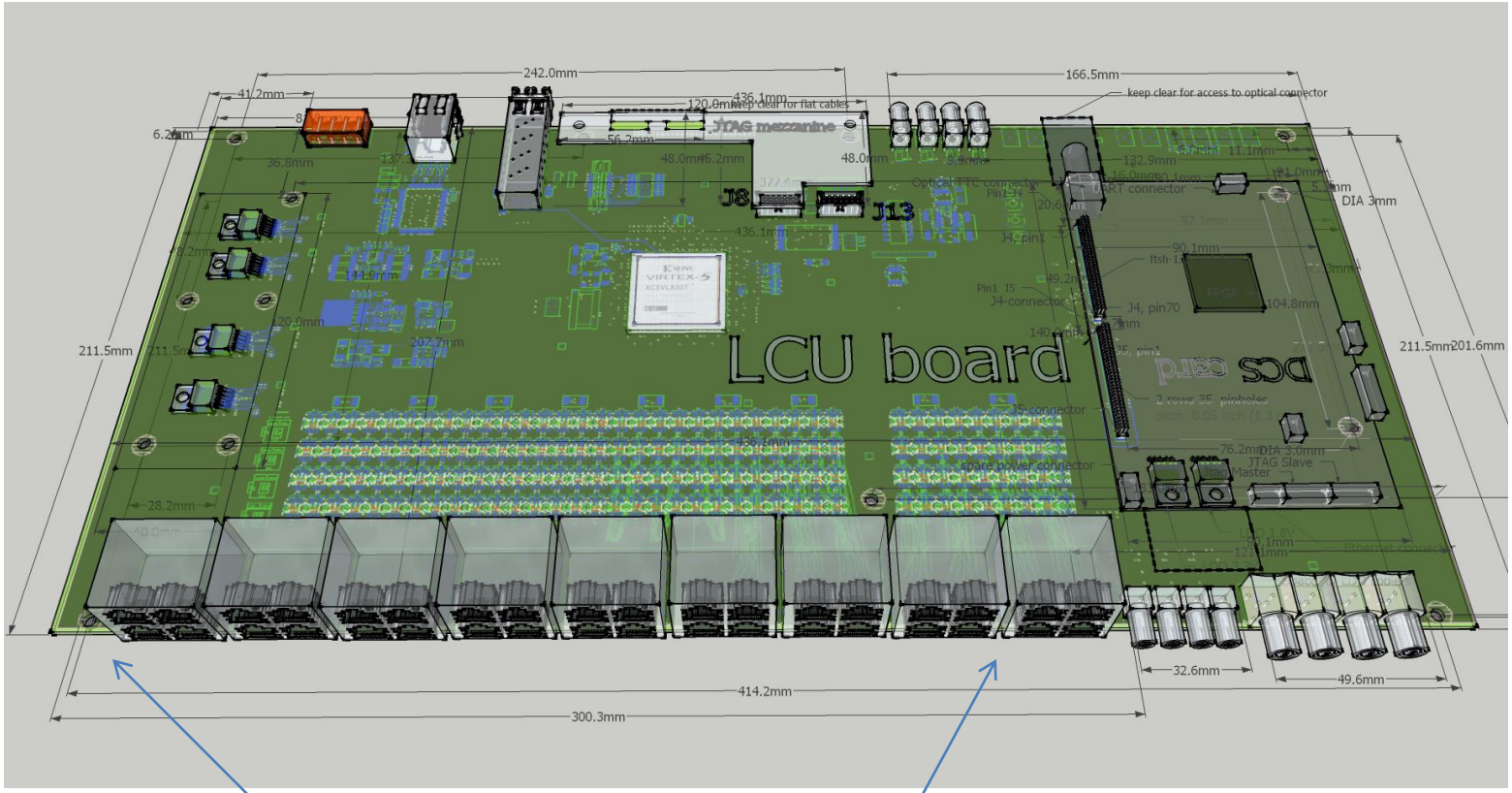
Trigger and clock signals
(NIM, LVDS)

Gigabit Ethernet
optical / copper
→ DAQ

ATX power

First SRU proto is called LCU*

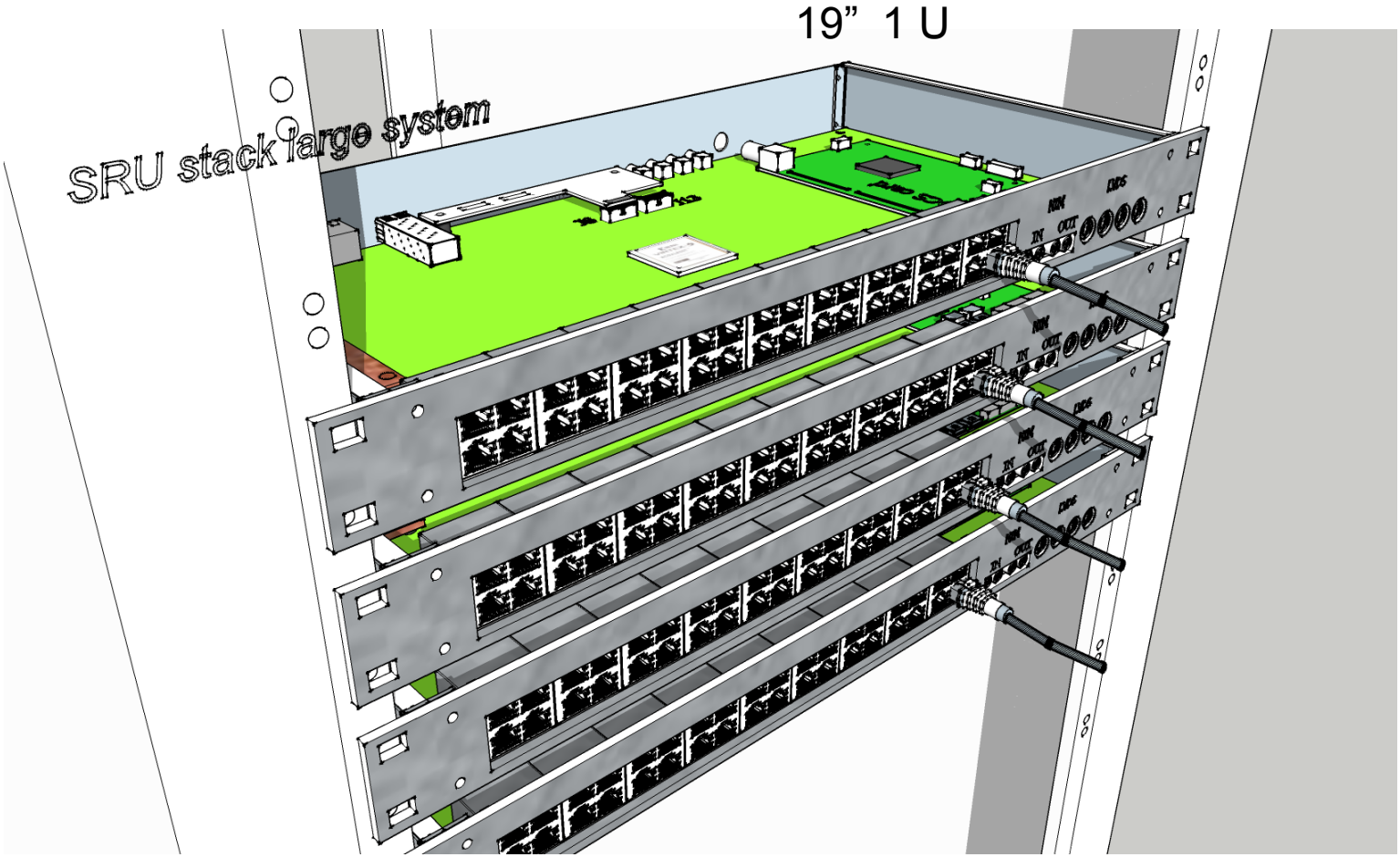
(design view of Allegro routed LCU by Intrasys, UK)



36 x copper DTC links to 36 FEC

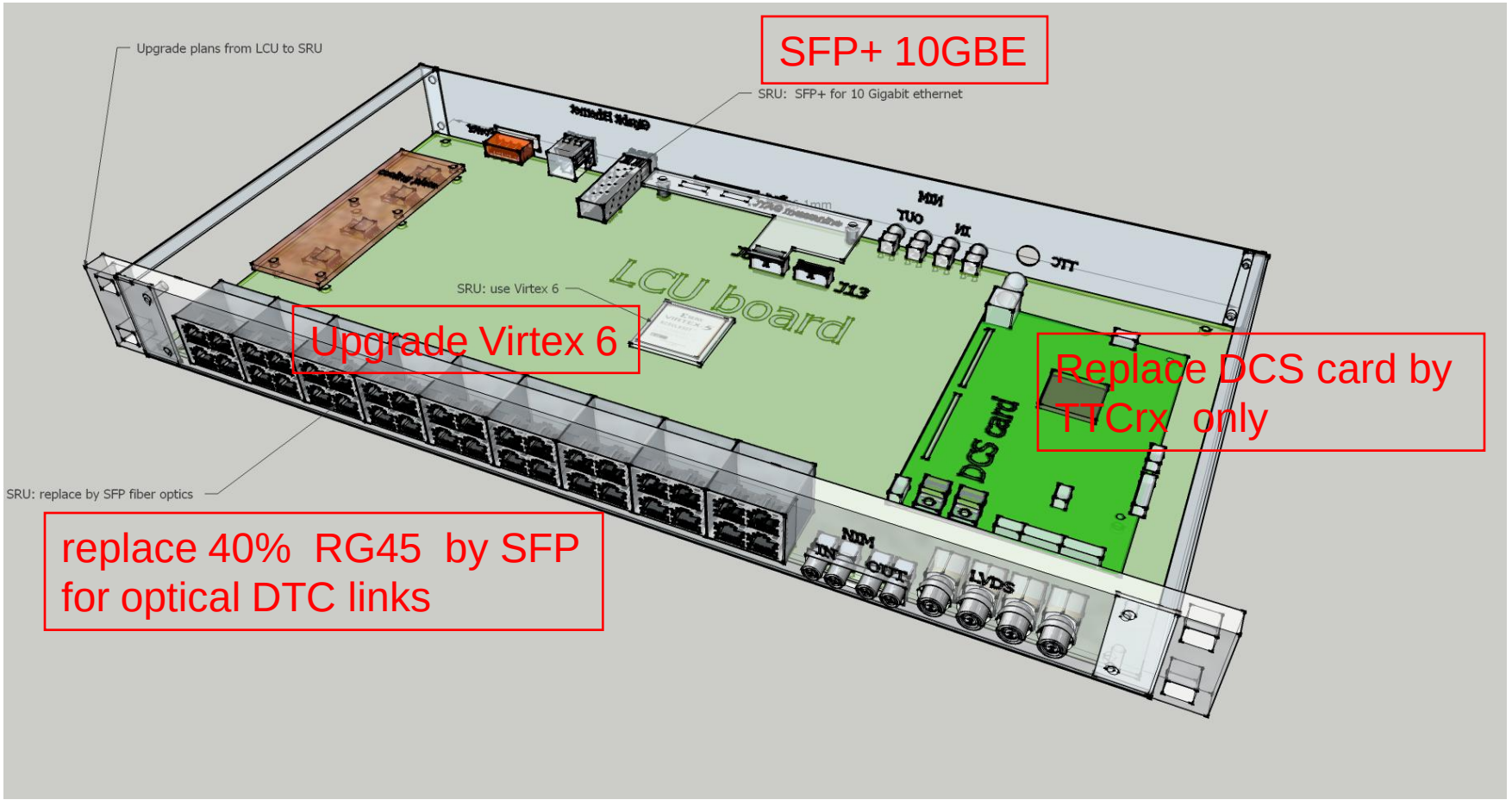
*LCU means LED control Unit since it was initially designed for the distributed ALICE EMCAL LED Control system

Large system (> 36 FEC cards)



Upgrade from LCU -> SRU

foreseen at CCNU after 1st experience with LCU early 2010



DTC link
data-trigger-control over single

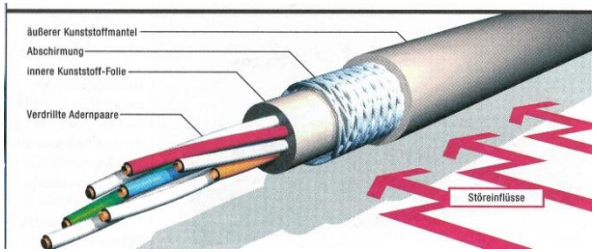
2 modes of operation defined by SRU clock: RO / CNTRL
FEC board controller senses clock to switch mode

Readout mode: clock = 40 MHz to FEC
data = 160 Mbit/s to SRU
3 streams trigger = select = readout-trigger to FEC
trigger = return = local trigger to SRU

Control mode: clock <= 4 MHz to FEC
data = Serial data out to SRU
1 stream select = Serial data in to FEC
return = coded status to SRU

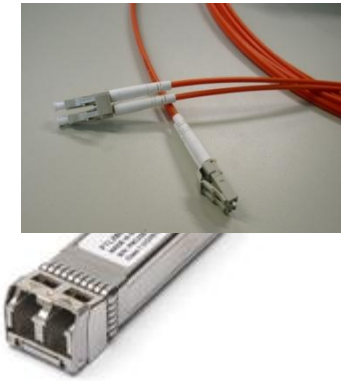
DTC links

a.) copper CAT -6 serial LVDS



4 x twisted pairs
CAT6 cable

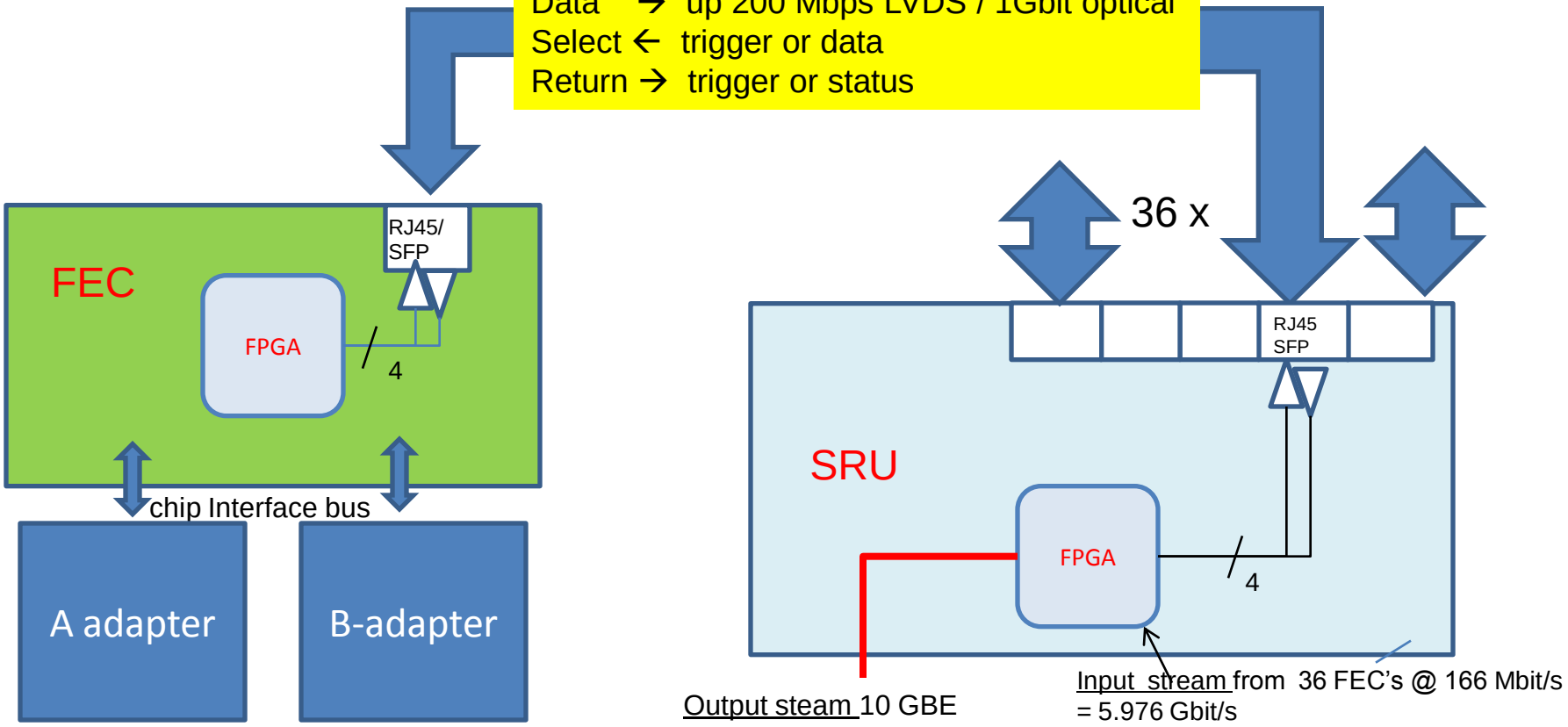
b.) MM fiber



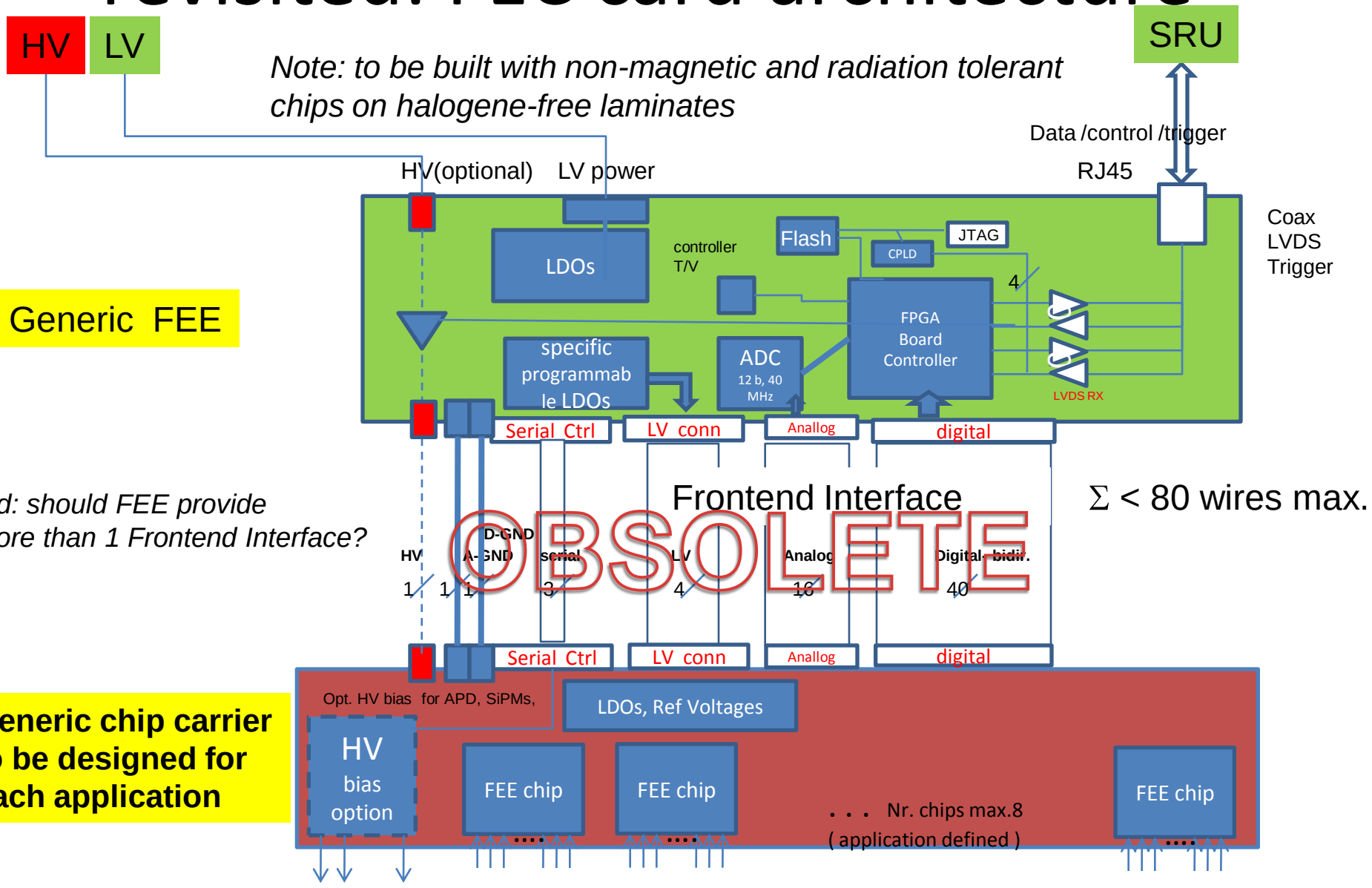
Note: 1st SRU has only copper

SFP RX/TX modules

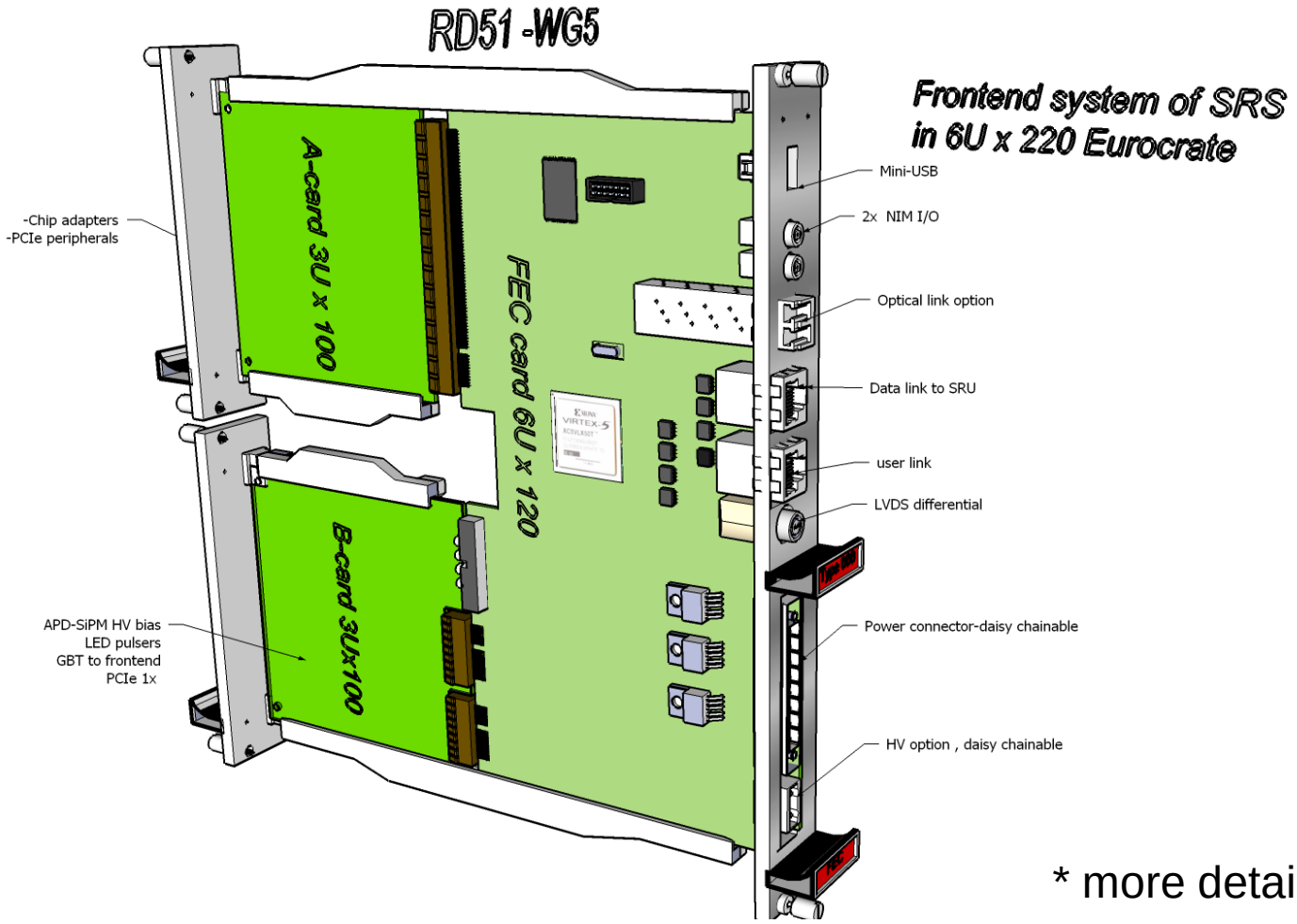
Clock ← 40MHz / 4 Mhz
Data → up 200 Mbps LVDS / 1Gbit optical
Select ← trigger or data
Return → trigger or status



revisited: FEC card architecture



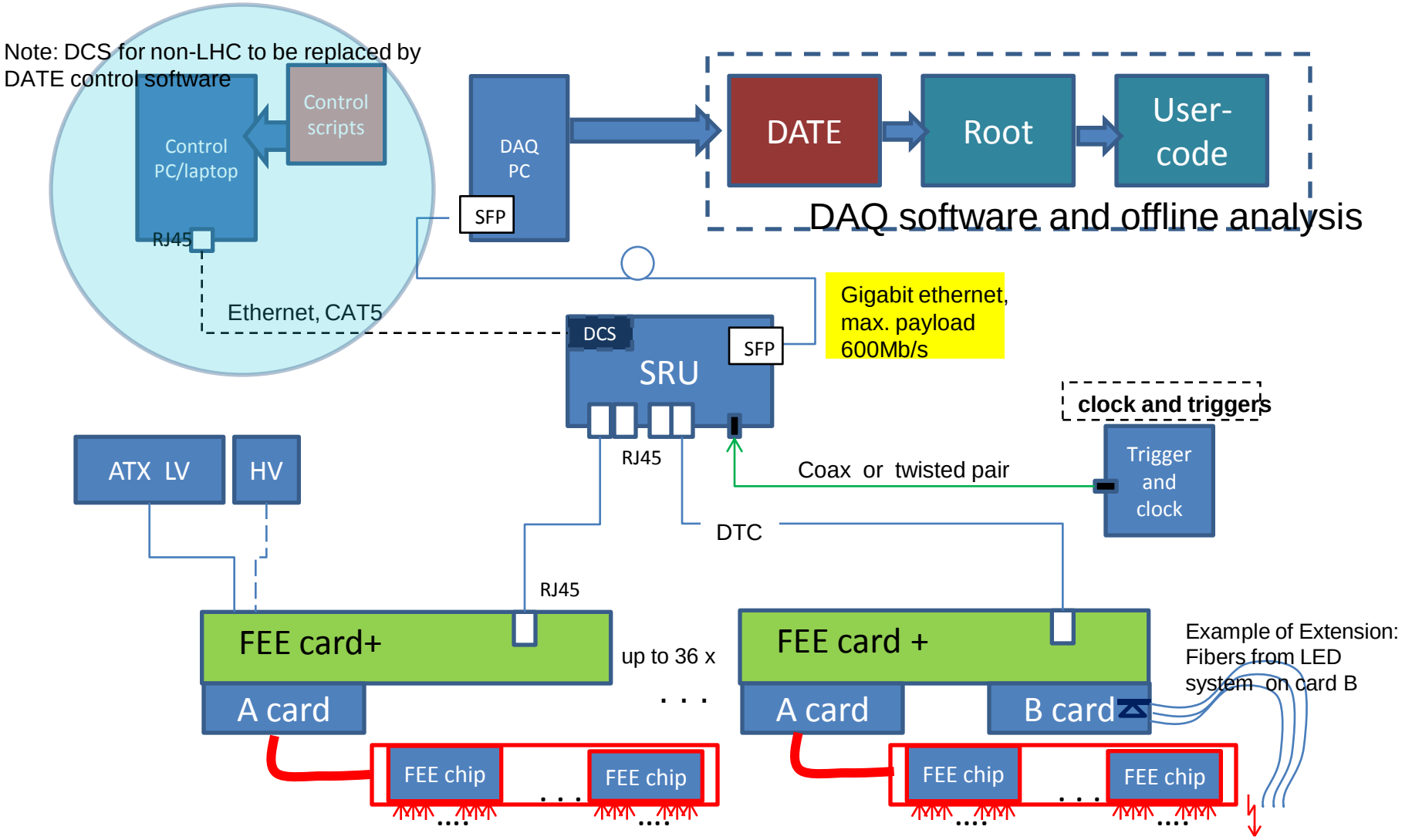
Solution: FEC card with adapters in Eurocard-format*



* more details see Valencia talk

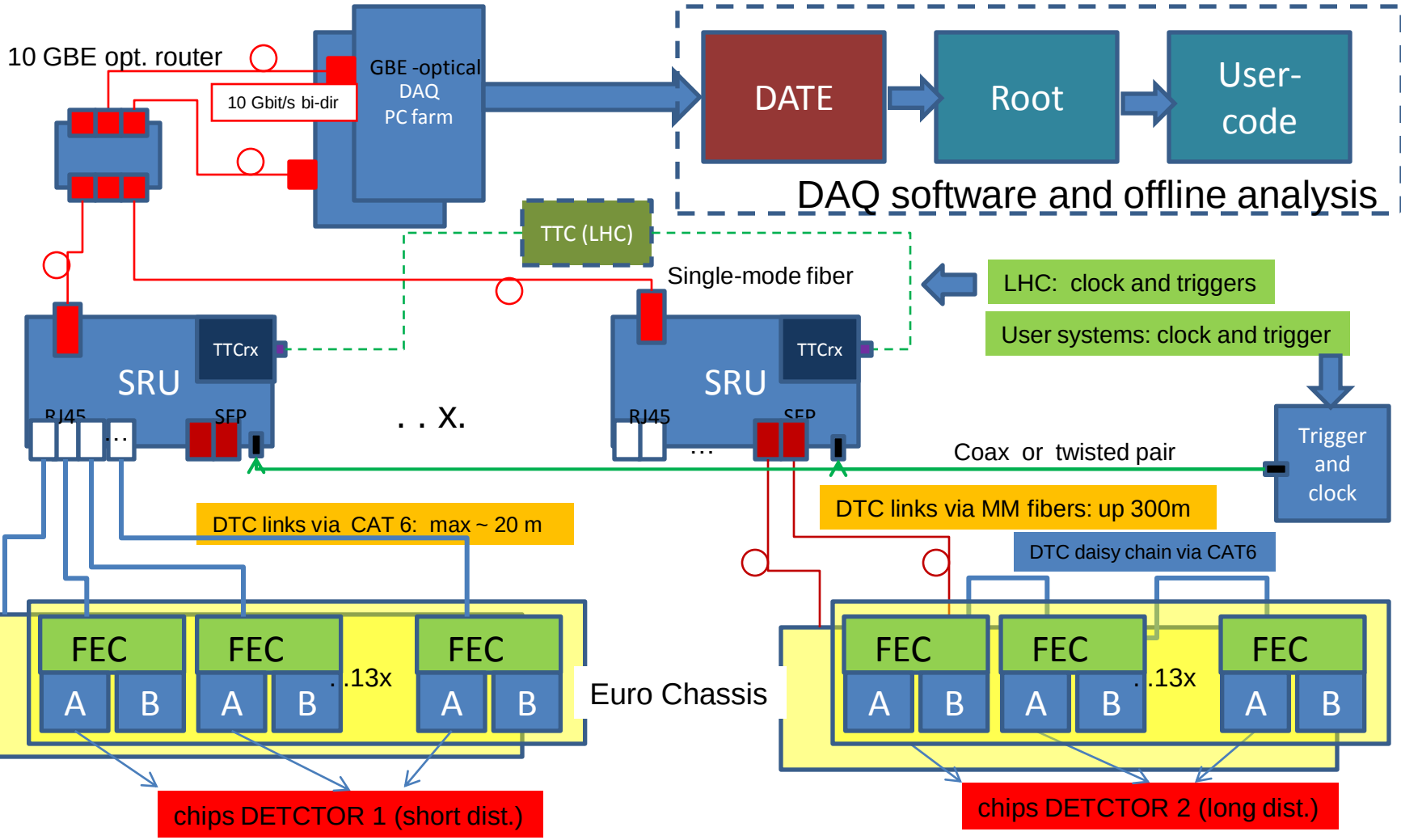
Small test system architecture

1 SRU, 1 GBE copper, User trigger+clock, DCS control



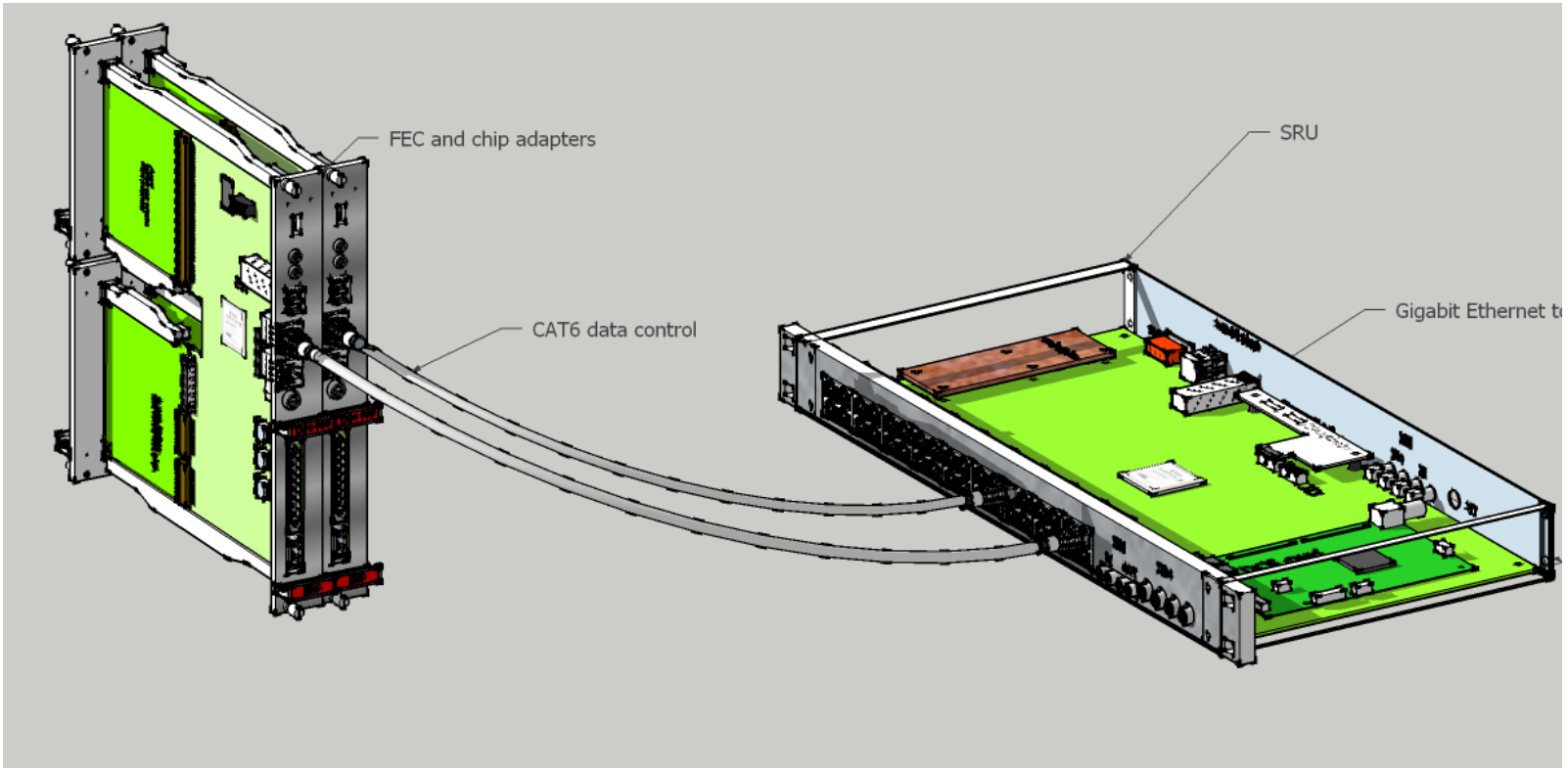
Large architecture (future)

n x SRU's, optical GBE router, TTC, Control via ethernet/DCS



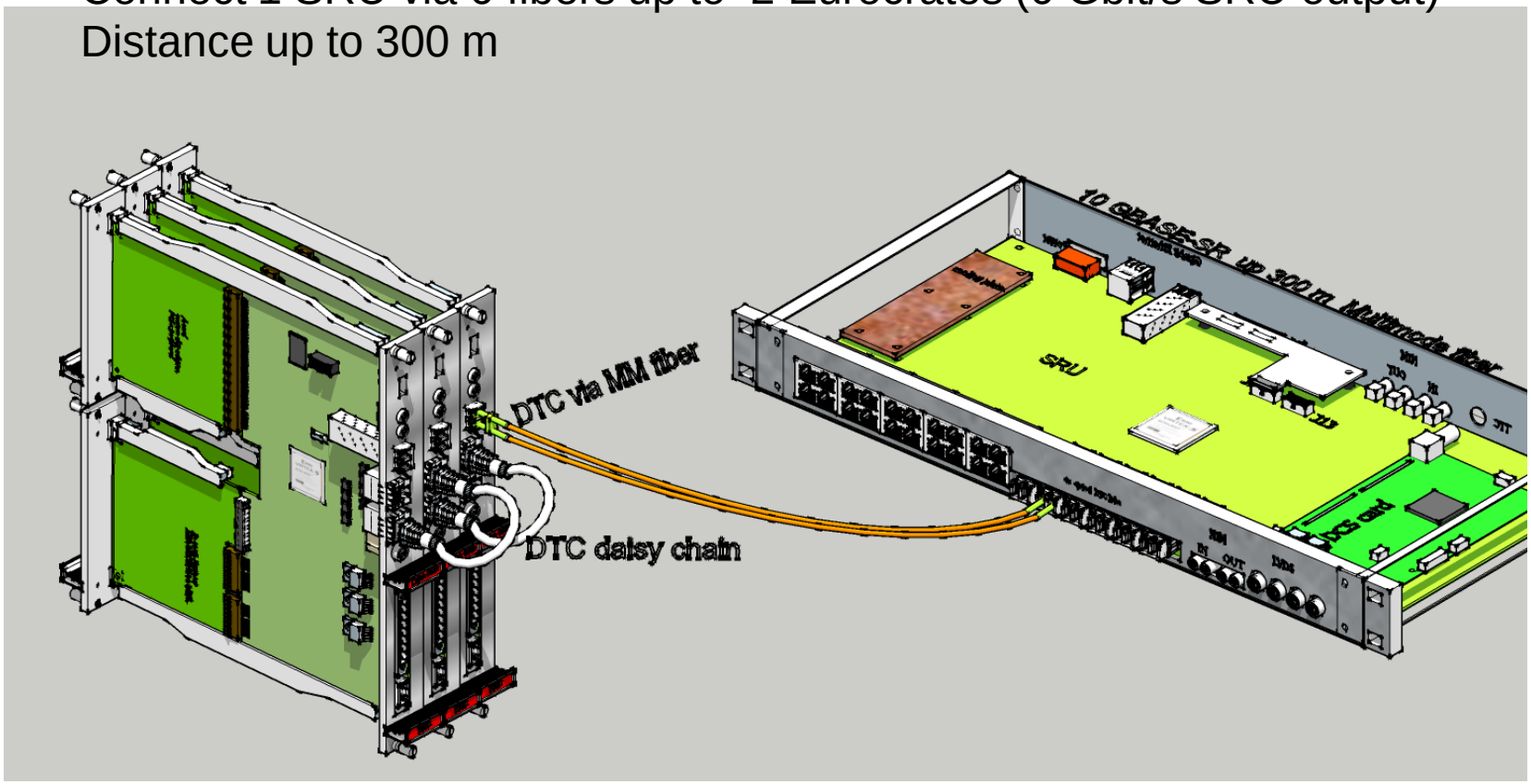
DTC links via CAT6 cable

Max 200 Mbit/s per cable
Connect 1 SRU up to 3 Eurocrates with 12 FEC cards each
Limitation: ca 20 m tbd (see Wuhan talk)



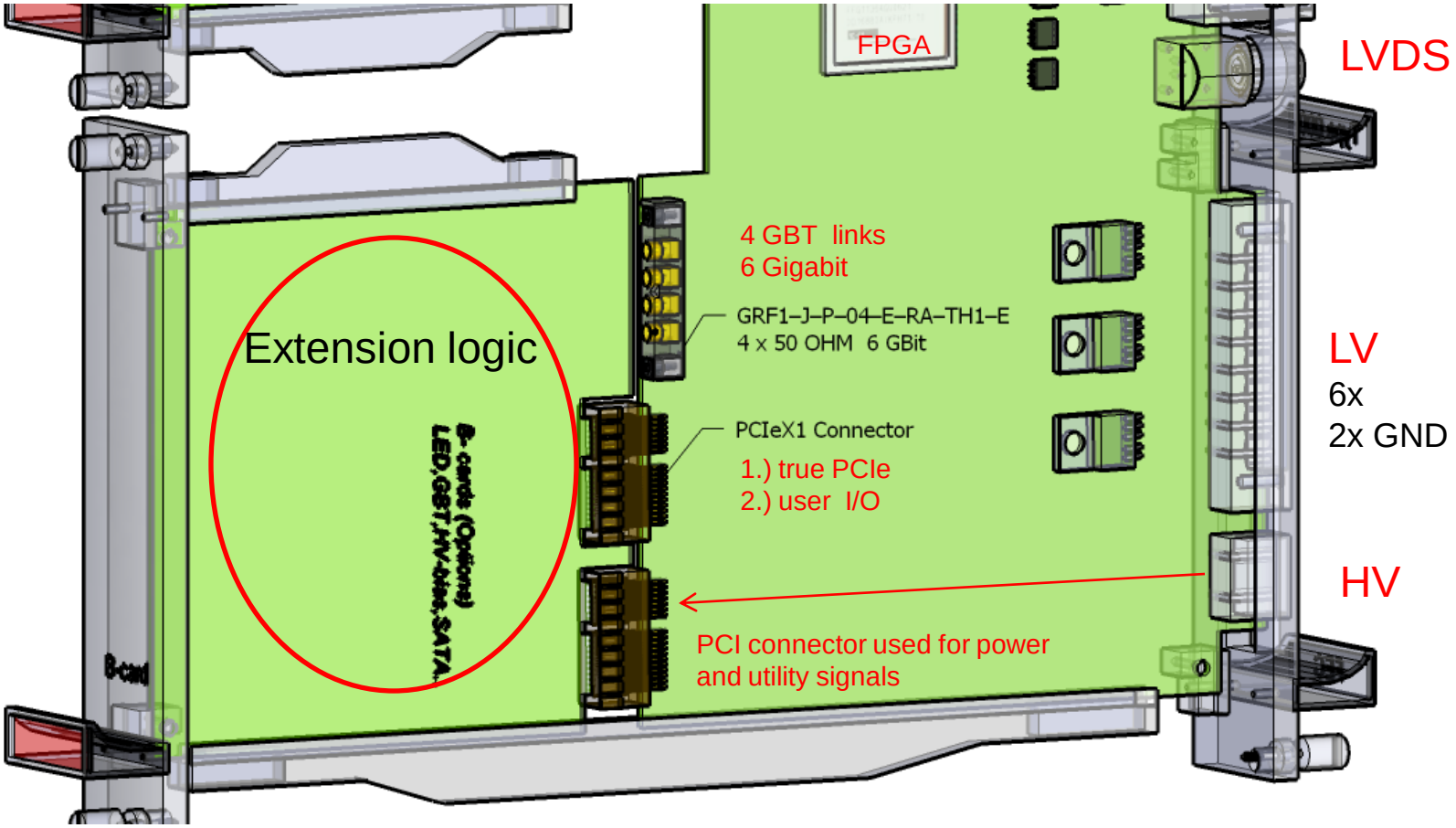
DTC via fiber

DTC fiber at 1 Gbit/s data rate to accomodate 1/3 Eurocrate (4 FECs)
Daisy chain (1Gbit/s) between FEC's via short CAT7 cables
Connect 1 SRU via 6 fibers up to 2 Eurocrates (6 Gbit/s SRU output)
Distance up to 300 m



Note: SRU will support mixed systems, copper and fiber

Extension Cards (B)



Extensions

Existing logic which can easily be ported

- HV bias 10 bit programmable for Si-PMs or APDs (up to 400 V)
- 1 ns, very high intensity light pulser, programmable over 64 ns range

Other possibilities: (see talk by S.Martoiu)

- Radhard GBT link to new frontend chips
- Triggerless systems buffer
- PCIe chips (Video, Sound, Image)

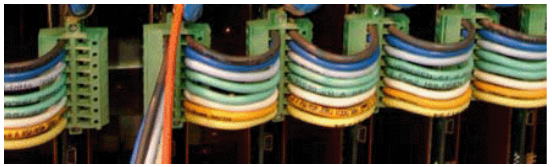
FEC system power

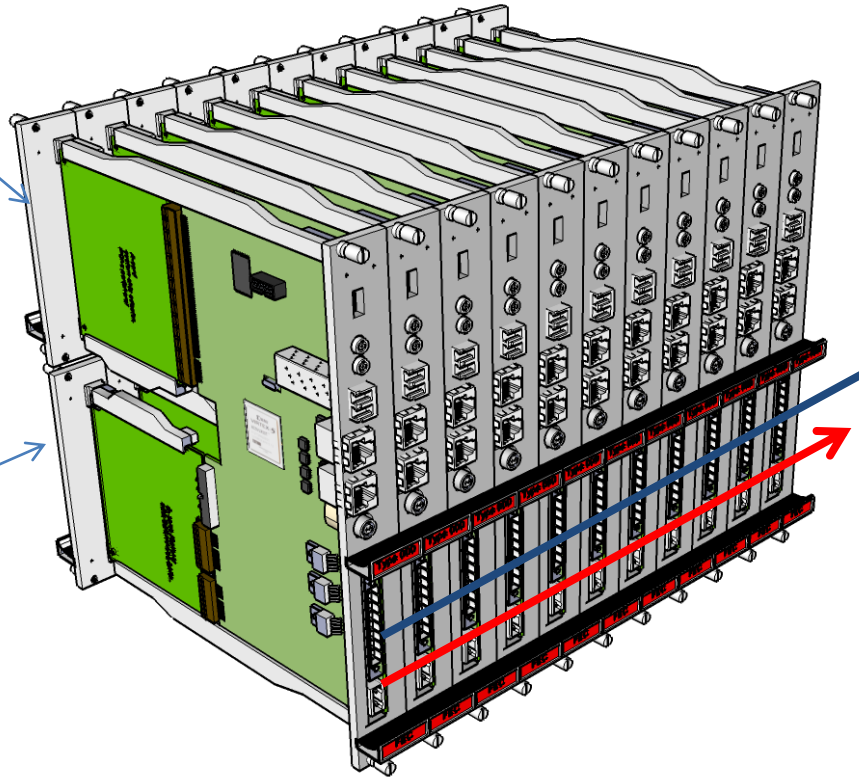
12 cards per FEC chassis

Frontend Chip carriers

Same Power Chain as PHOS/EMCal:

Daisy chained LV power to ATX supply





5 ATX Voltages 1 user defined

Daisy chained HV max 400V.

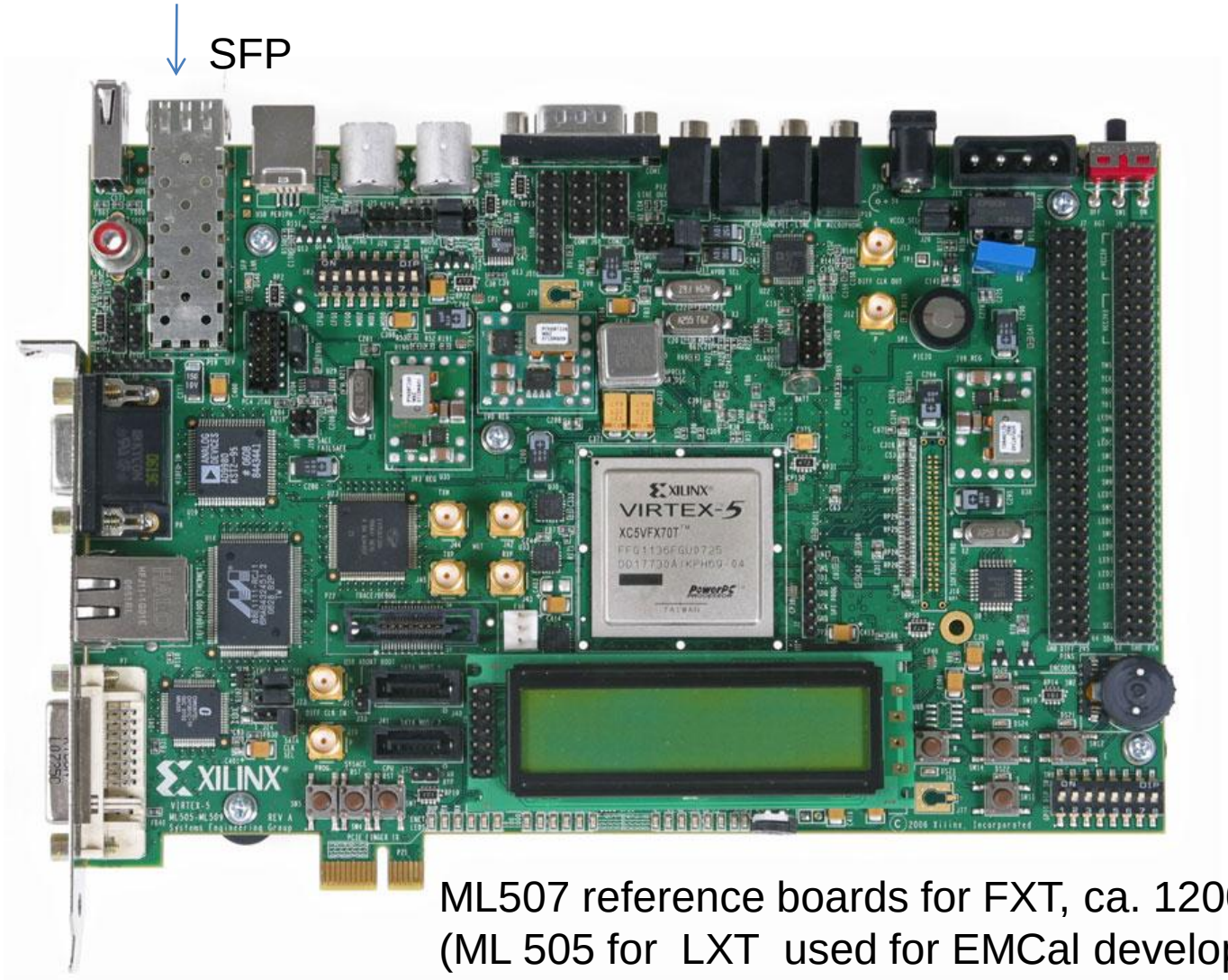
Extensions

Summary

- SRS evolved from proposal to ready-to-go
- First use (NEXT) planned for 2010
- Manpower reached critical mass
- Progress in all areas confirms optimistic timescale
- Porting of existing chip applications can start
- Extensions provide more possibilities

Backups

development platform already in use



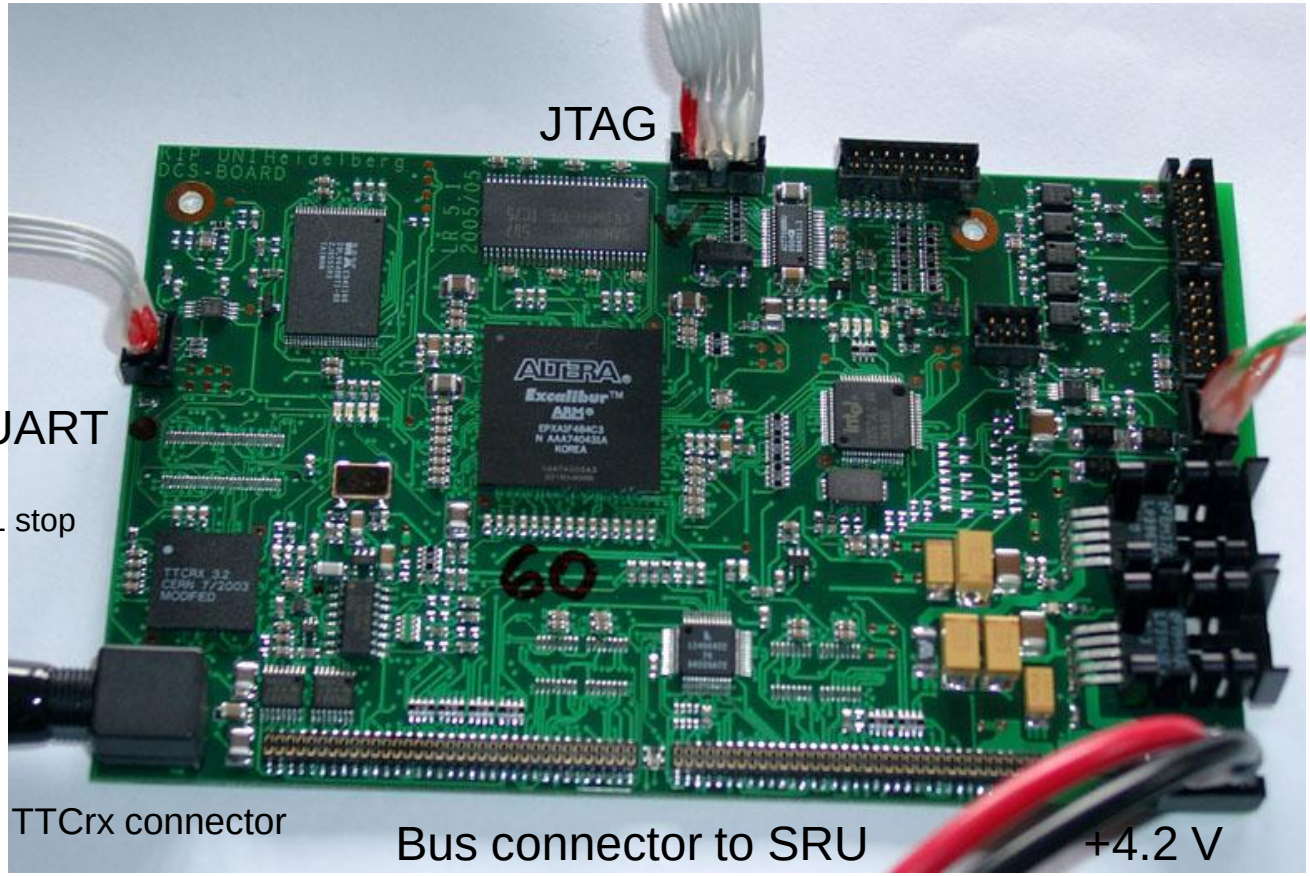
ML507 reference boards for FXT, ca. 1200 USD
(ML 505 for LXT used for EMCal development)

DCS card mezzanine (on SRU-1)

KIP Heidelberg

http://www.kip.uni-heidelberg.de/ti/DCS-Board/current/

Standard DCS node for ALICE detectors: contains also TTCrx receiver



RS232 terminal
Baud 5700, 8 bit, 1 stop
no parity

Micro-Linux in Altera FPGA
Control shell for memory-mapped 32 bit bus
Remote login and NFS mount via ethernet

Problem: procurement of TTCrx (only for LHC applications)