Chip Matrix

Past and Outlook for SRS

Sorin Martoiu, CERN, RD51

Classification

Analog chips:

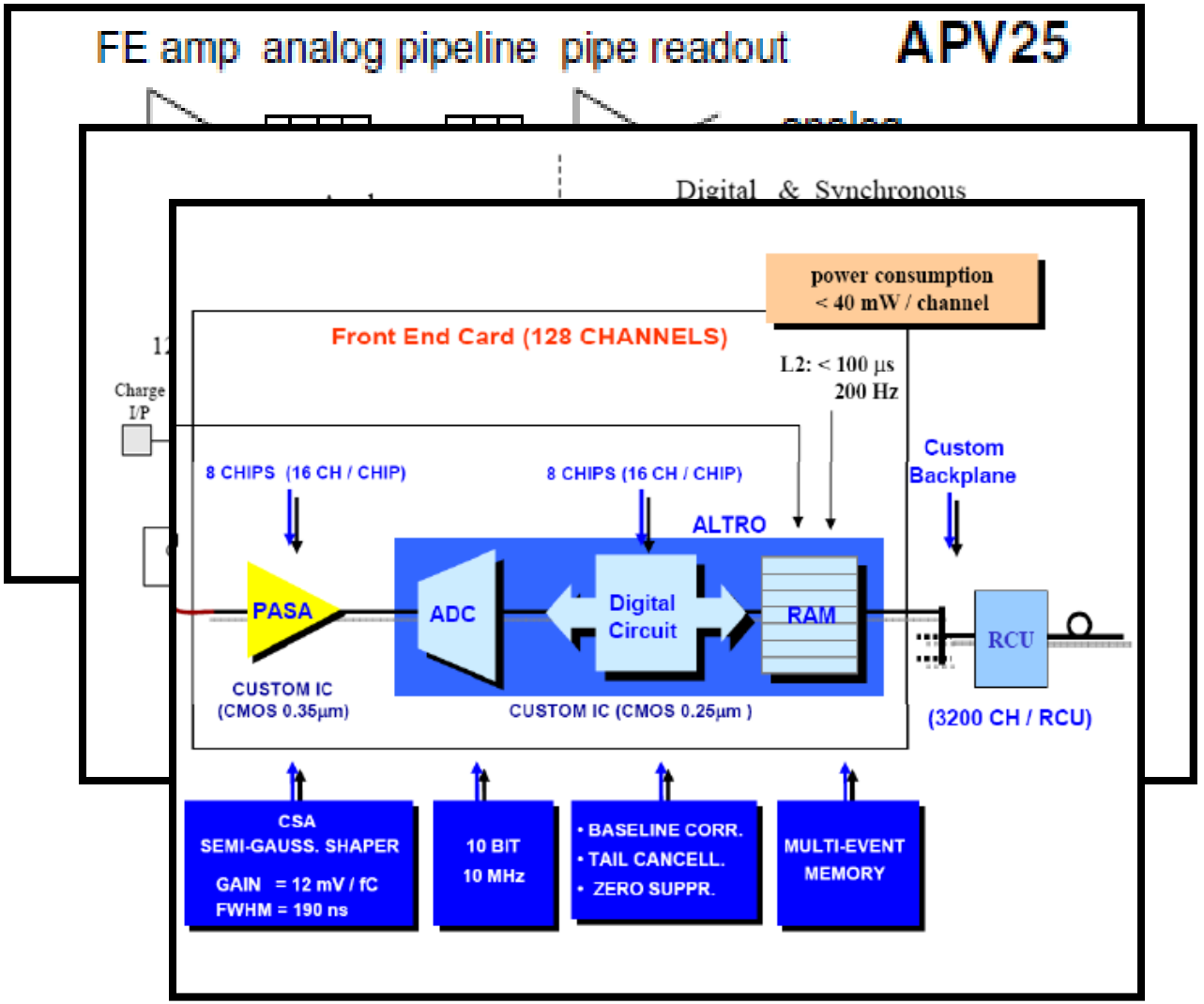
- APV25
- AFTER
- MSGCROC
- Beetle

Binary chips:

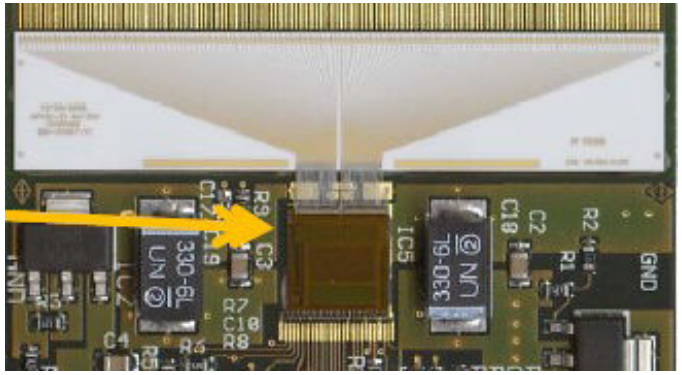
- VFAT
- NINO
- CARIOCA

ADC chips:

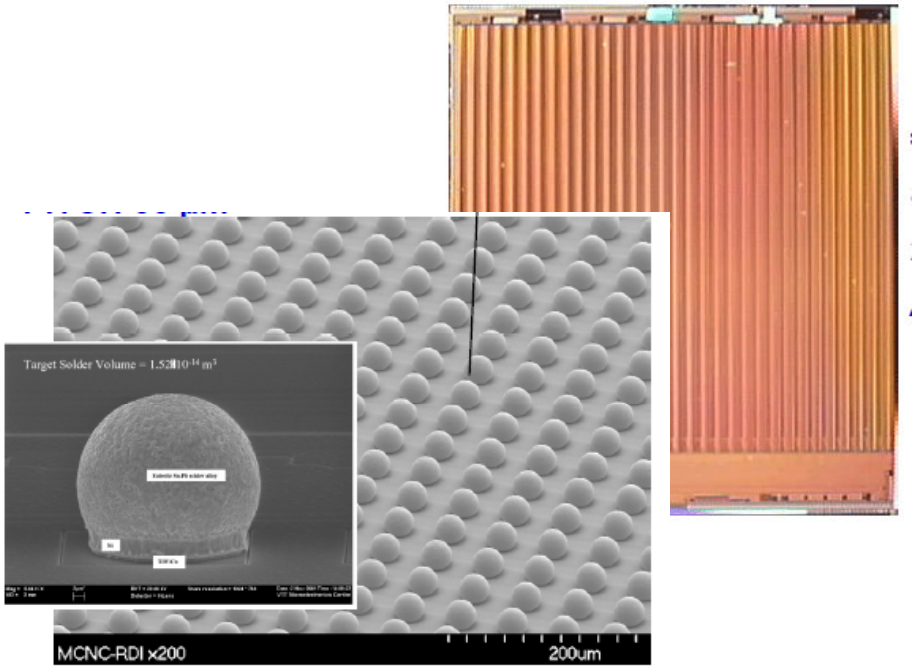
- PASA/ALTRO
- SALTRO
- SVX4
- SPIROC



Classification



Linear chips
(APV25)



Pixel chips
(MEDIPIX)

Name	Exp	Det	#ch	Shaper (ns)	Noise	Range (fC)	Pol.	ADC	f (MHz)	P/ch. (mW)	Feat.	Tech	Rad hard
APV25	CMS	Si strip	128	50	270+38e/pF	20	both	A	40	2.7	PD, PR	0.25 CMOS	10
AFTER	T2K	TPC	72	100-2000 s-gauss	(350-1800) + (22-1.8)e/pF	19	both	A	1-50 (100)	7.5	VG,VS	0.35 CMOS	no
MSGCROC	DETNI	Gas strip	32	T: 25 E: 85	2000e @ 40pF	800	both	A,1	2ns TDC		VG, ZS	0.35 CMOS	no
Beetle	LHCb		128	25	500+50e/pF	17.5	both	A/1	40	5.2	F-OR	0.25 CMOS	40
VFAT	TOTEM		128	22	650+50e/pF	18.5 (cal)	both	1	40	4.47	F-OR	0.25 CMOS	50
NINO	ALICE	TPC	8	1	1900+165/pF	2000 th<100	both	1	async	30	BR	0.25 CMOS	no
CARIOCA	LHCb	MWPC	8	<15 @ 220pF	2000+40e/pF	250	both	1	async	46	BR	0.25 CMOS	20
PASA+ ALTRO	ALICE TPC	TPC	16	190_{fwhm} s-gauss	570e @20 pF	160	both	10	20	< 40	BC, TC, ZS	0.35,0.25 CMOS	
SVX4	CDF, D0	Si strip	128	100-360	410+45e/pF	60fC	neg	8	106 (212)	2	ZS	0.25 CMOS	20
SPIROC	ILC, T2K	SiPM	36	A:25-175 T: 10	A: 1/11pe; T:1/24pe	2000 pe	neg	8-12	100ps TDC	0.025 *pulse*	dual-gain	0.35 SiGe	no

Legend: PD = peak detection, PR = pile-up rejection, VG = variable gain, VS = variable shaping, F-OR = fast-OR, BR = baseline restorer, BC = baseline correction, TC = tail correction, DC = data compression, ZS = zero suppression

Name	Memory	Mem type	L1 mem	Slow ctrl.	Data Out	A/D	Type	Freq.	Std.
APV25	192 analog	analog pipeline	10 ev.	I2C	frames	A	serial	20MHz	diff. current
AFTER	511 analog	Bucket wave sampling	n/a	serial (4 wires)	frames	A	serial	20-25MHz	diff
MSGCROC	4 ev.	analog + 14bit digital	n/a	I2C	events	A&D	A: serial D: 8bit bus	A: 32MHz D: 128MHz	A: diff D: LVDS
Beetle	160 s.	analog pipeline	16ev.	I2C	frames	A	serial 4 lines	40MHz	diff. current
VFAT	6.4us latency (256 s.)	SRAM	128 ev.	I2C	frames	D	serial	40 MHz	LVDS
NINO	n/a	n/a	n/a	n/a	discr. Output	D	parallel	async	LVDS
CARIOCA	n/a	n/a	n/a	?	discr. Output	D	parallel	async	LVDS
PASA+ ALTRO	<15 samples	latency	4(8) ev.	propietary	packets	D	parallel bus (40b)	40-60MHz	GTL
SVX4	46	analog pipeline	FIFO	serial bit stream	events	D	8b parallel	53	custom diff
SPIROC	16ev	analog	16ev SRAM	?	?	D	serial	5MHz	?

Pixel Chips

Name	#ch	Dim. (um^2)	Shaper	Noise	Range (fC)	Pol	ADC	Obs	P/ch (uW)	Tech	Rad hard
MEDIPIX-2	256x256	55x55	200ns	100e	16	both	1.5	photon-counting	7.6(a)	0.25 CMOS	0.3 MRad
TIMEPIX	256x256	55x55	90-180ns	100e	8 (lin) 32 (TOT)	both	1, TOT	ph-counting time energy	13.5	0.25 CMOS	no
MEDIPIX-3	256x256	55x55	100ns	72e	(8)	both	1-3	ph-counting color img	16.2	0.13 CMOS	yes
GOSSIP-2	16x16	55x55	30ns	70e	?	neg	1	1.8ns TDC	2	0.13 CMOS	no
GOSSIP-3	32x32	60x60	30ns	70e	5	neg	1, 8b TOT	1.73ns TDC	2	0.13 CMOS	no
GTK/NA62	40x45	300x300	5ns	2-300e	10	both	1	100ps TDC	1-2 mW	0.13 CMOS	yes

Future Chips

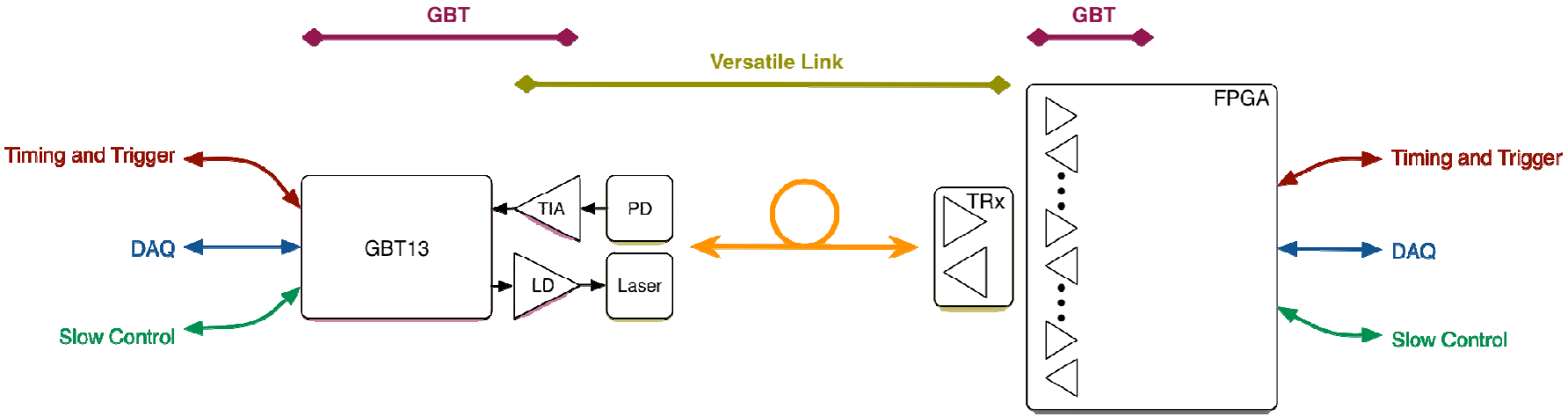
Name	Exp	Det	#ch	Shaper (ns)	Noise	Range (fC)	Pol.	ADC	f (MHz)	P/ch. (mW)	Feat.	Tech	Rad hard
S-ALTRO	ILC, T2K	TPC	32/64	30-120 s-gauss	270e @10pF 200+12e/pF	200	both	10	40 (160)	32-60	VG,VS, BC, TC, ZS	0.13 CMOS	no
CBC APV25 upg	CMS	Si strip	128	20	?	?	?	1	?	0.5		0.13 CMOS	yes
ABCNext	ATLAS	Si strip	128	25	<800e @ 5pF	10	both	1	40	3	ZS,DC	0.25 CMOS	yes
DIRAC2	ILC	uMega GEM/RPC	64	?	1fC @ 60pF	50-10pC	?	2	?	0.01 pulse	VG	0.35 CMOS	

Name	Memory	Mem type	L1 mem	Slow ctrl.	Data Out	A/D	Type	Freq.	Std.
S-ALTRO	?	?	?	?	packets	D	4b bus	160MHz	LVDS
CBC APV25 upg						D	**GBT e-port**		
ABCNext	256x128	digital pipeline	42 ev. (x3 s.)	?	?	D	serial	<160MHz	?
DIRAC2	?	?	?	?	packets	D	4b bus	160MHz	LVDS?

GBT - high speed bidirectional radiation hard optical link

- Bidirectional data transmission
  - Data Readout
  - TTC
  - Slow control and monitoring links
- Bandwidth:
  - Line rate: 4.8 Gb/s
  - Effective: 3.36 Gb/s

- Radiation tolerant chipset
  - GBTIA: Transimpedance optical receiver
  - GBLD: Laser driver
  - GBTX: Data and Timing Transceiver
  - GBT-SCA: Slow control ASIC
- GBT-FPGA IPs
  - Xilinx Virtex-4FX
  - ALTERA StratixII GX



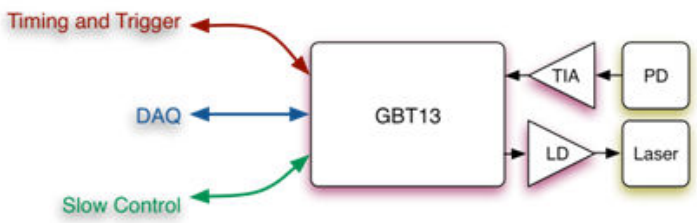
On-Detector
Custom Electronics & Packaging
Radiation Hard

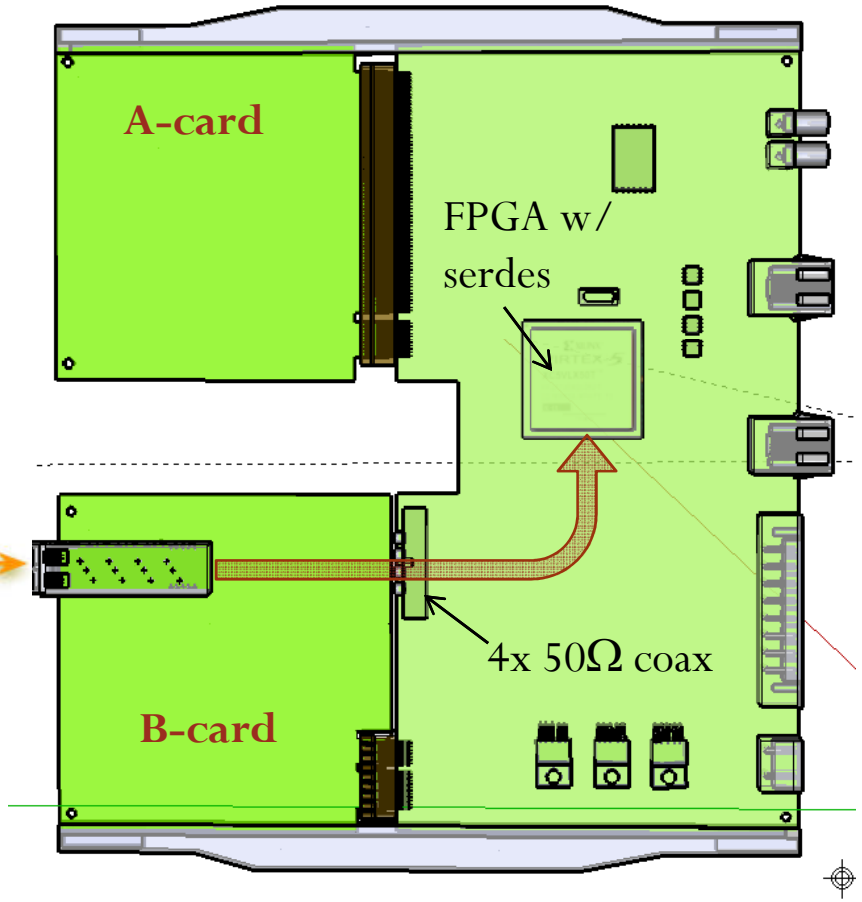
Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

http://cern.ch/proj-gbt; Paulo Moreira, CERN PH-ESE

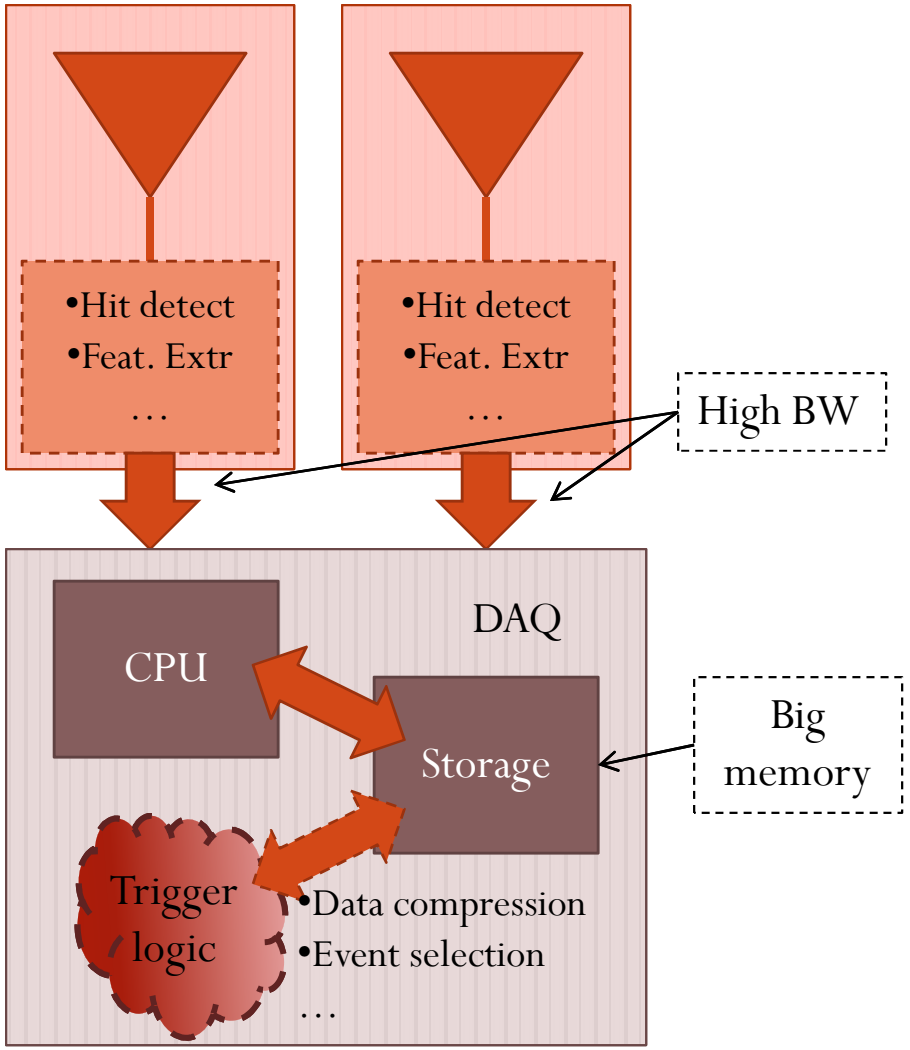
FEC GBT option

- Virtex5 RocketIO Transceivers:
  - LX – GTP 3.75Gbps
  - FX – GTX 6.5Gbps





Trigger(less)



If:

- Very long trigger latency
- Very complex trigger logic
- Physics dependent trigger logic
- Event rate too high

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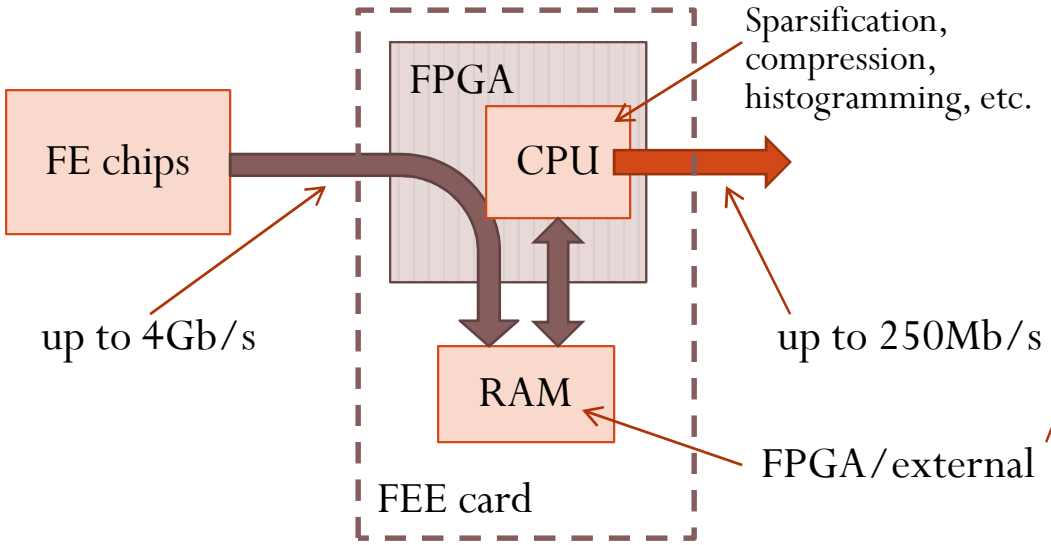
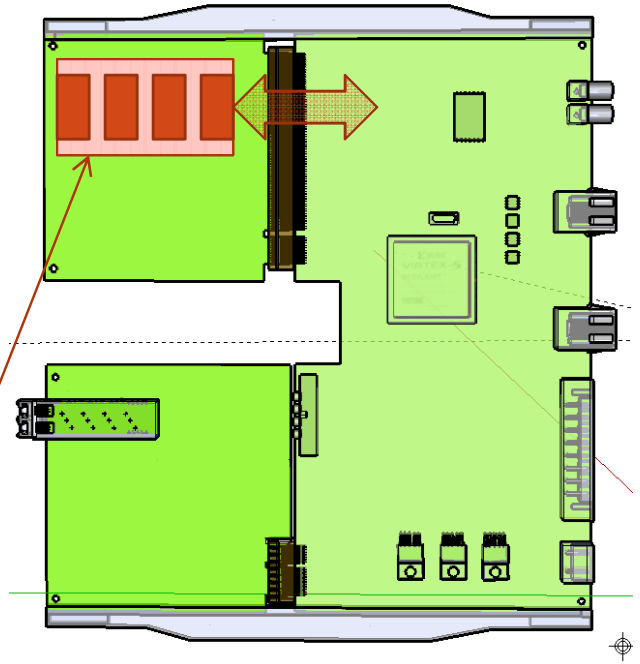
Some examples:

- ILC: burst of collisions at a rate of 2.6MHz over 1ms followed by 200ms without any interaction.
  - dead time free pipeline of 1 ms,
  - no hardware trigger,
  - front-end pipeline readout within 200 ms and
  - event selection by software.
- PANDA, CBM: triggerless FEE, data-push arch
- NA62: ~1GHz beam rate, 5s spill
  - Some FE operate triggerless
  - Events are selected inside DAQ

Triggerless option





- GTK/NA62 example:
  - inter-spill processing: 100MHz/chip x 4B x 5s = 2GB
  - on-line processing: 100MHz/chip x 4B x 5ms = 2MB

spill duration

trigger latency

Thank you