Status and planning on common readout system of RD51

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Introduction

Huazhong Normal University joined the RD51 group in July,2009. We join mainly in Scalable Readout System (SRS) group as proposed by Dr. Hans Muller.

Our interests:

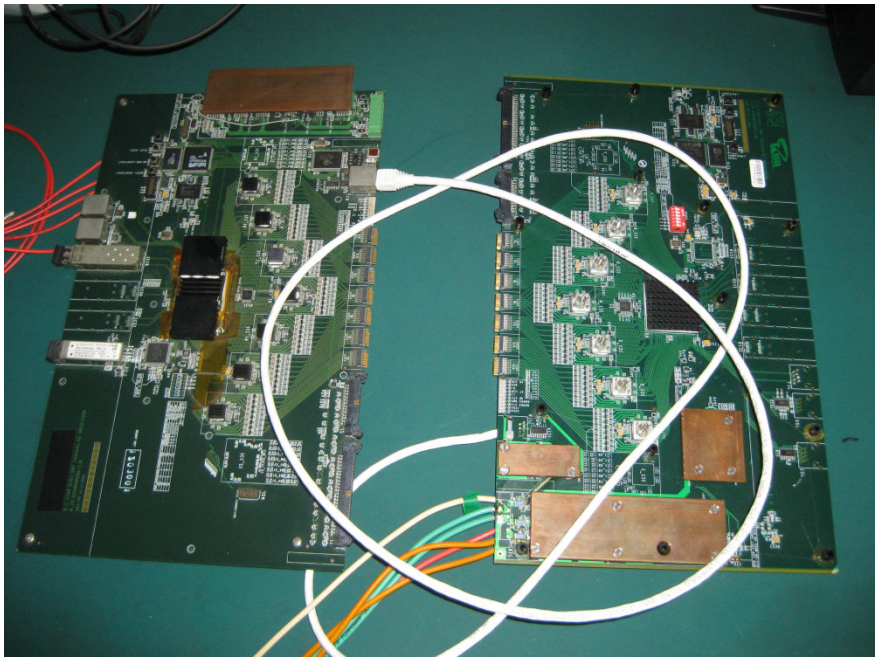
- Design the CAT6 data and control linl protocol of the SRS
- Design the Board Controller firmware for FEC and SRU
- Design ALTRO and APD bias cards for the FEC crate

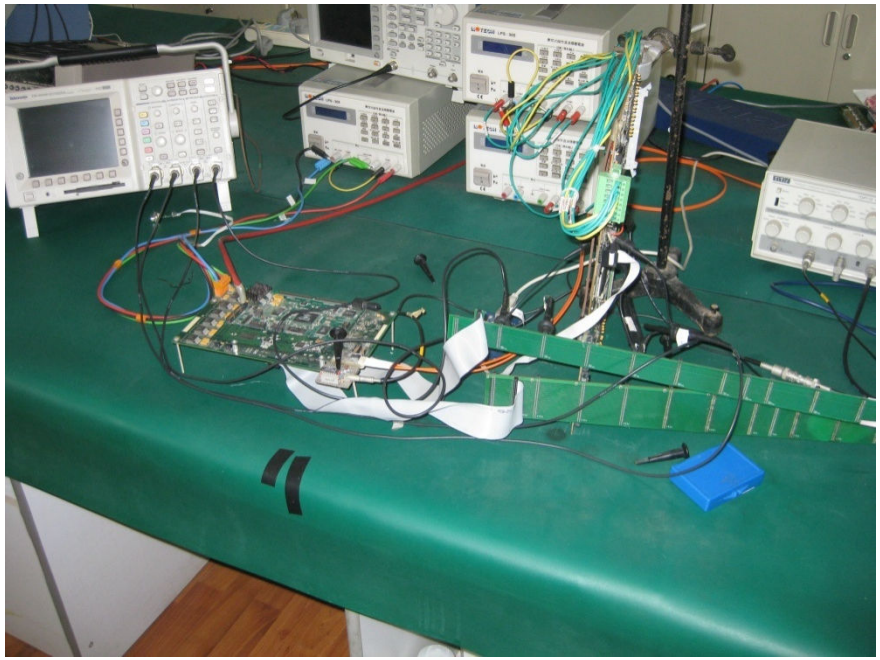
Experiences

1. Participation in desgin and full production of the FEC for ALICE/PHOS
2. Participation in RCU firmware upgrade for ALICE/TPC
3. Design and commissioning of Board Controller firmware for ALICE PHOS and EMCAL
4. Design of Virtex-based trigger algorithm and trigger data readout for ALICE/PHOS

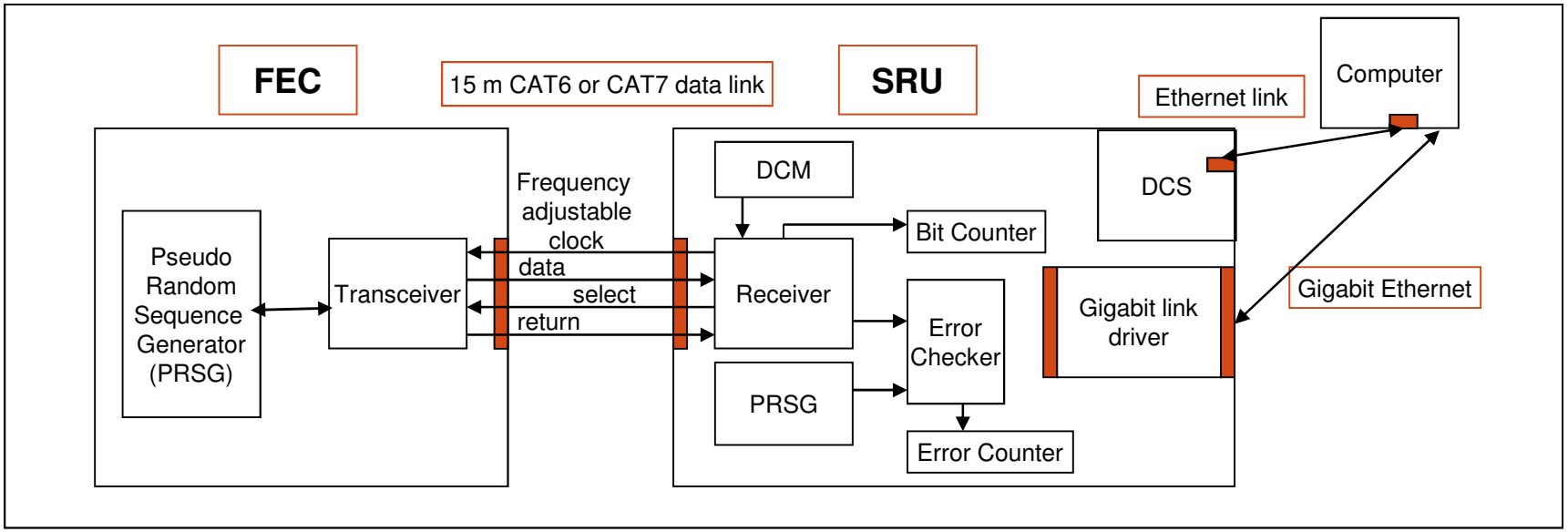
CAT6 data link testing platform

- Firstly, we will test the performance of CAT6 cable via two Virtex-2-pro FPGA card.
- We are ordering ML505 xilinx development board. Then we will test the CAT6 data link on Virtex5-LXT based development board ML505.





CAT6 data link test setup

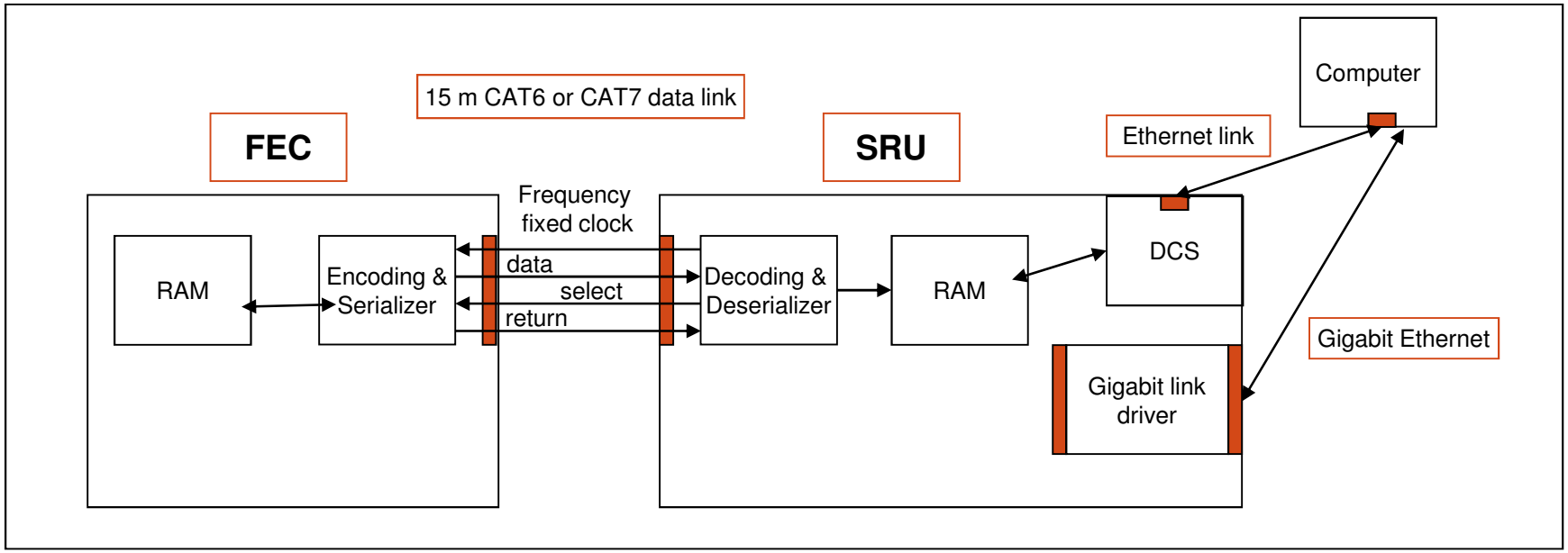


- ***Test aims***
  - Validating the stability of the CAT6 data link.
  - Test the maximum bandwidth cable length ratio for CAT6 and CAT7 cables.
- ***Note***
  - The clock frequency can be adjusted by SRU which controlled by DCS.
  - Pseudo random sequence generator uses Galois or Fibonacci configur

  -ation to generate data sequence.

- ***Test procedure***
  - SRU and FEC reset
  - SRU asserts the select line.
  - FEC starts its transceiver, sends a *SYNC* packet, starts the *PRSG*, and then sends the pseudo ramdom sequences.
  - SRU also starts its PRSG after received the whole *SYNC* packet.
  - The Error Checker checks bit error, and the Error Counter counts how many times the bit error occurs. The bit error counter can be read via DCS.

Frame encoding & decoding test setup



- ***Test aims***
  - **Validating the Frame encoding & decoding algorithm.**
  - **Test the stability of the CAT6 and CAT7 data link when applied Frame encoding & decoding algorithm.**
- ***Note***
  - **The clock frequency is fixed and it is determined by the result of CAT6 and CAT7 data link test.**

- ***Test procedure***
  - SRU and FEC reset
  - Write data of ***in.dat*** file into the RAM of FEC
  - SRU asserts the select line.
  - FEC starts the Encoding and Serializer FSM and then sends the data stream to SRU.
  - SRU receives data stream from FEC, deserializes and decodes the data, and then writes the data into the RAM of SRU.
  - Read the RAM of SRU via DCS and write it into ***out.dat*** file
  - Compare the contents of ***in.dat*** and ***out.dat*** files.

Protocol layer

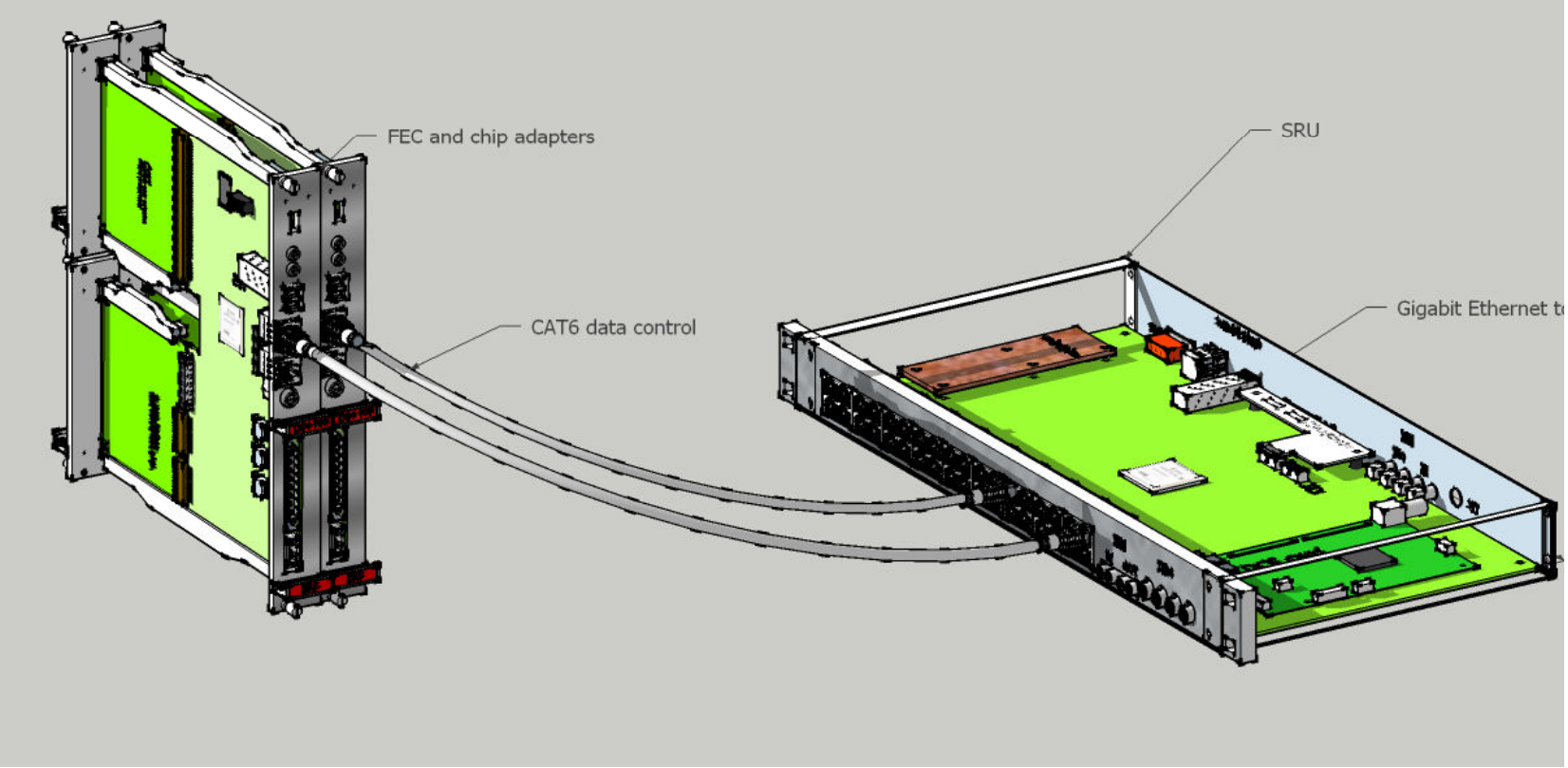
Frame Format						
SYNC	SOF (Start of the Frame)				DATA	
0xAAAA5555	PID	ADDR	LENGTH	CRC	N DATA	CRC

- ***SYNC*** : All packets begin with a synchronization which will be used by the receiver to align the incoming data.
- ***PID*** : Packet idenfier consists of a four-bit packet field followed by a four-bit check field.
- ***ADDR*** : Specifies the data source/destination addresses, 32 bits.
- ***LENGTH*** : Specifies the length of the data field in DATA packet.
- ***CRC*** : Cyclic redundancy checks (CRCs) are used to protect all non-PID fields in SOF and DATA packet.
- ***N DATA*** : a data field contains LENGTH bytes of data.

- ***Other Consideration :*** Try to apply asynchronous protocol with Handshake packet.

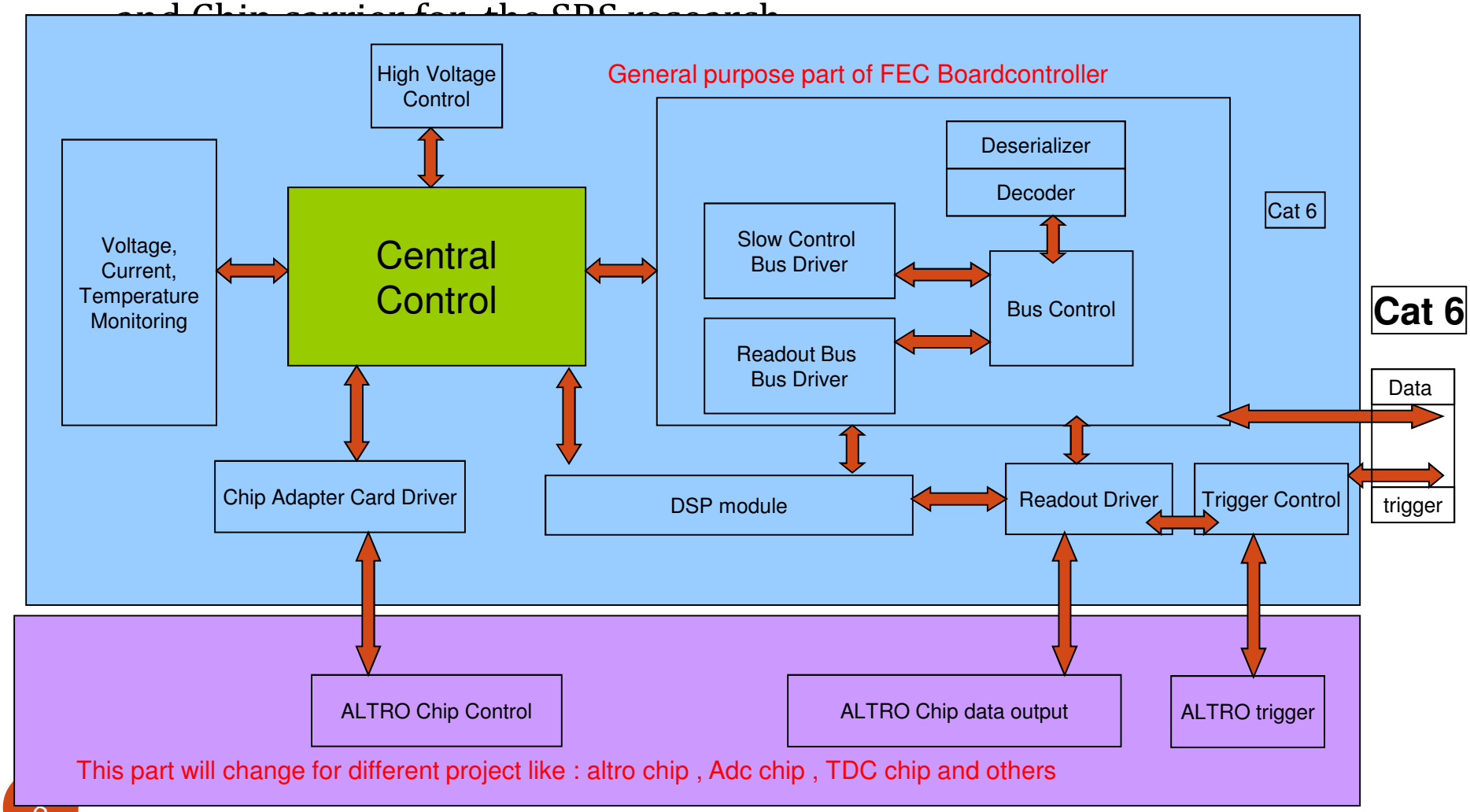
FEC first prototype design

- We will design the ALTRO chip adapter card A and the APD voltage bias controller card B, both based on PHOS FEC for the SRS system.
- We will provide the data and control link between SRU and FEC
- We are also interested in design of the final SRU.



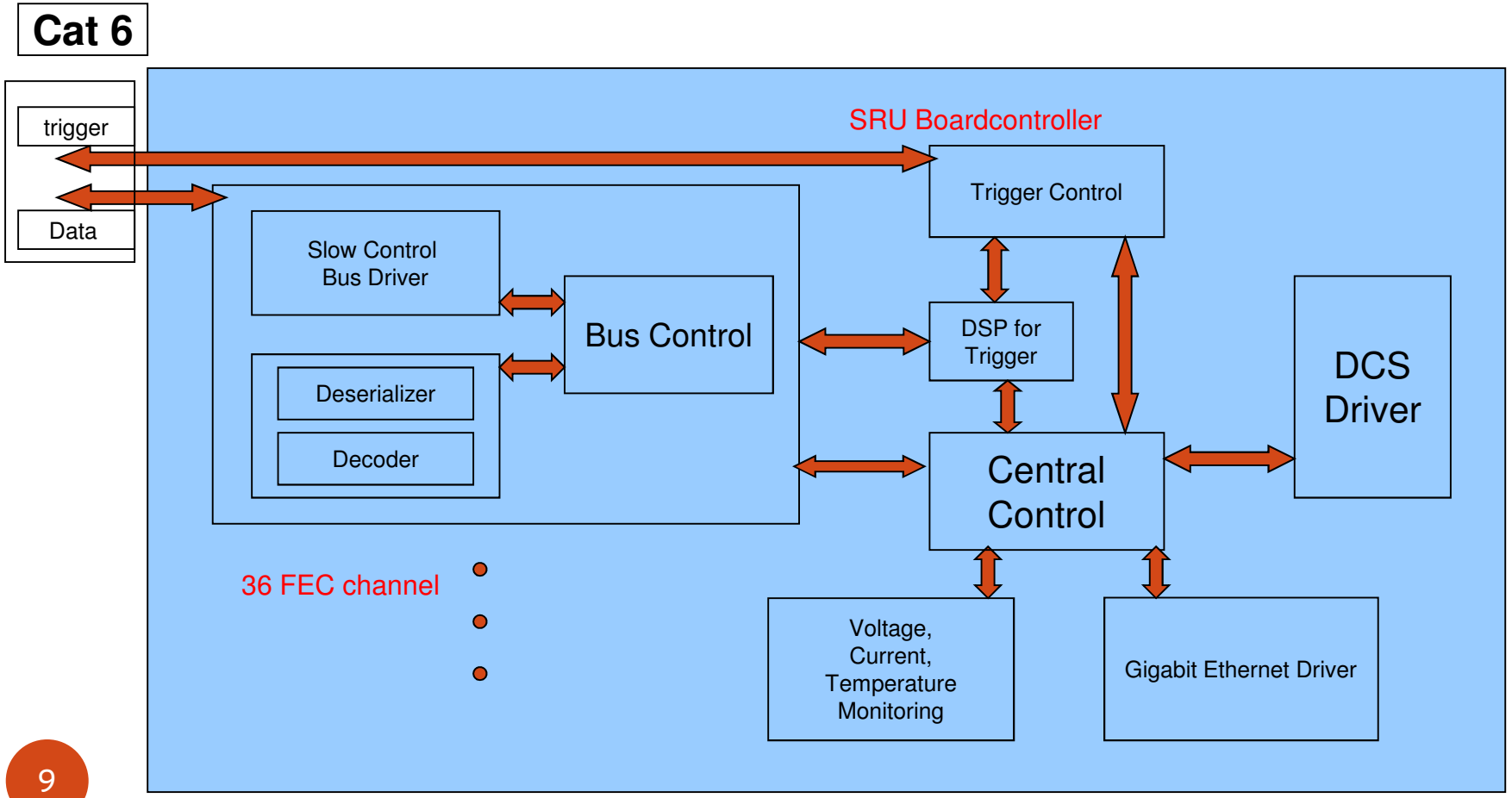
Board Controller of FEC

- Board Controller design is based on PHOS and EMCAL BC code, which was developed by Huazhong Normal University and is suitable for the New FEC and Chip carrier for the SRS research



Board Controller for SRU

- We will develop the Board controller for the SRU card and also be interested in design of the final SRU card.



Thank you for your attention!