

# Towards the scalable readout system: FEC electronics for APV25, AFTER and Timepix

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# Outline

- **A summary of front-end ASIC interface requirements**
- **A flexible interface front-end card (FEC)**
- **A-card application examples**

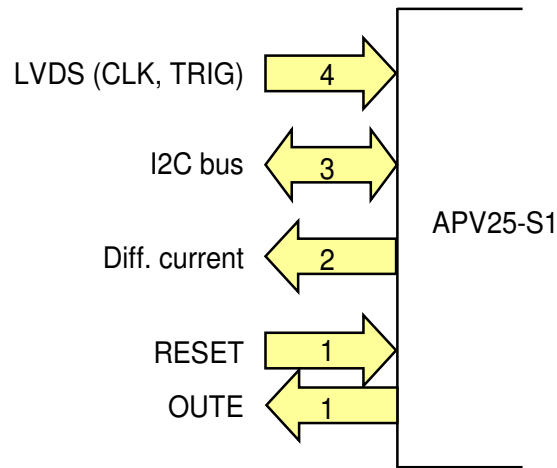
# A summary of front-end ASIC interface requirements

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## APV25

Info: "APV25-S1 User Guide Version 2.2", L. Jones (RAL), 5th Sept. 2001.

[http://www.te.rl.ac.uk/med/projects/High\\_Energy\\_Physics/CMS/APV25-S1/pdf/User\\_Guide\\_2.2.pdf](http://www.te.rl.ac.uk/med/projects/High_Energy_Physics/CMS/APV25-S1/pdf/User_Guide_2.2.pdf)



A possible interface to a chip carrier may consist of:

- One analog differential signal input per APV25 chip
- Two LVDS output pairs (clock, trigger)
- One I2C bus (three lines)
- Two additional CMOS I/Os (optional?)

Analogue signals must be sampled at 40 MHz

Signaling levels related to  $\pm 1,25V$  above bias level (GND)

A **voltage level translator** and **isolation circuit** is required to:

- Optically couple the slow signals (I2C bus)
- AC couple the fast signals (clock, trigger)
- Perform **I/V conversion** to 2 Vpp range and **AC coupling** for analog current outputs

Alternatively, optical transceivers can provide the required isolation.

# A summary of front-end ASIC interface requirements

## TIMEPIX

*“TimePix manual v1.0”, X. Llopart, CERN, Aug. 2006”*

A possible interface to a chip carrier for serial readout may consist of:

- |   |   |
|---|---|
| <ul style="list-style-type: none"><li>• 6x LVDS pairs:</li><li>• 6x 2.2V CMOS output signals:</li></ul> | <ul style="list-style-type: none"><li>enable in&amp;out, fclock in&amp;out, data in&amp;out</li><li>reset, shutter, mo, m1, polarity, enable_tpulse</li></ul> |
|---|---|

Signaling levels related to +2,2V power. So, **level translators** are needed in the FEC.

...though we would need more signals to...

- To allow pixel calibration we need 1xCMOS out, 1x **analog out**, 1x **calibration generator**
- To allow chip's internal DAC monitoring, we need 1x **analog input** per chip
- To substitute any of the TIMEPIX internal DACs, we need **1x analog out**
- To allow the test of (121,0) and (122,0) special pixels, 1+Nx8 more signals are needed

# A summary of front-end ASIC interface requirements

## **TIMEPIX readout via MUROS2**

*“MUROS2 User’s manual”, D. San Segundo Bello, NIKHEF, Jul. 2003*

The FEC can replace the National Instruments DIO-653X card. This requires 32 I/O lines:

- 15 control lines (3.3V TTL/CMOS)
- 1 CLOCK signal (3.3V TTL/CMOS)
- 16-bit Data bus (3.3V TTL/CMOS)

Additional signals are optional and include a shutter signal, a shutter monitor signal and an external clock (to override the MUROS2 board clock)

FEC should also provide +5V power (max. 1 A). This is not really required, as the MUROS2 board can use an additional +5V input.

We may also need an **analog multiplexer** to switch between 2 **DAC outputs** to produce sharp transitions.

# A summary of front-end ASIC interface requirements

## AFTER readout via T2K electronics

*“T2K TPC Read-out Electronics Digital Front-End Mezzanine Card”, Denis Calvet, CEA Saclay, Jul. 2008*

T2K’s front-end card –named FEC- has 4 AFTER chips and a 4-ch AD9229 ADC.

This board is designed to interface a FEM module using 43 signals + power and ground and a FX2CA-80P-1.27DSAL connector from Hirose (FEM side):

- 8 LVDS pairs
- 17 CMOS 3.3V outputs
- 5 CMOS 3.3V inputs
- 2 CMOS 3.3V bidirectional signals


Some of these signals would require **special circuitry** in the FEC (like tie to ground, pull-up or pull-down resistors, or R-2R summing circuits to produce voltage steps)

# A summary of front-end ASIC interface requirements

## Summary (signal directions seen from FEC)

Type	AFTER T2K card	TIMEPIX	MUROS2	APV25	ADC card
LVDS.IN	6	3	-	-	-
LVDS.OUT	2	3	-	2	-
I2C bus	1	-	-	1	1
DIG.OUT	15	6	32	2	
DIG.IN	5	-		-	
DIG.BIDIR	2	-		-	
ANALOG.IN	-	1/chip	-	1/chip	16
ANALOG.OUT	-	3	-	-	-
SIGNALING	3.3V	2.2V	5V	±1.25V	

TIMEPIX: charge-sharing test signals have not been included

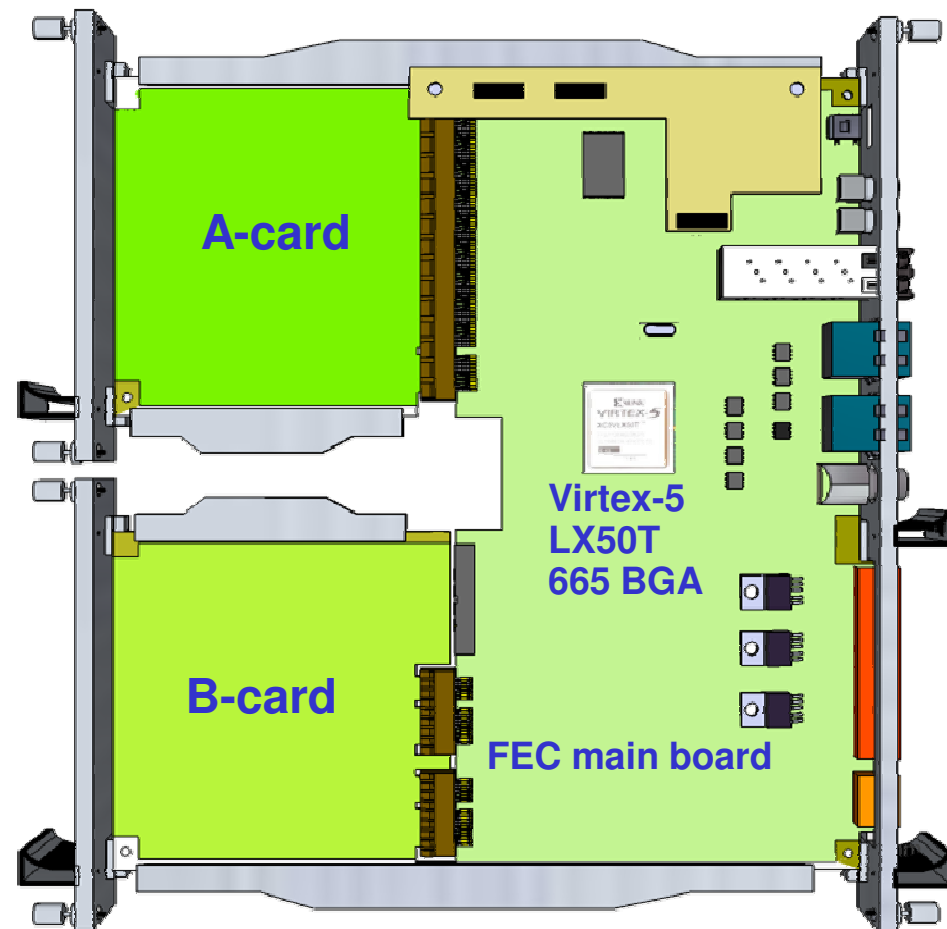
- **Very different interface and circuitry requirements:** voltage regulators, reference levels, connectors and specific circuitry (like summing circuits, isolation, I/V, analog multiplexer,...)
- **Even if we could address each specific design issue in a common interface circuitry, there is no flexibility to use other ASICs**
- **¿Is there a better solution?  Yes, a modular FEC**



# A flexible interface front-end card (FEC)

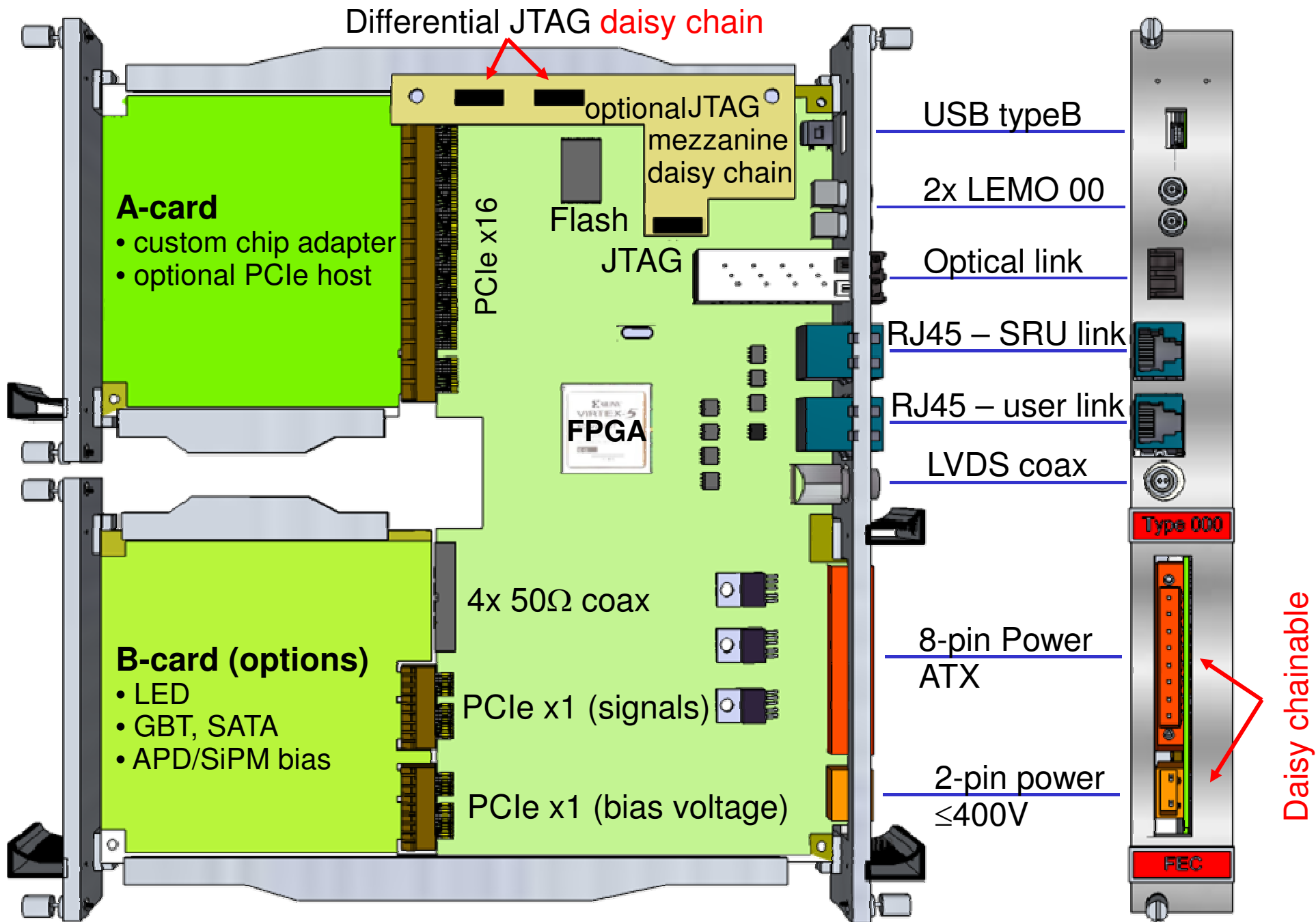
# A flexible interface front-end card (FEC)

- 6U module composed of a 6Ux120mm FEC main board and two 3Ux100mm adapter cards
- Module fits on standard 6Ux220mm chassis, with added 100mm card guides
- Front panel (two 3U) is application specific
- Back panel (6U) for power and I/O (DAQ, clock, trigger, control)

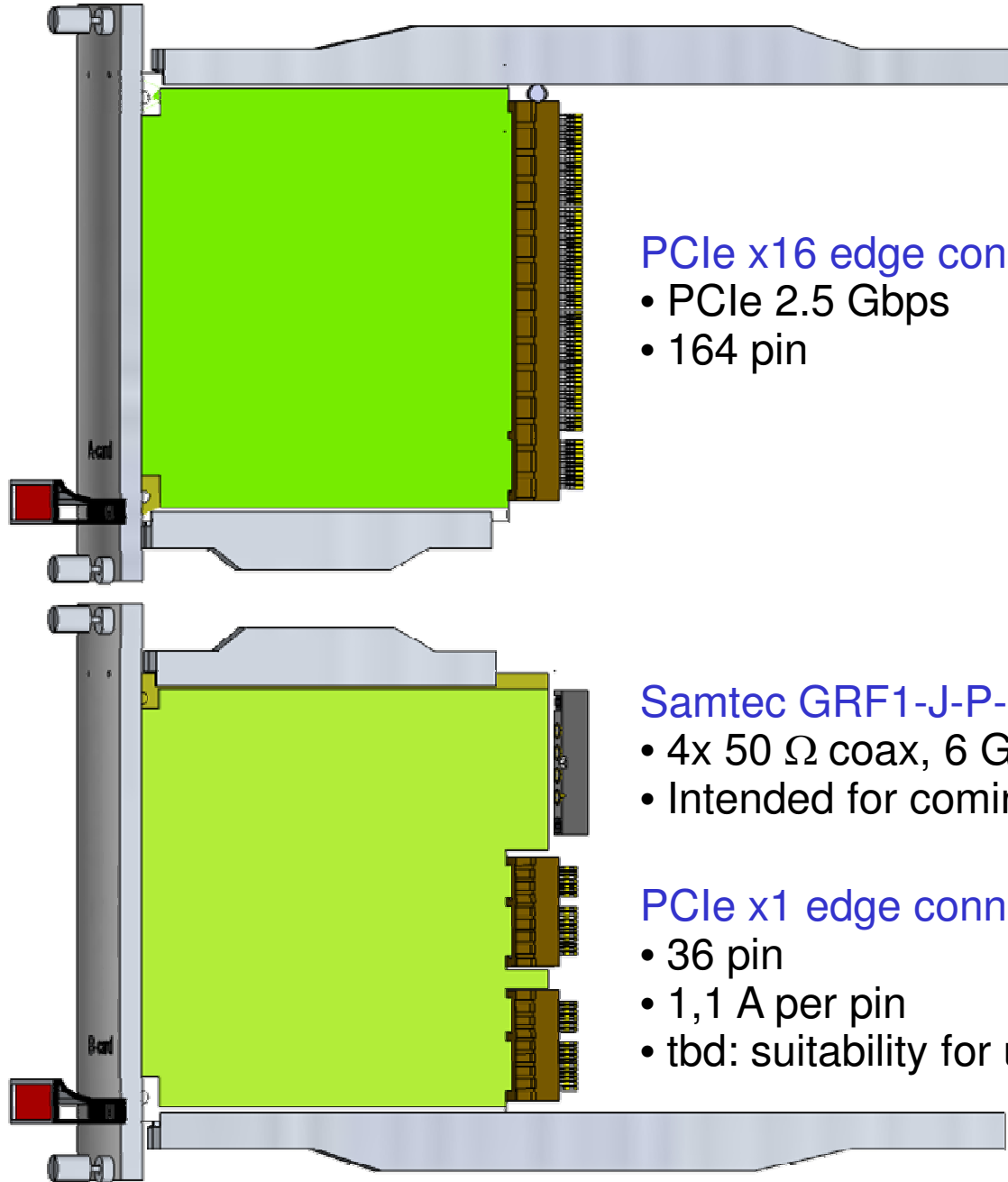


- An application-specific **adapter card (A-card)** includes voltage level translators, DACs, ADCs, voltage regulators, isolation, LVDS drivers and connectors
- An **optional second adapter card (B-card)** for additional features (APD/SiPM bias control, LED calibration pulsers, high-speed interfaces,...)
- A common **FEC main board** with:
  - FPGA connected to all signal I/O connectors
  - FPGA remote programming from JTAG daisy chain, optical link or SRU conn
  - ATX power conn and voltage regulators
  - Optional APD/SiPM bias voltage conn

# A flexible interface front-end card (FEC)



# A flexible interface front-end card (FEC)

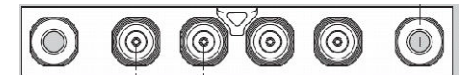


## PCIe x16 edge connector (straddle mount)

- PCIe 2.5 Gbps
- 164 pin

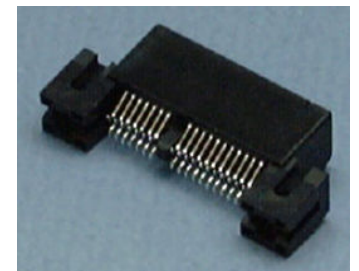
## Samtec GRF1-J-P-04-E-RA-TH1

- 4x 50  $\Omega$  coax, 6 GHz
- Intended for coming GBT interface



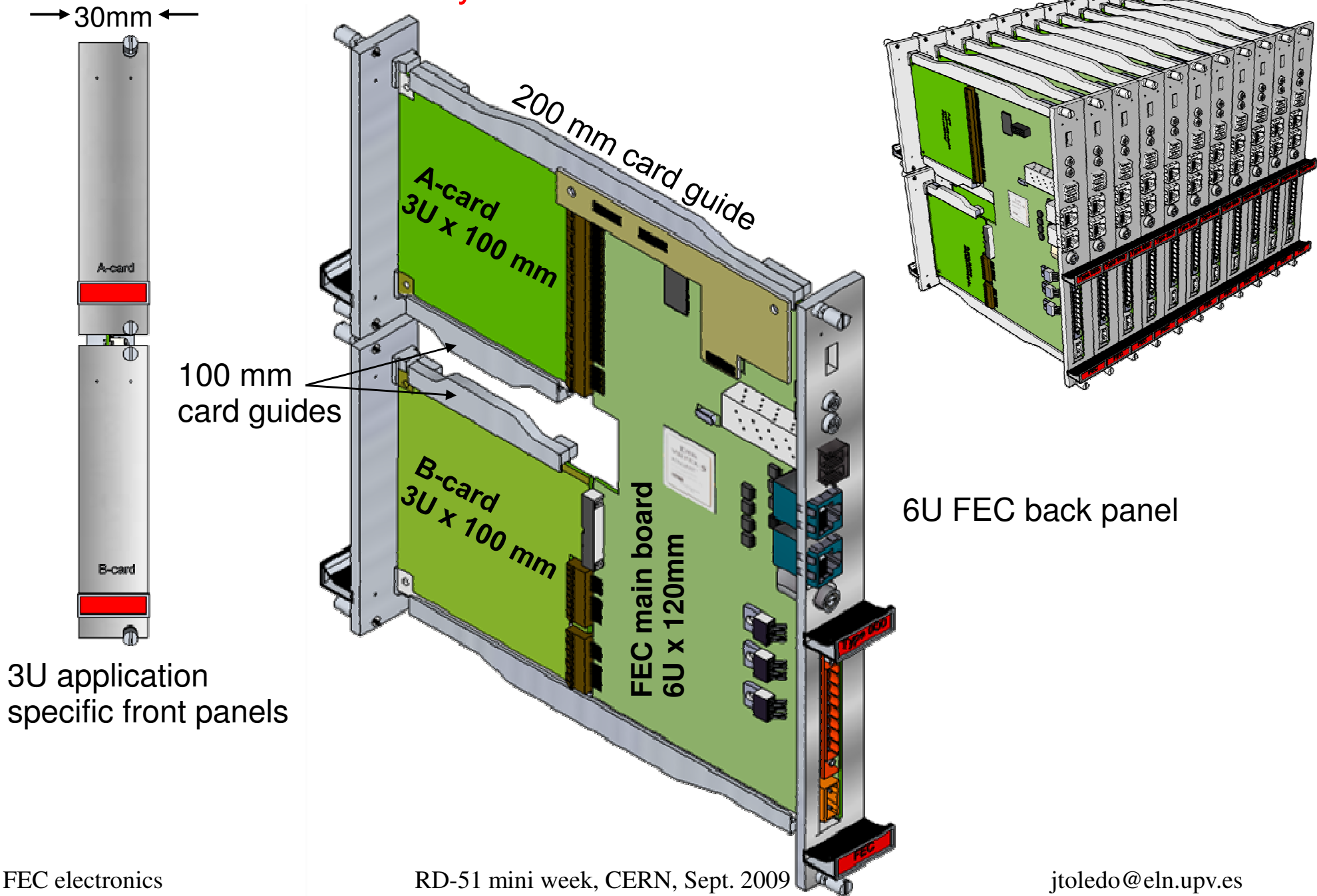
## PCIe x1 edge connector (straddle mount)

- 36 pin
- 1,1 A per pin
- tbd: suitability for up to 400V voltages



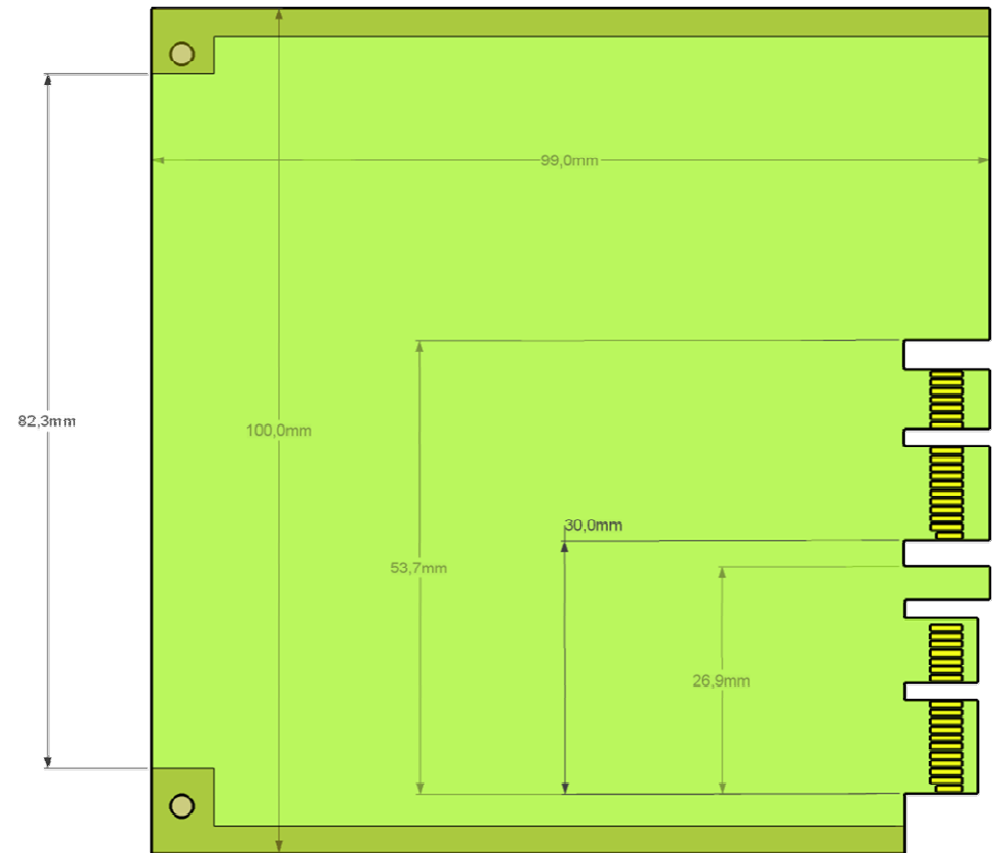
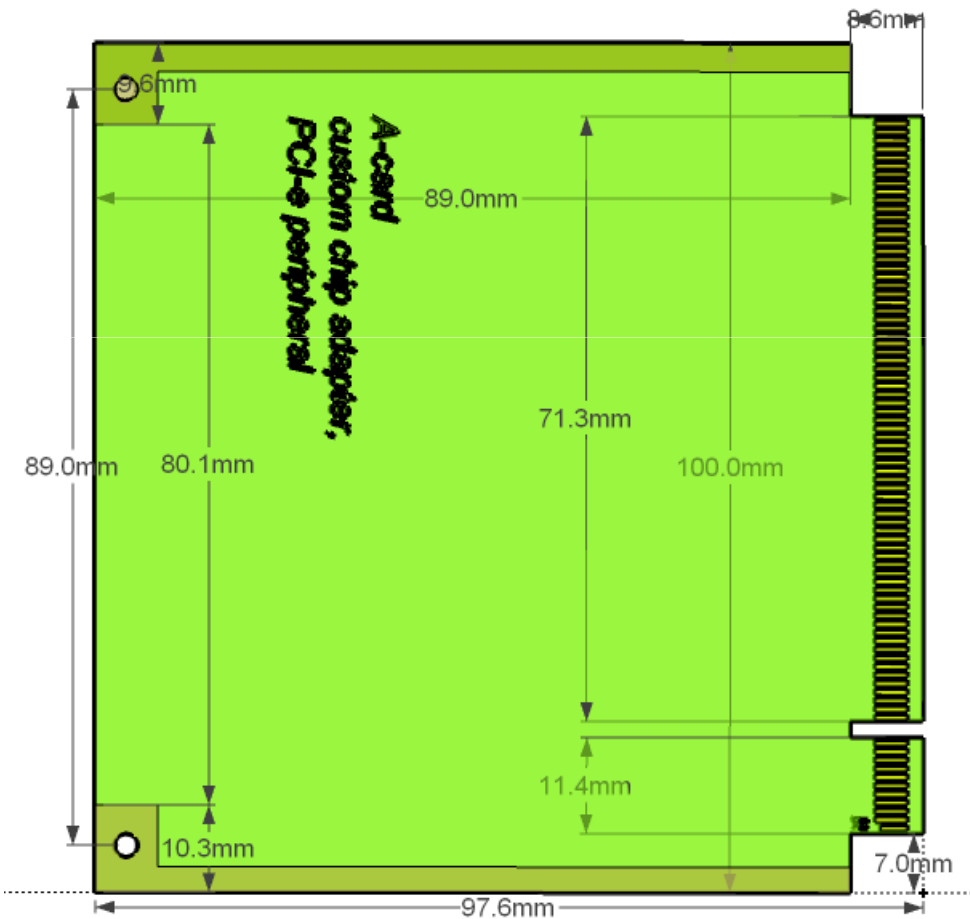
# A flexible interface front-end card (FEC)

Front-end system of SRS in 6U x 200 Eurocrate



# A flexible interface front-end card (FEC)

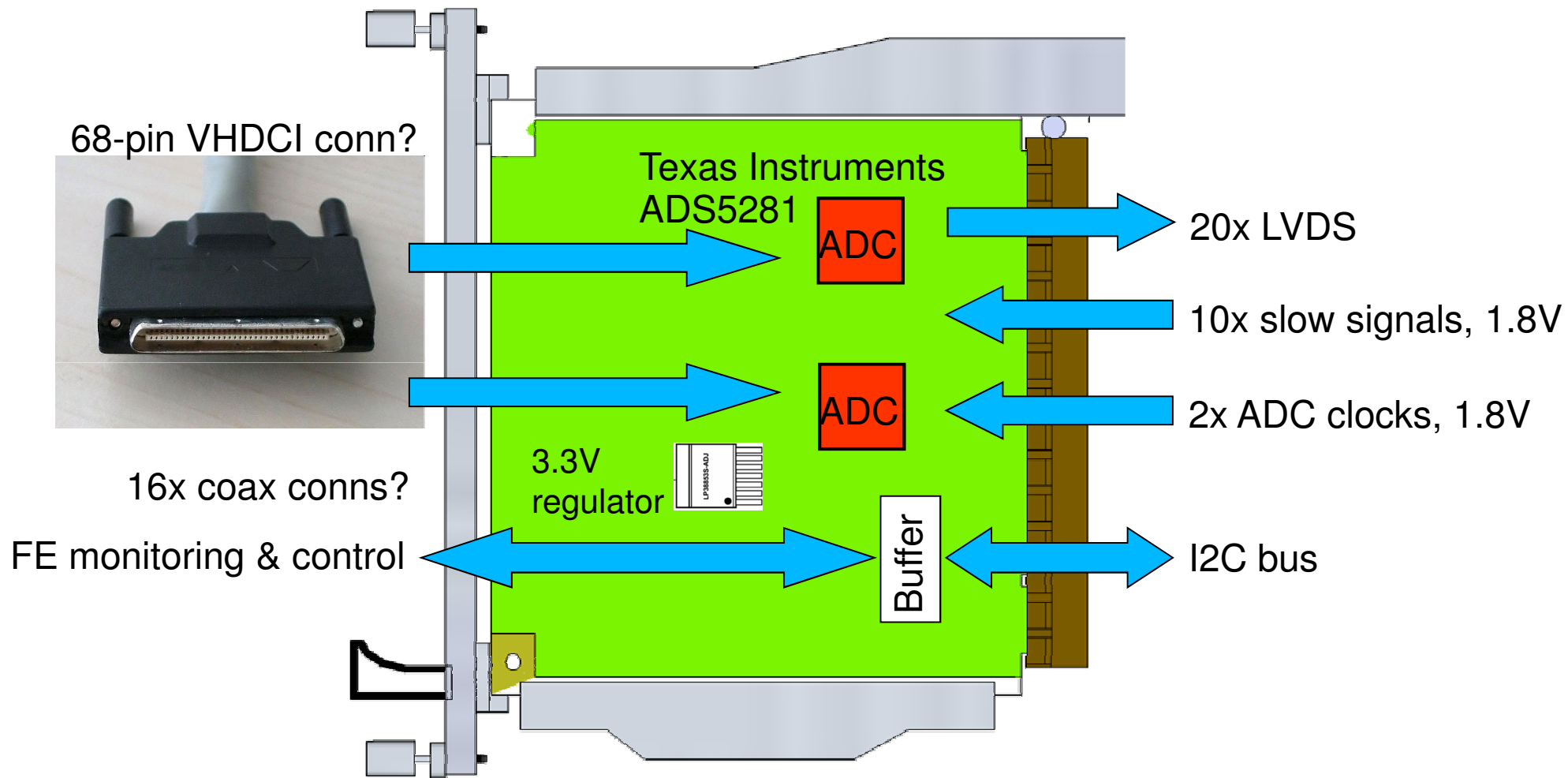
A-card and B-card mechanical drawings, connector pinout and electrical specs will be made available to allow user developments



# A-card application examples

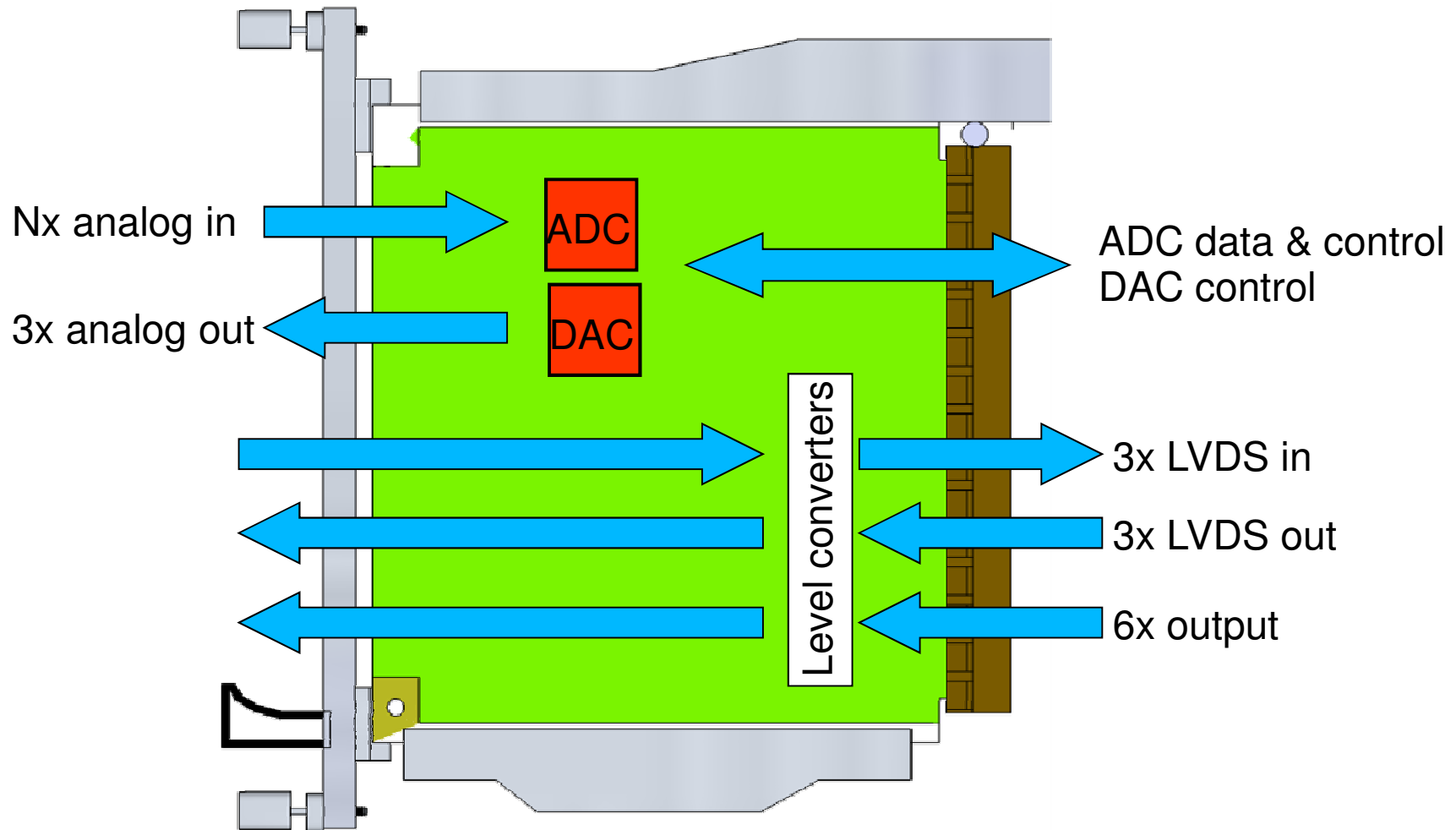
# Application example: 16ch 40MHz ADC

The first A-card we need in NEXT

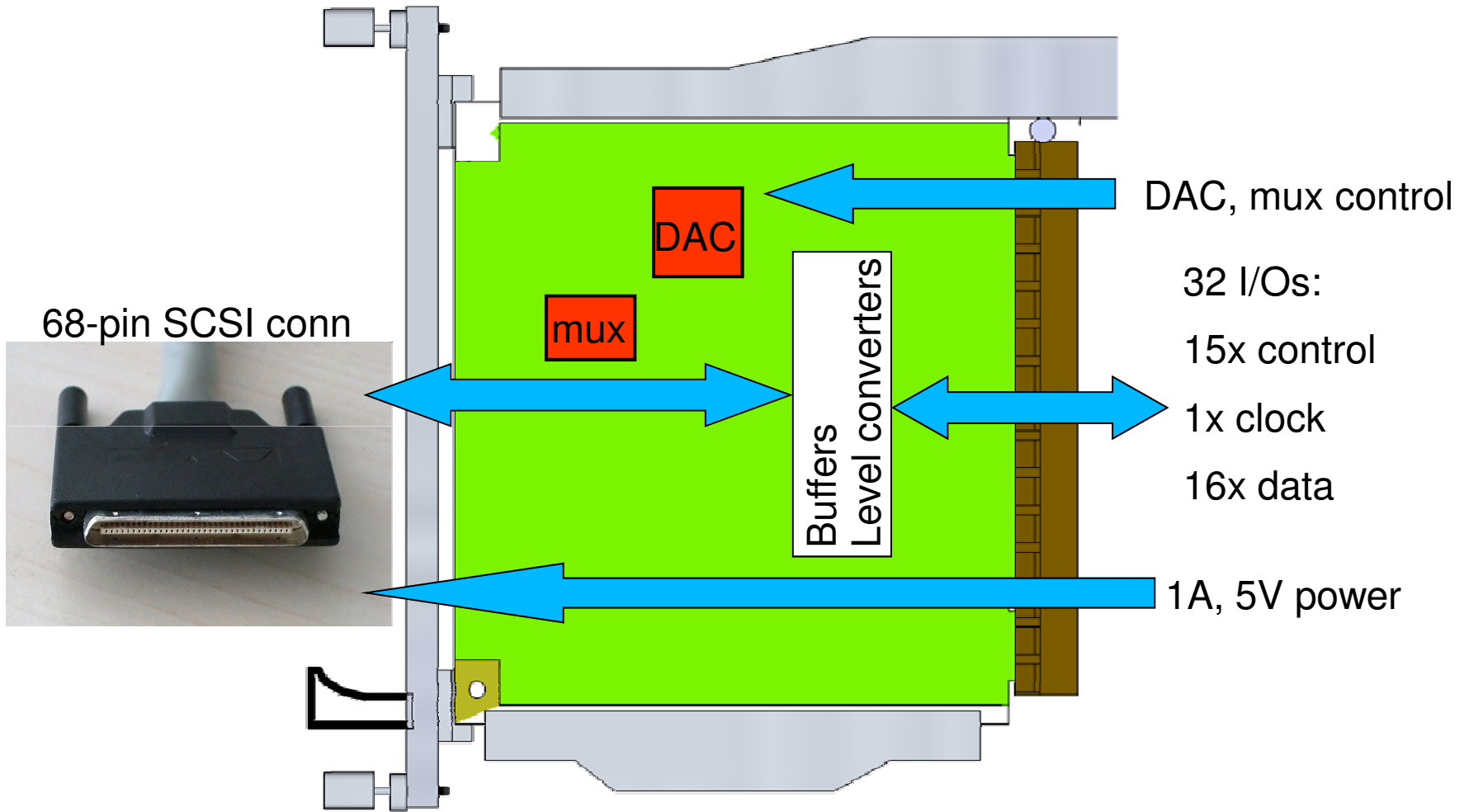




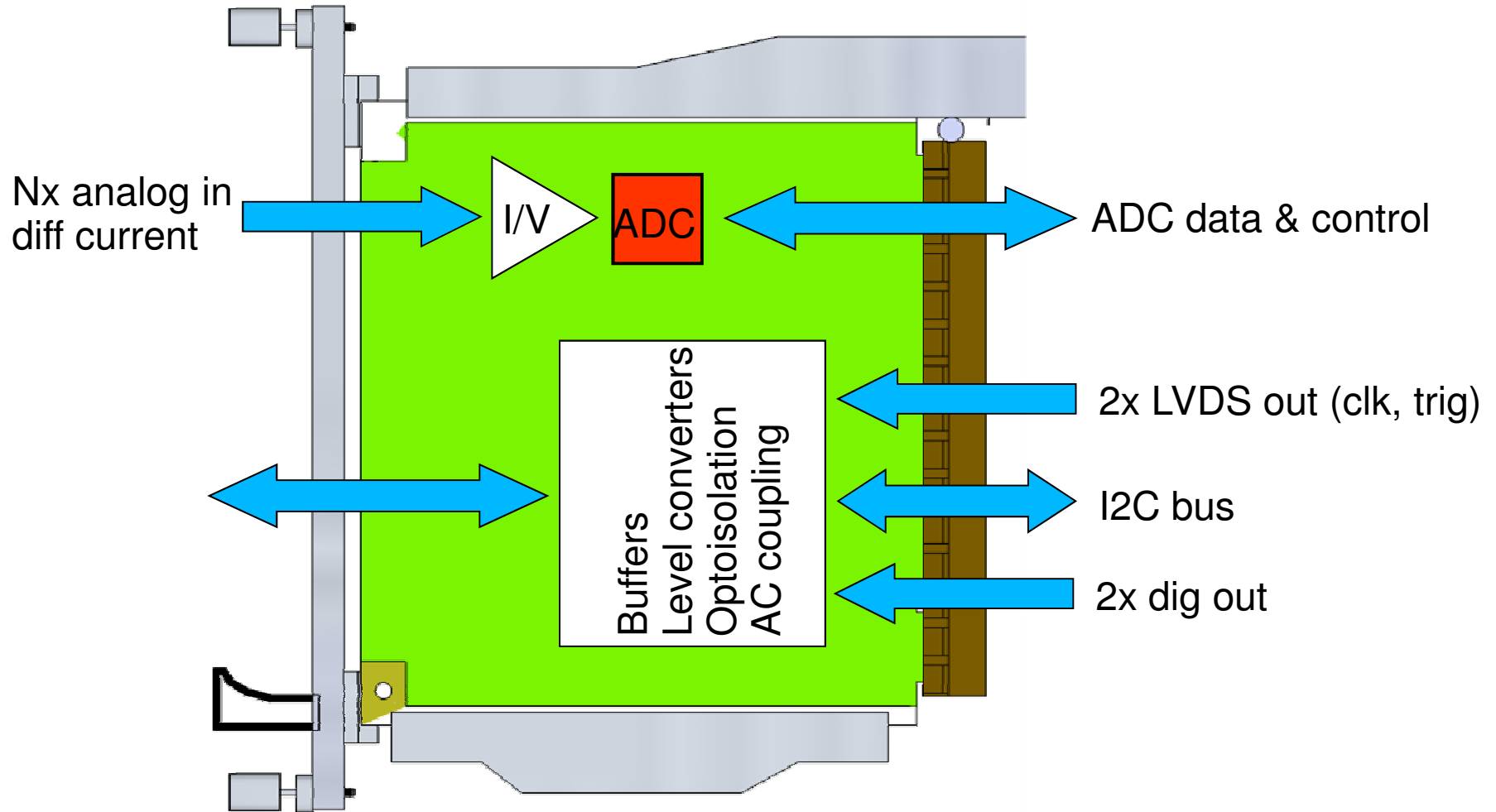
# Application example: TimePix



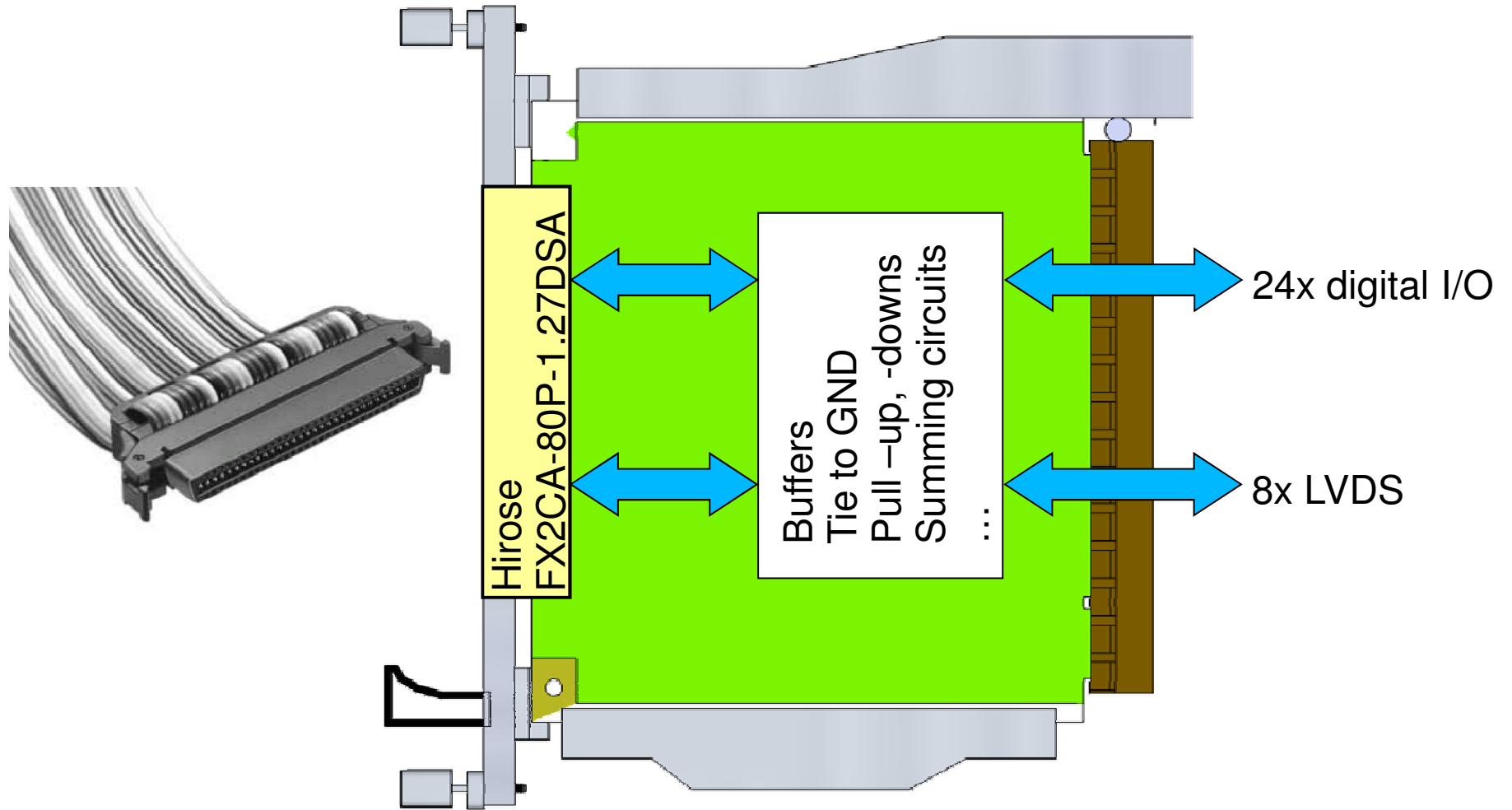
# Application example: MUROS2



# Application example: APV25



# Application example: T2K AFTER



# Conclusions

- ASIC interface requirements are too different for a common FEC design
- A modular FEC solution has been proposed for 6U x 220 Eurocrates
  - Front panel for FE interface and back panel for power, DAQ, trigger and control
  - A-card for application-specific ASIC interface
  - Optional B-card for other interesting FE features
- A-card, B-card specs to be released for user developments

Thank you !