APV25 VME based readout system for a Jlab GEM tracker

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- The Detector
- Front End Electronics
- Read Out Electronics

The Detector (1)

Jefferson LAB upgrade to 12 GeV framework program.

HALL-A SBS front tracker GEM based

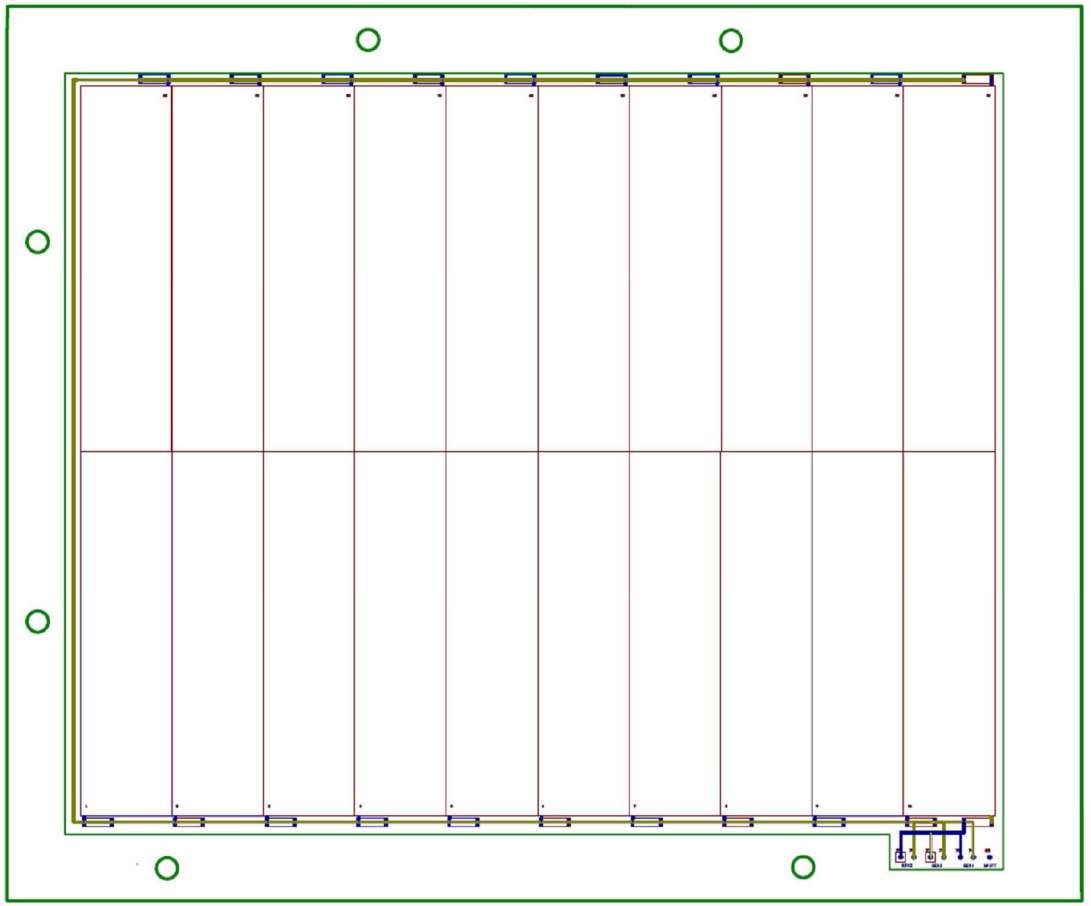
6 planes X-Y (+ U-V?)

Area: ≈ 40 x 50 cm^2

Gem foils divided in 20 sectors 20 x 5 cm^2

Each sector connected to HV through a SMD resistor placed along the frame (long sides).

Design and production by Rui De Oliveira.



The Detector (2)

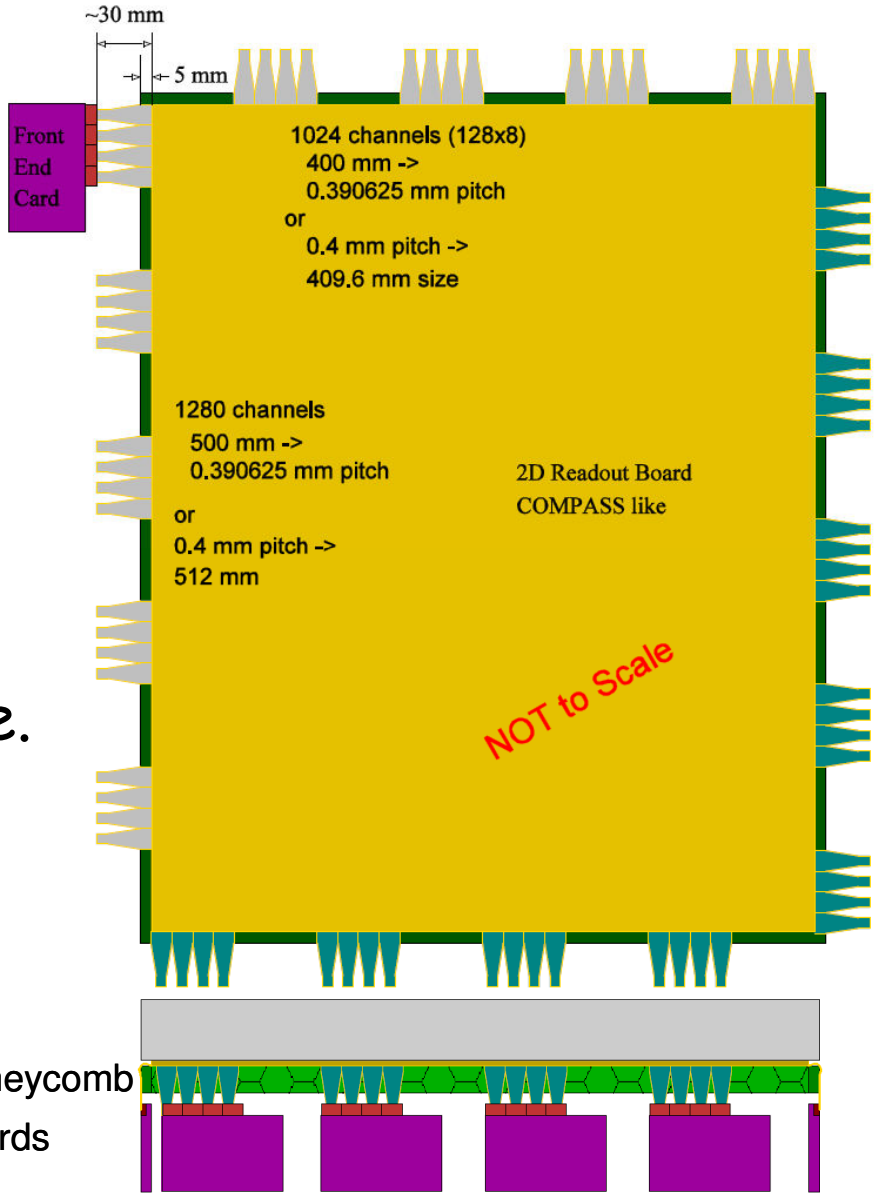
2D readout strips layers:
pitch = 0.4 mm, multiple of 128

1024 + 1280 strips per plane

In total about 14000 strips
(x 2 if U-V option adopted).

Use of Panasonic FPC
connectors, 0.3 mm pitch,
avoid soldering on readout plane.

Readout on both sides,
interleaved.

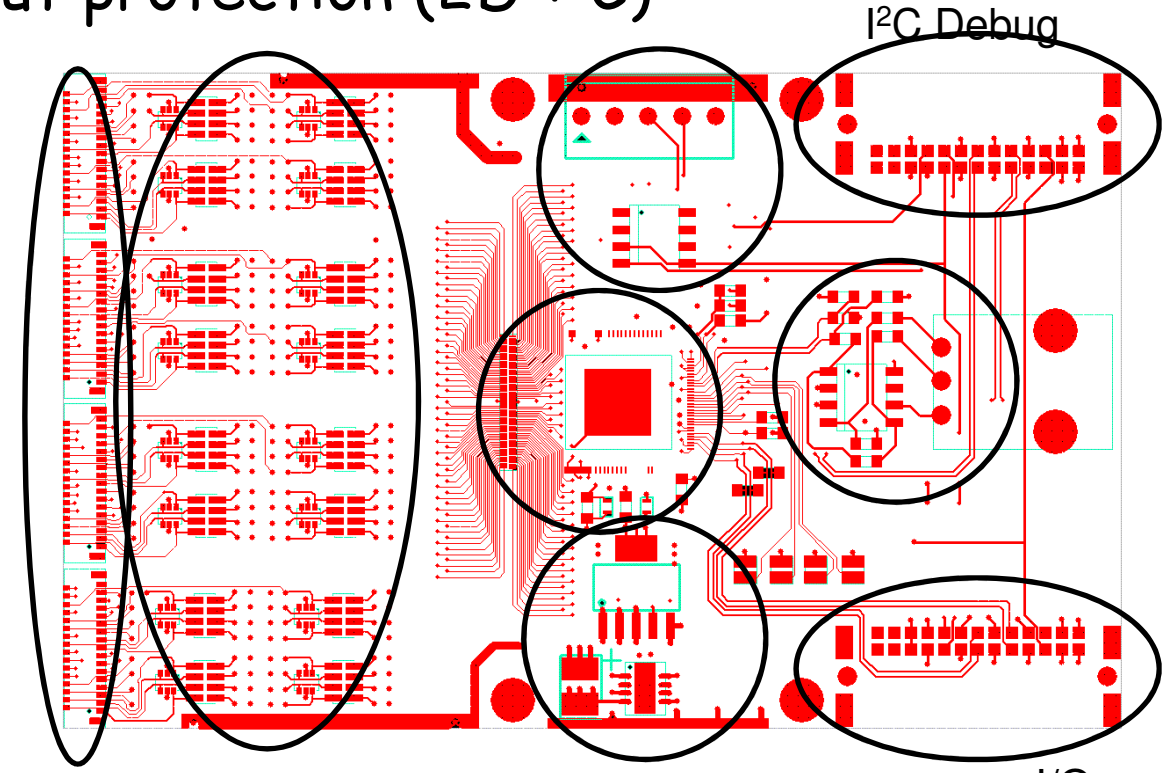


Front End (1)

Based on APV25 chip. We bought ≈ 600 naked chips.

128 channels per card (1 APV). Dimensions: 50 x 80 mm^2

Discrete input protection (2D + C)



Front End (2)

Design finished.

Some issues regarding output analog signal transmission and radiation tolerance (quite hot zone). Testing needed.

PCB ready for production: we are waiting quotations.

Double check with GEM readout plane needed.

SMD assembly using external fab.

APV wire bonding using internal facility (ATLAS pixel modules).

Standard assembly (through hole) in house, after wire bonding.

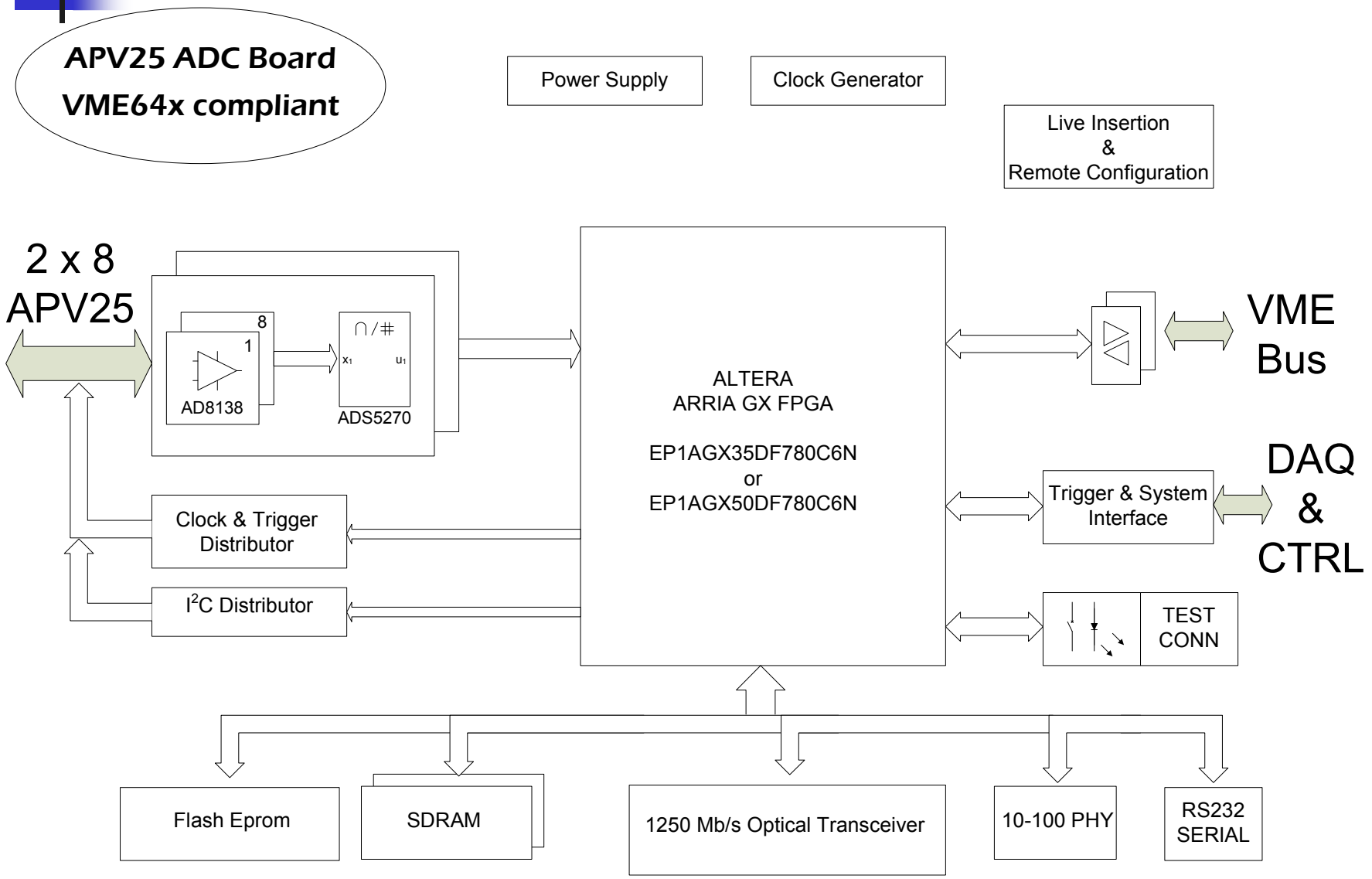
First prototype ready in 2 months (hope earlier!).

Readout (1)

Main features:

- Digitization of 16 APVs (2048 channels)
- APV serial stream decoding
- Zero suppression
- Big memory buffer, multi event
- Possibility to implement SOC:
  - Flash, Ethernet, Serial
- Remote logic reconfiguration, hot swappable
- Dual configuration:
  - goal: VME64x compliant
  - backup: Stand Alone (with optical link)

Readout (2)


APV25 ADC Board
VME64x compliant
Power Supply
Clock Generator
Live Insertion
&
Remote Configuration
2 x 8
APV25
8
1
AD8138
ADS5270
ALTERA
ARRIA GX FPGA
EP1AGX35DF780C6N
or
EP1AGX50DF780C6N
VME
Bus
Trigger & System
Interface
DAQ
&
CTRL
Clock & Trigger
Distributor
I2C Distributor
TEST
CONN
Flash Eprom
SDRAM
1250 Mb/s Optical Transceiver
10-100 PHY
RS232
SERIAL

Readout (3)

Status:

- Almost all components chosen
  - FPGA: Altera Arria GX
  - ADC: Texas ADS5270
- Schematic drawing almost done
  - Some details still missing (i.e. trigger & DAQ if)
- PCB design will start very soon
  - Footprint checking in progress
- Quotation for manufacturing already asked

➢ Ready for production in 2 months

Conclusions

The design of the system is in advanced phase.

Front end prototypes testing will teach a lot regarding output analog signal integrity and radiation tolerance.

A big effort is needed to develop the FPGA code:

- APV deserialization and decoding
- VME interface
- I^2C controller
- Trigger handling
- High speed serial interface (optical)