Analog/Mixed-Signal Design in FinFET Technologies

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Mobile SoC Migration to FinFET

Mobile SoC is now main driver for CMOS scaling

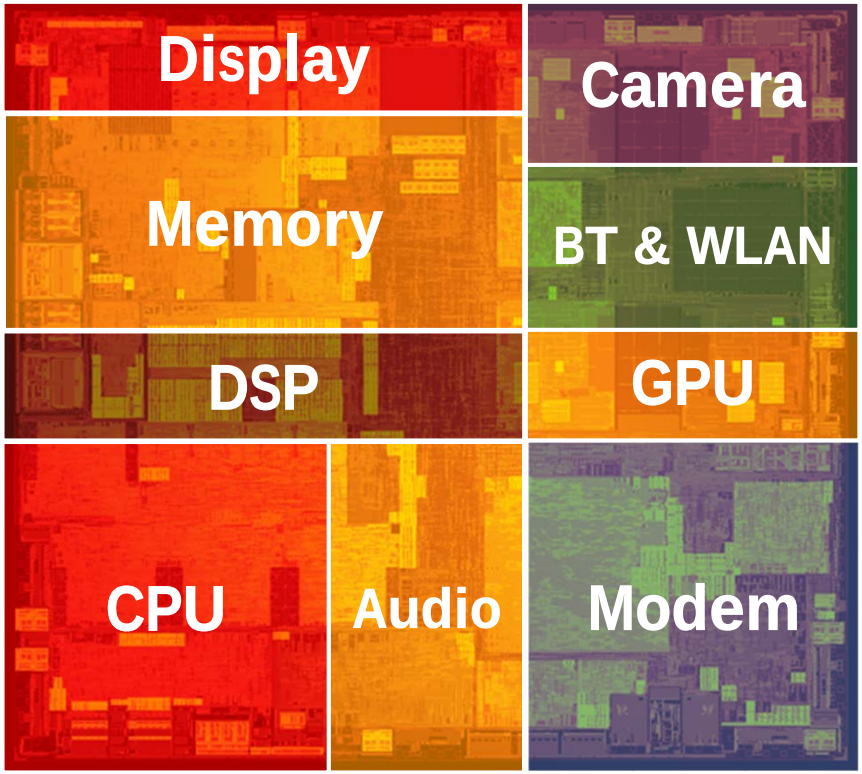
- Power, Performance, Area, Cost (PPAC) considerations, cost = f(volume)
- Snapdragon™ 820 - Qualcomm Technologies' first 14nm product
- Snapdragon™ 835 – World's first 10nm product

Plenty of analog/mixed-signal content

- PLLs & DLLs
- Wireline I/Os
- Data converters
- Bandgap references
- Thermal sensors
- Regulators
- ESD protection

SoC technology driven by logic & SRAM scaling needs due to cost

Not drawn to scale

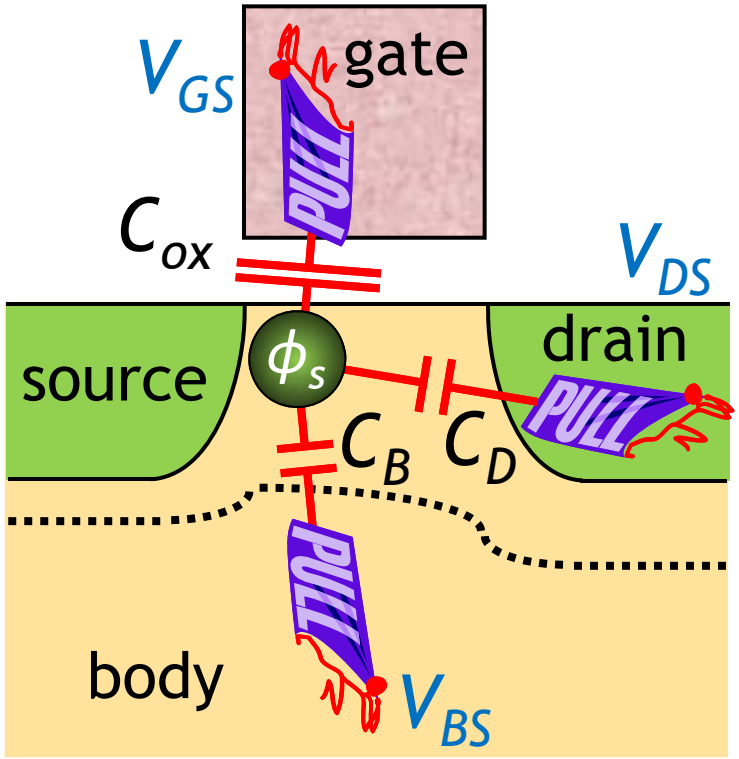


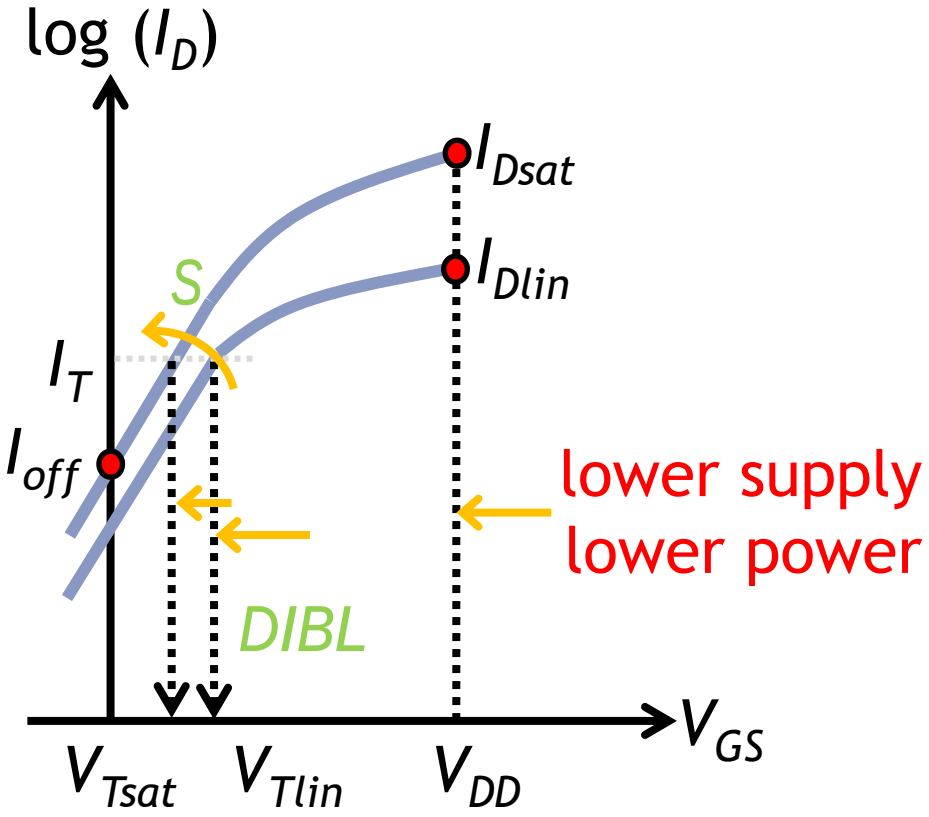
Terzioglu, Qualcomm [1]

Outline

- Fully-Depleted FinFET Basics
- Technology Considerations
- Design Considerations
- Conclusion

Towards Stronger Gate Control

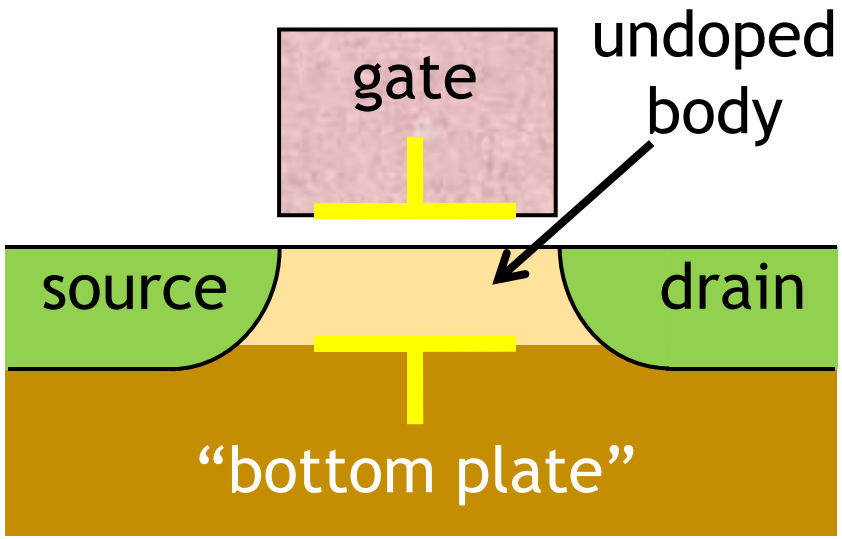




- Capacitor divider dictates source-barrier ϕ_s & I_D
- Fully-depleted finFET weakens C_B, C_D → steeper *S*, less *DIBL* & less body effect
- Lower supply & lower power for given I_{off} & I_D

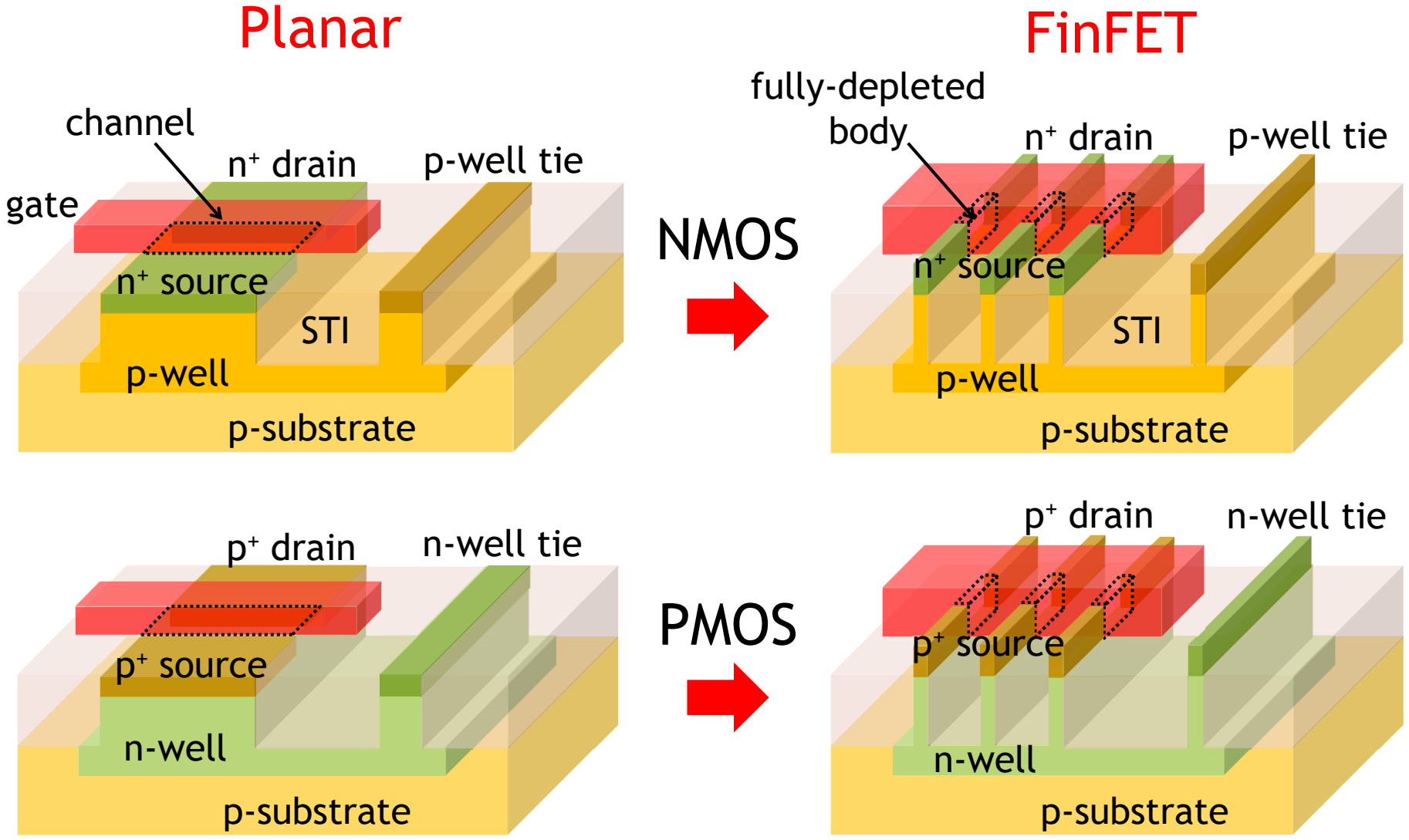
Concept of Fully-Depleted

- Dopants *not* fundamental to field-effect action, just provide mirror charge to set up *E*-field to induce surface inversion
- Use heavily-doped "bottom plate" under undoped body to terminate *E*-fields from gate (extremely retrograded well doping)
- Body becomes *fully-depleted* as it has no charge to offer
- Implementations
  - Planar on bulk
  - Planar on SOI (FD-SOI)
  - 3-D (e.g., finFET) on bulk
  - 3-D on SOI



Yan *et al.*, Bell Labs [2]
Fujita *et al.*, Fujitsu [3]
Cheng *et al.*, IBM [4]

Migrating to Fully-Depleted FinFET



Outline

- Fully-Depleted FinFET Basics
- Technology Considerations
  - Mechanical Stressors
  - High-K/Metal-Gate
  - Lithography
  - Middle-End-Of-Line
- Design Considerations
- Conclusion

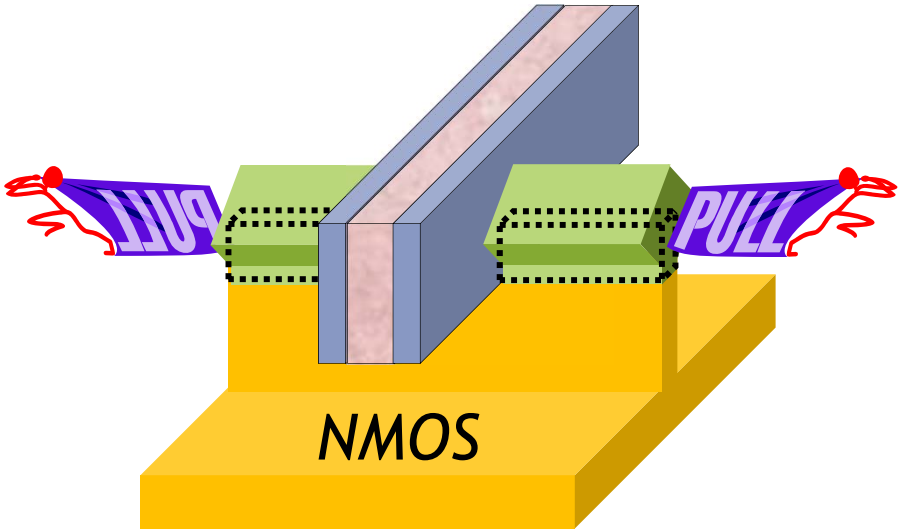
Journey to FinFETs

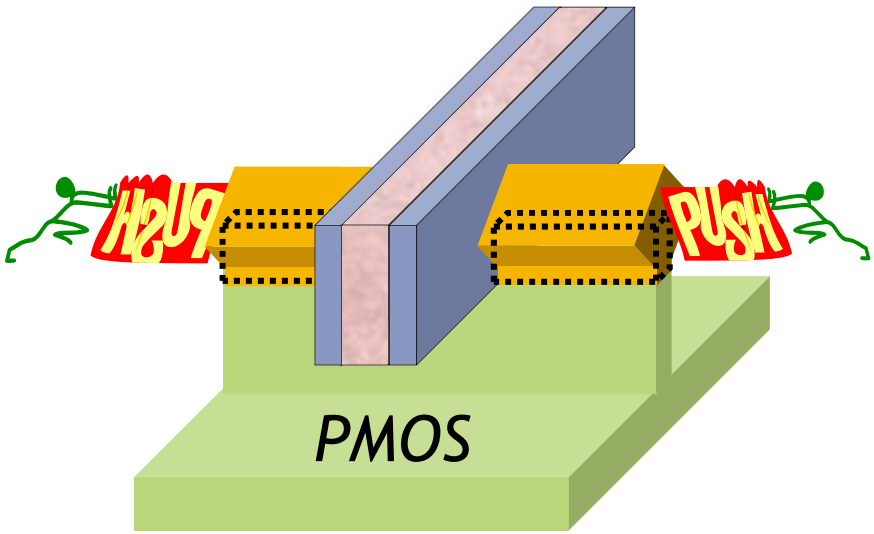
- 16/14nm complexity accumulated from scaling innovations introduced earlier across multiple earlier nodes

Technology Innovation	Foundry Debut	Reason Required
Mechanical stressors	40nm	Mobility boost for more FET drive & higher I_{on}/I_{off}
HKMG replacement gate integration	28nm (HK-first) 20nm (HK-last)	Higher C_{ox} for more FET drive & channel control
Multiple-patterning	20nm	Sub-80nm pitch lithography without EUV
Complex middle-end-of-line	20nm	Contact FET diffusion & gate with tighter CPP

Mechanical Stressors

- Mobility depends on channel lattice strain (piezoresistivity)
- Grow stressors to induce channel strain along *L*
  - Tensile for NMOS, compressive for PMOS
  - Techniques: S/D epitaxy, stress memorization, gate stress
- Anisotropic mobility & stress response
  - *L* vs. *W* direction, (100) fin top vs. (110) fin sidewall

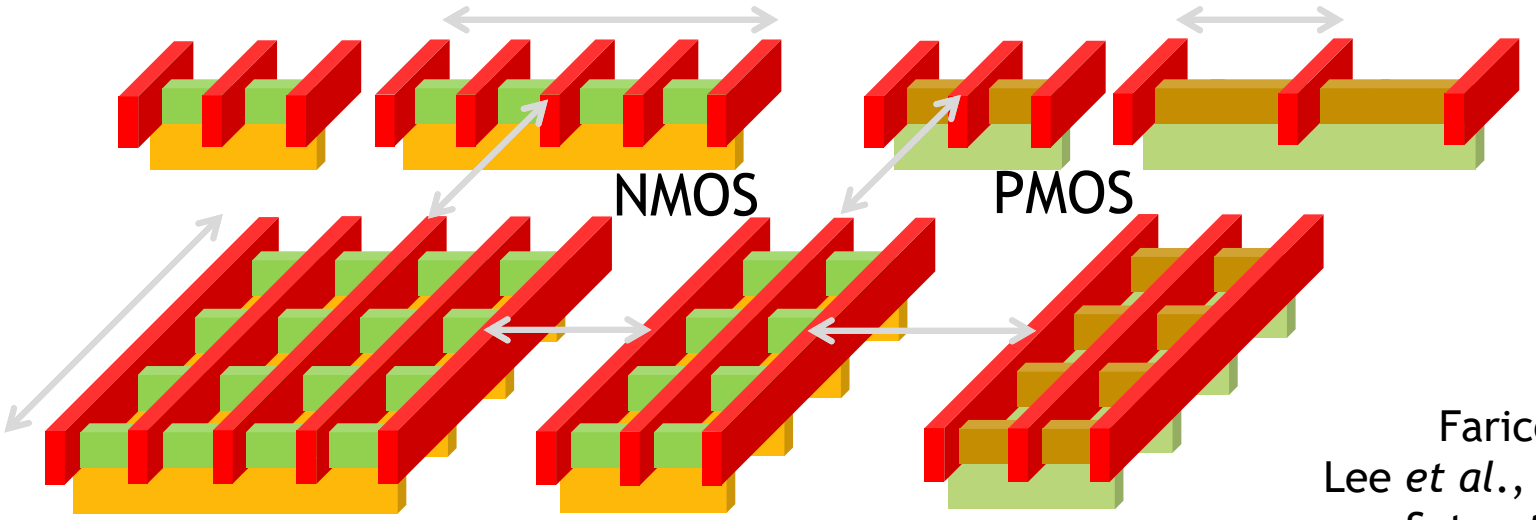




Garcia Bardon *et al.*, IMEC [5]
Liu *et al.*, Globalfoundries [6]

Stress-Related Layout Effects

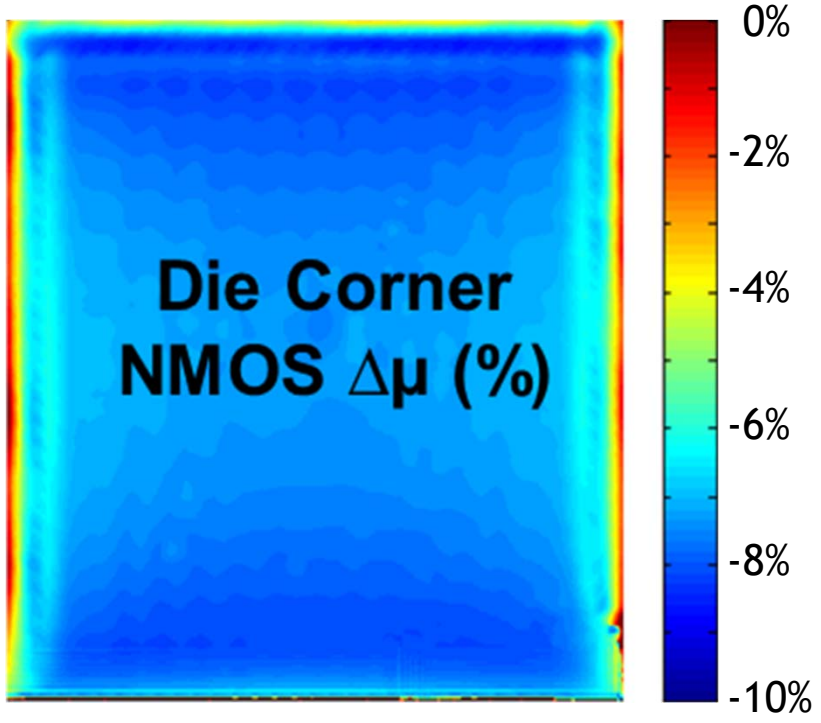
- Stressors are stronger in 16/14nm for more FET drive, so layout effects can be more severe → schematic/layout Δ
- Stress build-up in longer active, I_D/fin not constant vs. # fins
- Interaction with stress of surrounding isolation & ILD
- NMOS/PMOS stress mutually weaken each other
- New effects being discovered, e.g., gate-cut stress effect

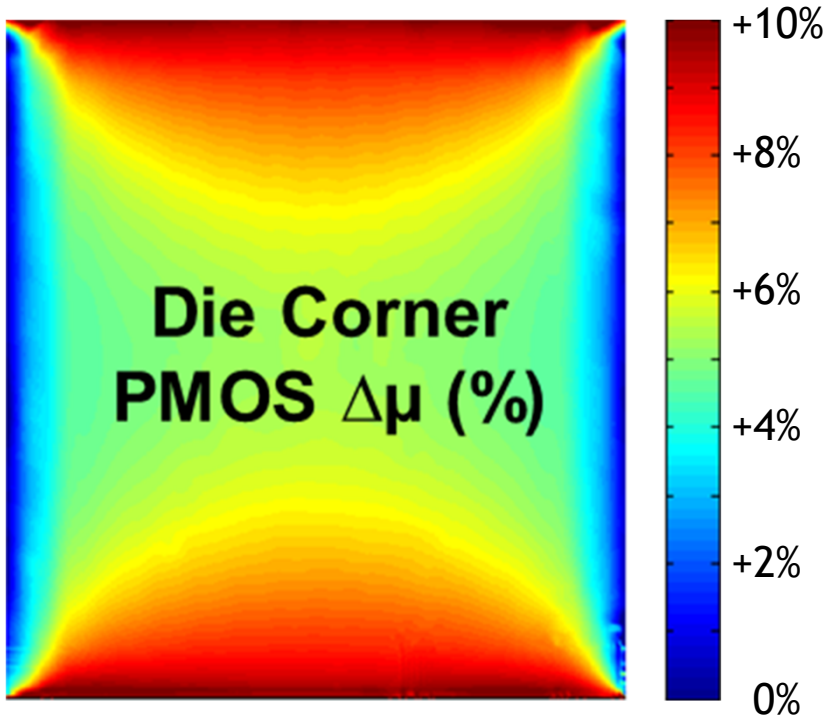


Faricelli, AMD [7]
Lee *et al.*, Samsung [8]
Sato *et al.*, IBM [9]

Electrical Chip-Package Interaction

- FET mobility sensitive to stress from die attach to package
- Package stress can impact long-range device matching (e.g., I/O impedance, bias references, data converters)

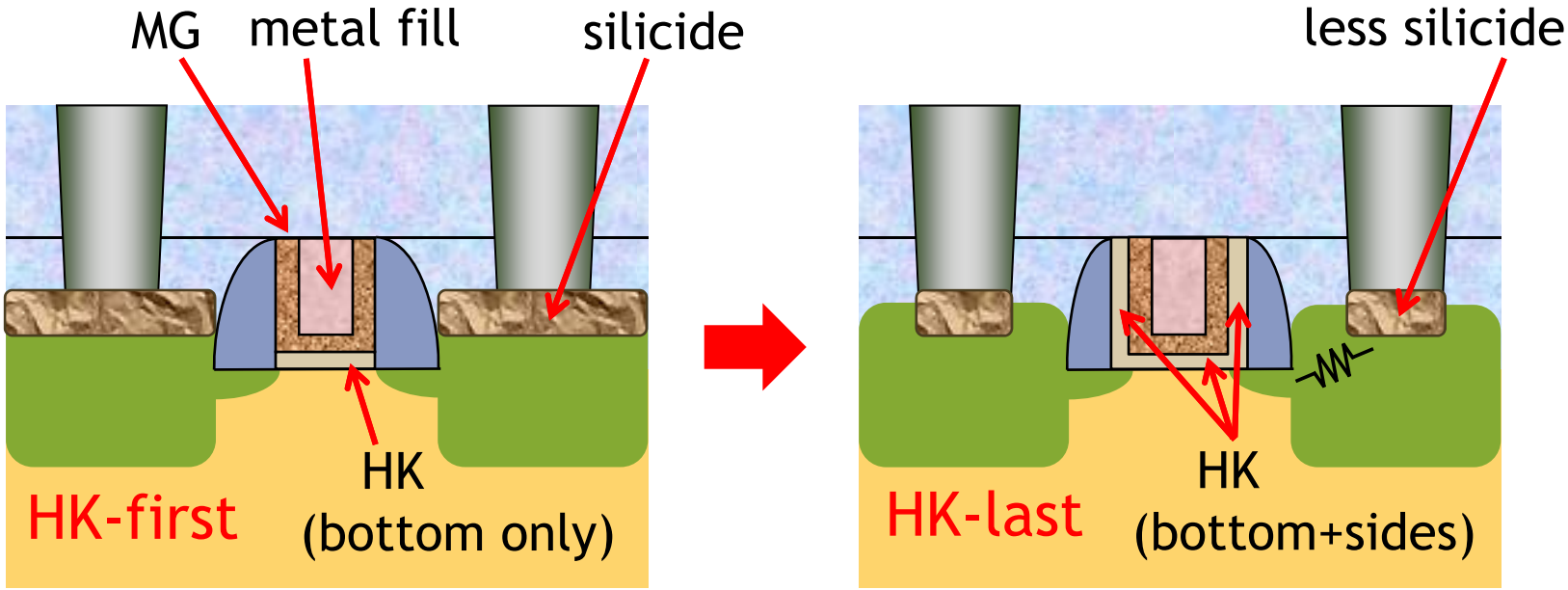




Terzioglu, Qualcomm [1]

High-*K*/Metal-Gate (HKMG)

- Increase C_{ox} with less I_{gate} & no poly depletion, but HK/MG interface is very delicate
- Replacement metal gate (RMG) after S/D anneal for stable V_T
- Gate = (ALD MG stack to set Φ_M) + (metal fill to reduce R_G)
- HK-first → HK-last for better gate edge control

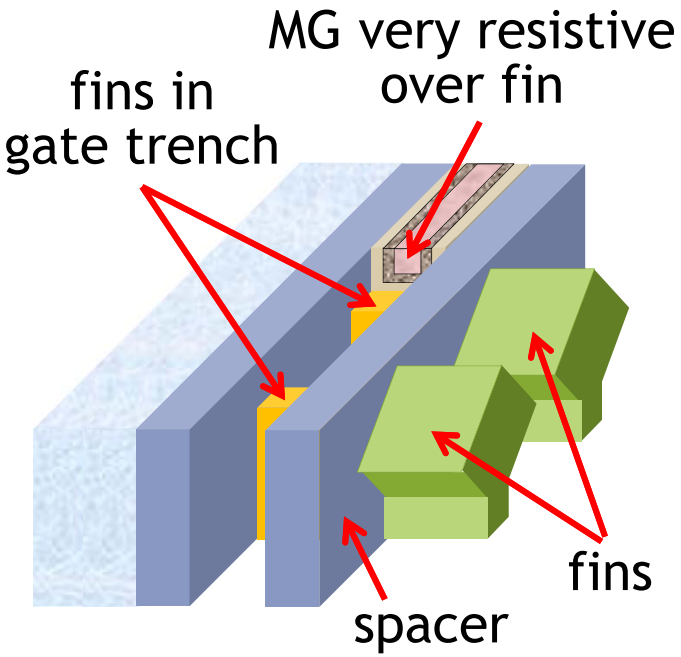


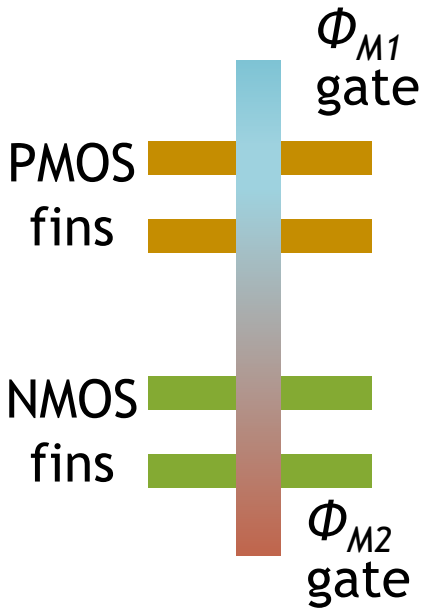
Auth *et al.*, Intel [10]

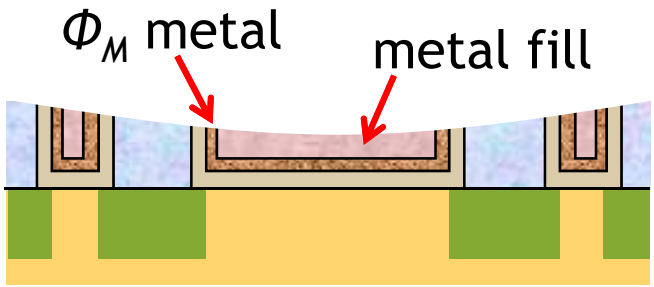
Packan *et al.*, Intel [11]

HKMG Concerns

- Very high R_{gate} → non-quasistatic effects
- Variation in MG grain orientation → V_T variation
- Metal boundary effect (ΔV_T near interface between two Φ_M)
- Gate density induced mismatch (ΔV_T from RMG CMP dishing)





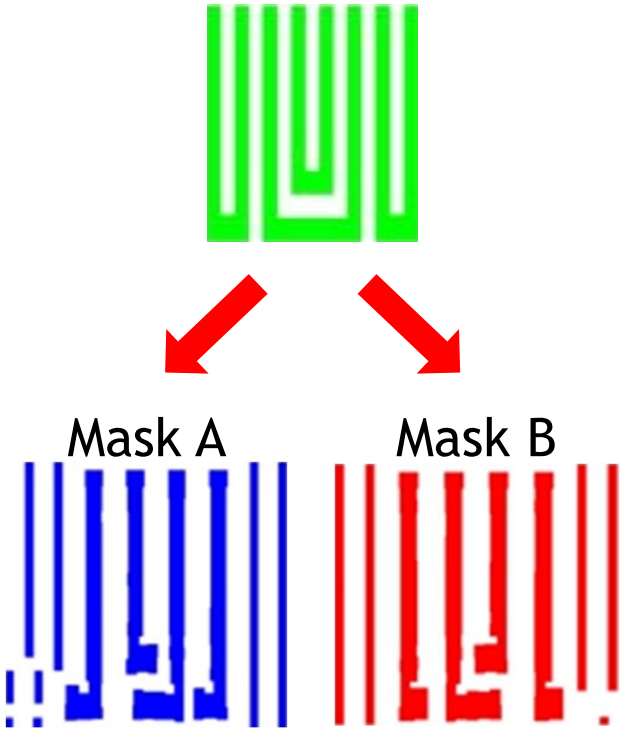


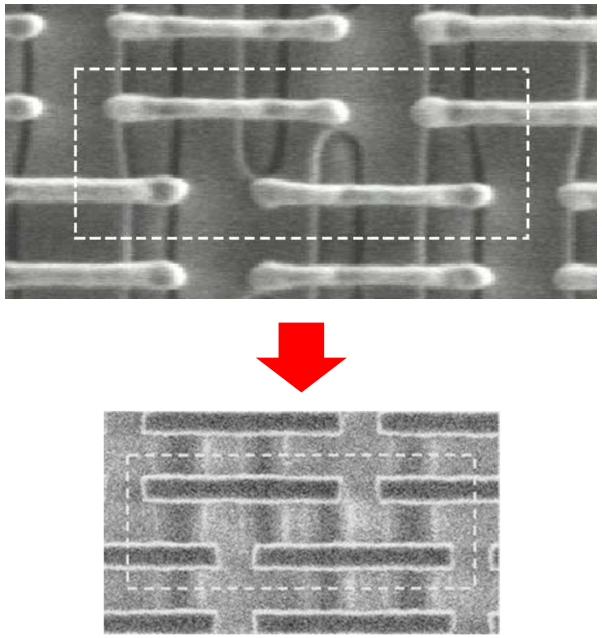
Asenov, U Glasgow [12]
Yamaguchi *et al.*, Toshiba [13]
Yang *et al.*, Qualcomm [14]

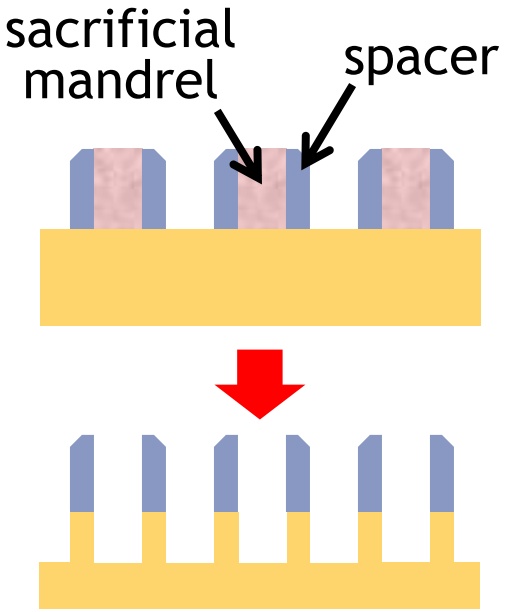
Lithography Innovations

- Needed for sub-80nm pitch, EUV not ready for production

1. Pitch splitting → mask coloring, overlay-related DRCs
2. Orthogonal cut mask → reduce line-end-to-end spacing
3. Spacer-based patterning for fins, adopting for gate



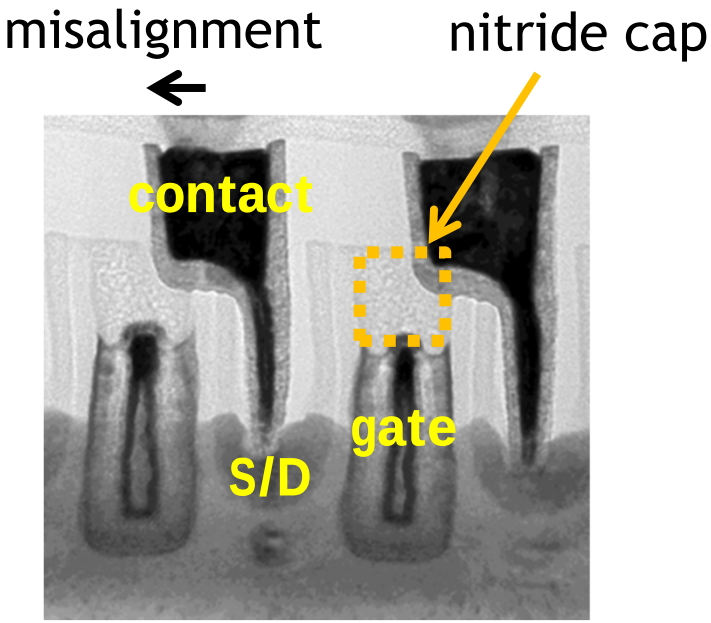


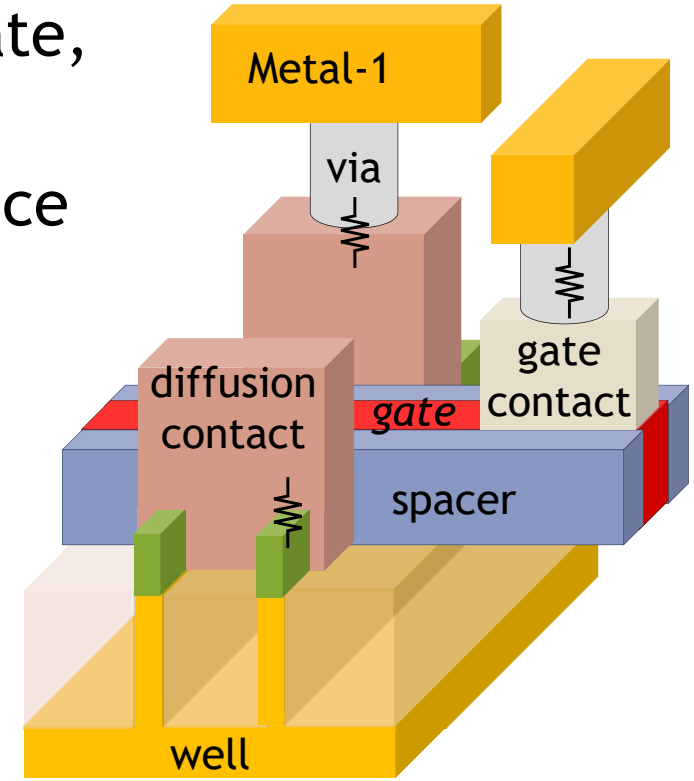


Auth *et al.*, Intel [10], [15]
Dorsch, www.semi.org [16]

Complex Middle-End-Of-Line (MEOL)

- Difficult to land diffusion & gate contacts on tight CPP
- Self-aligned contacts to prevent contact-to-gate shorts
- Separate contacts to diffusion & to gate, also insert via under Metal-1
- Significant BEOL, MEOL & R_{ext} resistance





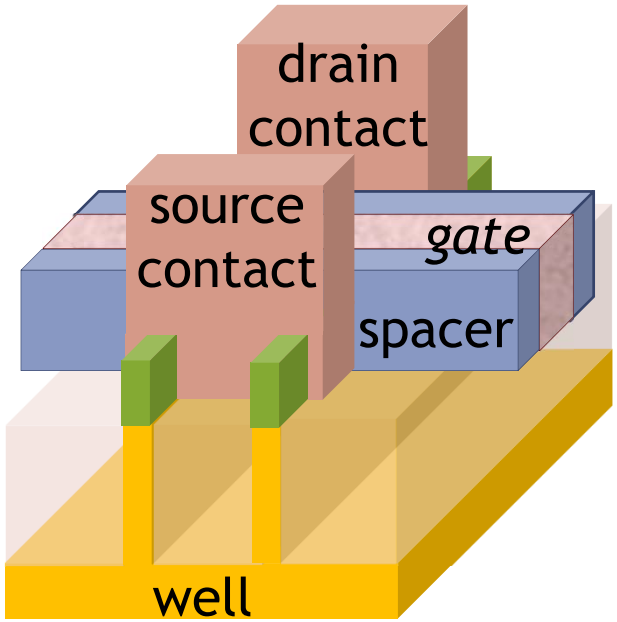
Auth *et al.*, Intel [15]
Rashed *et al.*, Globalfoundries [17]

Outline

- Fully-Depleted FinFET Basics
- Technology Considerations
- Design Considerations
  - General
  - Parasitic *C* & *R*
  - Stacked FET
  - Passives, PNP-BJT, ESD Diodes
  - I/O Voltages
- Conclusion

Designing with FinFET

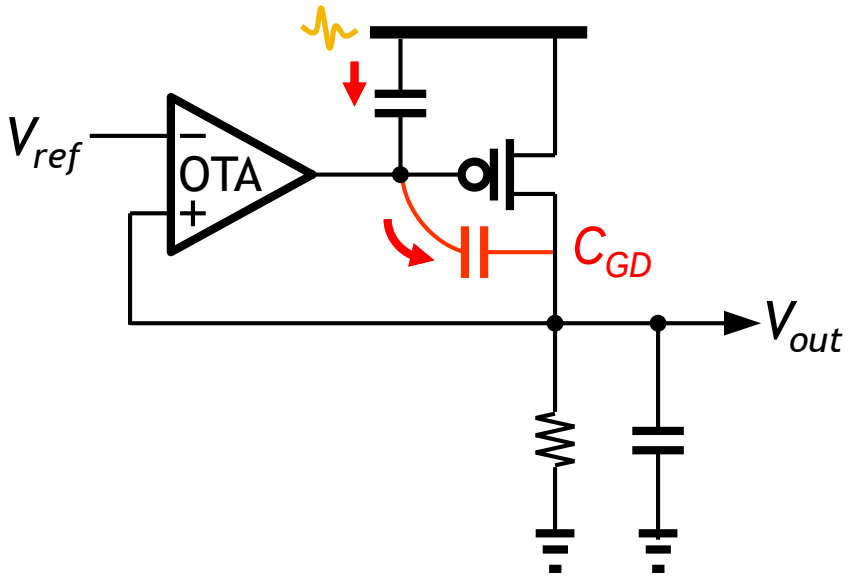
- More drive current for given footprint
- Quantized channel width
  - Challenge for logic & SRAM
  - OK for analog, enough g_m granularity
- Less DIBL → better r_{out}, 3× intrinsic gain
- Essentially no body effect ($\Delta V_T < 10mV$)
- Higher R_s & R_d spreading resistance
- Lower C_j but higher C_{gd} & C_{gs} coupling
- Higher R_{well} (R_{diode}, latch-up)
- Mismatch depends on fin geometry, MG grains, gate density, stress, less on RDF

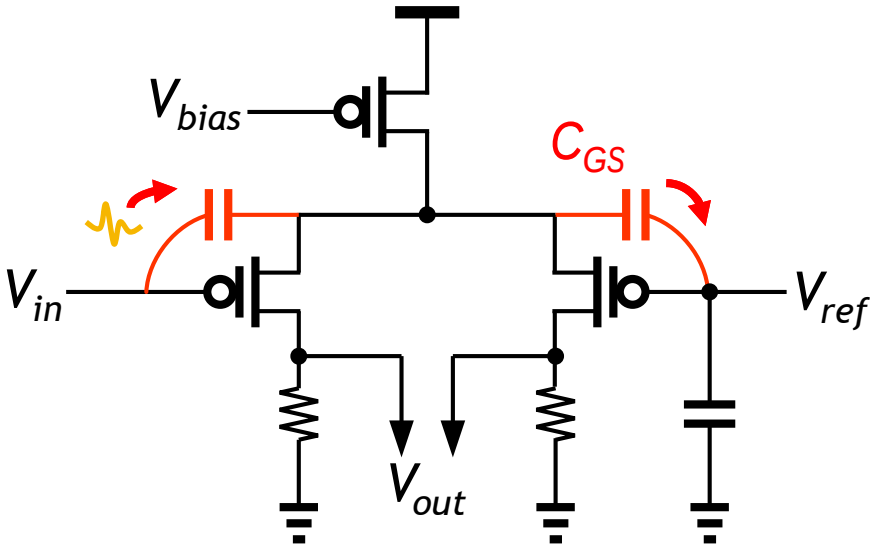


Sheu, TSMC [18]
Hsueh *et al.*, TSMC [19]

Stronger Parasitic Coupling

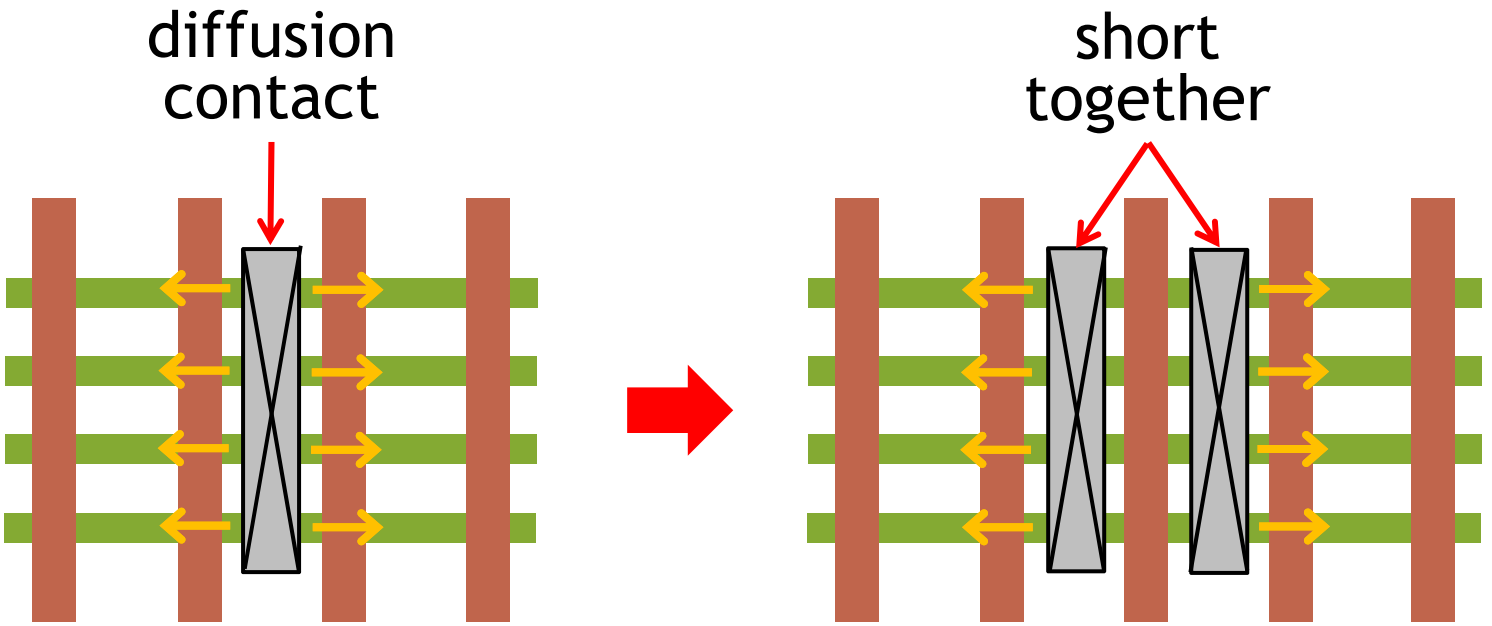
- S/D trench contacts & gate form vertical plate capacitors
- Worse supply rejection in LDO regulators
- Kickback noise to analog biasing signals, e.g., LPDDR RX
- Adding capacitance increases area & wake-up time (concern for burst-mode operation, e.g., IoT)





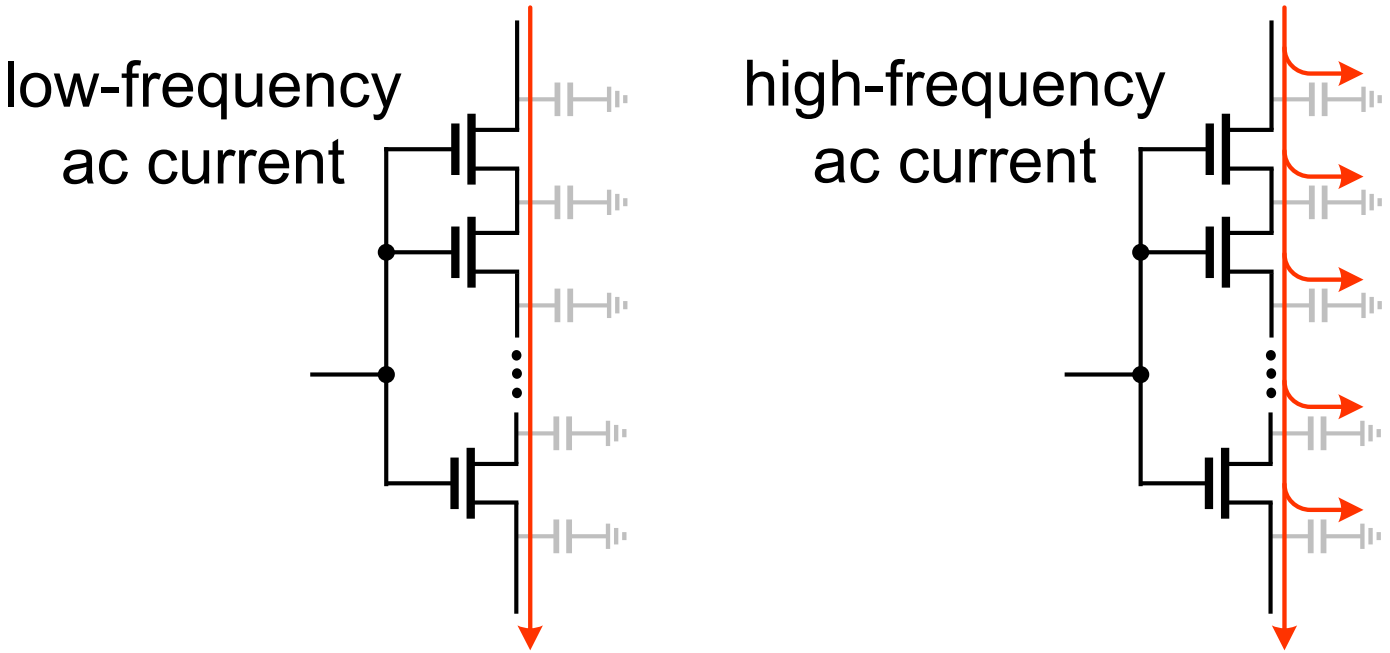
Dealing with High Series Resistance

- MEOL parasitic resistances very significant
- Double-source layout becoming common to halve S/D $R_{contact}$
- Drivers needs to drive very low impedances, e.g., 50Ω
- Better to unshare diffusions to reduce *R* despite higher *C*, contrary to "conventional wisdom"



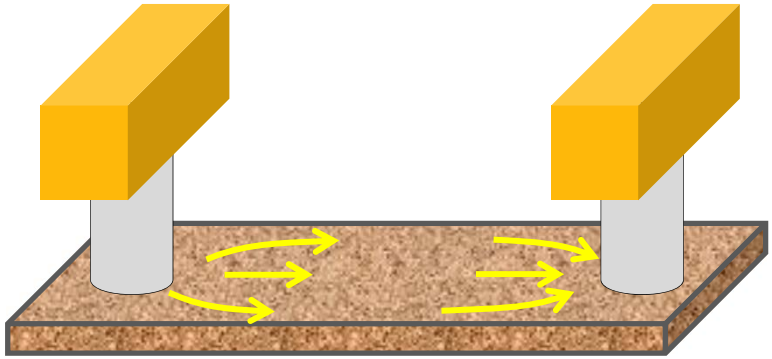
Stacked FET

- Ideal transconductor needs high r_{out} & long L
- L_{max} limited by gate litho/etch loading & HKMG integration
- Stacked FET is common but intermediate diffusion degrades r_{out} in GHz range
- Impact on intrinsic gain, common-mode noise rejection, …

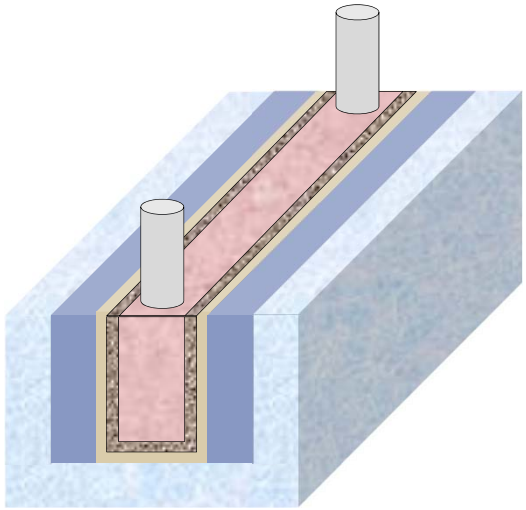


Resistor Options

- Precision MEOL resistor (thin metal compound on ILD0)
  - Difficult to build poly resistor ends in HK-last process
  - Ends not well defined, current spreading near contacts
  - Decouples resistor integration from FEOL

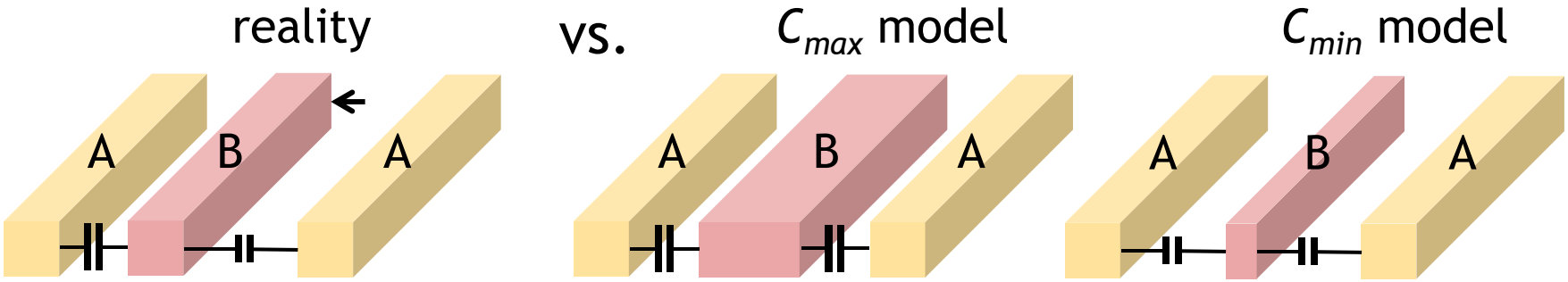


- Metal-gate resistor
  - Available for free
  - Not well controlled
  - ρ_{sheet} depends on gate density, W, W_{max} limit

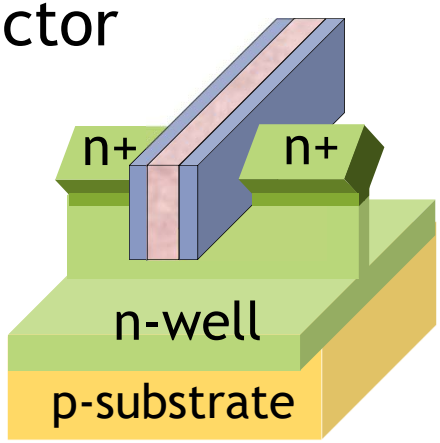


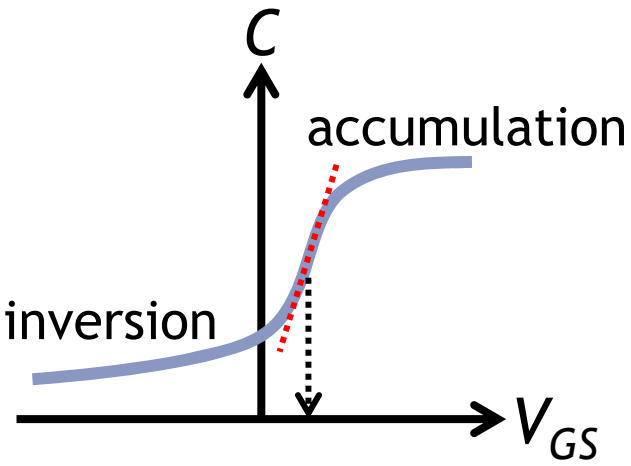
Capacitor Options

- Metal-Oxide-Metal (MOM) - Rarely has scaling helped analog ☺
  - Be careful with non-physical BEOL overlay corner models



- Accumulation-mode varactor
  - Steeper transition for higher K_{VCO}
  - Quarter-gap Φ_M gate material for higher V_T



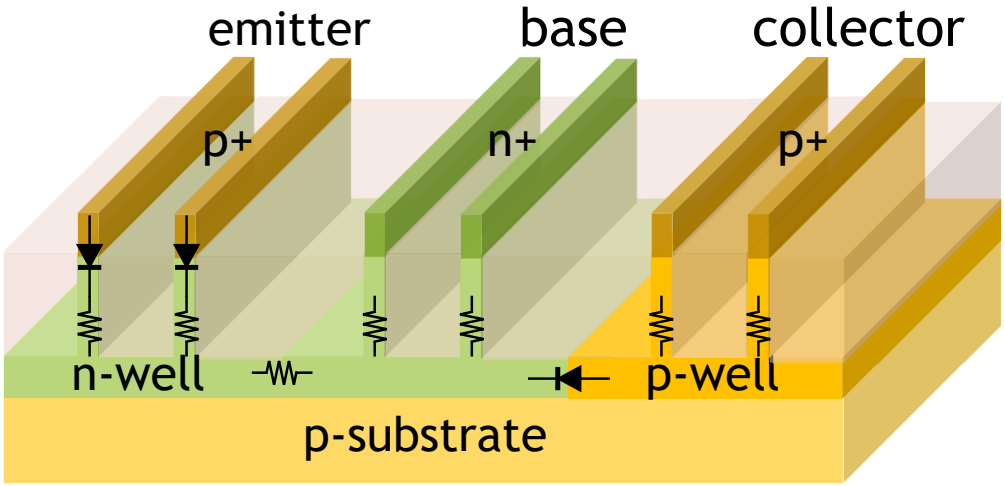


- Metal-Insulator-Metal (MIM) – Extra cost, less common

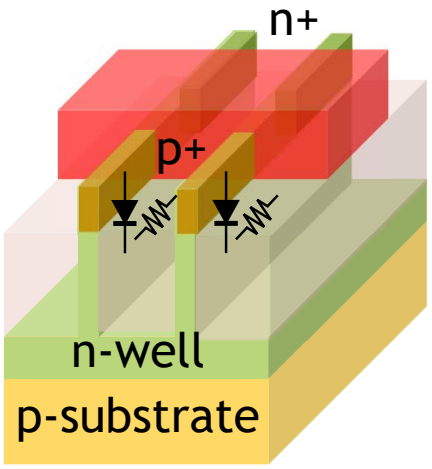
Chang *et al.*, UC Berkeley [20]

PNP-BJT & ESD Diodes

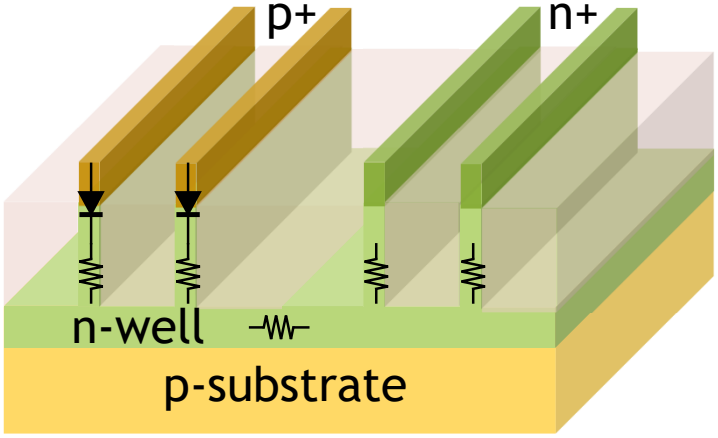
PNP-BJT



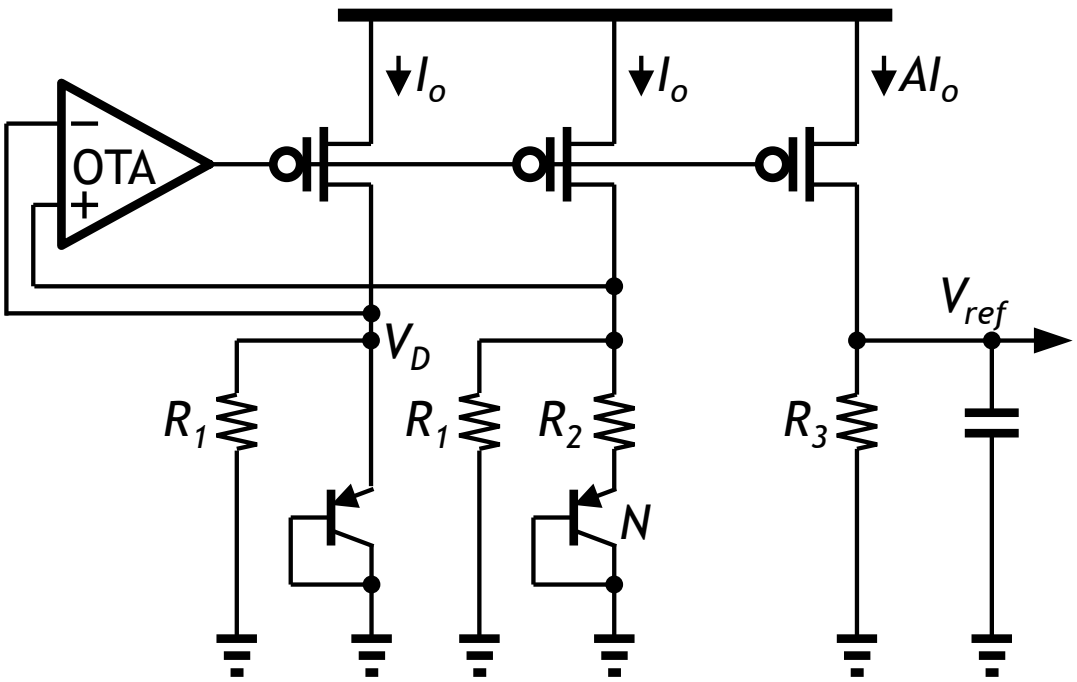
Gated ESD Diode

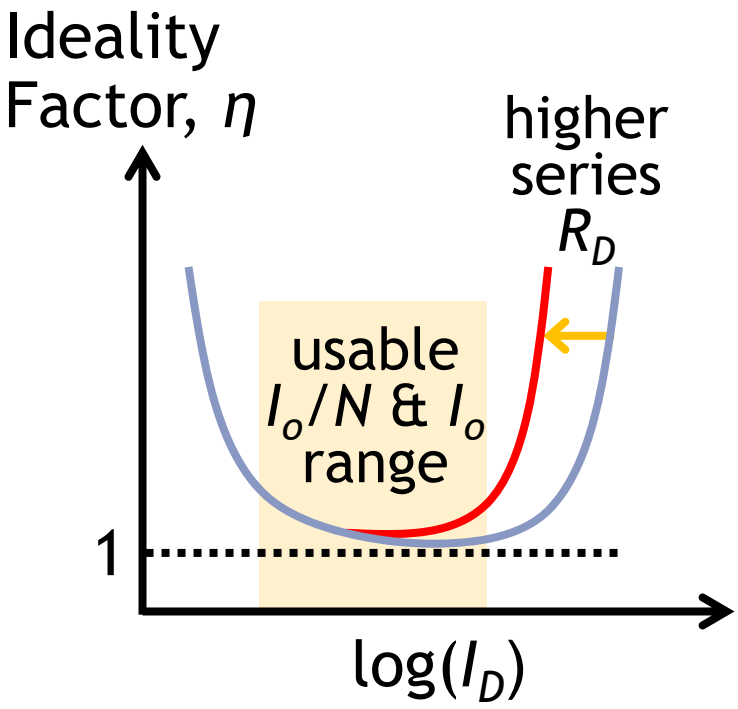


STI ESD Diode



Low-Voltage Bandgap Reference





$$V_{ref} = \underbrace{\frac{AR_3}{R_1}V_D}_{\text{CTAT}} + \underbrace{\frac{AR_3}{R_2}\frac{\eta kT}{q}\ln N}_{\text{PTAT}}$$

- PTAT+CTAT using currents
- More R_D → smaller N
- Higher V_D → headroom issue

Banba *et al.*, Toshiba [21]

I/O Voltage Not Scaling With Core Supply

- Many I/Os still use 1.8V signaling despite core V_{DD} reduction
  - Many peripheral ICs remain at lower cost nodes
  - Backward compatibility is key constraint for some I/Os
- Increasingly tough to keep 1.8V thick-oxide devices
  - Thick-oxide HKMG ALD fill not easy for tighter fin pitch
  - More complex level shifters to deal with wider voltage gap
  - Some standards no longer support legacy modes in favor of higher link rate & lower power (e.g., LPDDR5)
- Need ecosystem consensus
  - Industry has migrated from 5.0V to 3.3V to 2.5V to 1.8V
  - Obvious power & area benefit to migrate to say 1.2V
  - 1.8V remains an industry-wide issue until next transition

Wei *et al.*, Globalfoundries [22]

Considerations for HEP Application

- Significant logic area scaling migrating to finFET
  - Though not as good as 4x reduction from 28nm to 14nm (marketing)
- Mature 14nm & 10nm process
  - No model corner uncertainty → less overdesign & perf. compromise
- Hf-based HK gate dielectric reliability
  - May be prone to hysteretic (ferroelectric) polarization & worse BTI at high radiation levels, causing undesirable V_T shift
  - HK polarization issues resolved for "typical" CMOS usage
- Latch-up prevention
  - High fin resistance enforces stricter well-tie spacing & guard ring DRCs
- Beta ratio (NMOS-to-PMOS drive strength) → 1
  - Mechanical stressors & (110) fin sidewall much more effective to boost hole vs. electron mobility → strong PMOS
  - Circumvent need for pre-charge logic to get higher performance
- Device mismatch
  - Fully-depleted structure intrinsically superior (less/no RDF)
  - Benefit reduced by new mismatch sources (fin dimensional control, MG grain orientation, LDE sensitivities)

Conclusion

- 14nm mobile SoCs in production for 2+ years, 10nm SoCs in production for ½ year; no showstoppers to migrate AMS designs to finFET
- 16/14nm AMS design is about understanding all the scaling technologies that led to finFET as much as understanding finFET itself
- FinFET/HKMG/MEOL parasitics & local layout effects have significantly increased AMS design effort
- Logic & SRAM will continue to drive CMOS scaling priorities into 7nm & 5nm

References (1/2)

[1] E. Terzioglu, "Design and technology co-optimization for mobile SoCs," in *Int. Conf. on IC Design & Technology*, Keynote, Leuven, Belgium, Jun. 2015.

[2] R.-H. Yan *et al.*, "Scaling the Si MOSFET: From bulk to SOI to bulk," *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1704–1710, Jul. 1992.

[3] K. Fujita *et al.*, "Advanced channel engineering achieving aggressive reduction of V_T variation for ultra-low power applications," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, pp. 32.3.1–32.3.4, Dec. 2011.

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