Test beam studies of monolithic HV-CMOS pixel detectors for HL-LHC

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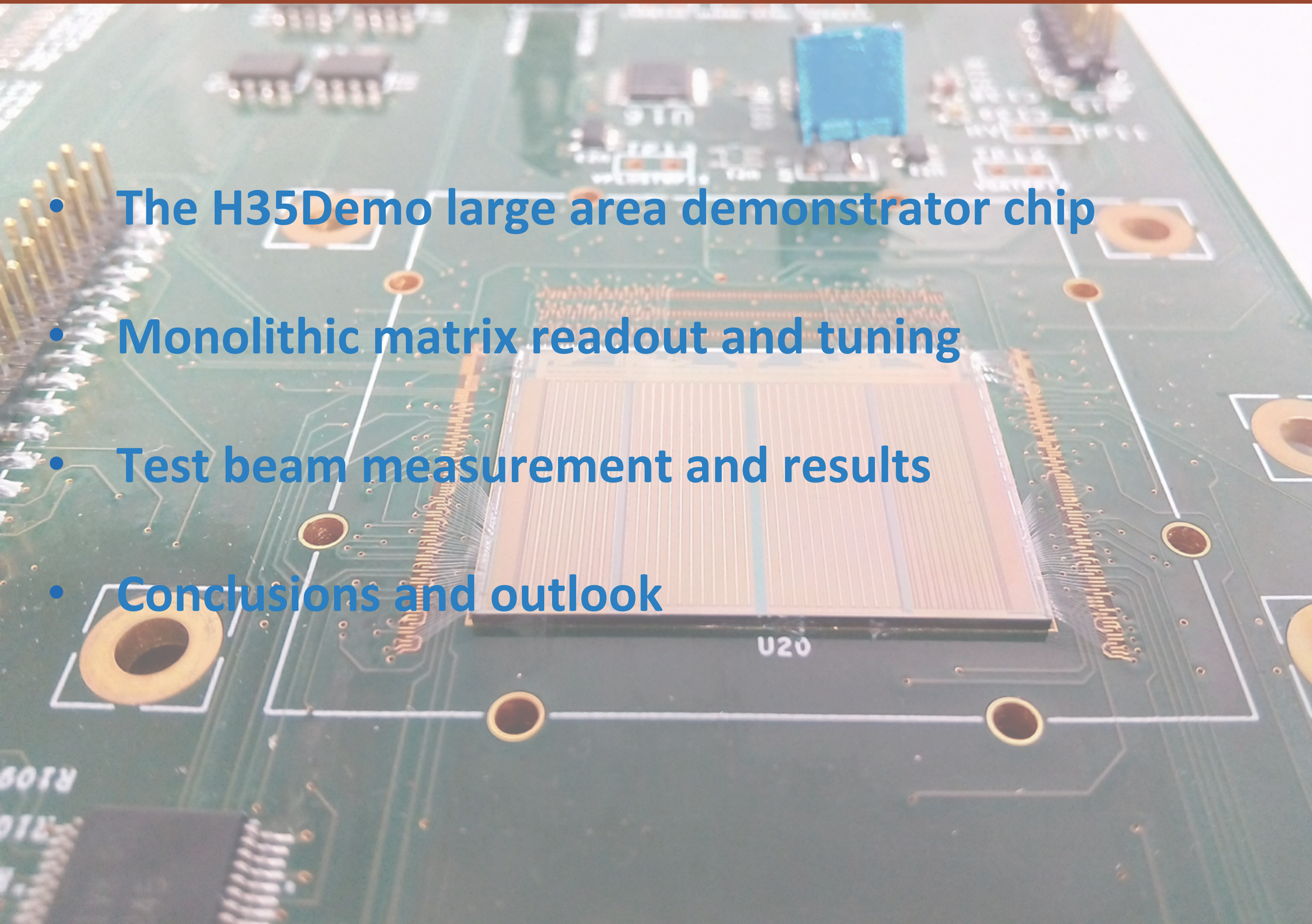
Test beam measurements in collaboration with University of Geneva

UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES

31th RD50 Workshop
CERN, 21th November 2017

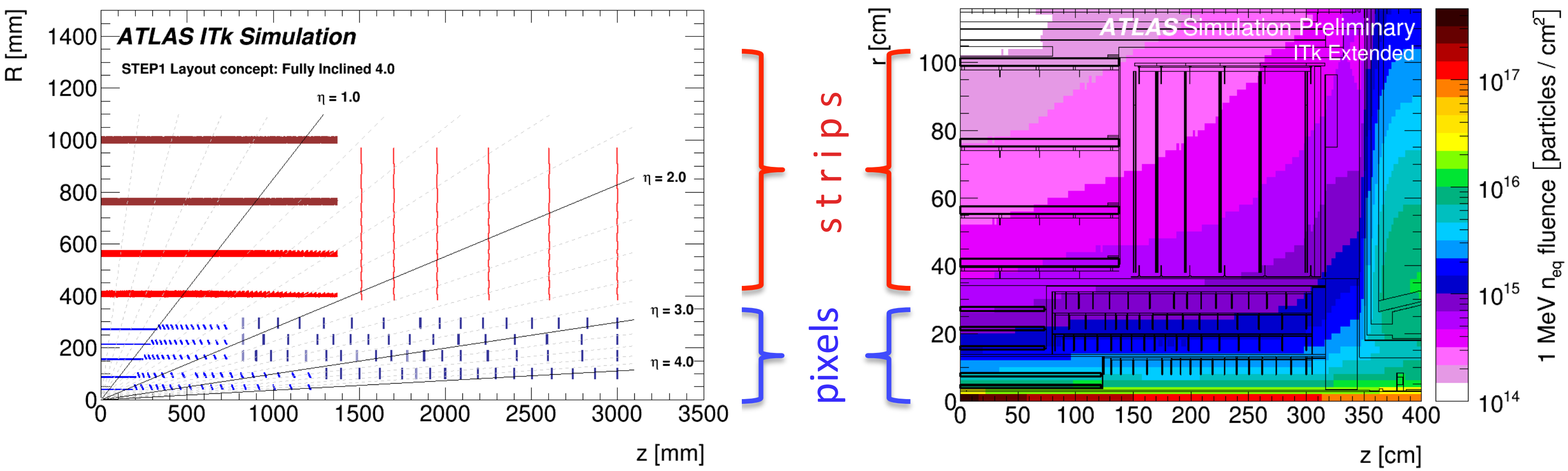
Outline



- The H35Demo large area demonstrator chip
- Monolithic matrix readout and tuning
- Test beam measurement and results
- Conclusions and outlook

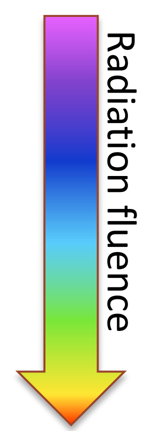
The ITk upgrade for HL-LHC

Replace the whole ATLAS Inner Detector with a new full-silicon Inner Tracker (ITk)



- New layout with 5 pixel barrel layers & large η coverage

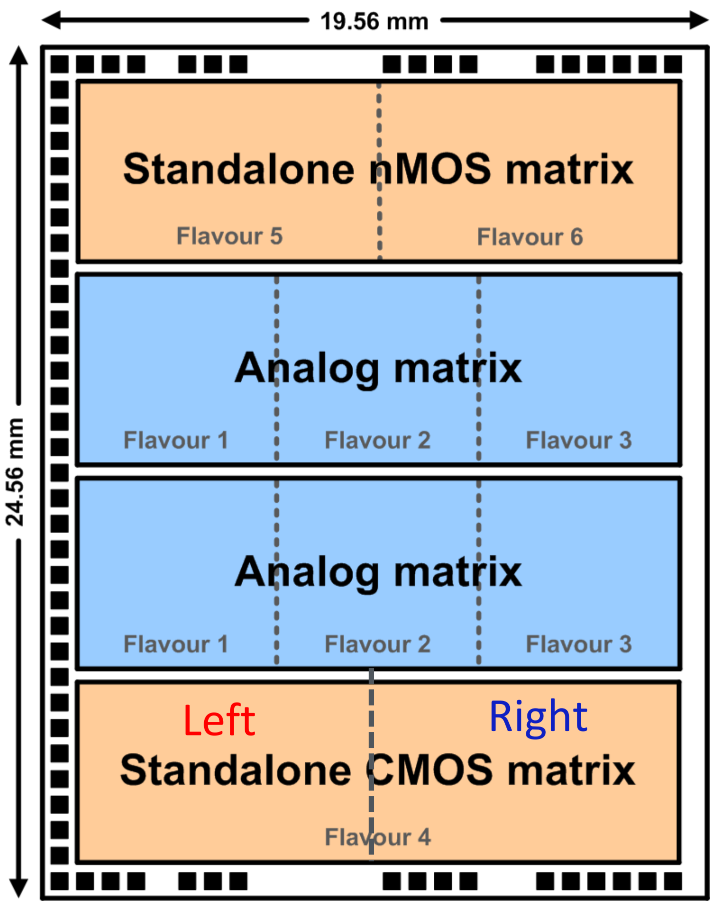
- Sensor technologies under investigation:
  - Outer pixel layers (large area to cover)
    - HR/HV-CMOS pixel detectors ➔ 1.5e15 $n_{eq}cm^{-2}$
    - n-in-p planar silicon sensors (150 µm thick)
  - Inner pixel layers
    - Thin n-in-p planar silicon sensors (100 µm thick)
    - 3D silicon sensors (baseline for the innermost layer)



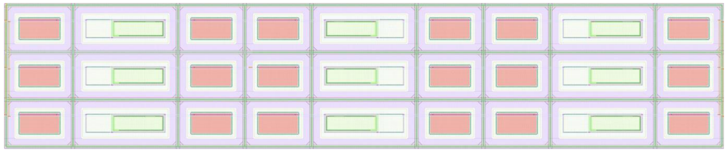
The H35 Demonstrator

AMS 350 nm High Voltage CMOS: different ρ: 20–80–200–1000 Ωcm

Designed by KIT, IFAE and Univ. of Liverpool



- Standalone nMOS matrix:
  - Digital pixels with in-pixel nMOS comparator
  - Two flavors: with and without Time Walk (TW) compensation
- Analog matrices (2 arrays):
  - To be Capacitive Coupled (CC) to FE-I4 readout chips
- Standalone CMOS matrix:
  - Analog pixels with off-pixel CMOS comparator:
    - 1 comparator in the Left part
    - 2 comparators the Right part



\+ test structures without electronics for TCT studies

S. Terzo (IFAE, Barcelona) – 31st RD50 Workshop, CERN

The H35 Demonstrator

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AMS 350 nm High Voltage CMOS: different ρ: 20–80–200–1000 Ωcm

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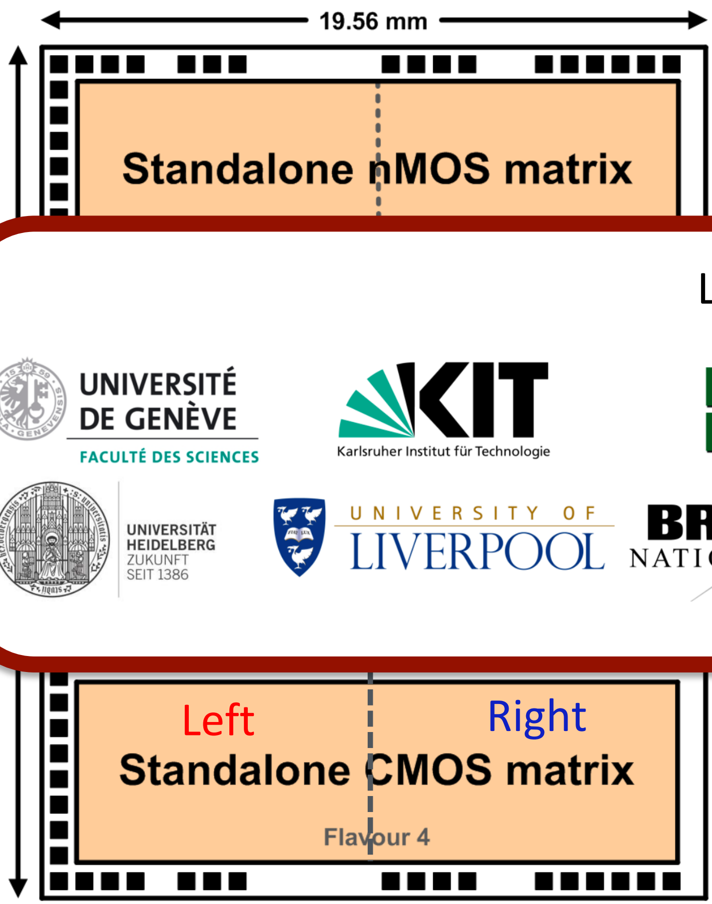
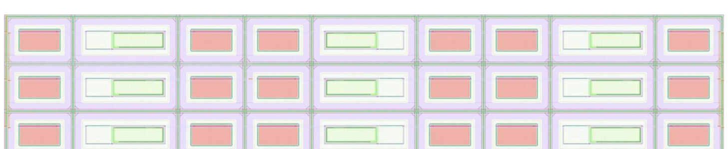


- Standalone nMOS matrix:
  - Digital pixels with in-pixel nMOS

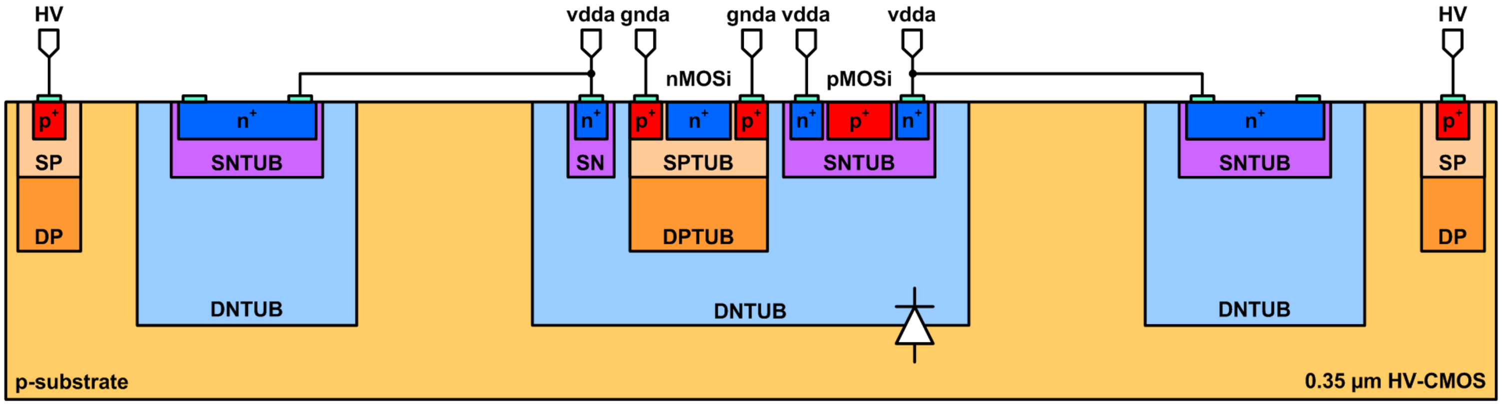
Large collaboration

- Analog pixels with off-pixel CMOS comparator:
  - 1 comparator in the Left part
  - 2 comparators the Right part



\+ test structures without electronics for TCT studies

The H35 pixel structure



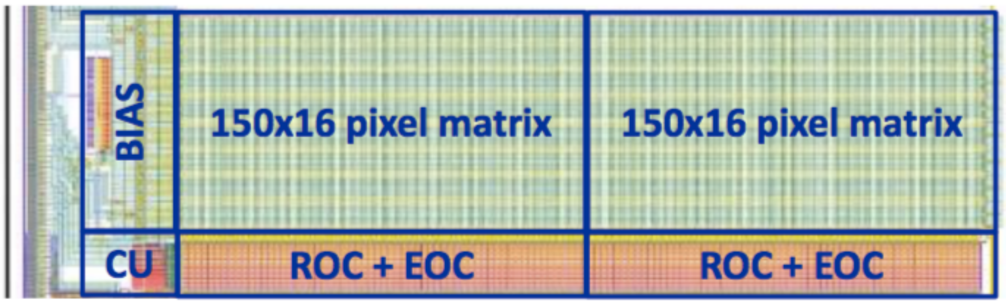
- Pixel size: 50x250 µm^2

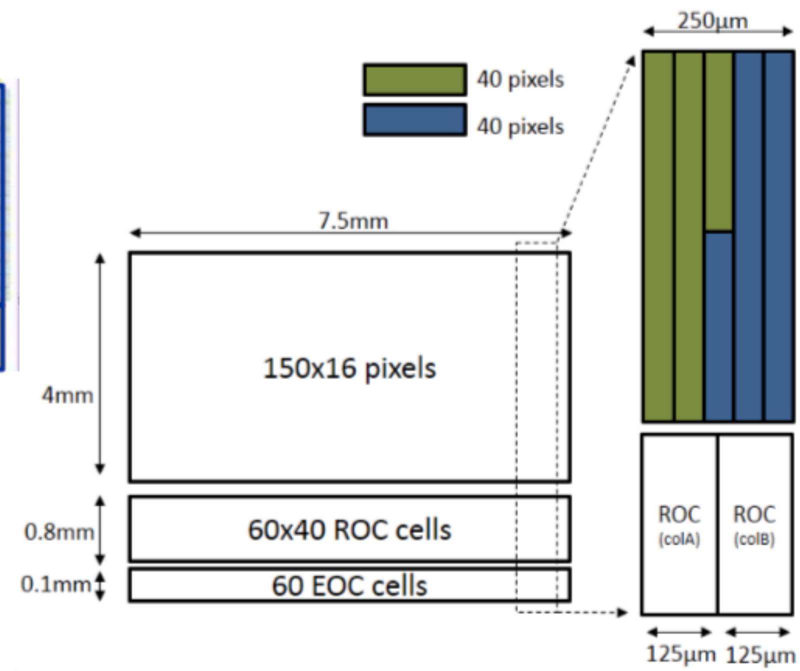
- Large fill factor: nMOS and pMOS transistors embedded in the same deep n-wells acting as collecting electrodes
    - p-substrate + 3 separate deep n-wells* to reduce the capacitance ➔ less noise, better timing - power consumption
    - Short charge drift ➔ reduced trapping after irradiation
    - More uniform electric field

- Bias voltage applied from the top
    - Single side processing
    - Bias voltage > 150 V

*all matrices but monolithic nMOS

The monolithic CMOS matrix

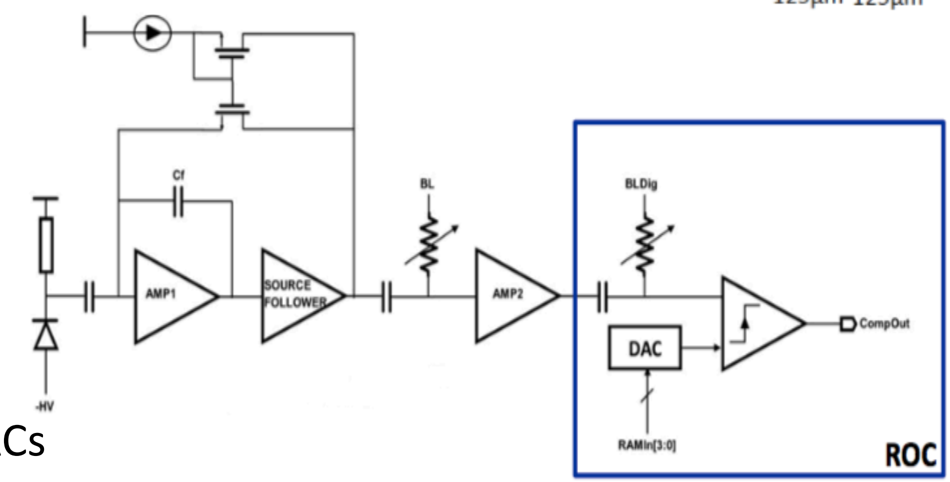




- Analog electronics on pixel

- Digital electronics in the periphery
  - ReadOutCell (ROC)
  - End Of Column (EOC)
  - Control Unit (CU)

- No discriminator on pixel:
  - Placed in the ROC
  - Both sides share the same global registers, but have different trim DACs
  - Difficult to optimize both sides at the same time → we privilege the left part

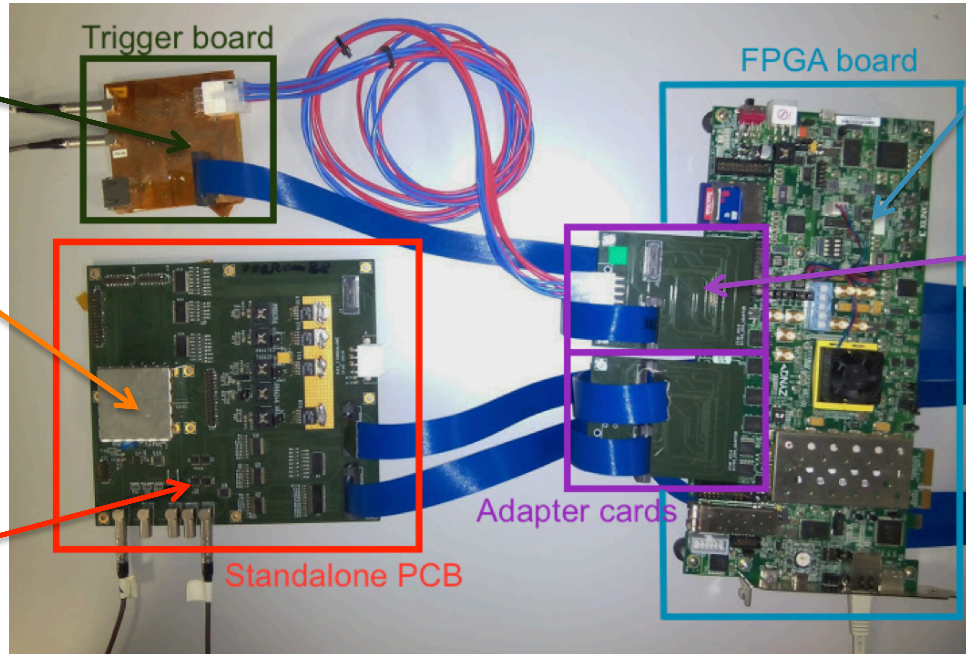


Monolithic matrix readout at IFAE

Trigger board
- Trigger in
- Busy out
- RJ45

H35demo chip
- Both CMOS and nMOS matrices wire-bonded

H35demo PCB
- Voltage regulators
- Sensor bias input
- Injection pulse input
- Analog signal output

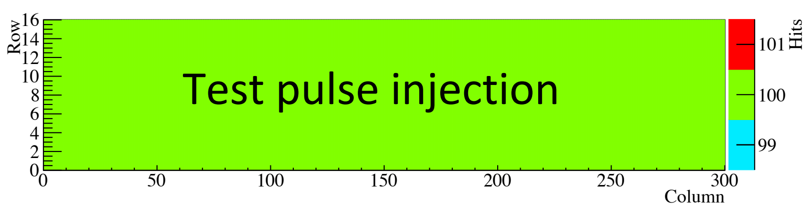


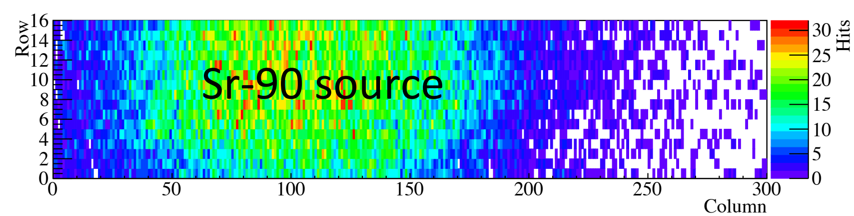
FPGA board
- Xilinx ZC706

Adapter PCBs
- 1x H35 PCB
- 1x test signals
- 1x trigger board

External
- Pulse generator
- Power supplies

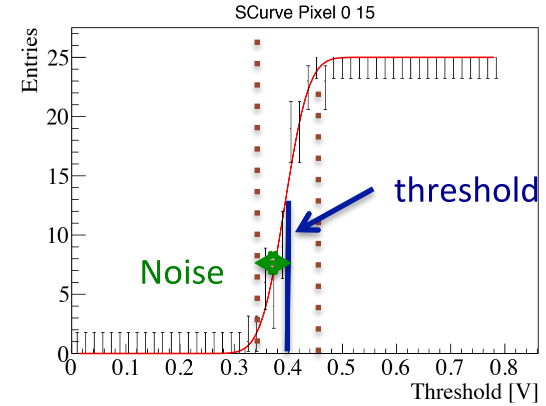
PCBs, FPGA firmware and software developed at IFAE



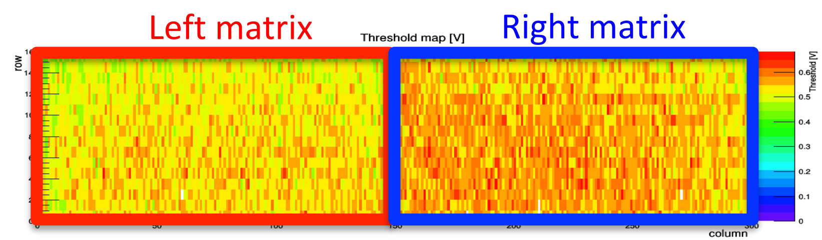


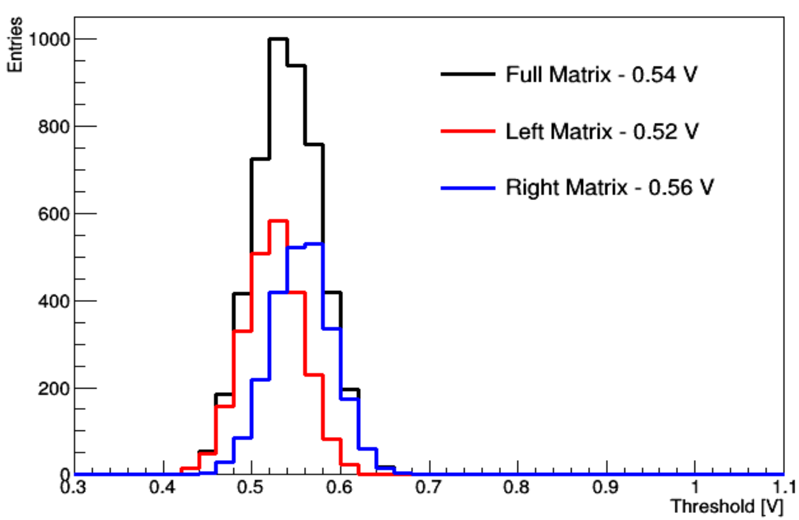
CMOS matrix tuning

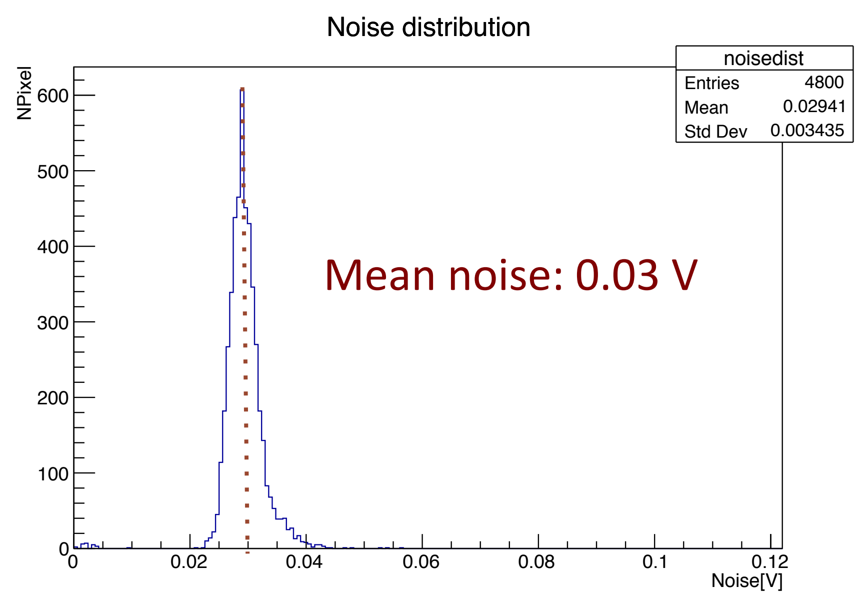
- Threshold tuning:
  - Global threshold tuned changing the in-pixel amplification
  - Off-pixel discriminator tuned to reduce the noise



- Not irradiated chips:
  - Noise = 29±3 mV
  - Threshold/noise > 17
  - Threshold in the right matrix usually systematically higher than in the left part







CMOS matrix tuning (irradiated)

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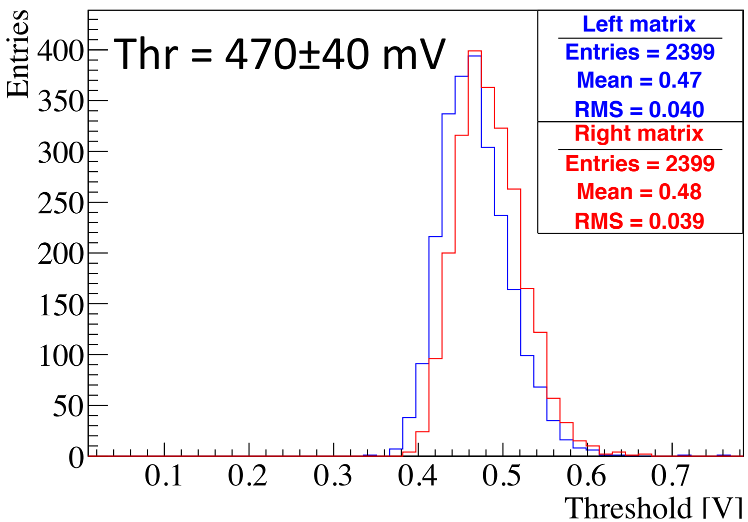
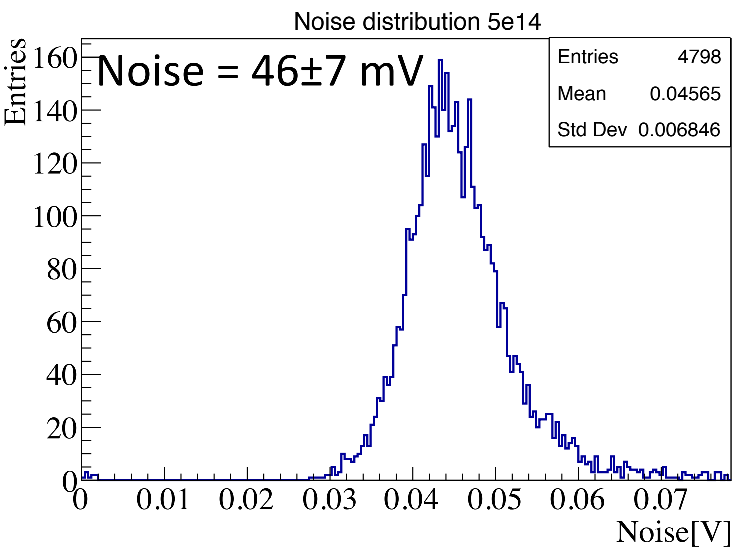
Irradiated to 5e14:

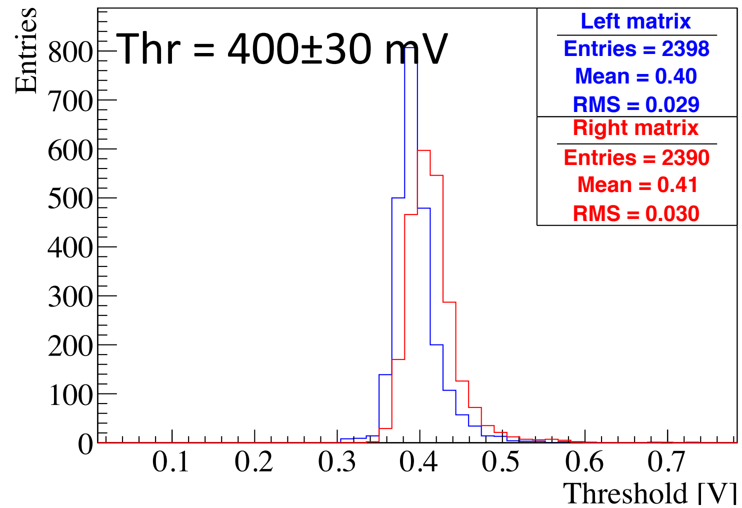
- Threshold settings: 5 mV
- Threshold/Noise > 10

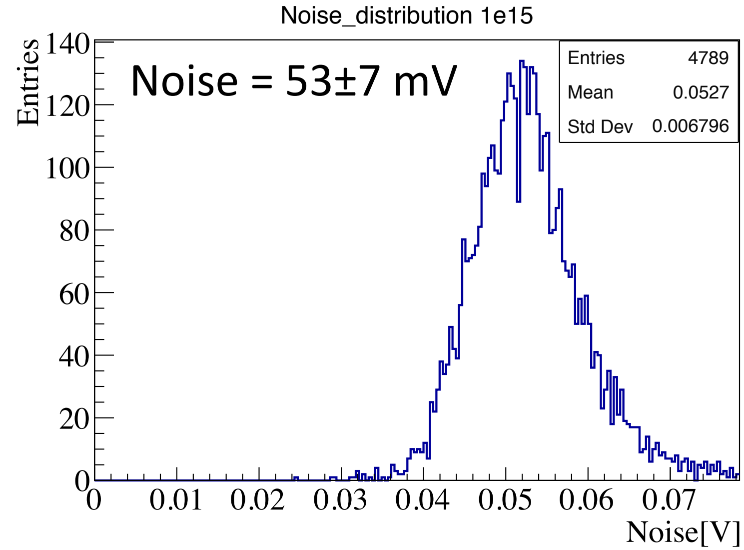




Irradiated to 1e15:

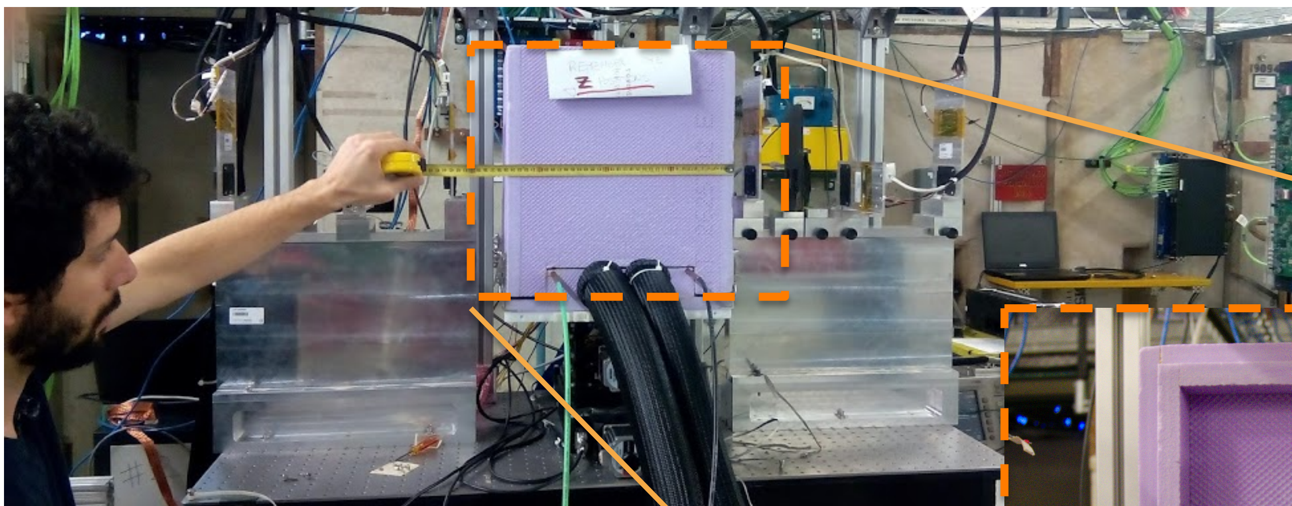
- Threshold settings: 5 mV
- Threshold/Noise > 7

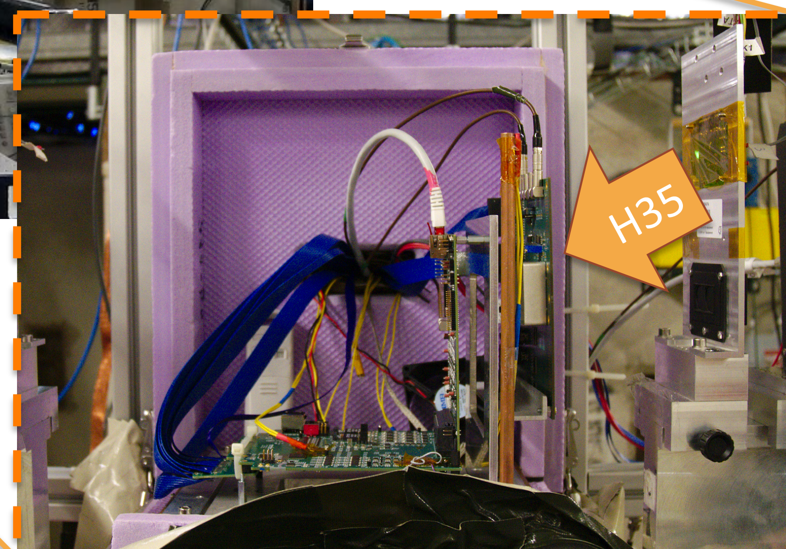




Test beam @ Fermilab

- Beam test @ Fermilab in April 2017
  - 120 GeV protons
  - In collaboration with University of Geneva & Argonne Laboratory
- Un-irradiated and very first time irradiated H35 monolithic matrices
  - IFAE readout system for the H35 monolithic matrices*
  - UniGe FE-I4 telescope** for tracking (6 planes)



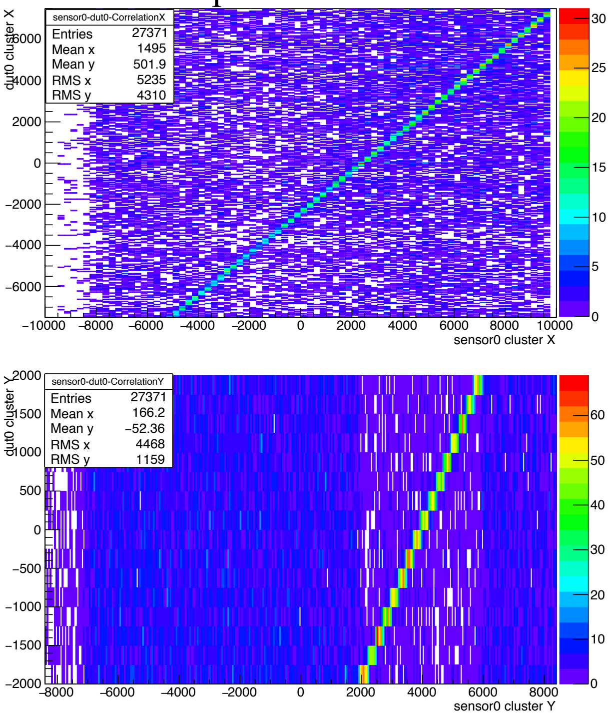


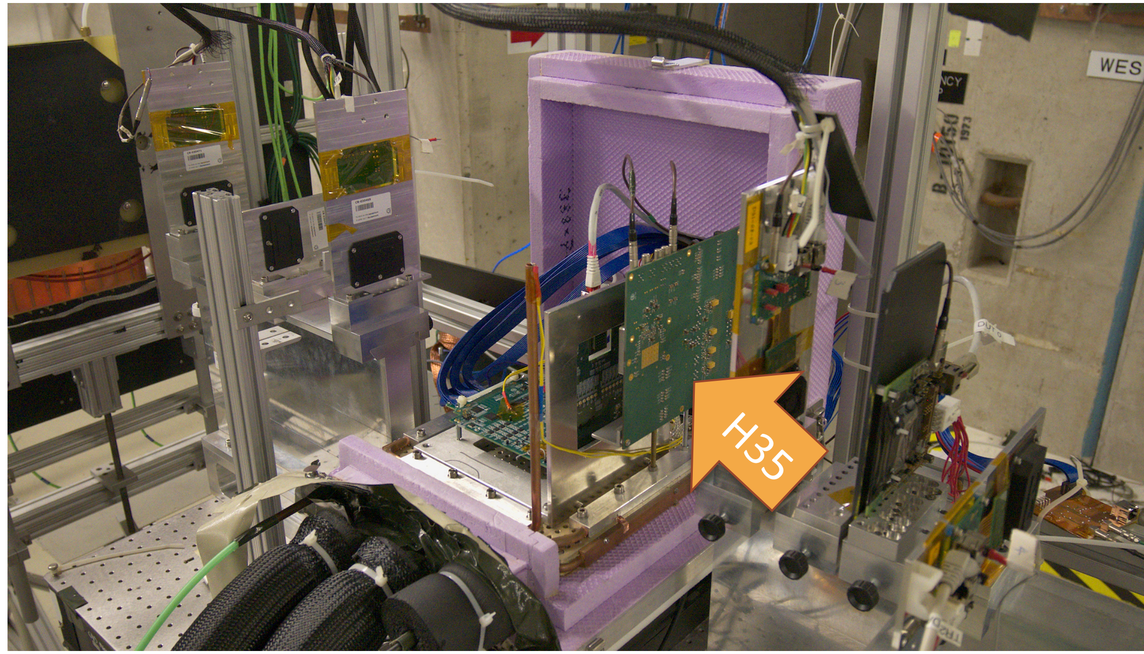
*S.Terzo et al., JINST 12 (2017) no.6, C06009

**M.Benoit et al., JINST11 (2016) no.7, P07003

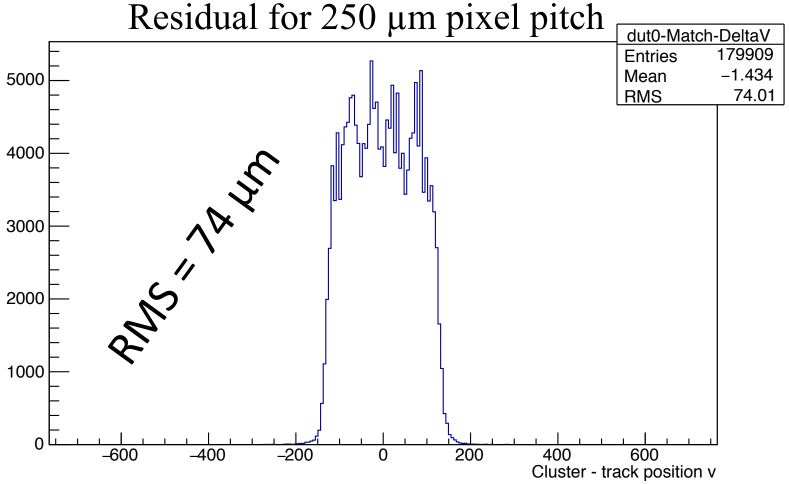
H35Demo integration

Telescope – H35 correlations

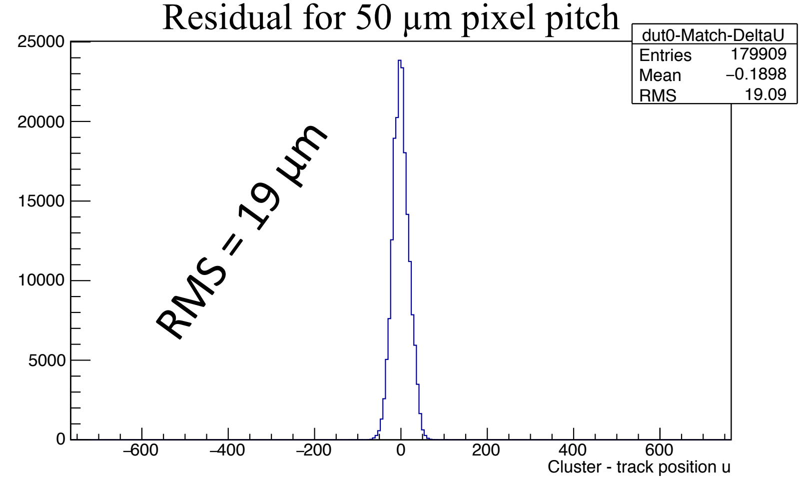




Residual for 250 µm pixel pitch

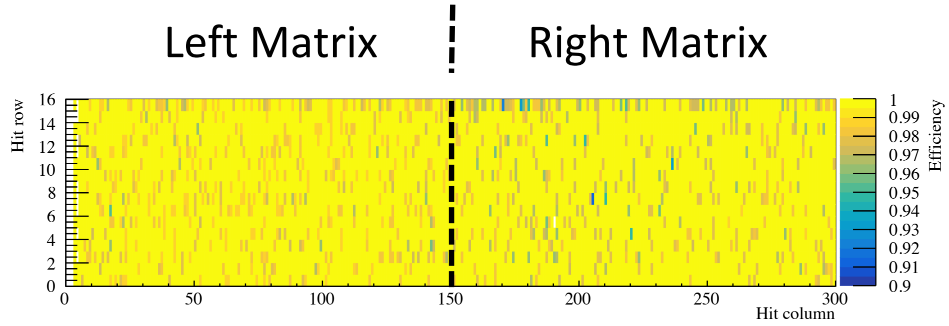


Residual for 50 µm pixel pitch

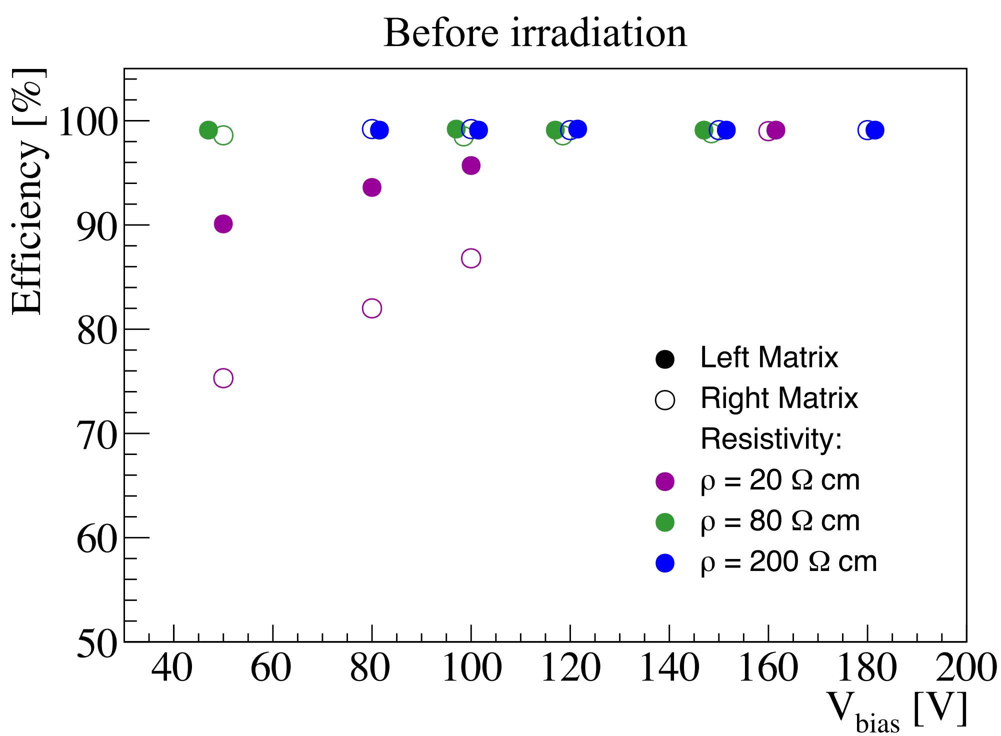


Hit efficiency results

- H35demo CMOS matrix:
  - Different resistivities: 20 – 80 – 200 Ωcm
  - Efficiency calculated separately for the left and right part of the matrix due to the different off-pixel comparator settings



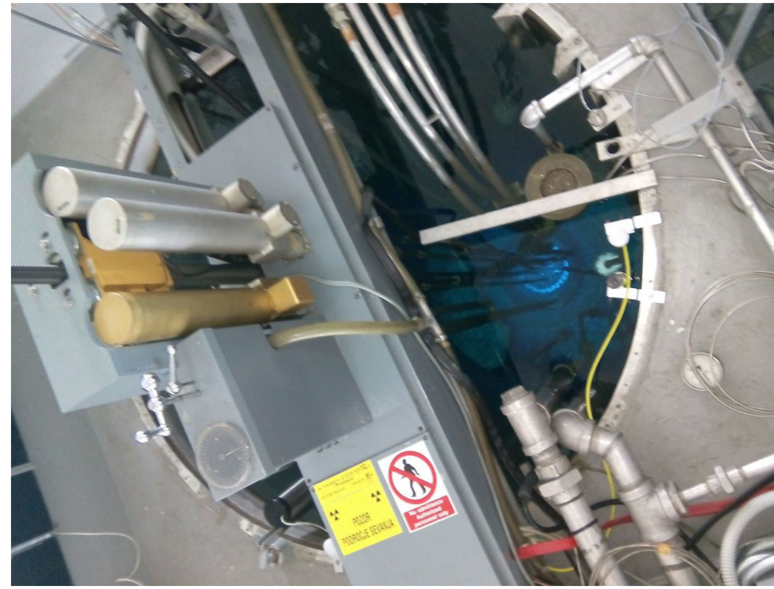
Efficiency map for 200 Ωcm @ 180 V



> Efficiency of >99% for sensors with resistivity >= 80 Ωcm
>
> 20 Ωcm samples need about 160 V to reach full efficiency

Irradiated detectors

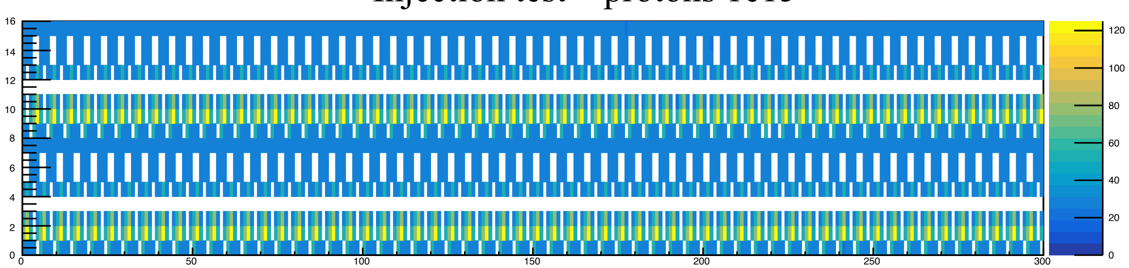
- 200 Ωcm chips have been irradiated with neutrons in the TRIGA reactor in Ljubljana up to 2e15 $n_{eq}cm^{-2}$



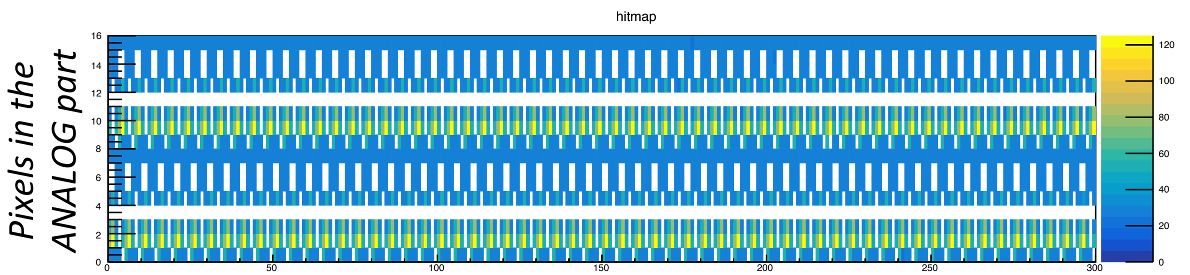
- And at KIT with 23 MeV protons up to 1e15 $n_{eq}cm^{-2}$

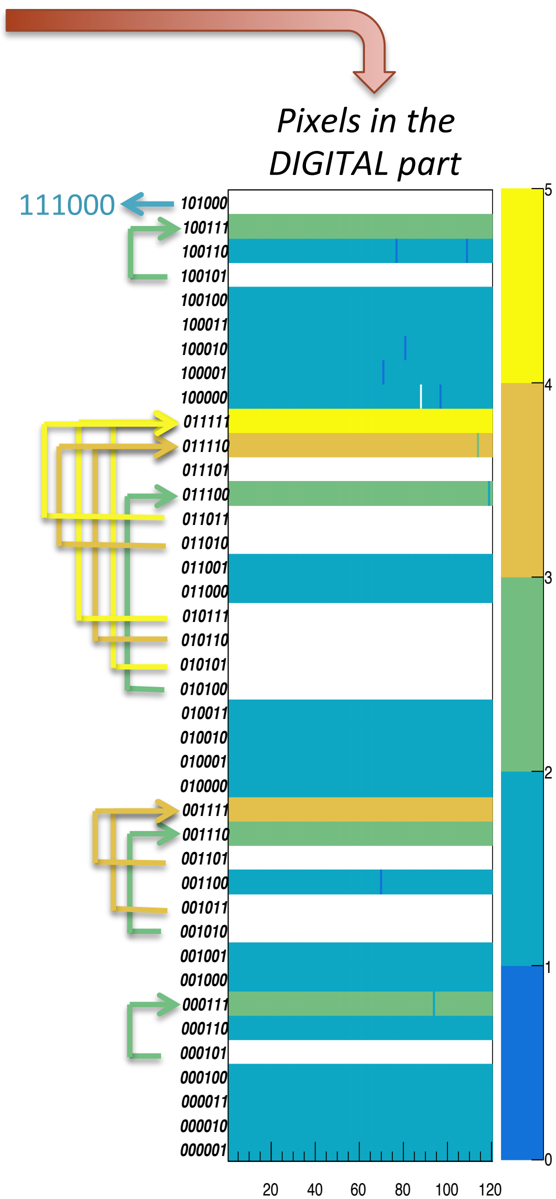
- We observed a digital pattern in the injection test:
  - After proton irradiation >=1e14 $n_{eq}cm^{-2}$
  - After neutron irradiation >=1e15 $n_{eq}cm^{-2}$ at low temperature
- The number of pixel misbehaving increases with the fluence and it is particularly enhanced for proton irradiations

Injection test – protons 1e15

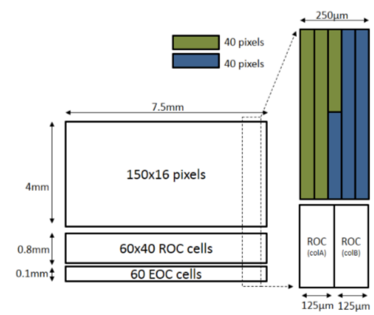


Address crosstalk





- The 16x300 analog pixels in the CMOS matrix are connected one-to-one to 40x120 pixels in the digital periphery



- The addresses are generated in the periphery with adjacent transistors

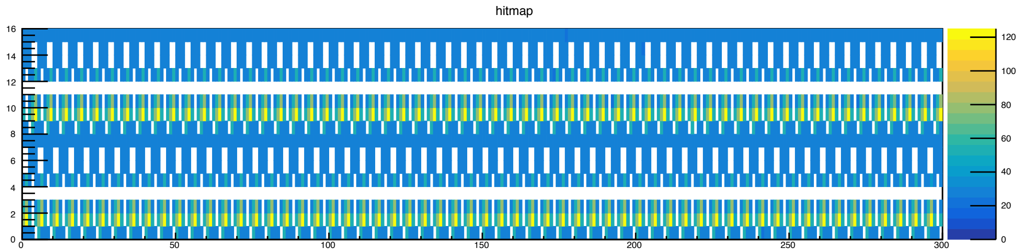
1 0 1
1-> 0 <-1
1 1 1

- Due to strong capacitive couplings between adjacent lines it is possible to have crosstalk between addresses

- This has been corrected in the design of the H18 ATLASPix1 by adding additional capacitors between the lines

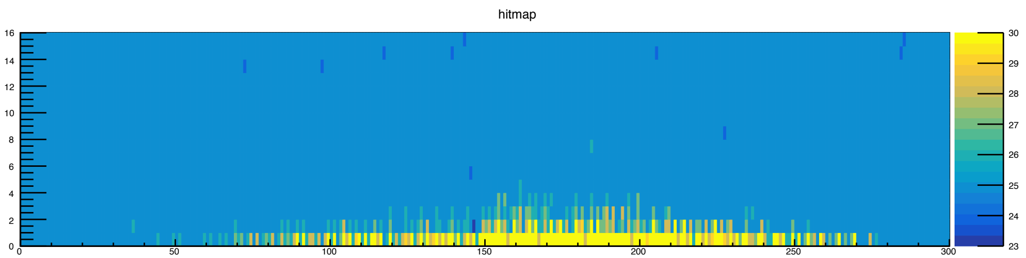
Solution

- Standard settings of the digital voltage: VDDD = 3.3V



- Increasing VDDD from 3.3V -> 5V

+1.7V



Noisy pixels in the first rows

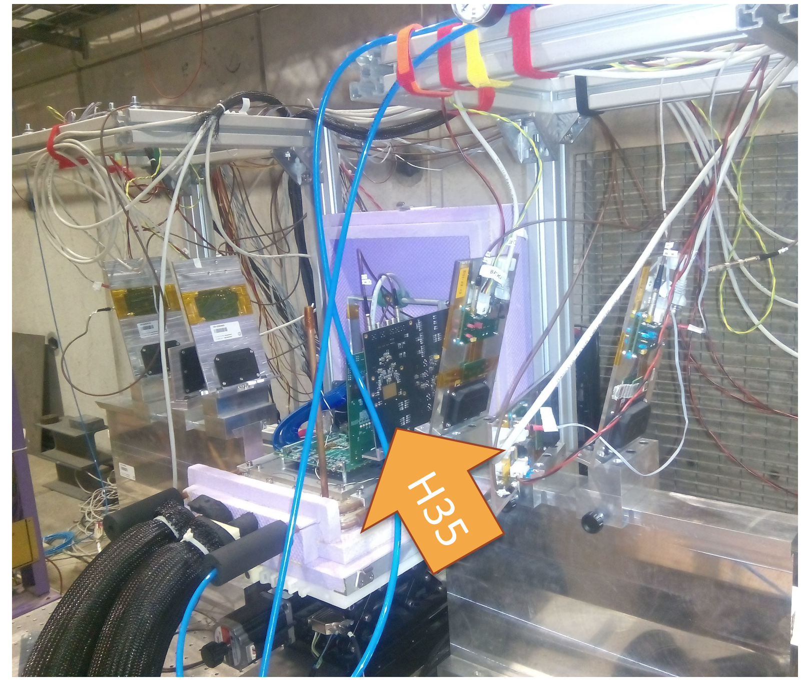
- The digital voltage needs to be increased depending on the irradiation levels:
  - Proton irradiated samples require very high VDDD which lead to a noise increase
  - Neutron irradiated samples require instead moderate VDDD increase (less than 4V)

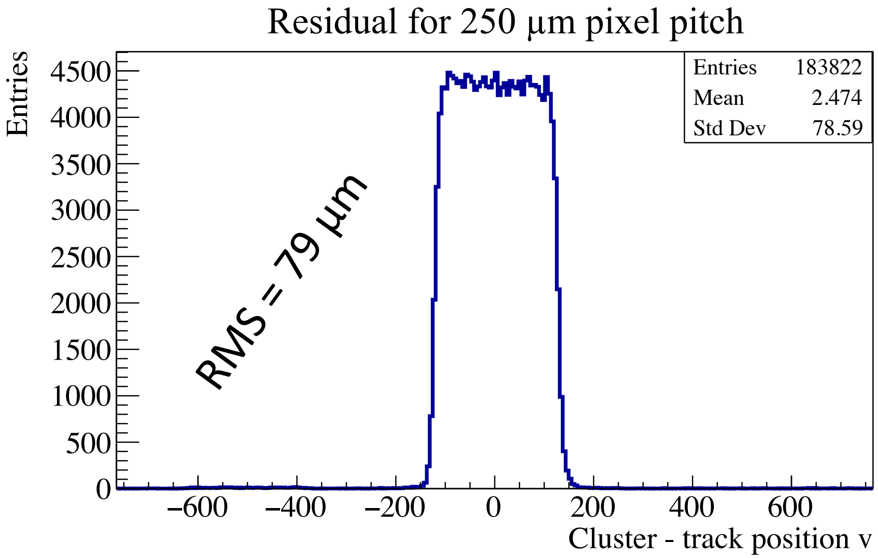
- The performance of these detectors will be studied in a test beam planned in DESY for next week

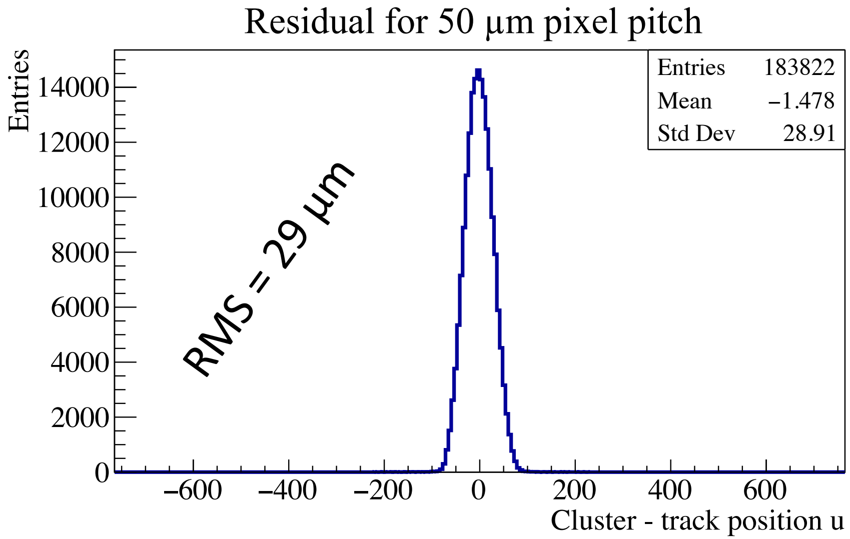
Test beam @ CERN SpS

- Beam test @ SpS in September 2017
  - 120 GeV protons
  - In collaboration with UniGe

- Irradiated H35 CMOS monolithic matrices
  - Sensor are cooled to about -20˚C
  - IFAE readout system for the H35 monolithic matrices
  - UniGe FE-I4 telescope for tracking (6 tilted planes)

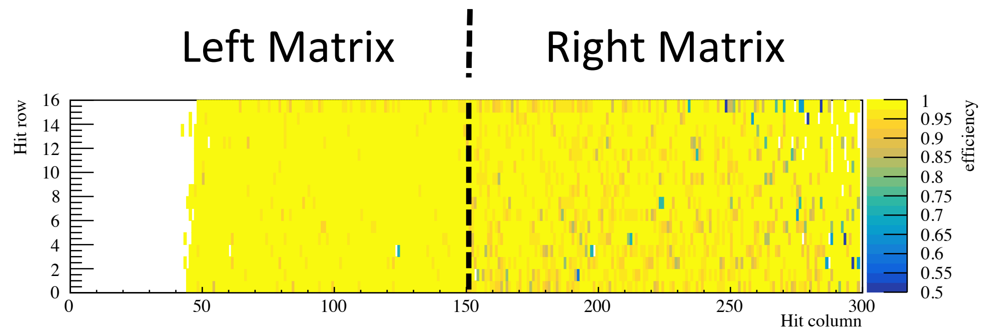




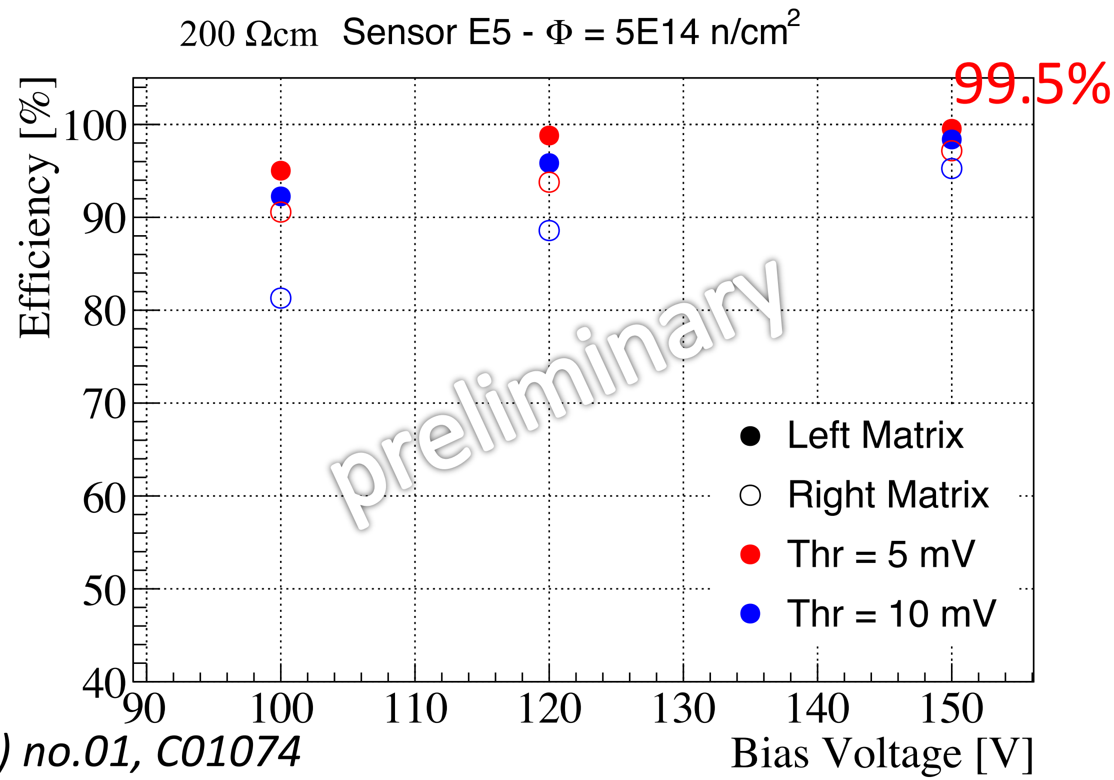


Efficiency irradiated 5e14

- 200 Ωcm sample irradiated with neutrons to 5e14 $n_{eq}cm^{-2}$
  - Depleted region of ≈50-60 μm at 120-150 V (from E-TCTs*)
  - Efficiency in the right matrix is systematically lower (different discriminator tuning in the digital periphery)



Efficiency map lowest threshold @ 150 V



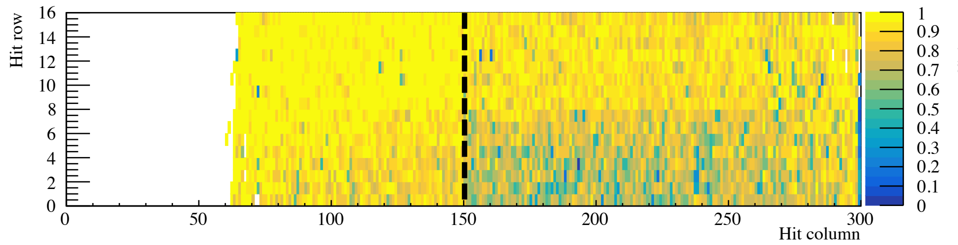
Efficiency of >98% with bias voltage of 120-150 V in the left matrix

*E.Cavallaro et al., JINST 12 (2017) no.01, C01074

Efficiency irradiated 1e15

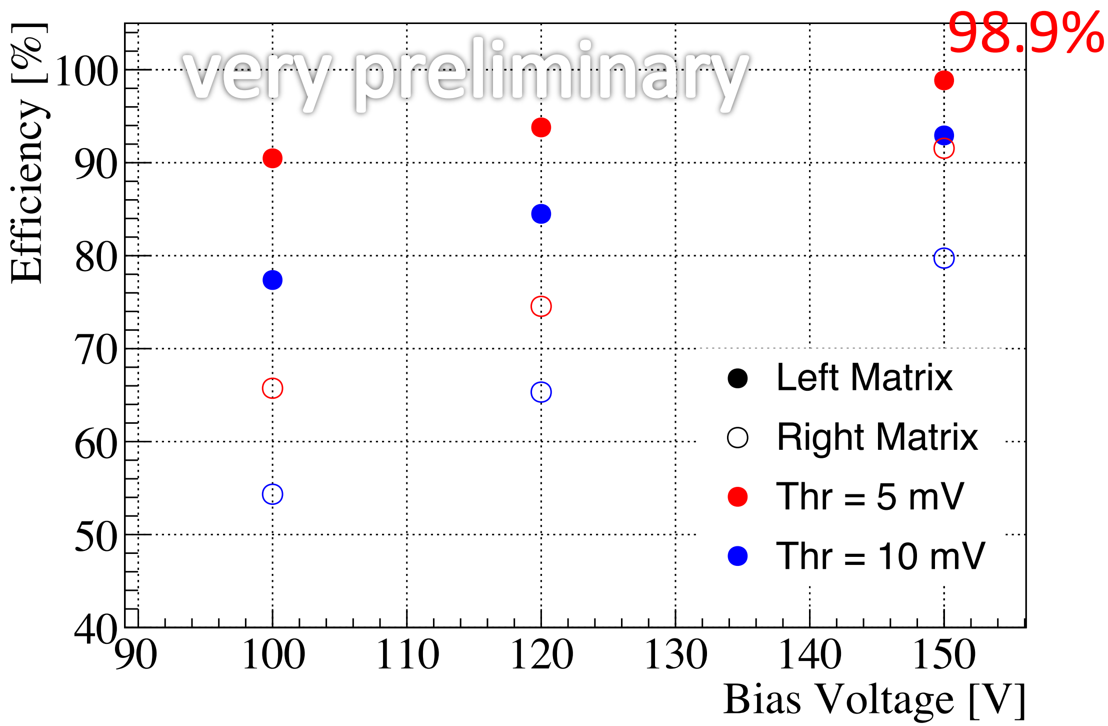
- 200 Ωcm sample irradiated with neutrons to 1e15 $n_{eq}cm^{-2}$
  - Depleted region of ≈60-70 µm at 120-150 V (from E-TCTs)
  - Strange up/down asymmetry still to be understood (possible mis-alignment?? Or crosstalk effect?)

Left Matrix | Right Matrix



Efficiency map lowest threshold @ 150 V

200 Ωcm Sensor E7 - Φ = 1E15 n/cm²



Efficiency of 99±1% in the left matrix with bias voltage of 150 V and the lower threshold settings

Conclusion & outlook

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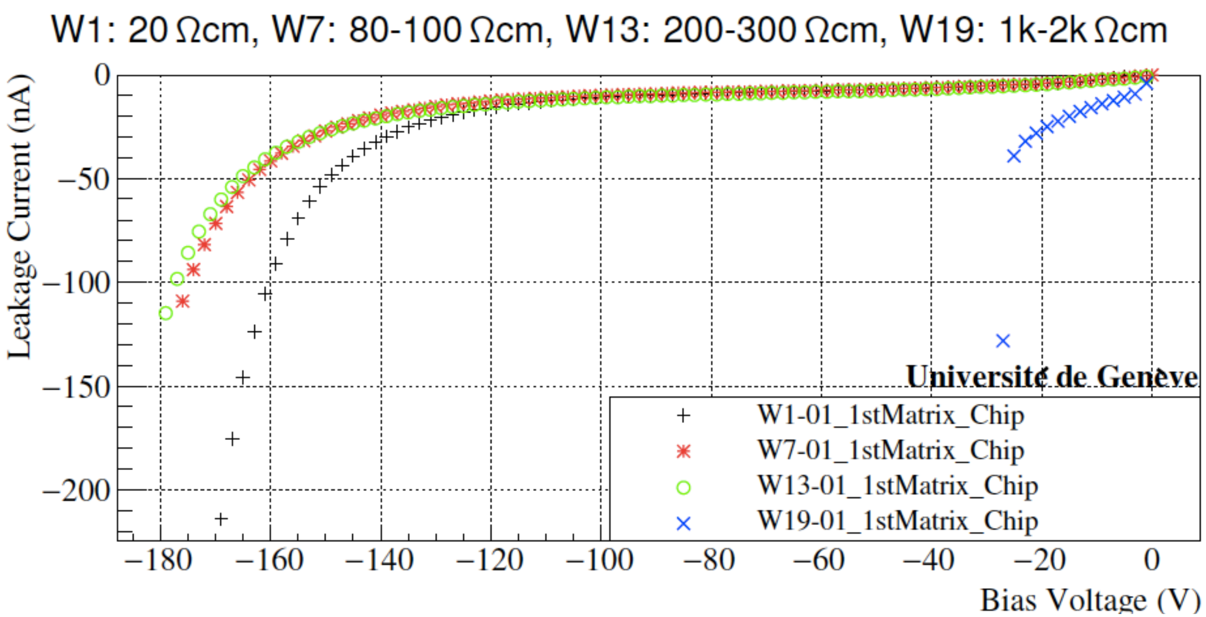
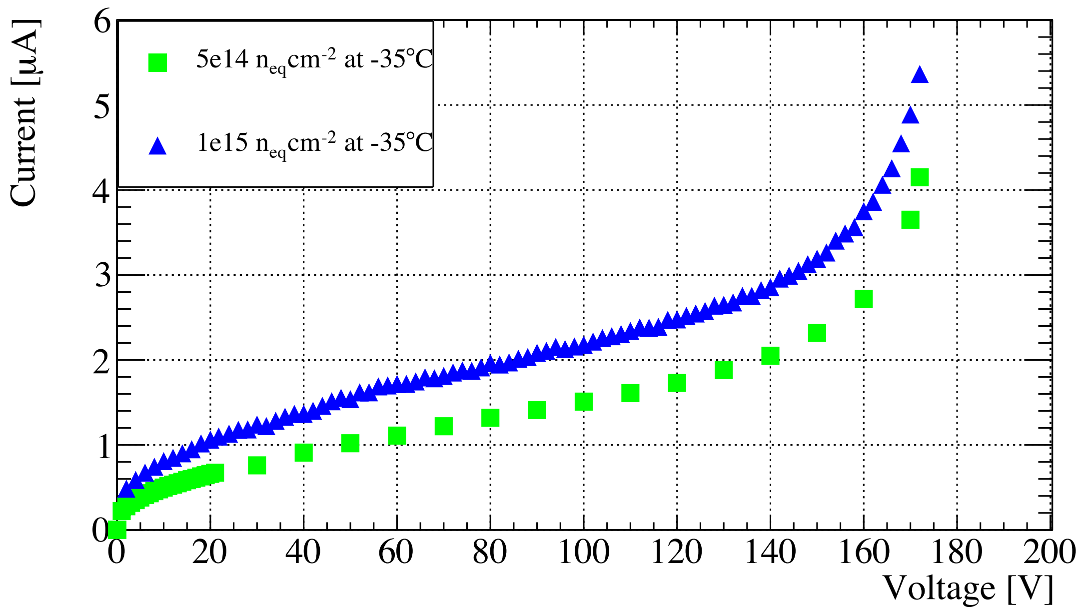
BIST

- Characterization of the H35Demo chip at IFAE
  - New readout system developed for the H35Demo monolithic matrices
    - Tuning and readout at 320 MHz clock (25 ns events)
  - Full efficiency measured before irradiation for chips with resistivity >=80 Ωcm with a bias voltage >= 50 V
- Very first result of irradiated fully monolithic HV-CMOS pixel detectors for ATLAS ITk
  - Measured 200 Ωcm samples after neutron irradiation to 1e15 $n_{eq}cm^{-2}$
    - Preliminary results show the possibility of reaching an efficiency of about 99% operating the detectors with a bias voltage of 150 V
- What's next:
  - Explore the limits of the H35Demo chip technology while waiting for the new ATLASPix designs in 180 nm
  - Test beam @ DESY at the end of November:
    - Neutron irradiated chips up to 2e15 $n_{eq}cm^{-2}$
    - Proton irradiated chips up to 1e15 $n_{eq}cm^{-2}$

Backup

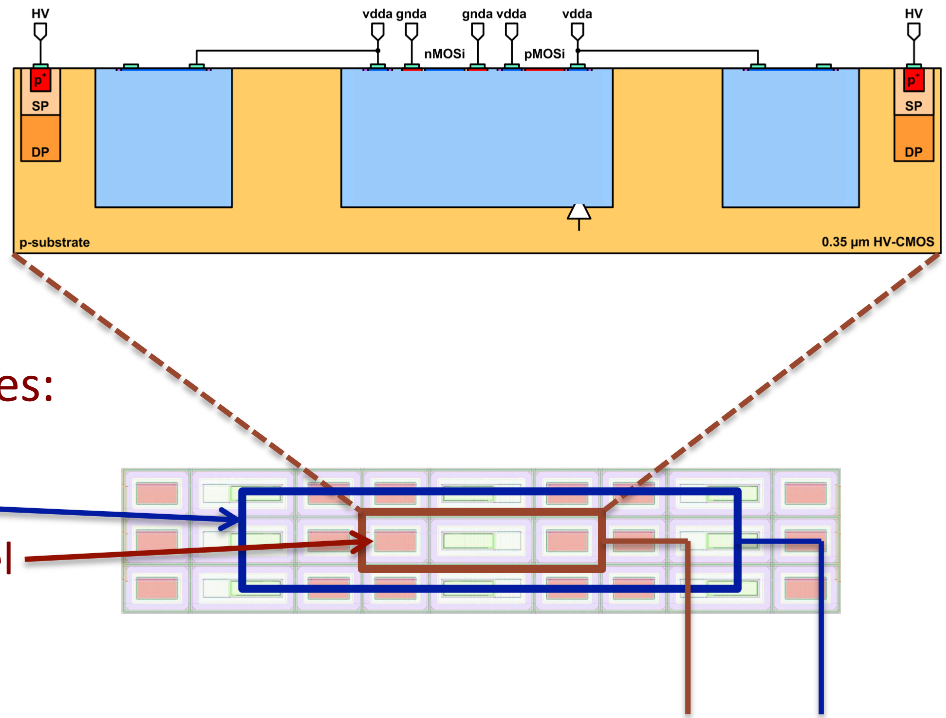
H35 – matrix IVs





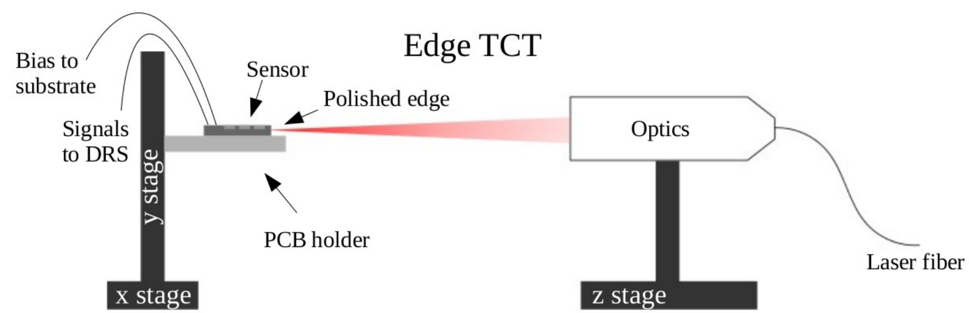
Sensor characterization

- H35 pixel cell structure
  - p-substrate + 3 deep n wells
    - ➢ Lower capacitance (noise, timing)
    - ➢ Reduce trapping
  - Bias from the top -> single sided



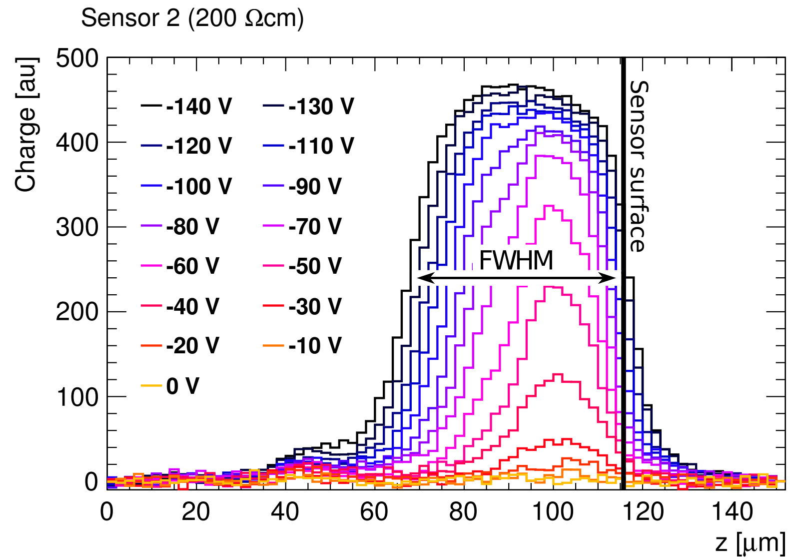
- Characterization of H35 test structures:
  - 3x3 pixel structures w/o electronics
  - External pixels shorted together
  - Separate readout of the central pixel
  - ρ= **80 Ωcm** – **200 Ωcm** – **1 kΩcm**

- The Edge-TCT setup:
  - Infra-red laser (1064 nm)
    - Beam spot about 10 µm FWHM
    - Pulses of about 500 ps
  - Readout: DRS4 evaluation board
    - 700 MHz bandwidth
    - 5 GSPS
    - 200 ns sampling depth
    - Four channels: 1 × trigger, 1 × beam monitor, 2 × readout



Depletion: before irradiation

- Depletion depth is defined by the FWHM of the charge collection profile

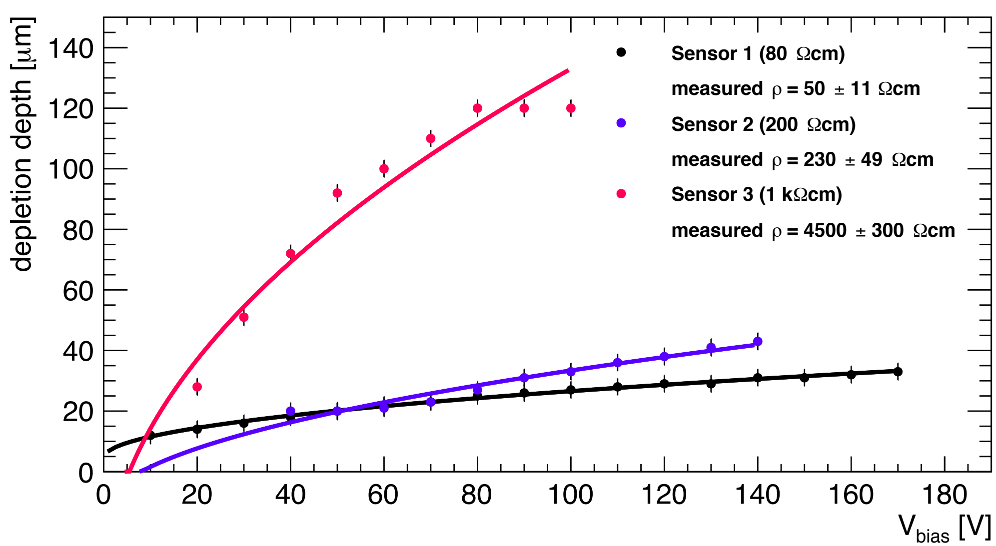


- Resistivity obtained fitting the depletion depth as a function of the bias voltages

$$d(V) = d_0 + \alpha\sqrt{\rho V}$$

with $\alpha = \sqrt{2\varepsilon\varepsilon_0\mu}$

	ρ nominal	ρ measured
Sensor 1	80 Ωcm	50 ± 11 Ωcm
Sensor 2	200 Ωcm	230 ± 49 Ωcm
Sensor 3	1000 Ωcm	4500 ± 300 Ωcm



Depletion: before irradiation

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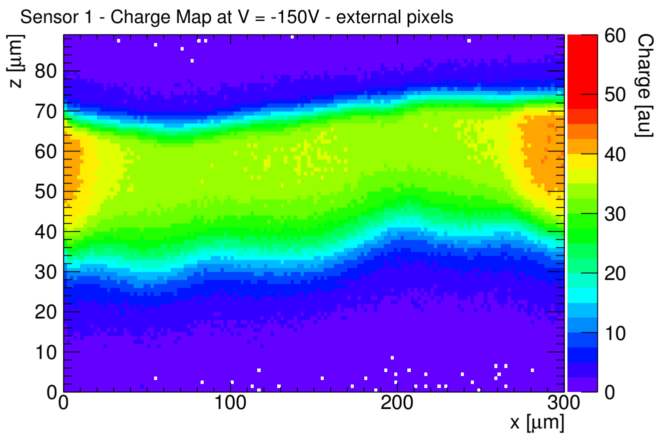
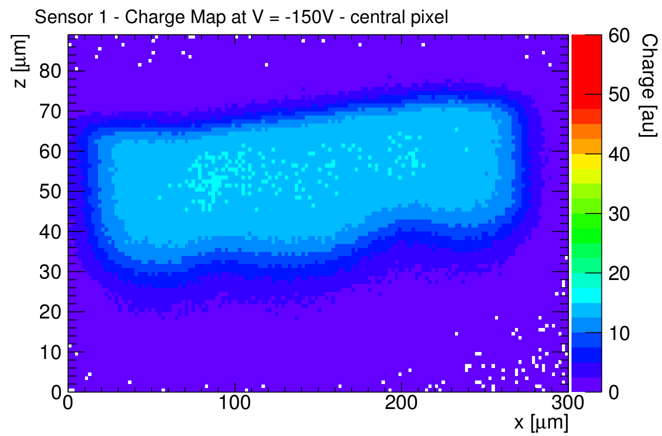
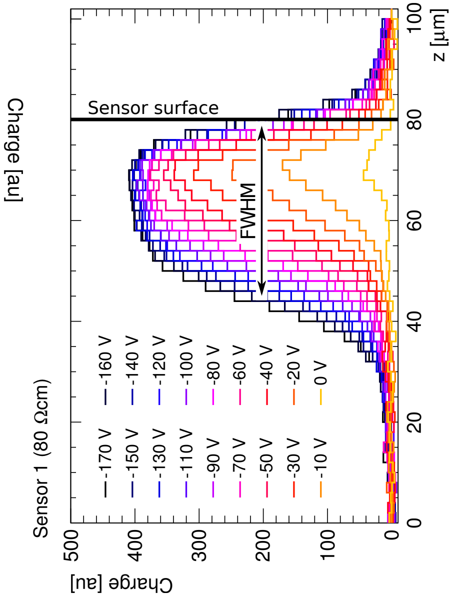
80 Ωcm



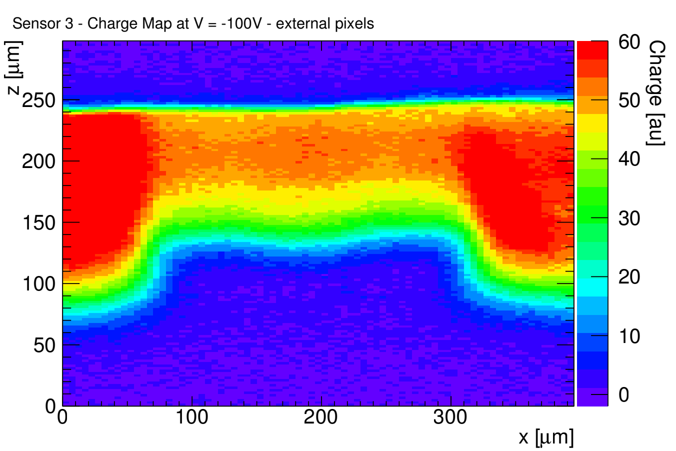


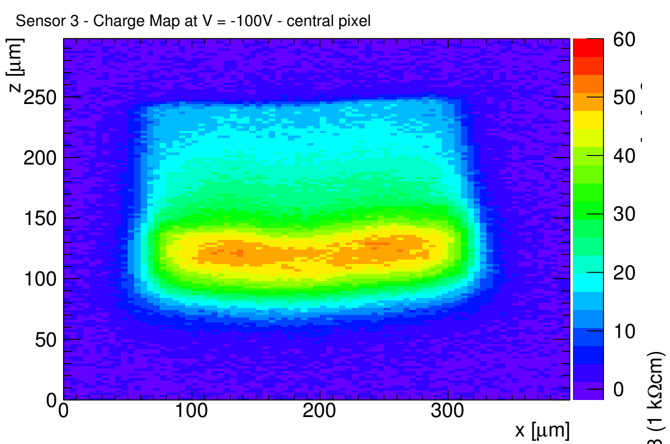


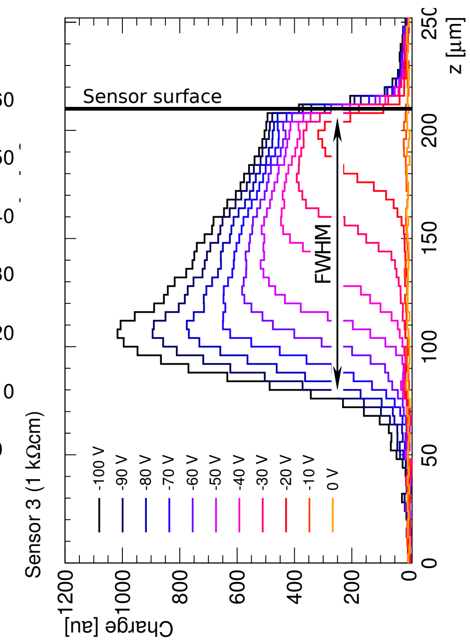
External pixels

Central pixel

1000 Ωcm







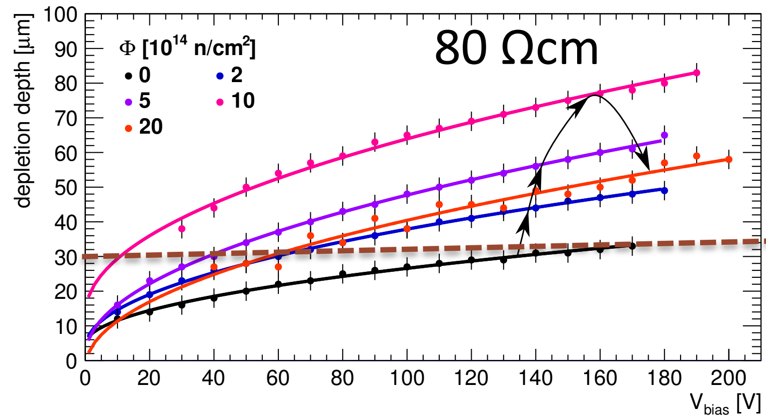
When depletion gets larger of 100 µm the central pixel starts to collect charge from the neighboring pixels

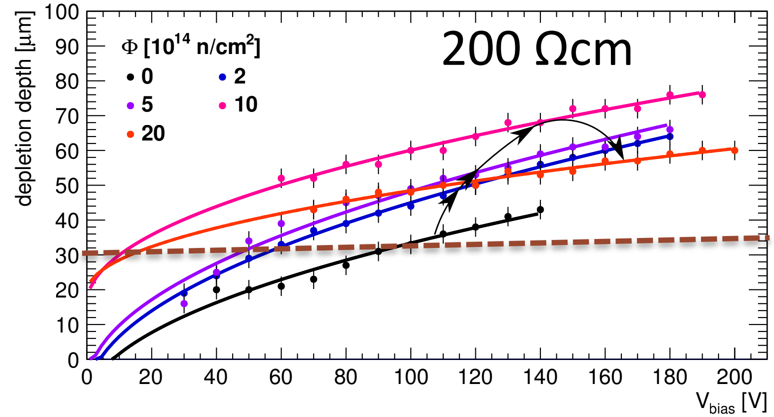
Depletion: after irradiation

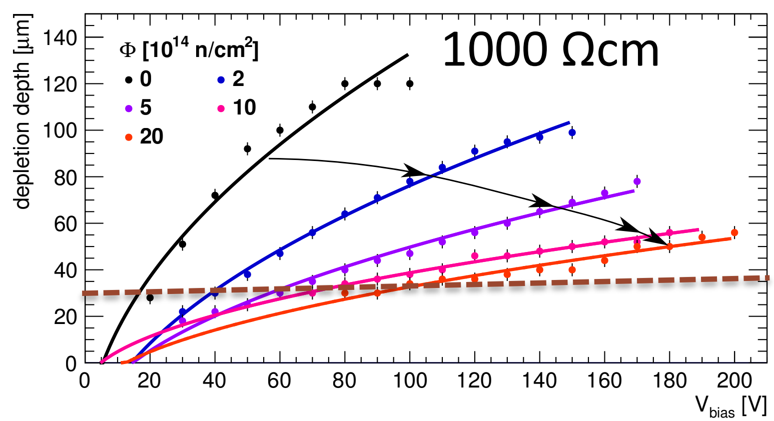
- Irradiation at the TRIGA neutron reactor at JSI, Ljubljana:
  - Now: **2e14**, **5e14**, **10e14**, **20e14** $n_{eq}cm^{-2}$
  - Next steps: 5e15 and 1e16 $n_{eq}cm^{-2}$

- Acceptor removal effect visible for lower substrate resistivities which leads to an <u>increase of the depletion depth after irradiation</u> up to 2e15 $n_{eq}cm^{-2}$

- Due to the low initial acceptor concentration in the 1000 Ωcm sample the creation of stable acceptors dominates and the <u>depletion depth decreases after irradiation</u>





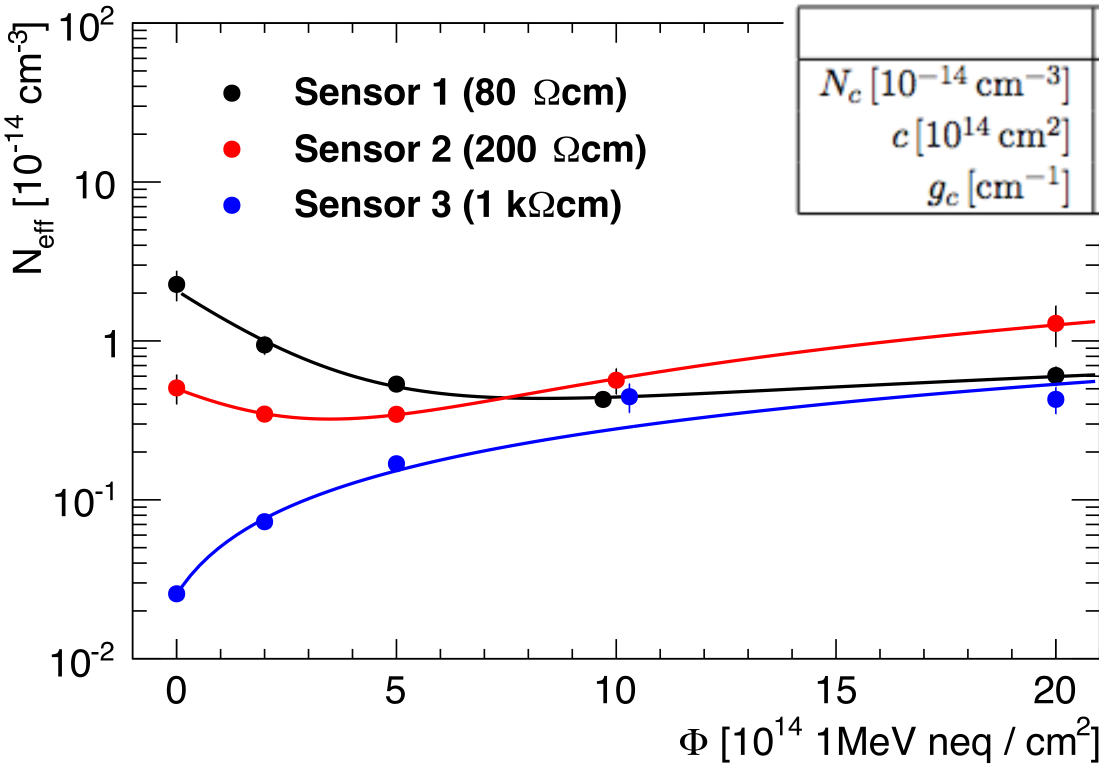


Effective doping concentration

- Effective doping concentration obtained from:

$$d(V) = d_0 + \alpha\sqrt{\rho V} = d_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{eN_{eff}}V}$$

$$N_{eff} = \underbrace{N_{eff0}}_{\text{Initial doping}} - \underbrace{N_c \cdot (1 - exp(-c \cdot \Phi_{eq}))}_{\text{Acceptor removal}} + \underbrace{g_c \cdot \Phi_{eq}}_{\text{Acceptor introduction}}$$

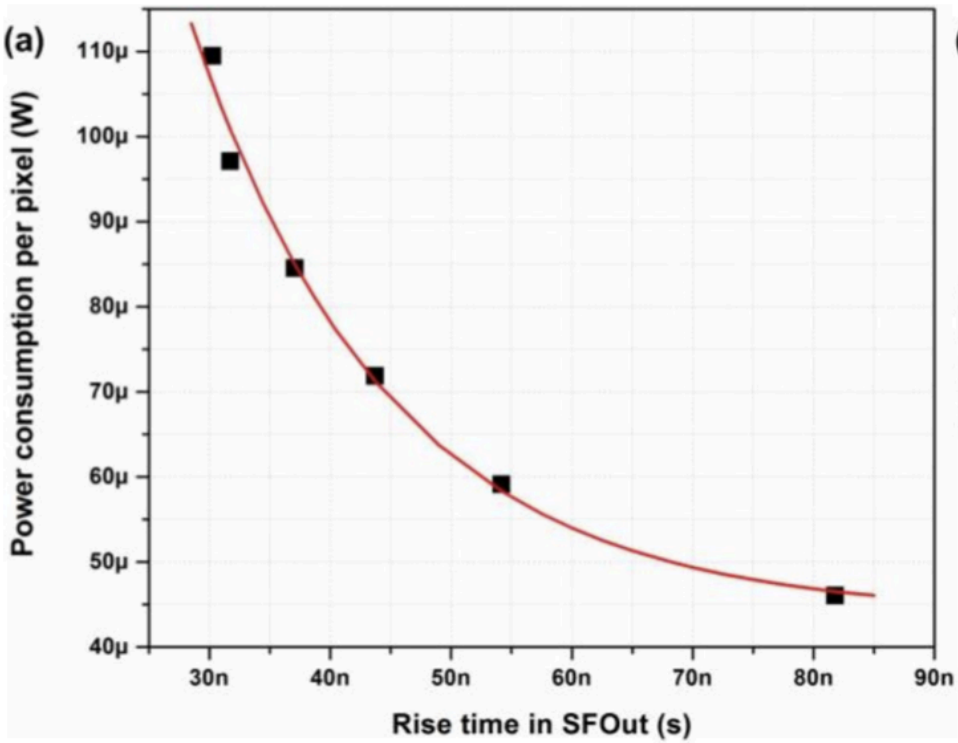


	Sensor 1	Sensor 2	Sensor 3
$N_c\,[10^{-14}\,\mathrm{cm}^{-3}]$	1.8 ± 0.4	0.7 ± 0.5	–
$c\,[10^{14}\,\mathrm{cm}^2]$	0.5 ± 0.2	0.3 ± 0.3	–
$g_c\,[\mathrm{cm}^{-1}]$	0.02 ± 0.01	0.07 ± 0.04	0.03 ± 0.02

After about 1e15 n_{eq}/cm^2 N_{eff} tends to the similar values for all resistivities

E.Cavallaro et al., JINST 12 (2017) no.01, C01074

Power vs. rise time



- Simulation of the power consumption as a function of the rise time for analog pixels with high gain
- For low gain pixels (-p-tub +extra capacitor) the rise time can go down to 20 ns with aggressive settings

E. Vilella et al. JINST11 (2016) C01012

Test beam @ SpS in 2016

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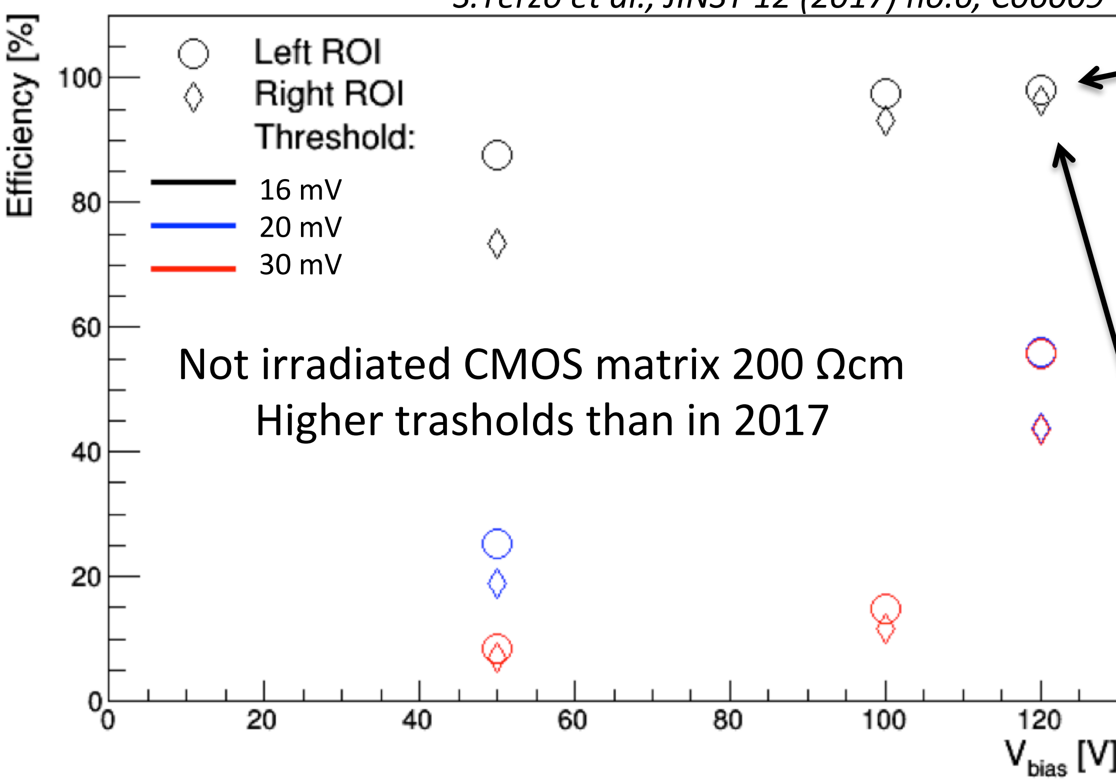
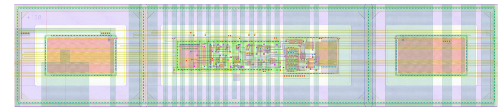
- Efficiency saturation depends on the threshold
  - Higher threshold requires more bias
    ➔ increase the depletion depth

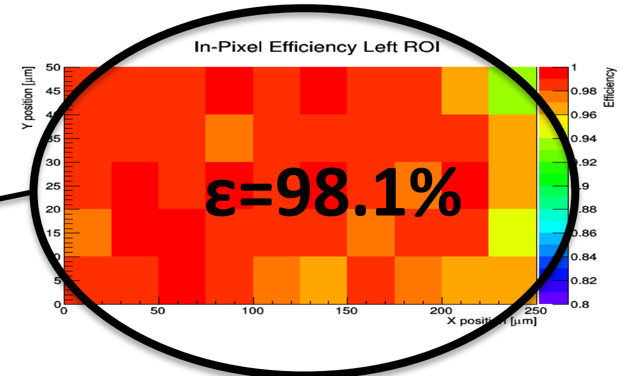
- Higher efficiency in the left matrix
  - Mean threshold right > mean threshold left
  - Right matrix: efficiency lost close to pixel edges

S.Terzo et al., JINST 12 (2017) no.6, C06009

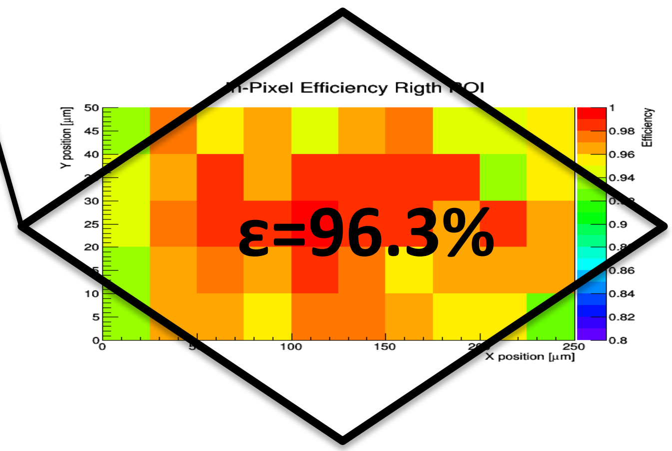


In-pixel efficiency maps
at 120 V and Thr: 16 mV





Left matrix



Right matrix