TCT for the characterization of silicon interfaces obtained by CMOS compatible wafer bonding

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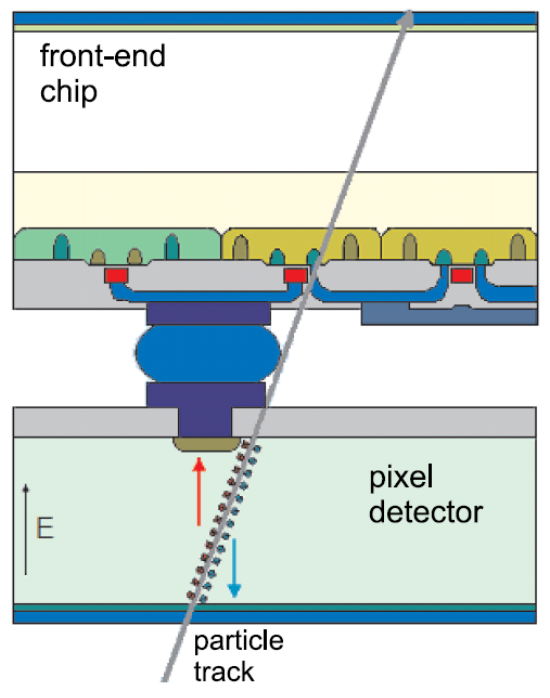
[3]https://edlab.epfl.ch/

Outline

- CMOS compatible wafer bonding
  - Bonded Monolithic Active Silicon Sensors
- TCT for bonding interface characterization
  - Analytical modeling of TCT for bonding interface characterization
  - Fabrication of test structure for TCT bonding interface characterization
- Electrical injection TCT
  - Working principle
  - Clean room fabrication of test structures
  - Measurements setup description
  - Measurements and proof of principle

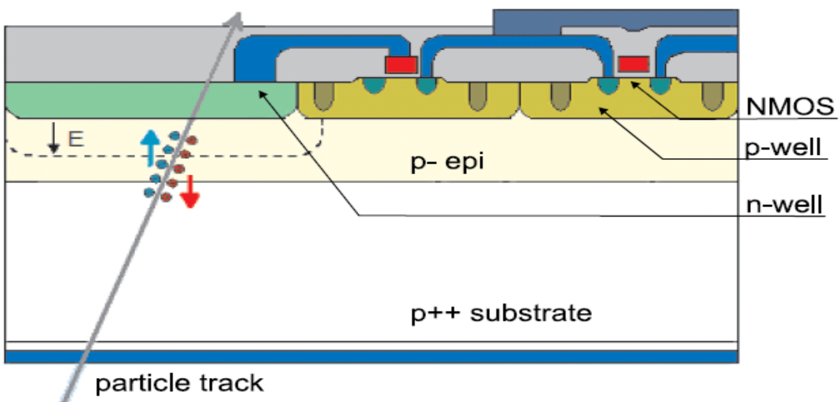
Pixel detectors

Hybrid silicon pixel detector



Monolithic Active Pixel Sensor (MAPS)

- Robust
- Thin detectors
- Low parasitic capacitance
- No need for expensive bump bonding



Petra Riedler, Monolithic silicon pixel sensors and technology challenges of the alice its, 2015.
L. Rossi et al., Pixel Detectors: From Fundamentals to Applications, *Springer*, 2006.

Fabrication of monolithic pixel detectors

Electronics driven

- Low resistivity silicon
- High performance electronics
- Low performance sensing (small depletion region)

Sensor driven

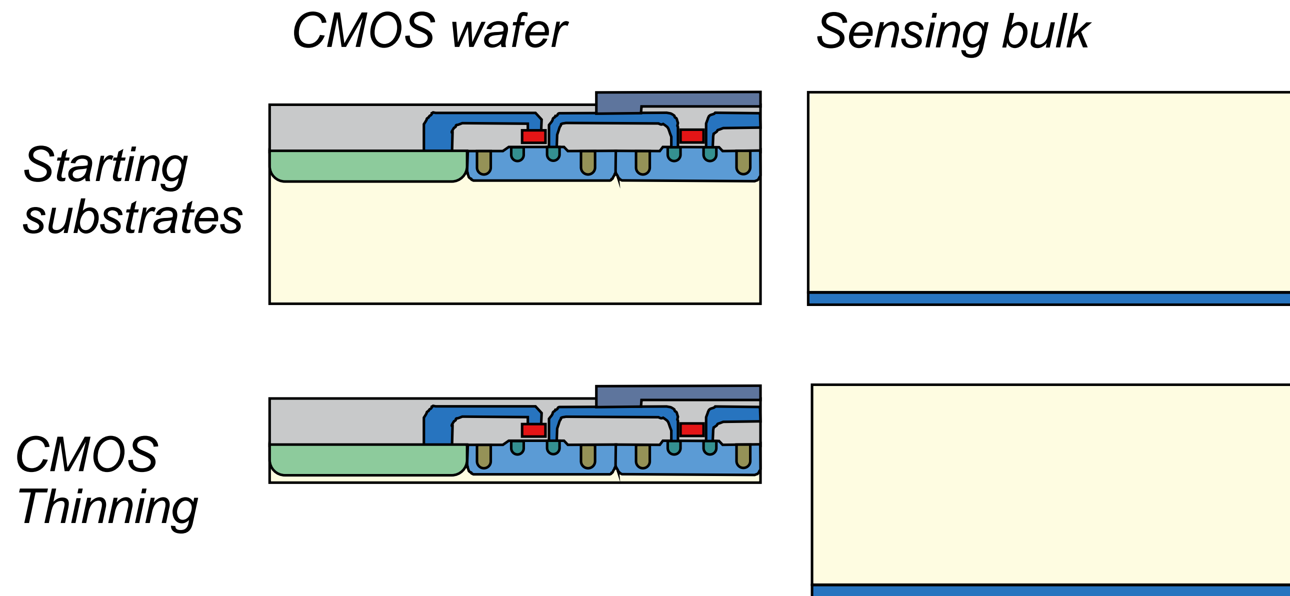
- High resistivity silicon
- Difficult electronics design
- High performance sensing (large depletion region)

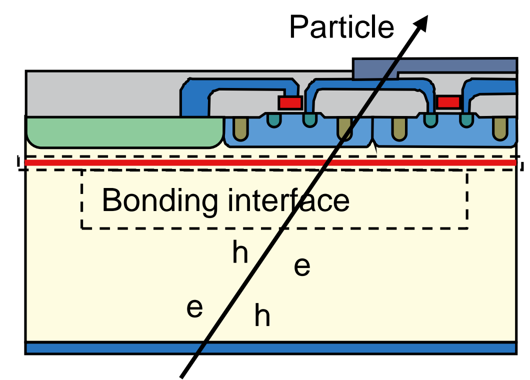
L. Rossi et al., Pixel Detectors: From Fundamentals to Applications, *Springer*, 2006.

Bonded monolithic detectors

Monolithic Active Pixel Sensors fabrication

- Bonding of sensing bulk on the back side of CMOS circuitry
- Monolithic silicon detectors with optimized characteristics:
  - CMOS on low resistivity silicon
  - Sensing bulk on high resistivity silicon
- Bonding interface electrical properties to be studied

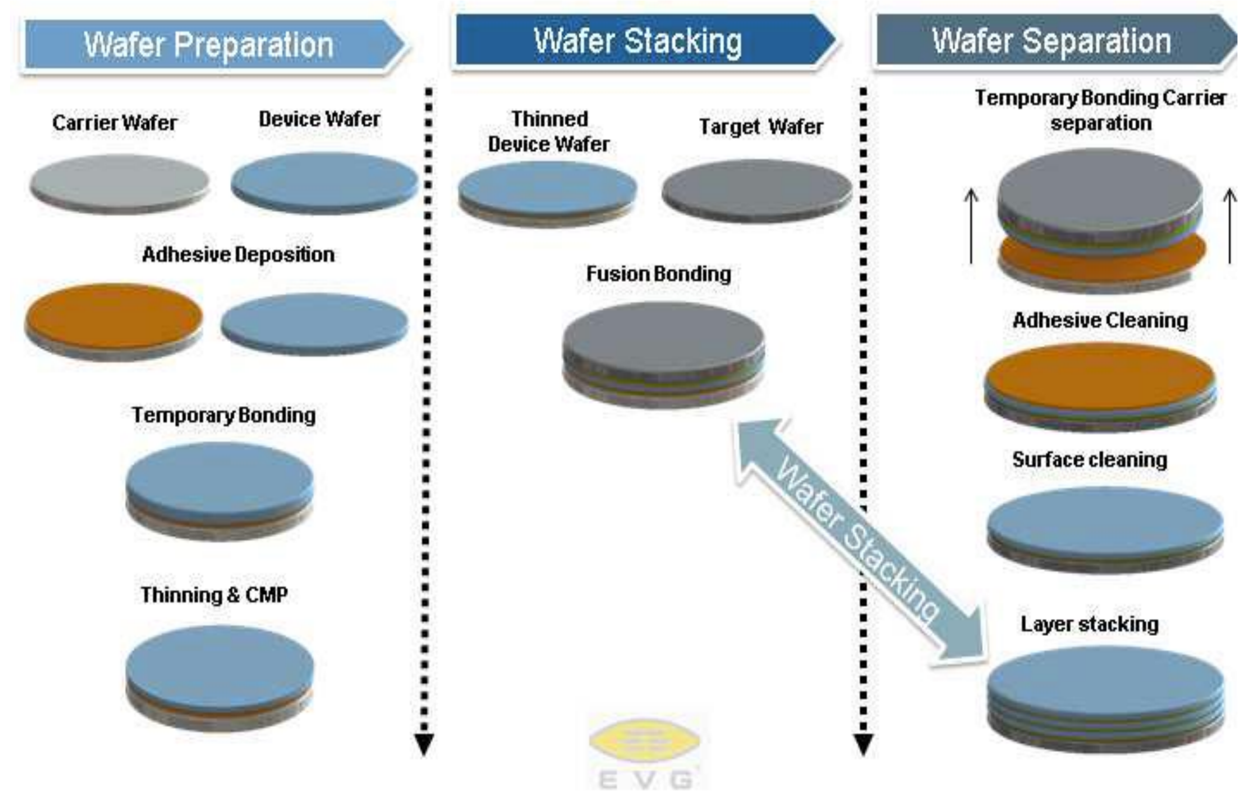




CMOS compatible wafer bonding

Process

- Complete process in vacuum (EVG®580 ComBond®)
- Dry etching of native SiO_2
- Bonding at 200°C for 60 min, with an applied pressure of 0.06MPa
- Possibility of thin wafers stacking



Results

- Si bulk fracture strength reached (2.5 J/m^2)
- Oxide-free amorphous silicon interface (3 nm)

C. Flötgen et al., "Novel Surface Preparation Methods for Covalent and Conductive Bonded Interfaces Fabrication", *ECS Trans.*, vol. 64, no. 5, pp. 103–110, 2014.
J. Burggraf, J. Bravin, H. Wiesbauer, and V. Dragoi, "Monolithic thin wafer stacking using low temperture direct bonding", *ECS Trans.*, vol. 64, no. 5, pp. 95–101, 2014.

Method of interface characterization using TCT

Amorphous silicon at the bonding interface can be modeled as a layer with a trap density 1e16 cm^{-3}

Analytical modeling of TCT transient current for bonding interfaces, 2 cases:

Junction depletion region does not reach the interface

Interface

Al (junction)

p--

Pt (ohmic)

Electric field

Position

Junction depletion region reaches the interface

Interface

Al (junction)

p--

Pt (ohmic)

Electric field

Position

J. Bronuzzi et al., "*Principle and modelling of transient current technique for interface traps characterization in monolithic pixel detectors obtained by CMOS-compatible wafer bonding*", *JINST,* 11 P08016, 2016.

TCT for bonding interface traps

Different applied voltage

0.5 V

•interface not included in depletion region

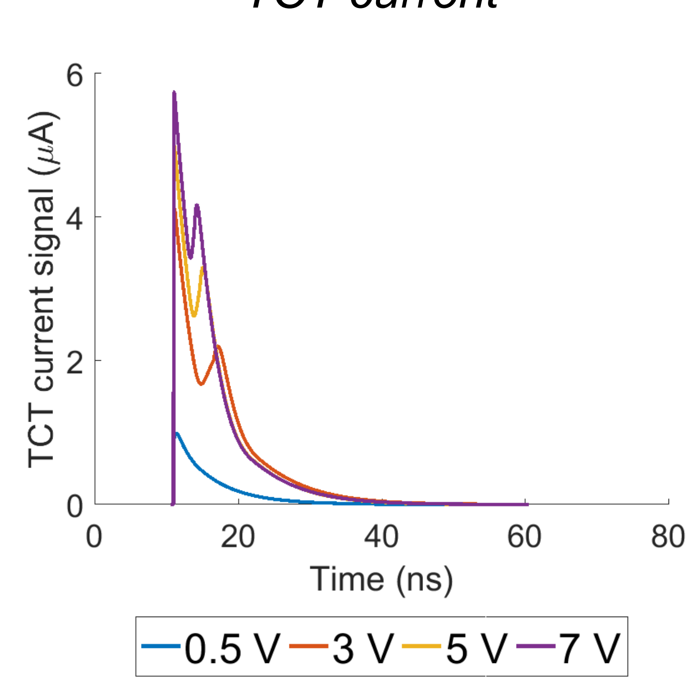
•TCT current not affected by interface

3-5-7 V

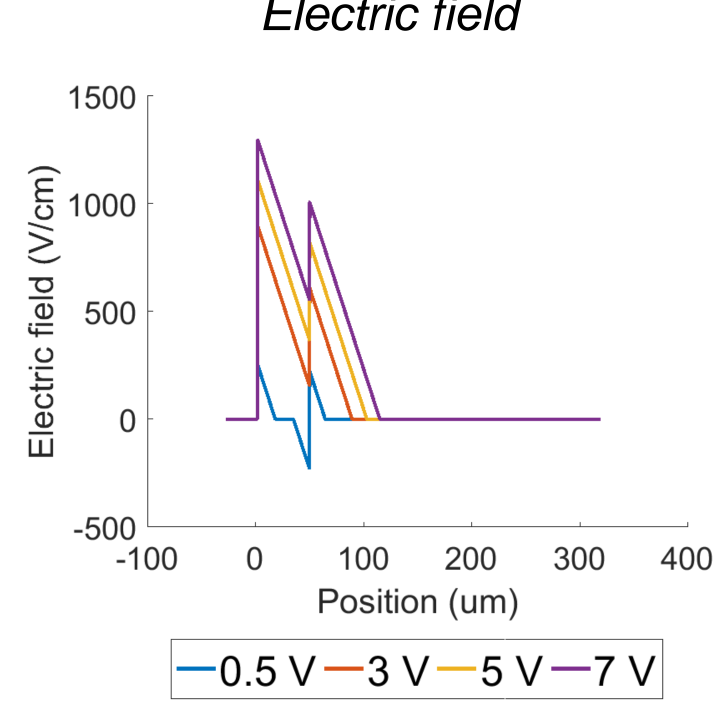
•interface included in depletion region

•TCT current affected by interface

TCT current



Electric field



TCT for bonding interface traps

Different traps type

Acceptors	*Donors*	*Acceptors and Donors*
•Acceptors generate negative charge	•Donors generate positive charge	•Charge compensation
↓	↓	↓
•Electric field decreased	•Electric field increases	•No discontinuity in electric field
↓	↓	↓
Not clear signature in TCT signal	TCT current affected by interface	Not clear signature in TCT signal

TCT current

Electric field

Test structures fabrication

CMOS compatible bonding of silicon wafers at CEA-LETI:

- Silicon wafers: 8 inches, magnetic Czochralski P-type, ρ > 5000 ohm.cm
- Thinning (tolerance 1 μm), to have interface close to surface, and bonding (pressure 30 kN)
- Downsizing from 8 inches to 4 inches through laser cut
- Fabrication of Schottky diodes on top of wafers (at CMi EPFL) to be studied with TCT

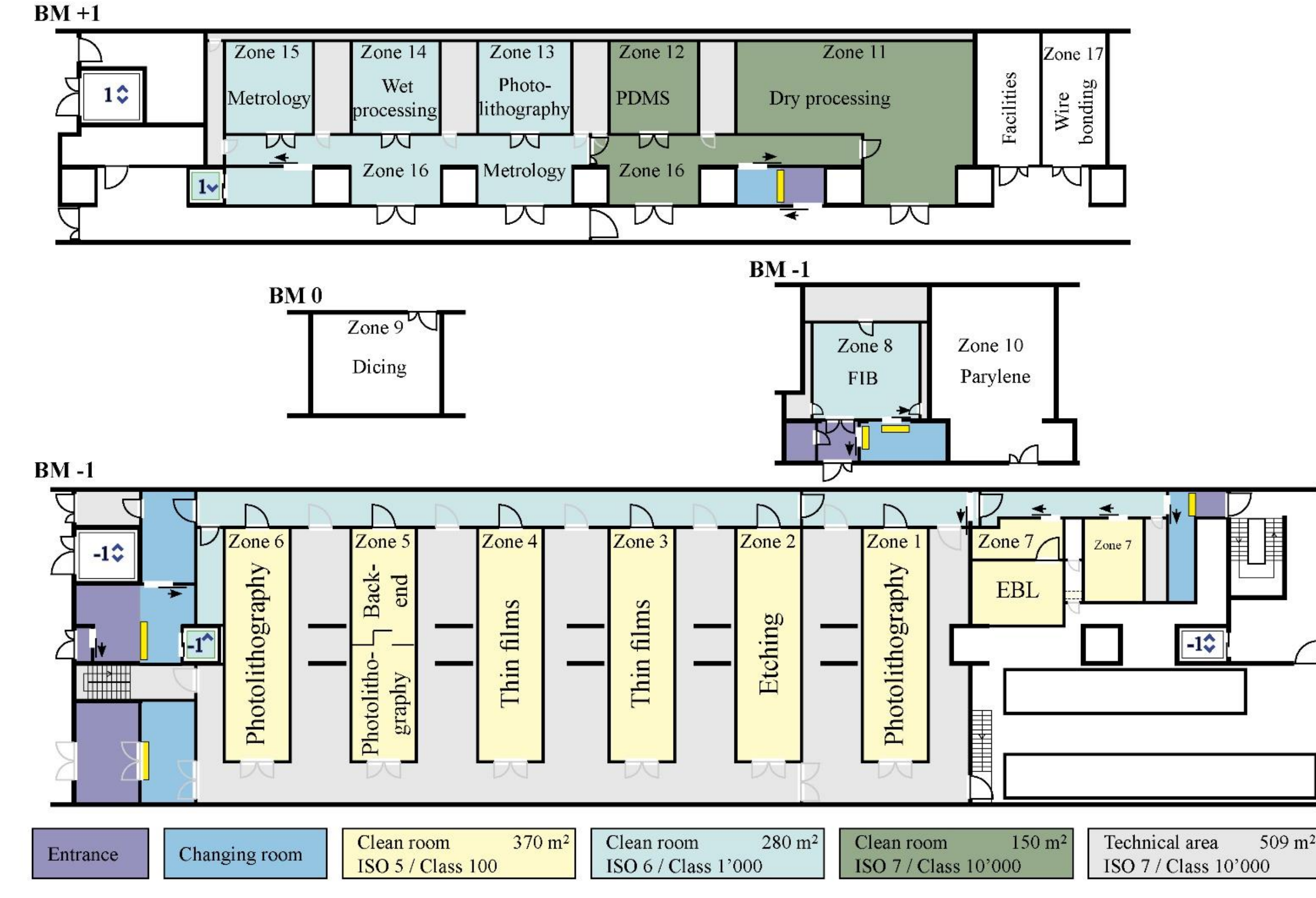
Substrate	Top wafer thickness	Surface preparation	Annealing temperature
P1	20um	Hydrophobic	400°C
P2	20um	Hydrophilic	400°C
P3	50um	Hydrophobic	400°C
P4	50um	Hydrophobic	400°C
P5	50um	Hydrophobic	T amb
P6	50um	Hydrophobic	T amb
P7	50um	Hydrophilic	400°C
P8	50um	Hydrophilic	400°C
P9	50um	Hydrophilic	T amb

Start wafers	
Thinning top wafer	
Bonding	
Downsizing	
Schottky diodes fabrication	

Center of Micronanotechnology

- The Center of Micronanotechnology (CMi) is a ISO5-6-7 clean room complex at the École Polytechnique Federale de Lausanne
- CMi facilities are used for education, academic purposes and research

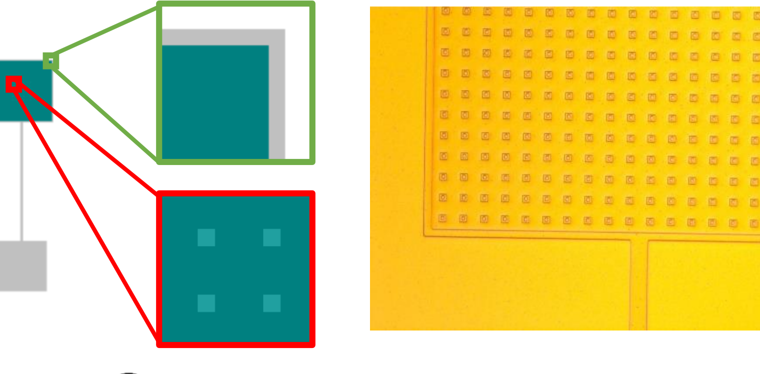
https://cmi.epfl.ch/



Validation of TCT on Schottky diodes

- Tests performed on structures fabricated at CMi
- 4 inches wafers
- Resistivity > 2000 ohm.cm
- Float zone P-type
- Al for schottky contacts
- Pt for ohmic contacts

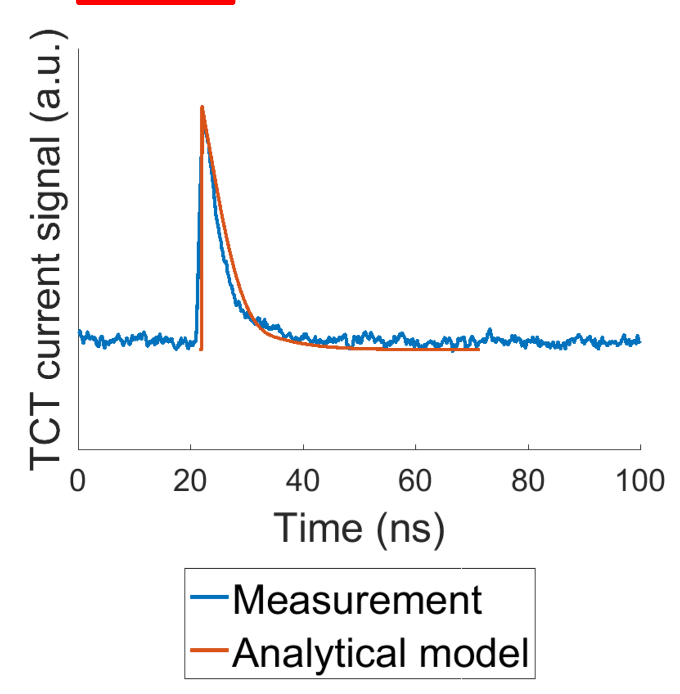
Diode



Next steps:

- Schottky diodes fabrication on bonded wafers
- TCT measurements on Schottky diodes on bonded wafers

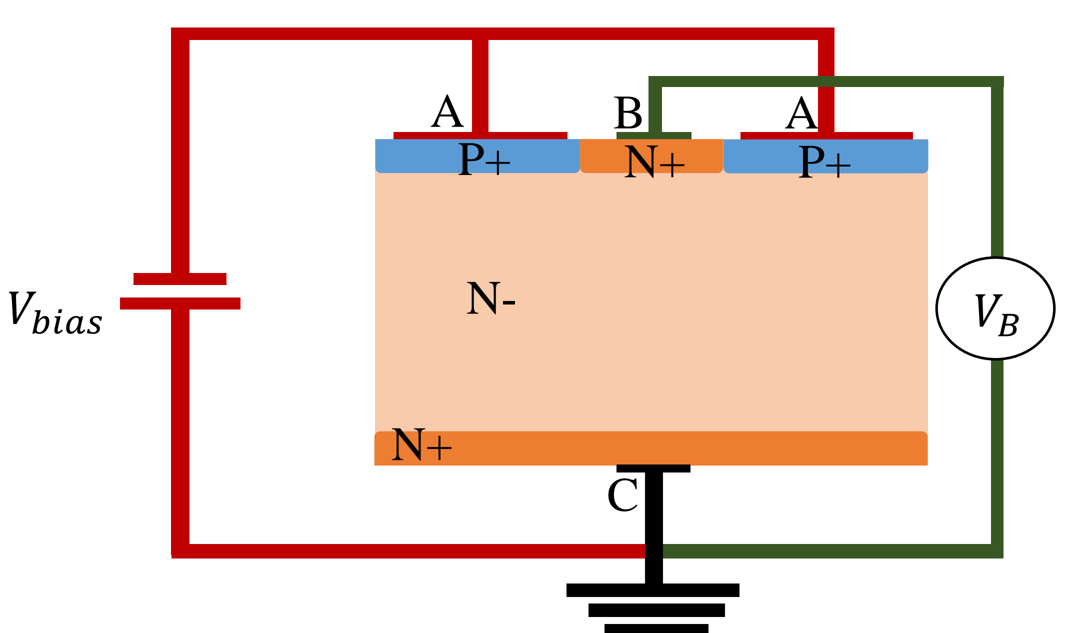
TCT signal (at 40 V)

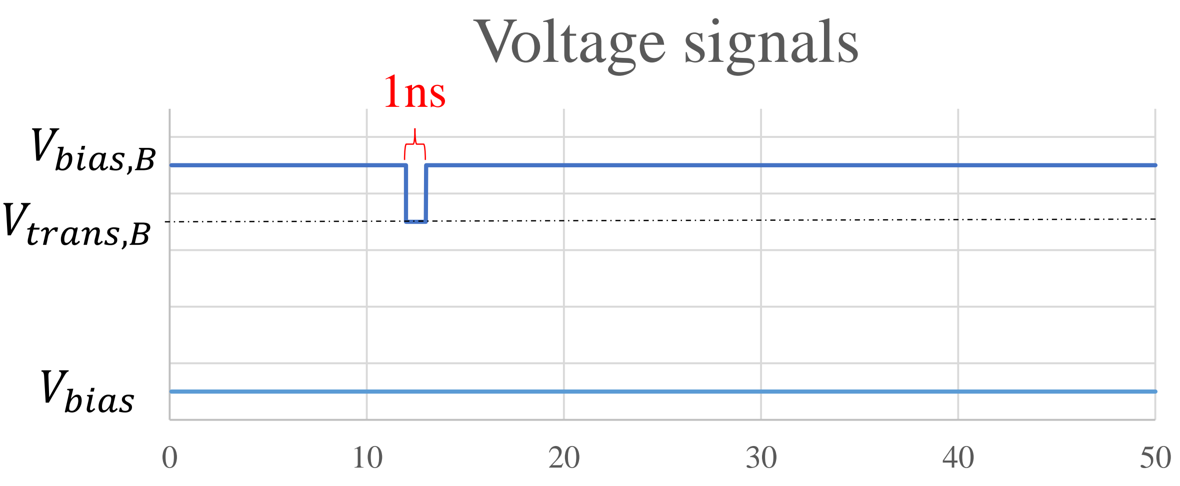


CMi: https://cmi.epfl.ch/

Electrical injection TCT

- Instead of Schottky diodes, integrate TCT charge injection in silicon
- PiN Diode doping profile modified
- Nanosecond voltage pulse applied on the N-type well

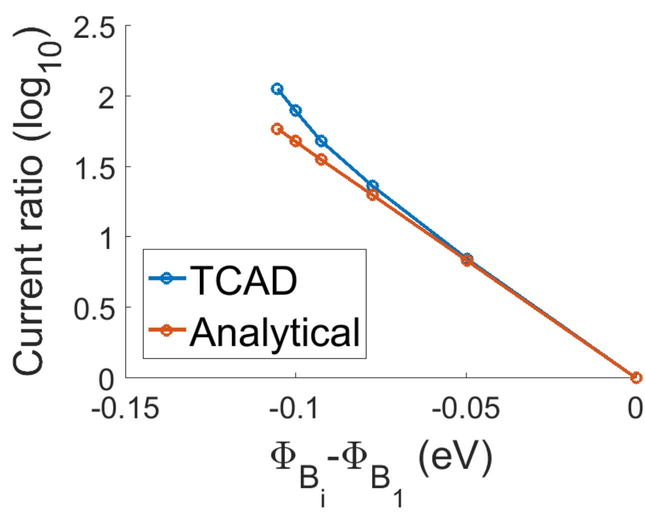




Physical principle

Thermionic emission

$$J_i/J_1 = e^{\frac{\phi_{B_1}-\phi_{B_i}}{kT}}$$



Steady state

cutline

ConductionBandEnergy (eV)
2.000e+02
1.990e+02
1.980e+02
1.970e+02
1.960e+02

Conduction barrier potential (eV)

Position (μm)

Injection

cutline

ConductionBandEnergy (eV)
2.000e+02
1.992e+02
1.985e+02
1.978e+02
1.970e+02

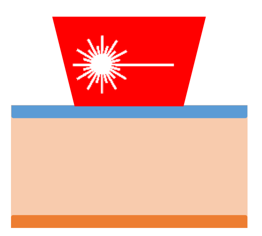
Conduction barrier potential (eV)

Position (μm)

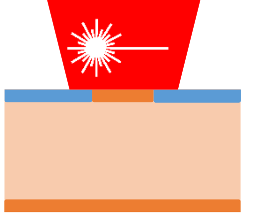
Light and electrical injection

3 Studies

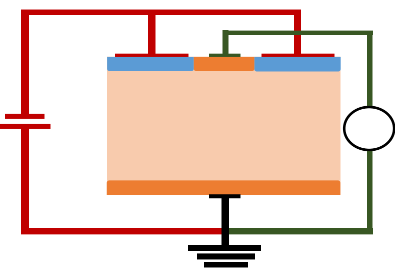
Optical injection on standard diode

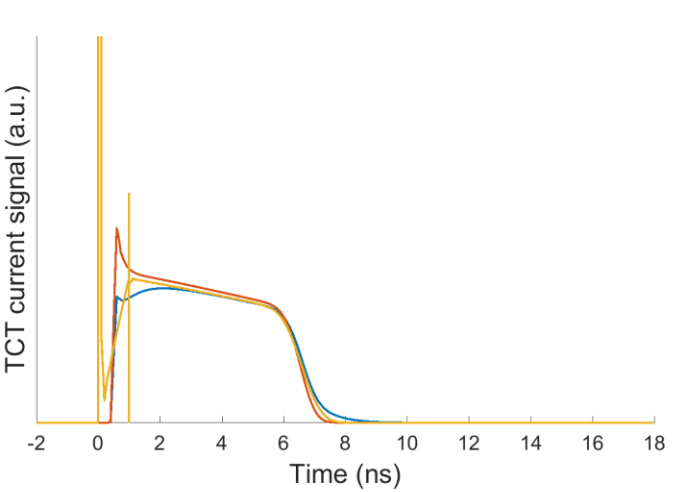


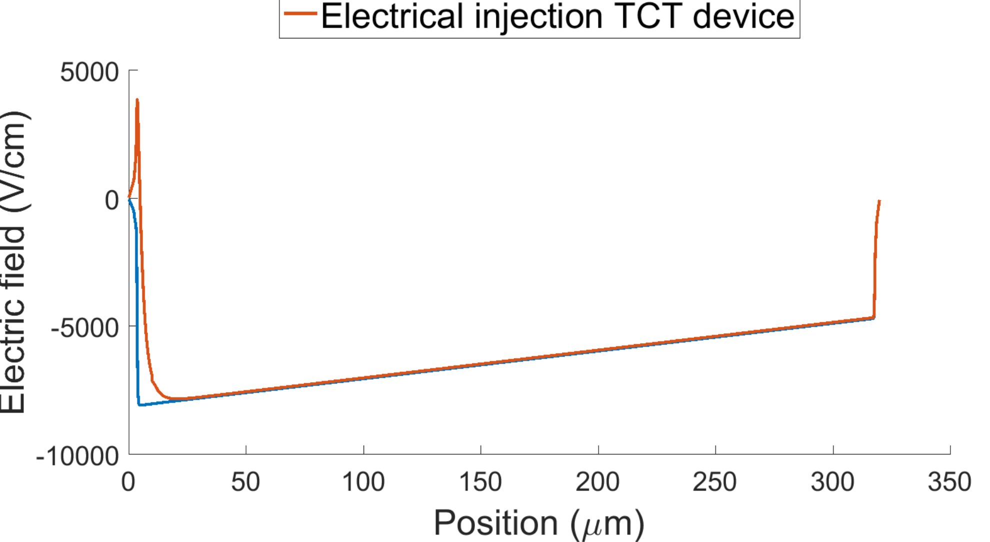
Optical injection on Electrical injection TCT (el-TCT) device



Electrical injection

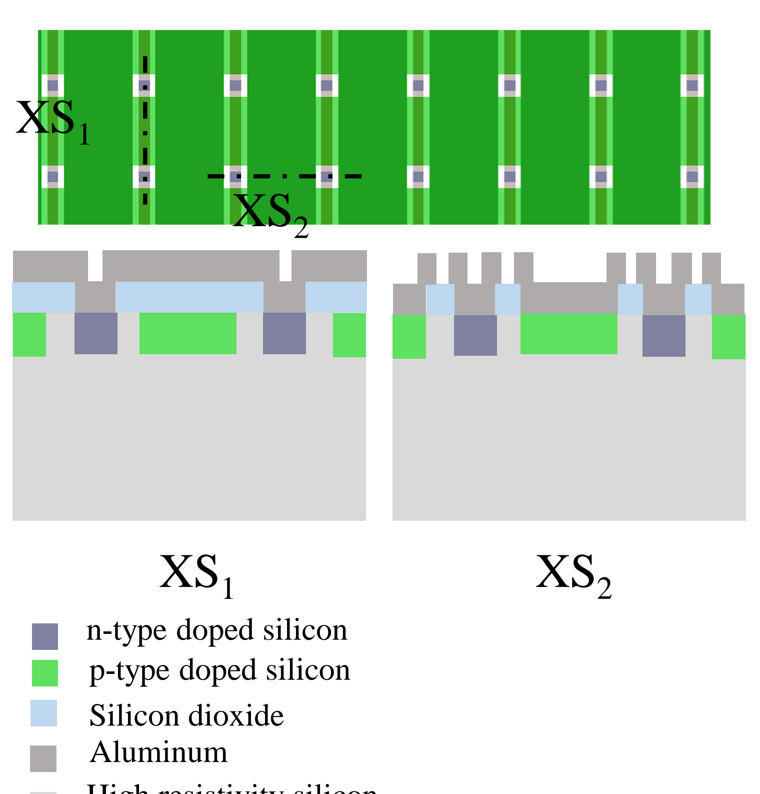


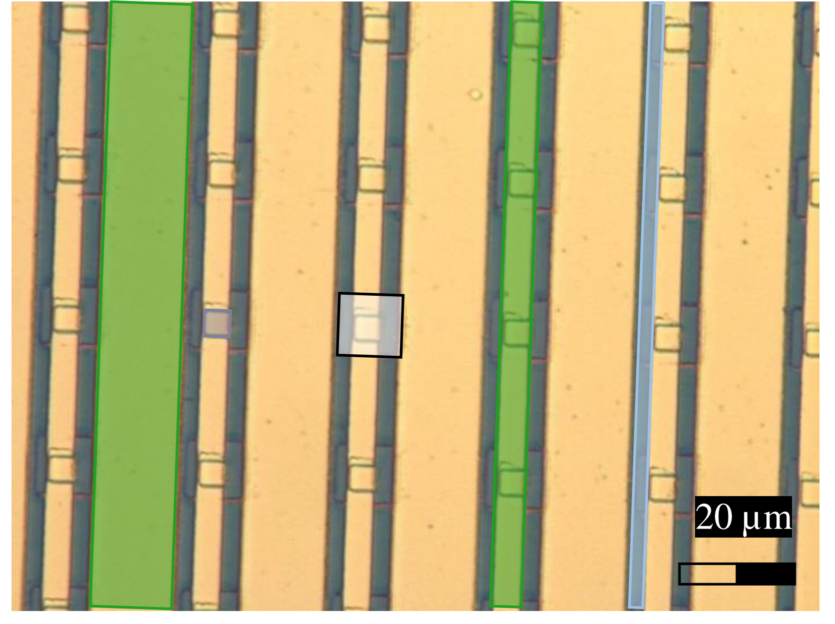




Fabrication and measurements setup

Device fabricated at CMi

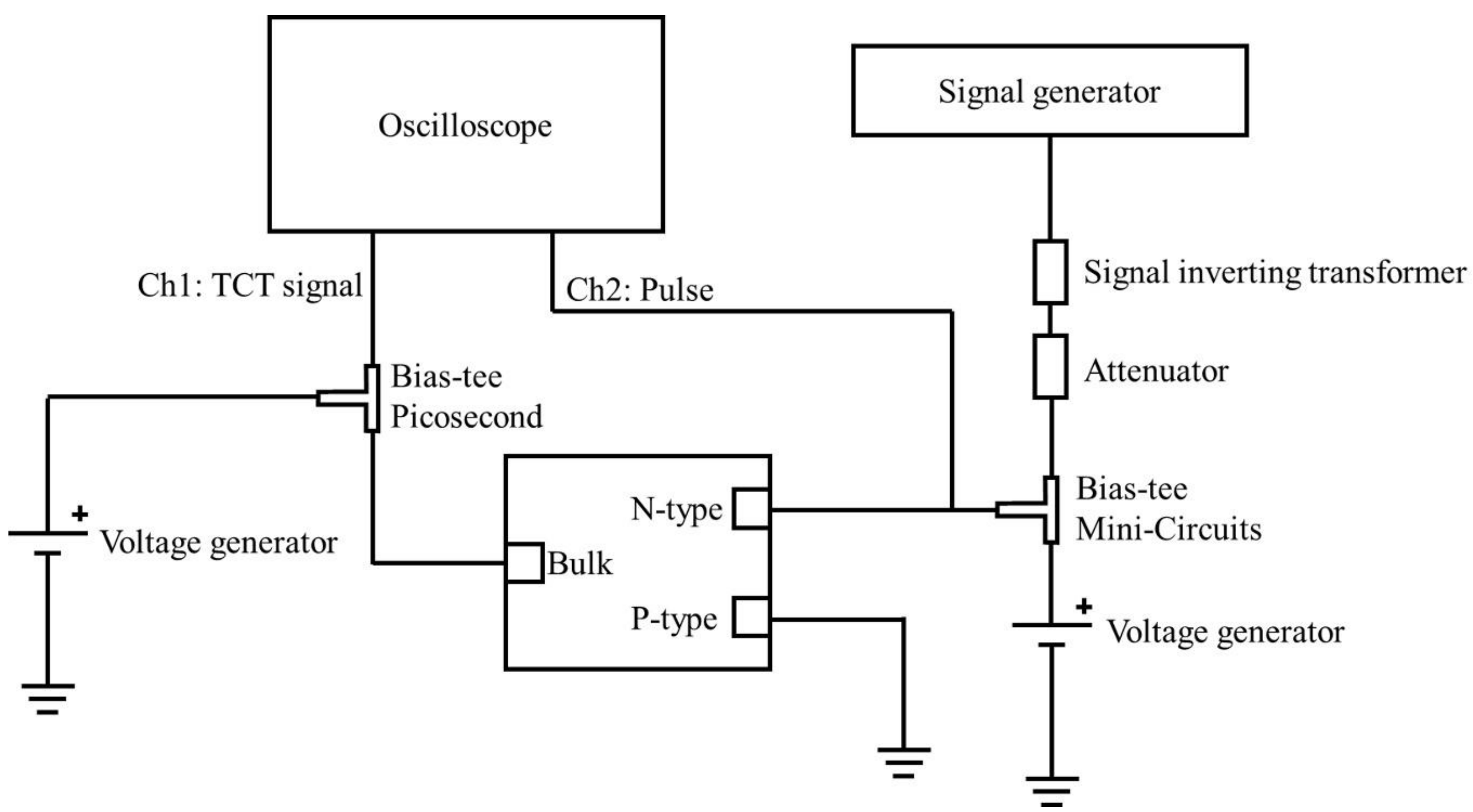




n-type doped silicon
Aluminium
Silicon dioxide
Spacing between n and p-type doped silicon

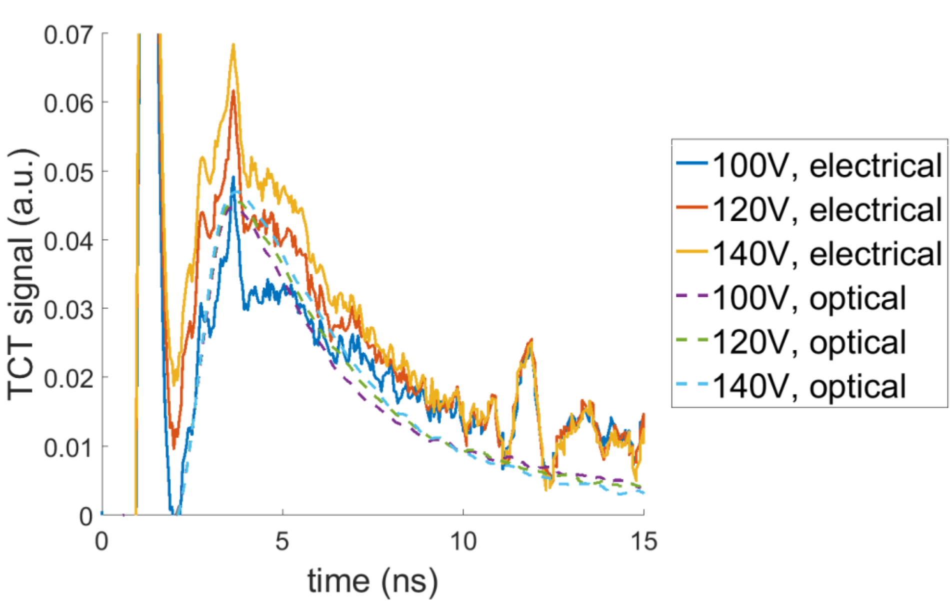
Setup components

- Signal generator: Picosecond Pulse Labs 10,050A
- Bias-tees:
  - Picosecond Pulse Labs 5531
  - Mini-Circuits ZFBT-6GW
- Voltage generators:
  - Keithley 2410
  - Agilent E3631A
- Oscilloscope: infiniium MSO9404A



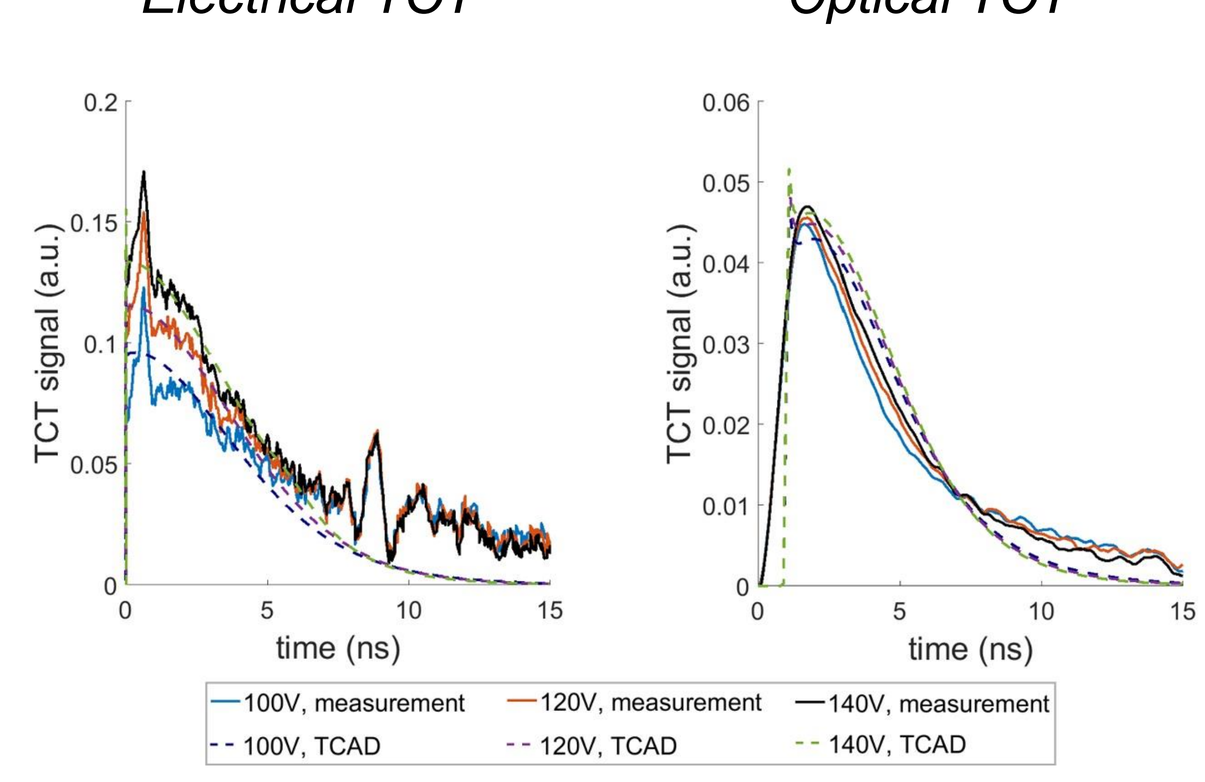
Proof of principle of el-TCT

Measurements: comparison electrical and optical TCT



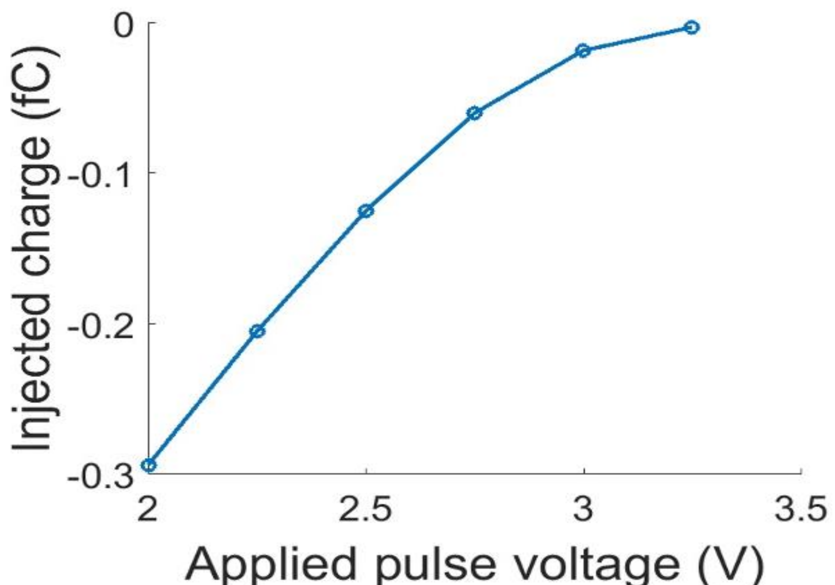
Comparison TCAD simulations and measurements

Electrical TCT *Optical TCT*

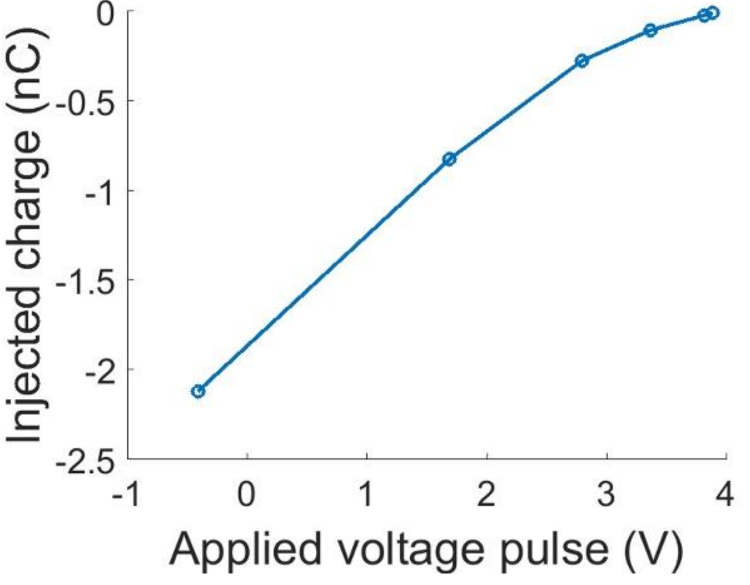


Proof of principle of electrical TCT

TCAD simulations of injected charge



Measurements of injected charge



Conclusions and outlook

New manufacturing technique for monolithic silicon sensors is being investigated:

- Characterization of bonding interface with TCT has been modeled
- Fabrication of devices for TCT bonding interface characterization is in progress
- Measurements will be performed at CERN in the early 2018

El-TCT has been developed:

- The proof of principle has been demonstrated
- Evaluation of el-TCT for online measurements of radiation induced damage in silicon samples at IRRAD proton facility in 2018

Thank you for the attention
Questions?