CiS Forschungsinstitut für Mikrosensorik GmbH

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Ongoing activities at CiS

- active edge sensors
- sensor thinning by cavity etching
- flip chipping

31st RD50 Workshop, CERN, 22.11.2017

reduction of inactive sensor edge

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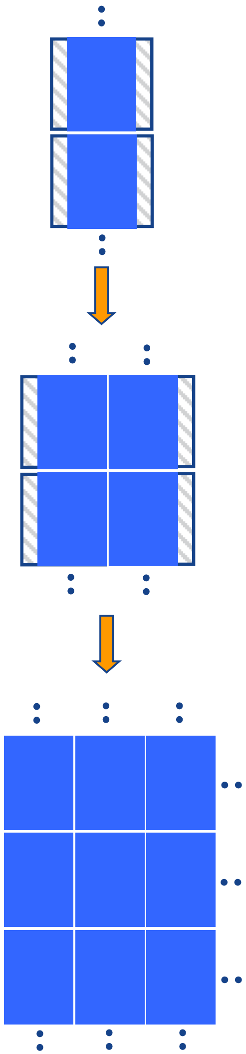
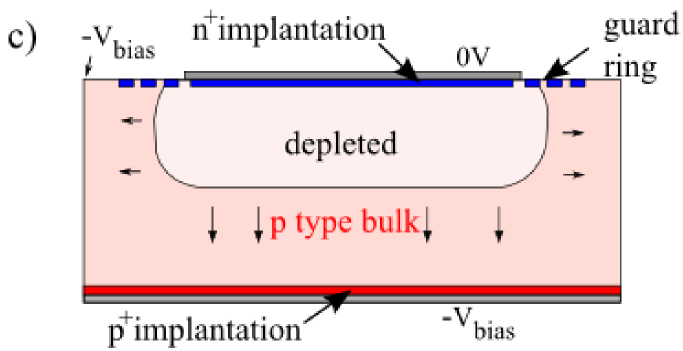
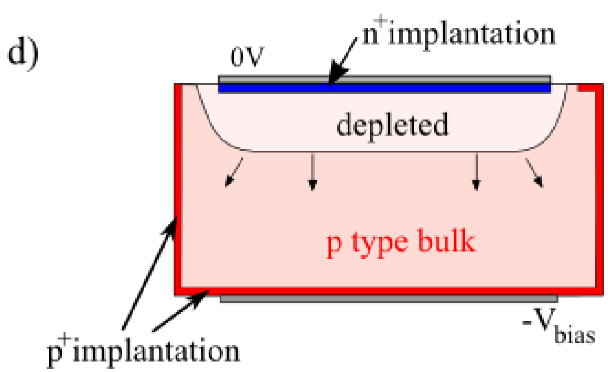
- conventional planar sensors need to have inactive sensor edges
  - gradual potential drop (high voltage to ground)
  - safety margin
- active edges:
  - reduction of inactive sensor edge by doping of side walls to minimum
  - non-shingled arrangement of the sensors becomes feasible



conventional



active edge



active edge sensor run trial plan

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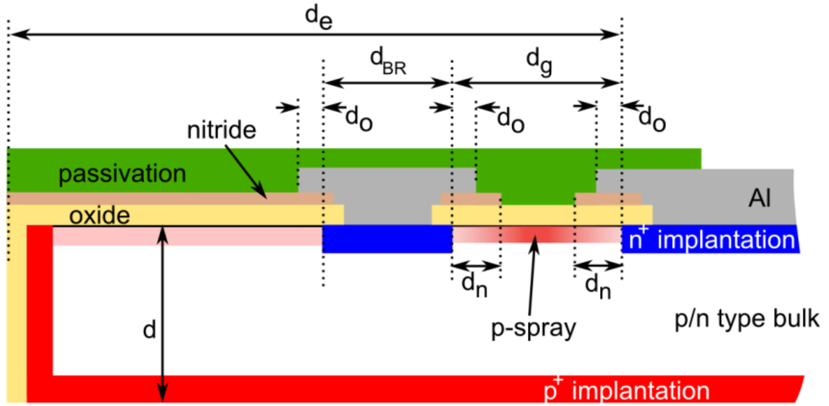
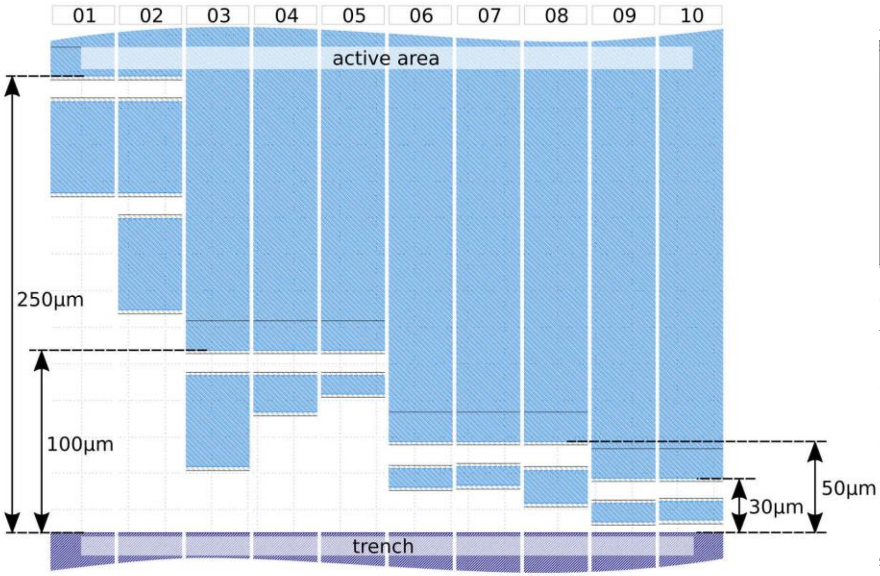
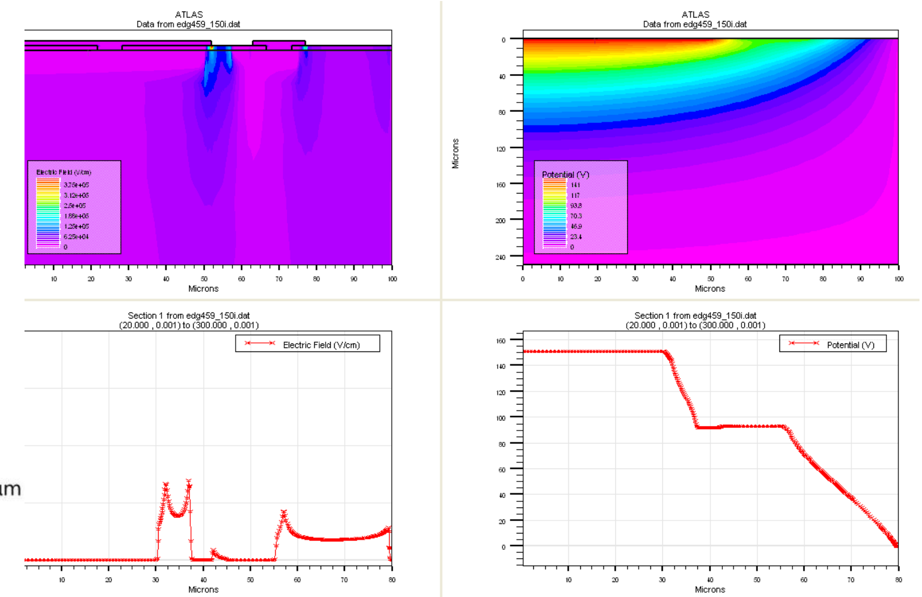
- several parameters are varied which can be compared
  - numerous edge designs have been simulated
  - the 10 most promising designs were implemented in the layout
    - d_e = 250, 100, 50 & 30µm







active edge sensor run wafer layout

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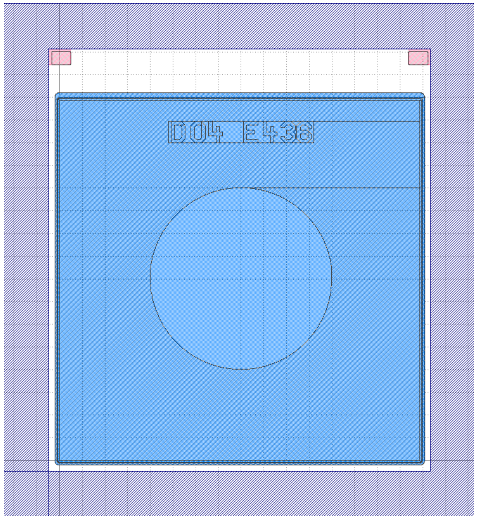
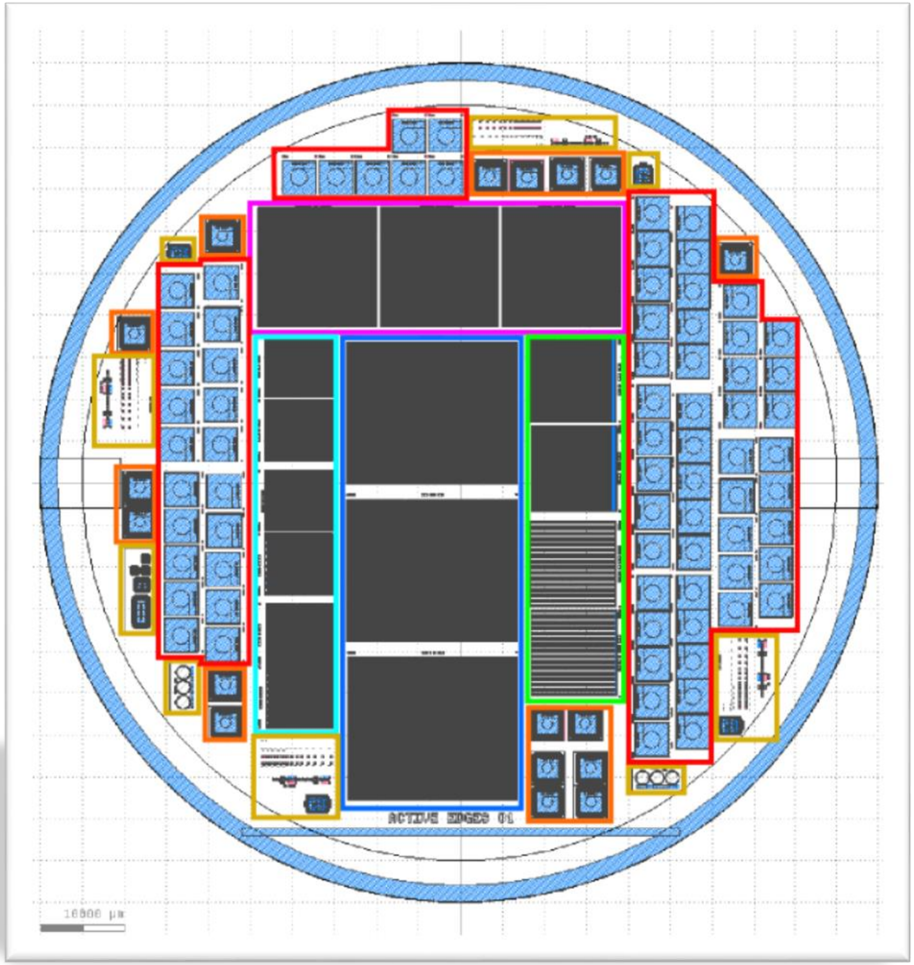
- numerous active edge diodes with systematic variations of edge design
- reference diodes
- FE-I4 & FE-I3 SCS
  - moderated p-spray
  - not moderated p-spray
- micro strip sensors (80µm pitch)
- MediPix/TimePix sensors
- test structures
- trench widths: 30...500µm





active edge sensor run
wafer run finished successfully

- wafer material
  - p- and n-type bulk
  - sensor thickness
- three side wall doping methods
  - 4-quadrant ion implantation (4QI)
  - plasma immersion ion implantation (PIII)
  - BBr_3 deposition from gaseous phase
- several challenging process steps had to be approached

	wafer thickness	processed wafers
p-type	300µm	13
p-type	100µm	12
n-type	320µm	13
n-type	100µm	12

4QI, 4E15, 15°

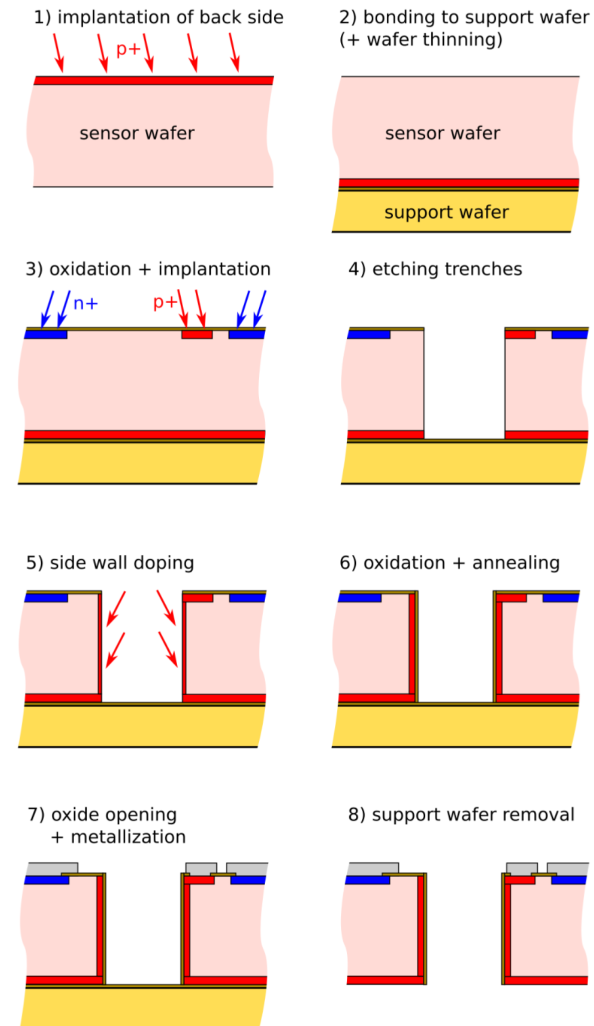
4QI, 2E15, 30°

PIII, 1E15

PIII, 5E15

PIII, 1E16

BBr_3



active edge sensor run

wafer run finished successfully

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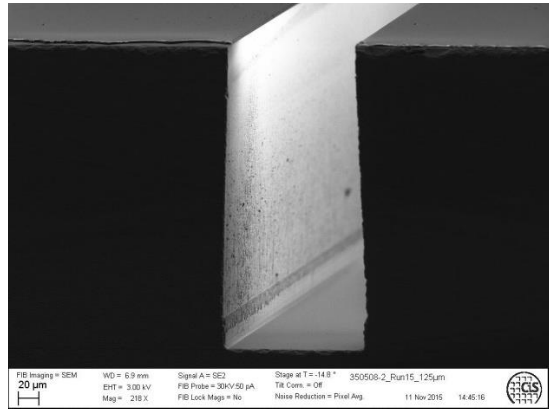
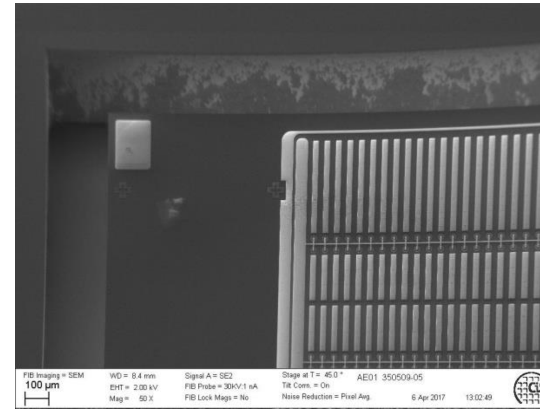
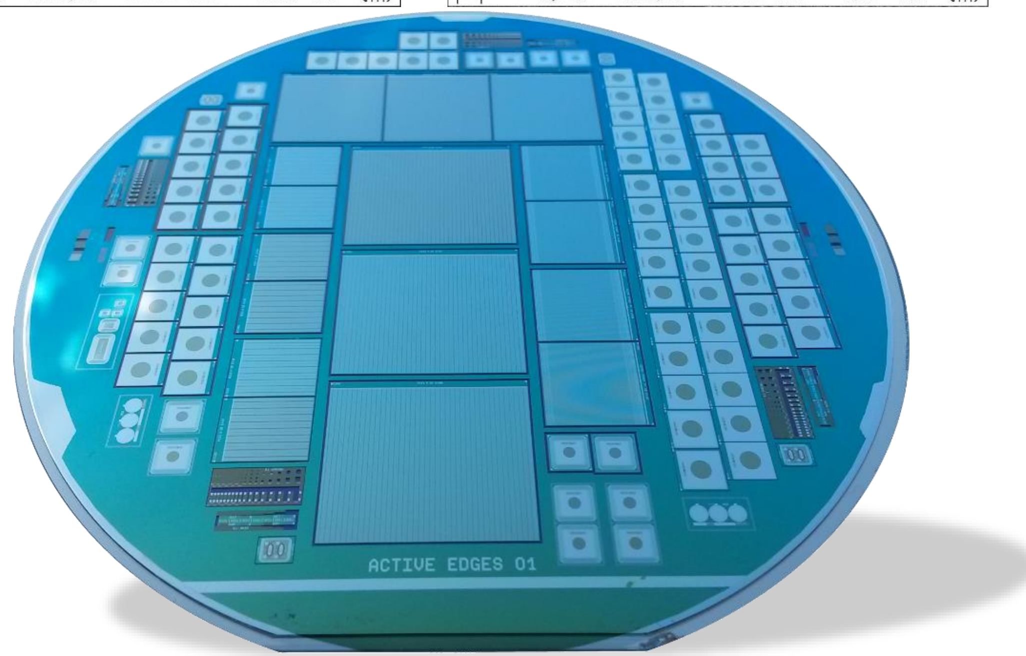
  - p- and n-type bulk
  - sensor thickness
- three side wall doping methods
  - 4-quadrant ion implantation (4QI)
  - plasma immersion ion implantation (PIII)
  - BBr_3 deposition from gaseous phase
- several challenging process steps had to be approached
- removal of support wafer not yet done







active edge sensor run
CV measurements

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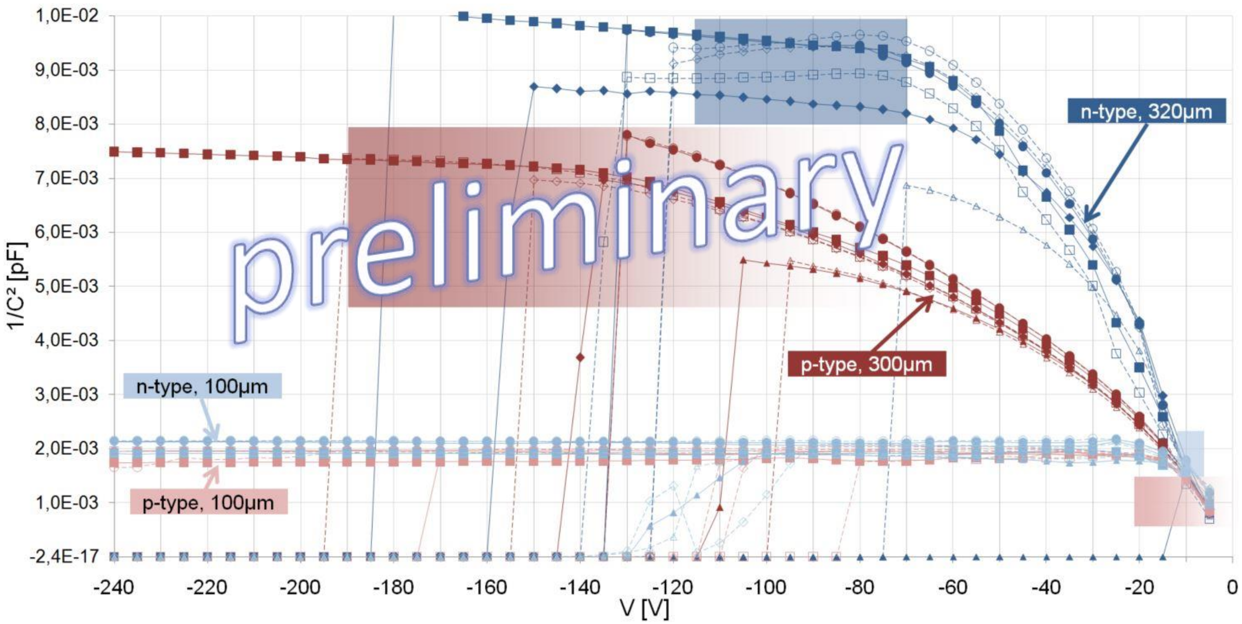


- depletion voltages fit well to theory

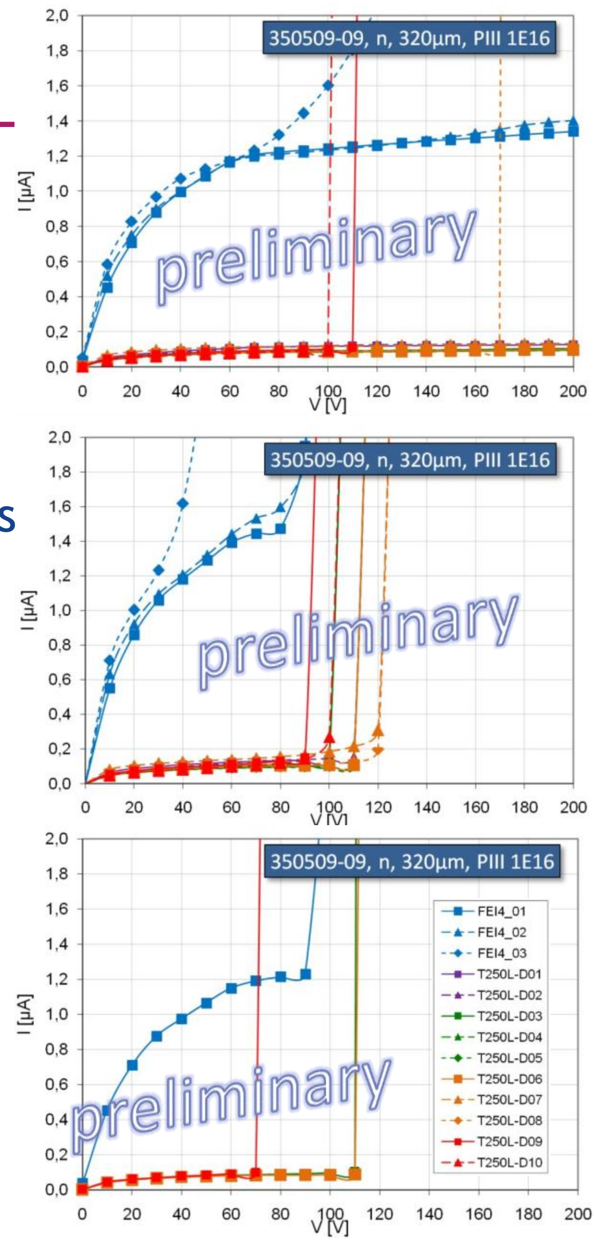
	wafer thickness	V_{depl} calculated	V_{depl} measured	➔ V_{op}
p-type	300µm	<190V	130V	170V
p-type	100µm	<21V	<20V	50V
n-type	320µm	70…115V	60V	100V
n-type	100µm	7…11V	<20V	50V

active edge sensor run
IV measurements

- initial measurements
  done by hand at random
  - promising results
  - no breakdowns until 200V
    for most of the diodes
- systematic automatic measurements
  - disagreement of the IV-curves
  - large fraction of sensors
    break down at ~80...120V
- cross check by hand
  - low break downs remain

➔assumption:
sensors have been affected
or damaged non-reversibly
by the automatic measurements

➔yet no reasons found



measured by hand

↓

automatically measured

↓

measured by hand

CiS

active edge sensor run
IV measurements

CiS

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  done by hand at random
  - promising results
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    for most of the diodes
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sensors have been affected
or damaged non-reversibly
by the automatic measurements

➔yet no reasons found

problem:

- systematic automatic measurements are only of limited information value
- investigation of the impact of the different parameters on the breakdown voltage (V_{BD}) is not clearly possible anymore
- V_{BD} might have been higher
- significant conclusions can only be drawn up to V_{BD}
  - level of leakage current before V_{BD}
  - V_{BD} even before 80...120V?

active edge sensor run
level of leakage current

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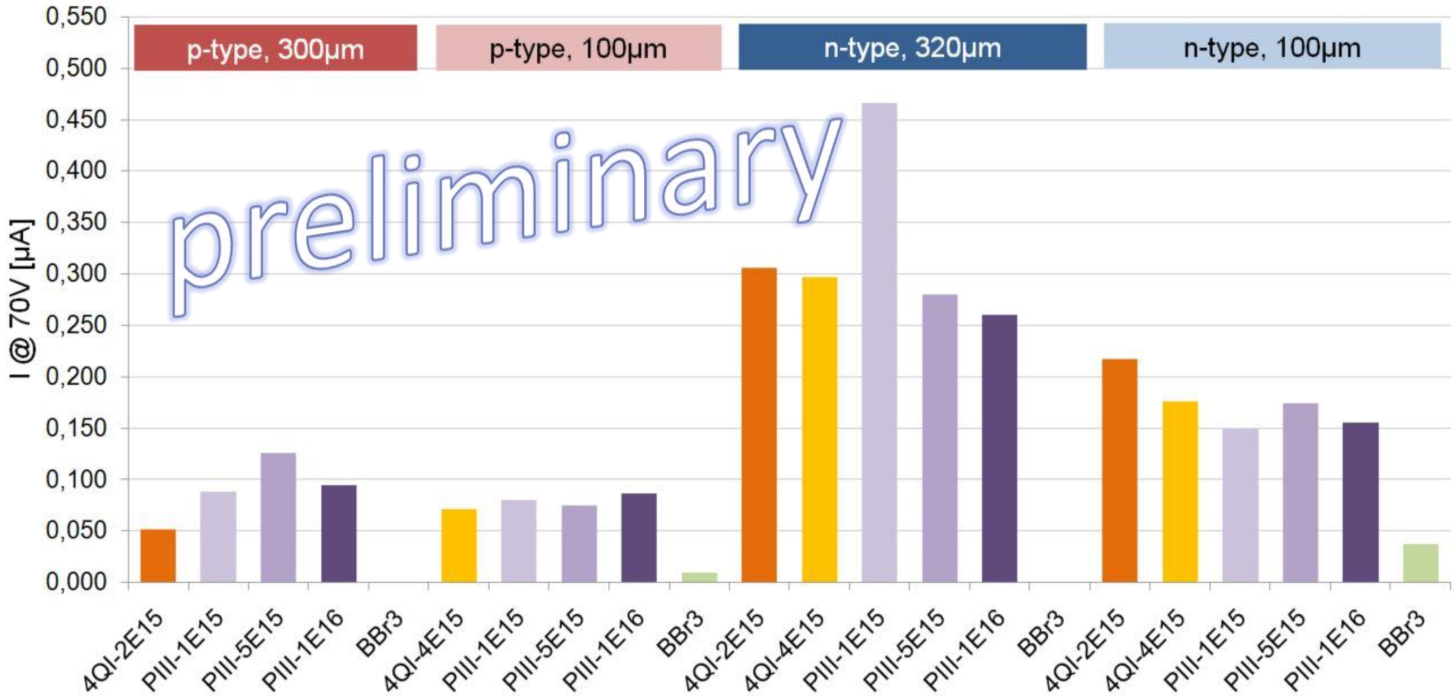
- I@V=70V
- average of all diodes
- quality criteria:

  I@70V>2µm
  slope > 5



- no significant difference between 4QI and PIII
- for **BBr_3: leakage currents are lower** by a factor of 5...10
  - fits to the doping profiles
- in general: influence of substrate material is more significant

active edge sensor run break down voltages

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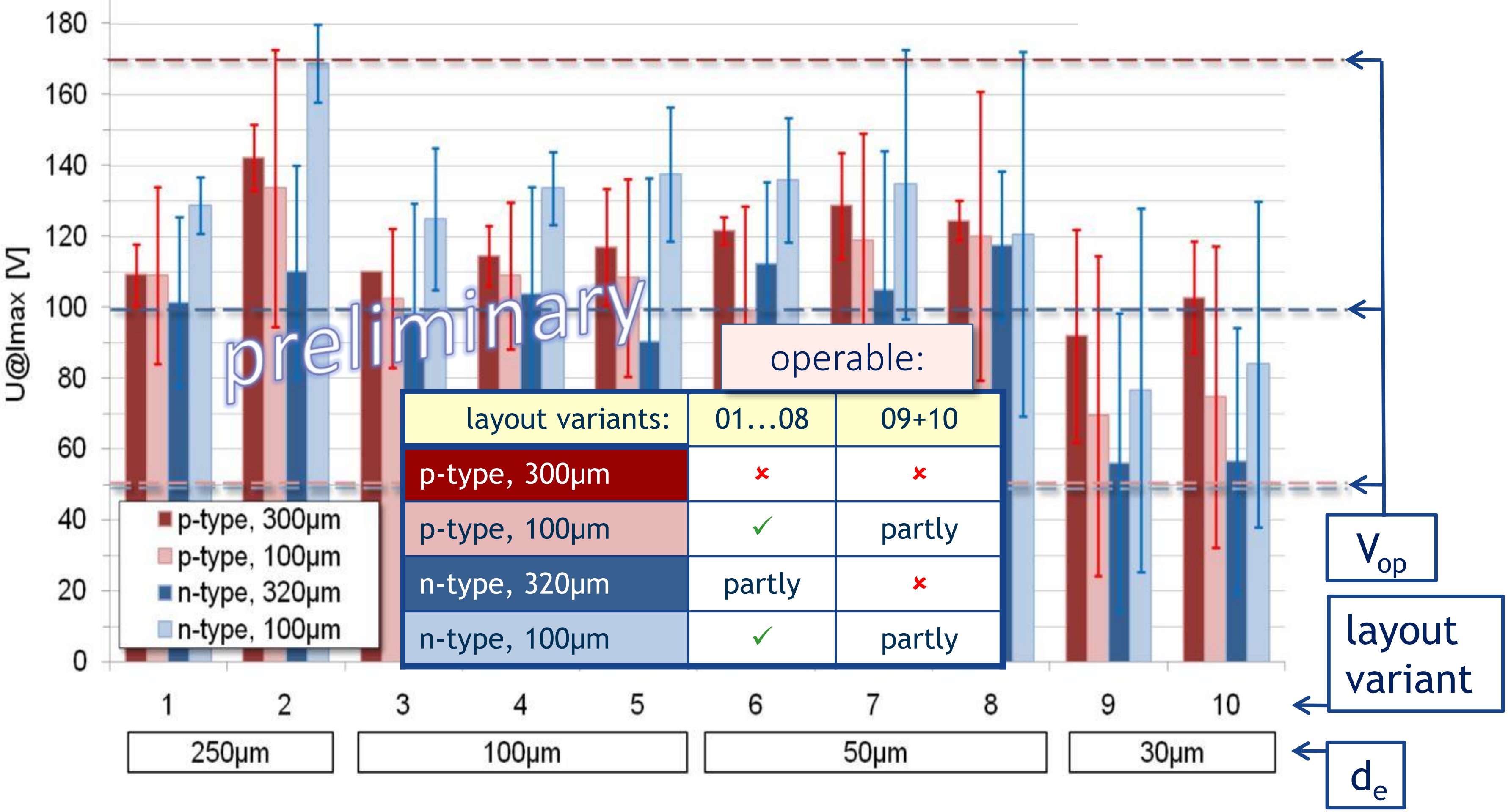
- V_{BD} =~80...120V for layout variant 01...08
- trend to lower V_{BD} visible for variant 09+10

- V_{BD} = V@2µA
- average of all diodes



operable:

layout variants:	01…08	09+10
p-type, 300µm	×	×
p-type, 100µm	✓	partly
n-type, 320µm	partly	×
n-type, 100µm	✓	partly

sensor thinning by cavity etching single sided sensors

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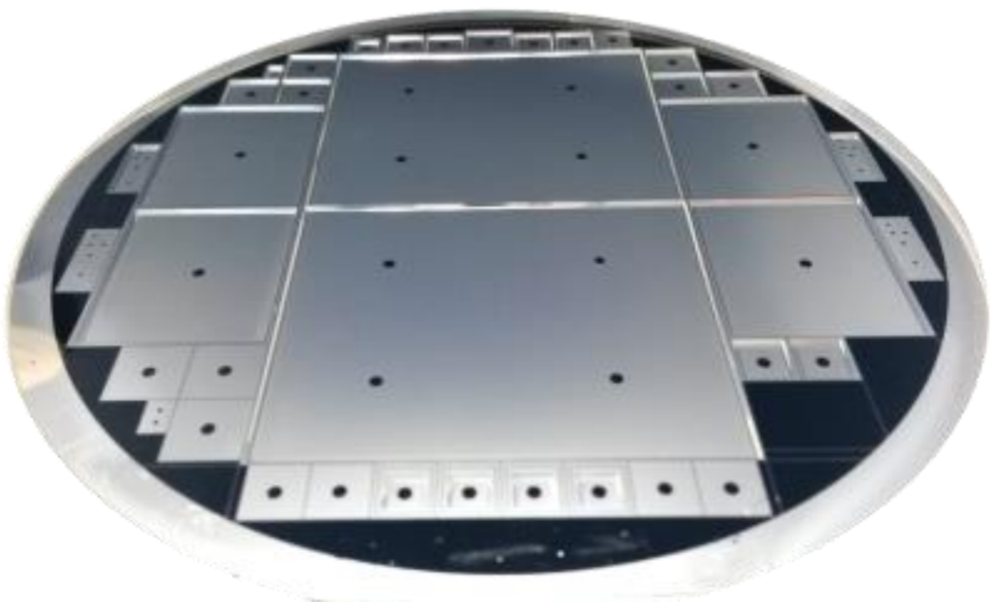
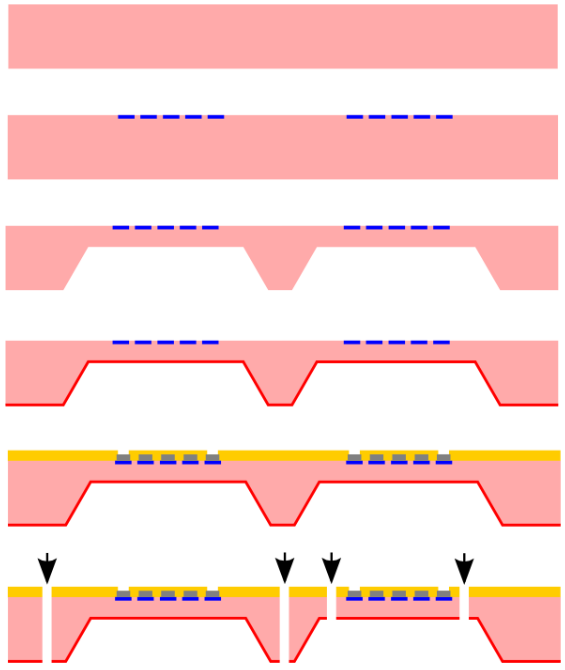
- successful n-in-p run on 4“ wafers



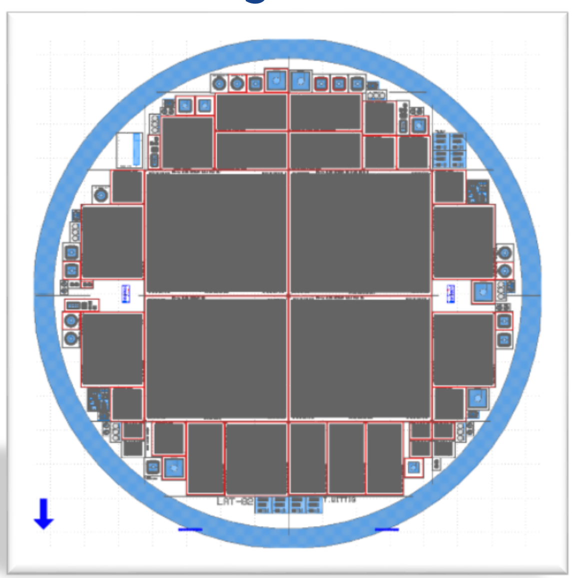


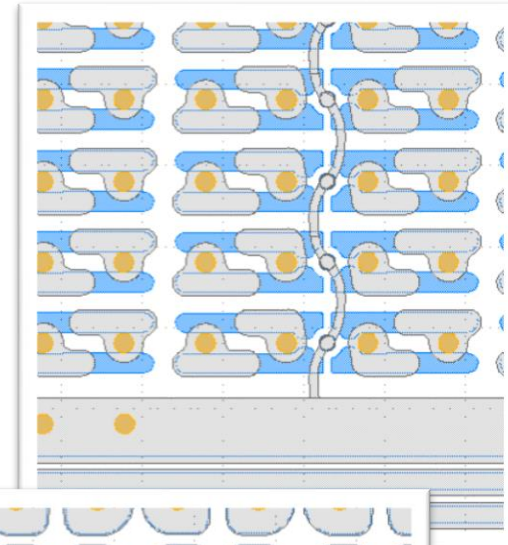
ATLAS ITk design
MPP Anna Macchiolo

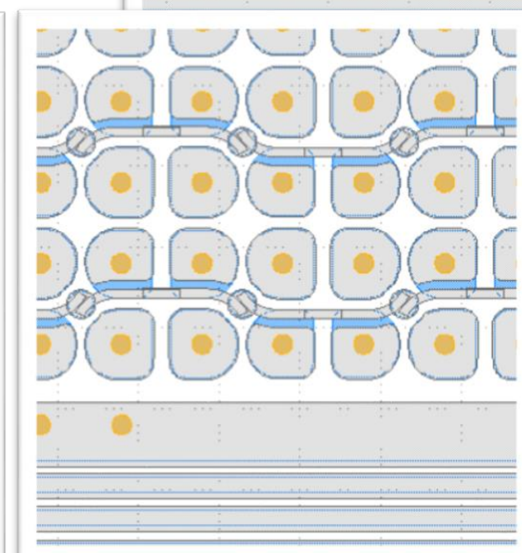
sensor thinning by cavity etching single sided sensors

CiS

- successful n-in-p run on 4“ wafers
- technology is currently transferred to 6“ wafer size
  - *production finish expected begin 2018*
    cavity etching step is currently performed
- same kind of sensors for comparison
  - FE-I4 quads & SCS
- additionally several other new designs
  - RD53 test chip
  - CMS Roc4Sens
  - Omegapix
  - Medipix
  - test structures …







ATLAS ITk design
MPP Anna Macchiolo

sensor thinning by cavity etching double sided sensors

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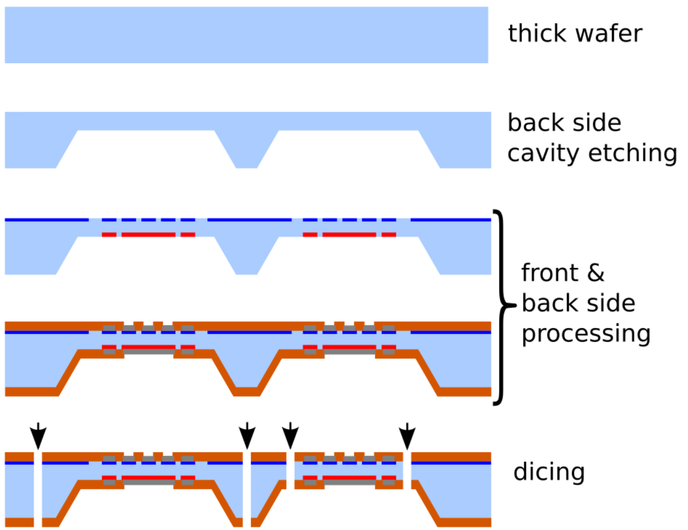
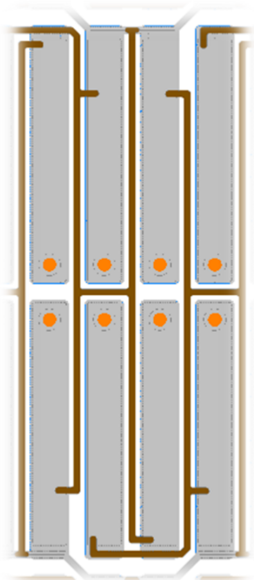
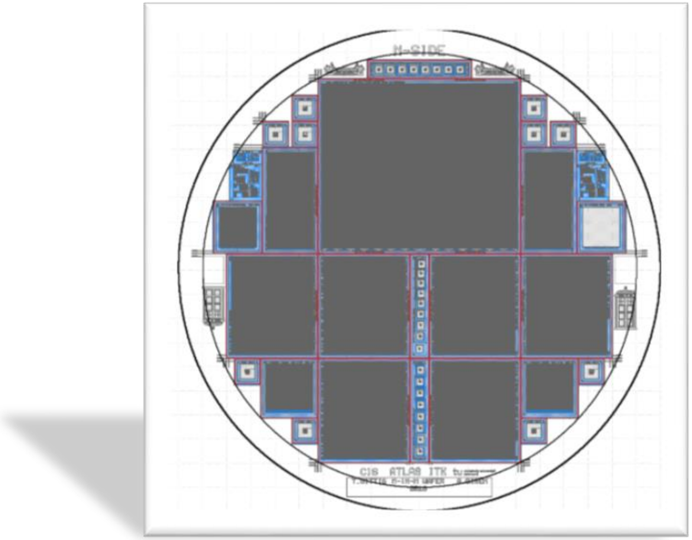
- technology of cavity etching is transferred to a double sided wafer process (n-in-n pixels)
- upcoming 4“ wafer run in cooperation with TU Dortmund
- same kind of sensors for comparison
  - FE-I4 quads and SCS
- additionally several other new designs
  - RD53 test chip
  - micro strip sensors
  - test structures …
  - implementation of Poly-Si bias resistors
- R&D of technology implementation already started
  - photo lithography within cavities quite challenging
- a reference run (200µm thick, without cavity thinning) is close to finalization







Flip chipping
FEI4 on ATLAS pixel sensors

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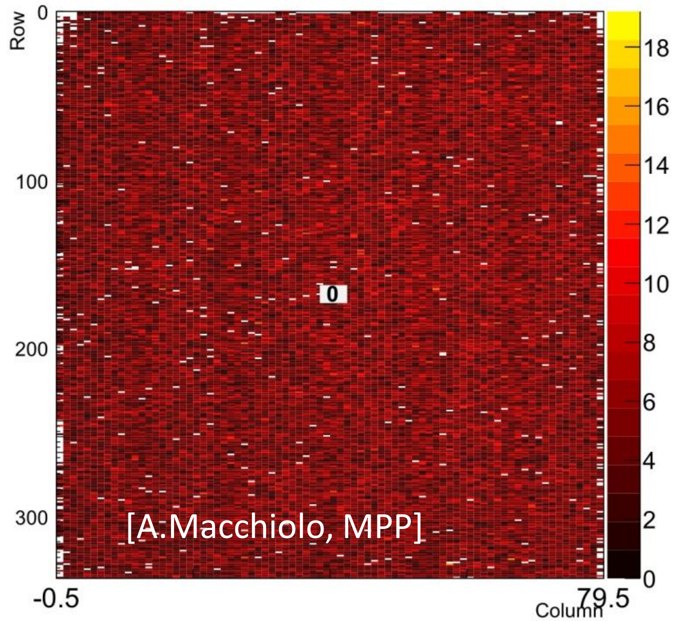

- gained experience with the alignment of the FE-I4 SCS
- first quad module is assembled
  - positioning is more challenging
  - need to callibrate and try out different flip chip tool to see whether it works better

- thin FE-I4 sensors have been flip chipped at CiS successfully
  - sensors with CiS UBM (Ni or Pt)
  - chips with IZM bumps

further R&D sites

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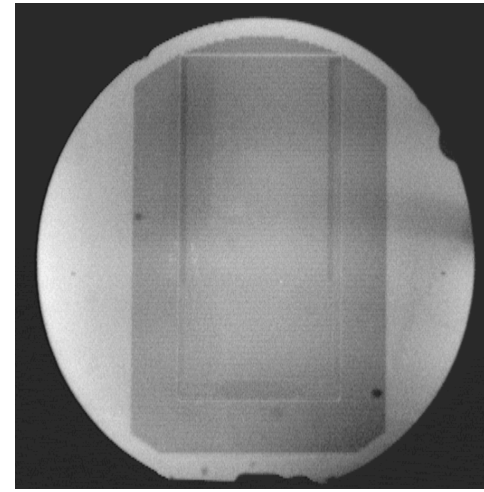
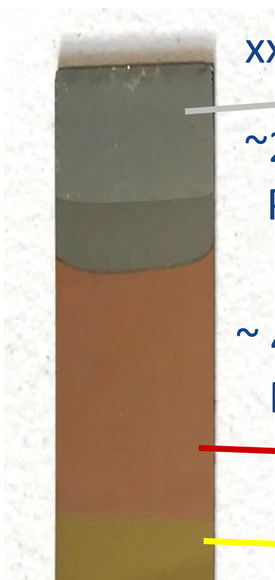
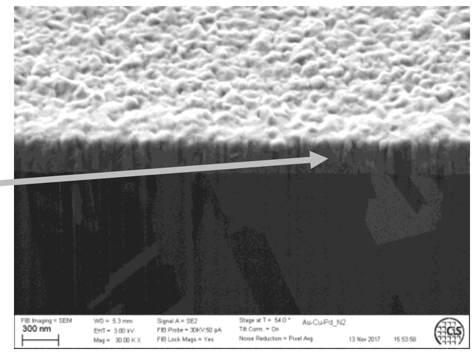
- Micro-channel cooling (4inch MEMS silicon devices)



- New materials:
  - chemical Cu deposition (pillars, power lines,…)

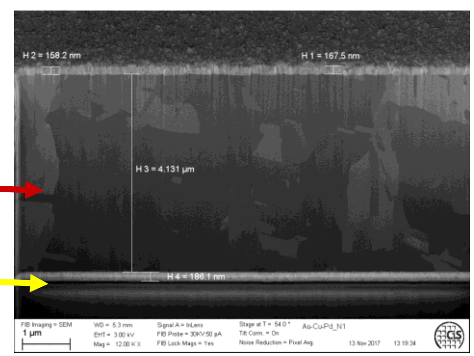


xx µm SAC solder



~250 nm thick Palladium layer

~ 4 µm thick Nickel layer



Seedlayer: Au

conclusion

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- active edge wafer run is successfully finished
  - proof of principle is provided
  - despite apparent damages,
    at least the thin sensors show good yield
    with inactive edges down to 50µm
  - side wall doping with BBr_3 seems to be advantageous
    - low leakage currents
    - small trenches sufficient
    - rather cheap process
- large area cavity thinning
  - successful single sided process is currently transferred to 6“ wafer size
  - R&D to study feasibility of a double sided process has been started
- flip chipping with thin FE-I4 sensors is in progress
  - assembly of SC modules work well
  - assembly of quad modules is still optimised

contact

CiS

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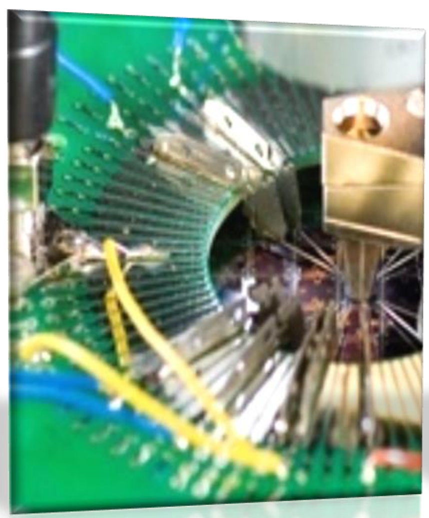
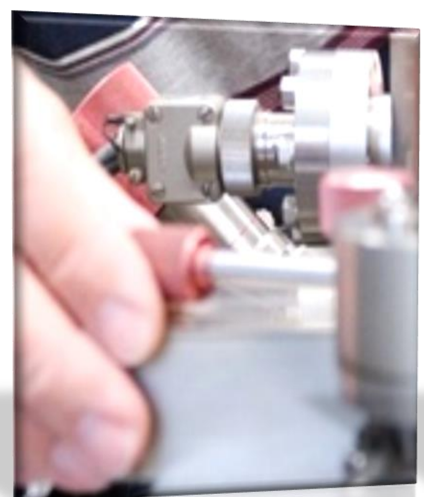


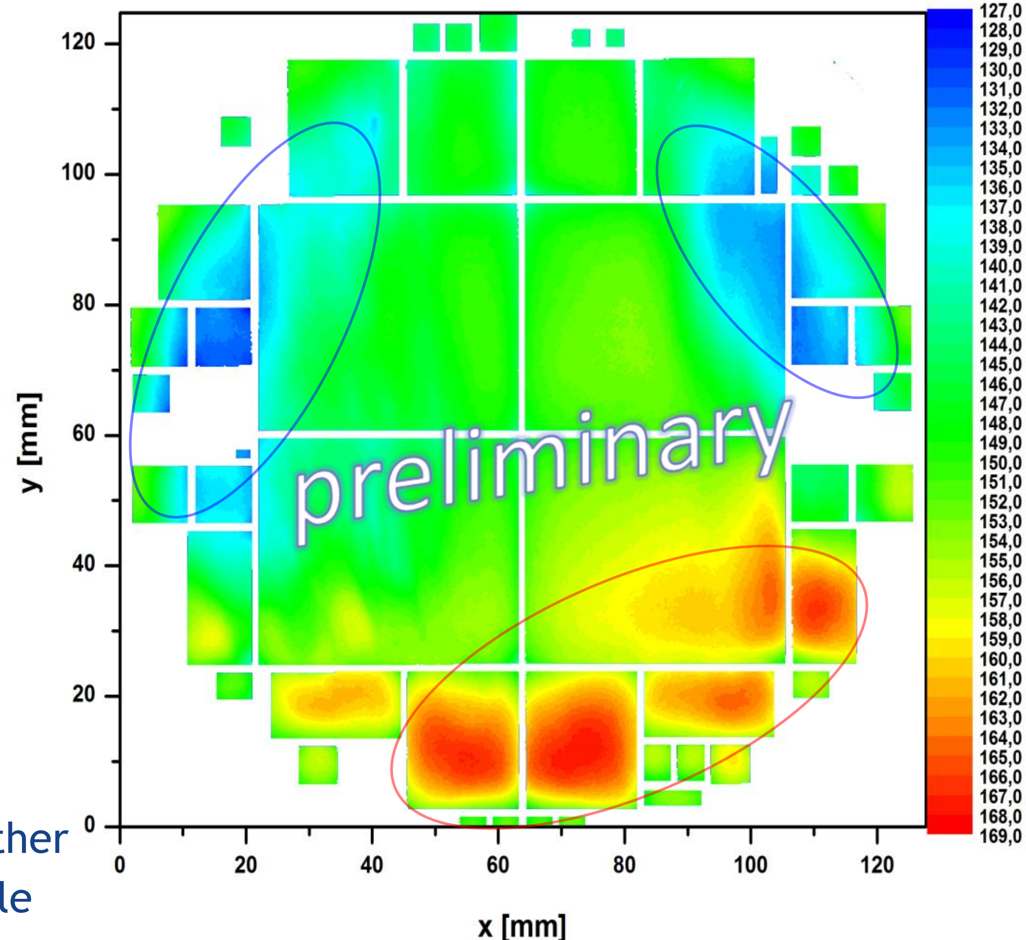


Backup

sensor thinning by cavity etching
6” dummy wafer run

CiS

- first 6” dummy wafer run finished to study mechanical properties after KOH etching
- in principle, the technology works
  - larger areas with good homogeneity
- but: areas of higher deviations are visible
  - patterns are more or less similar from wafer to wafer
  - systematic reason is assumed
    - inhomogeneous circulation in the KOH bath
    - wafers stand too close together
    - no rotation of wafers possible
  - ➔ several possibilities for optimizations are available
    - slight increase in costs for small scale runs



V1: four $42x36mm^2$ areas

sensor thinning by cavity etching 6” dummy wafer run

CiS

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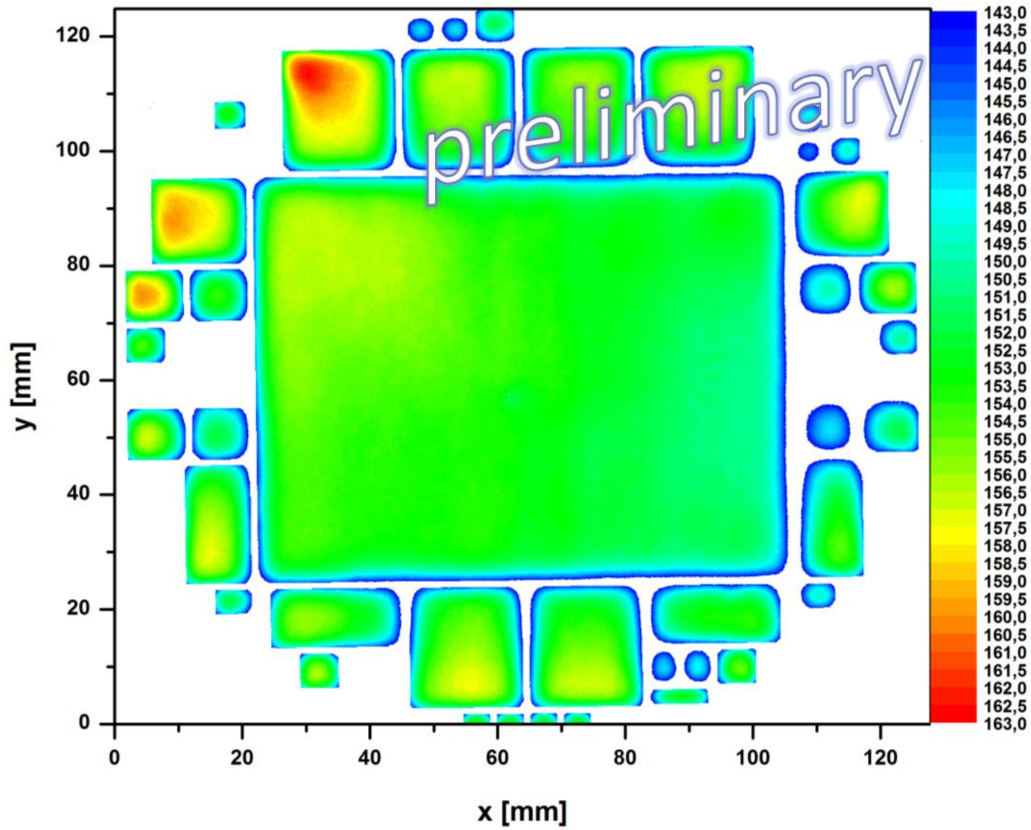

V2: one $84x72mm^2$ area

UBM @ CiS

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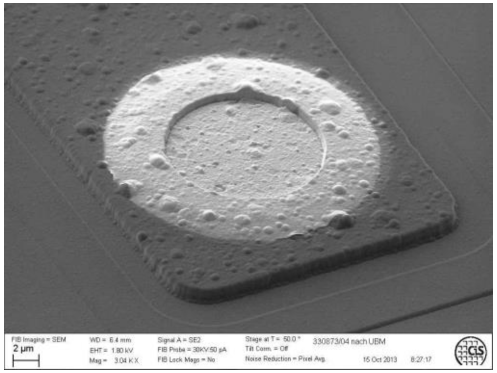
mask-based (thick lift-off) electroless Ni-UBM	mask-less Ni-UBM

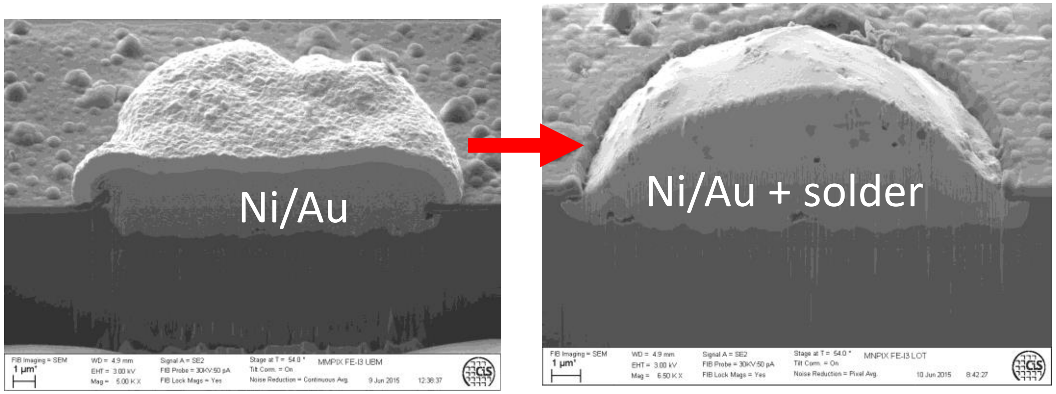
mask-based (thick lift-off) electroless Ni-UBM

- done for CMS-Pixel production, in combination with In-bumps
- process is partly outsourced
- relatively thin film on sensor surface
- already tested with (IZM) solder bumps

mask-less Ni-UBM

- Ni is growing on Alu surface on all passivation openings
- covered with Au layer
- can be done in-house
- already tested with immersion soldering to obtain solder caps





deails of active edge sensor run

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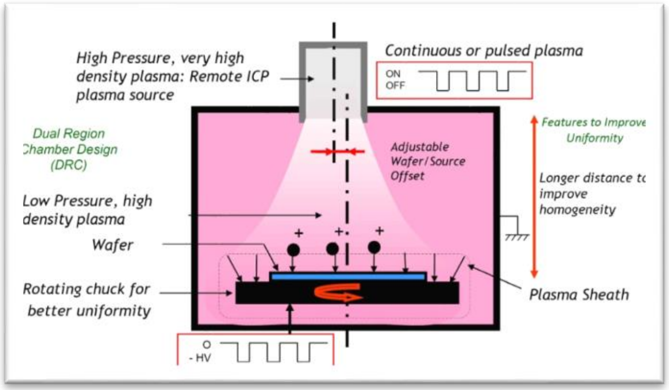
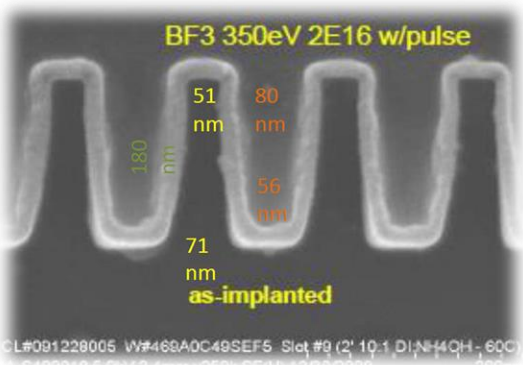
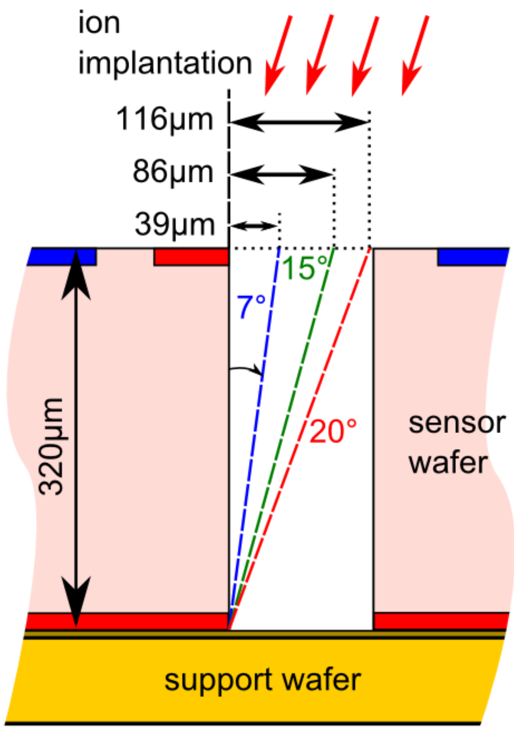
Several parameters are varied which can be compared

- p- and n-type bulk
- sensor thickness (300 & 100µm)
- three side wall doping methods
  - 4-quadrant ion implantation (4QI)
  - plasma immersion ion implantation (PIII)
  - BBr_3 deposition from gaseous phase







ideas to remove of support wafer

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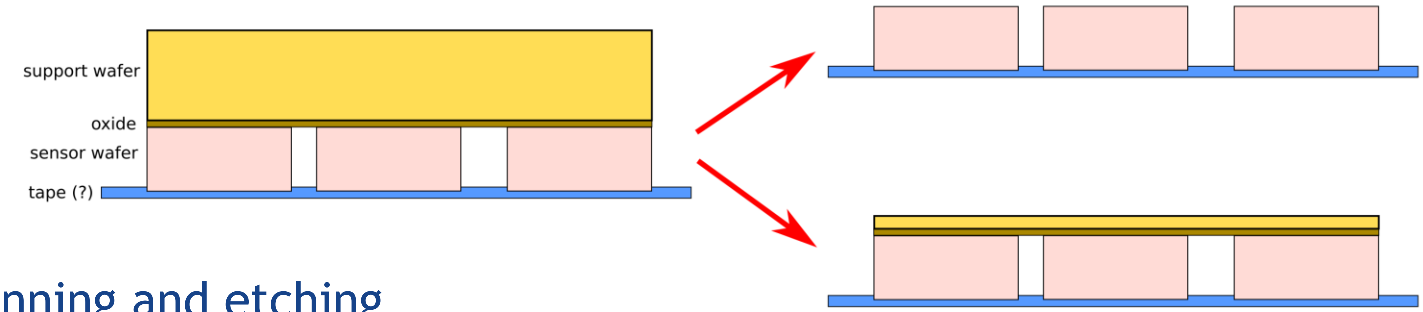
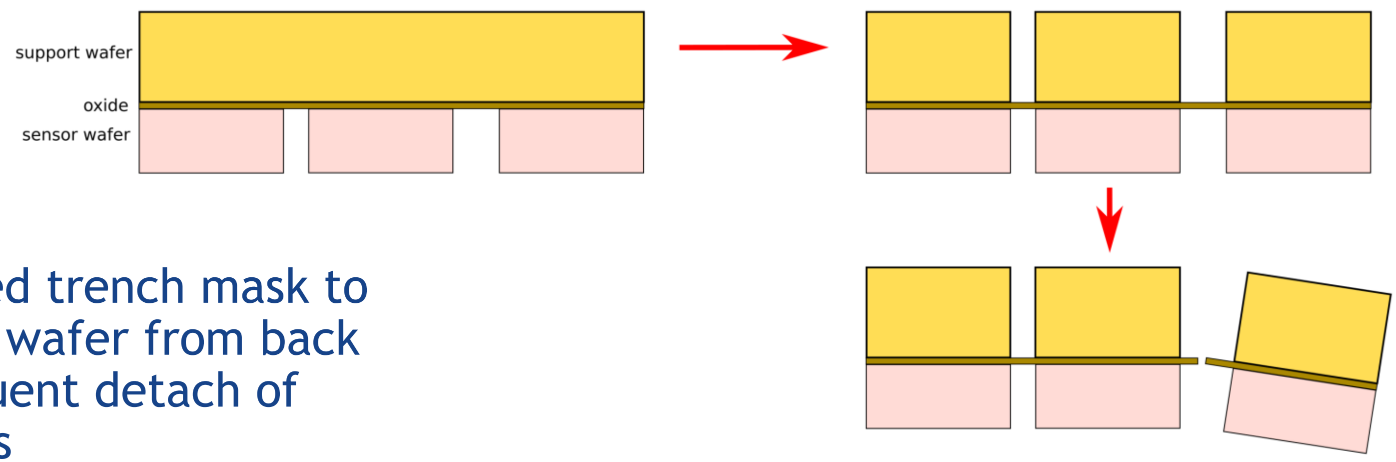


- back side thinning and etching of support wafer



- using mirrored trench mask to etch support wafer from back side; subsequent detach of single sensors

IV of BBr$_3$ doped samples

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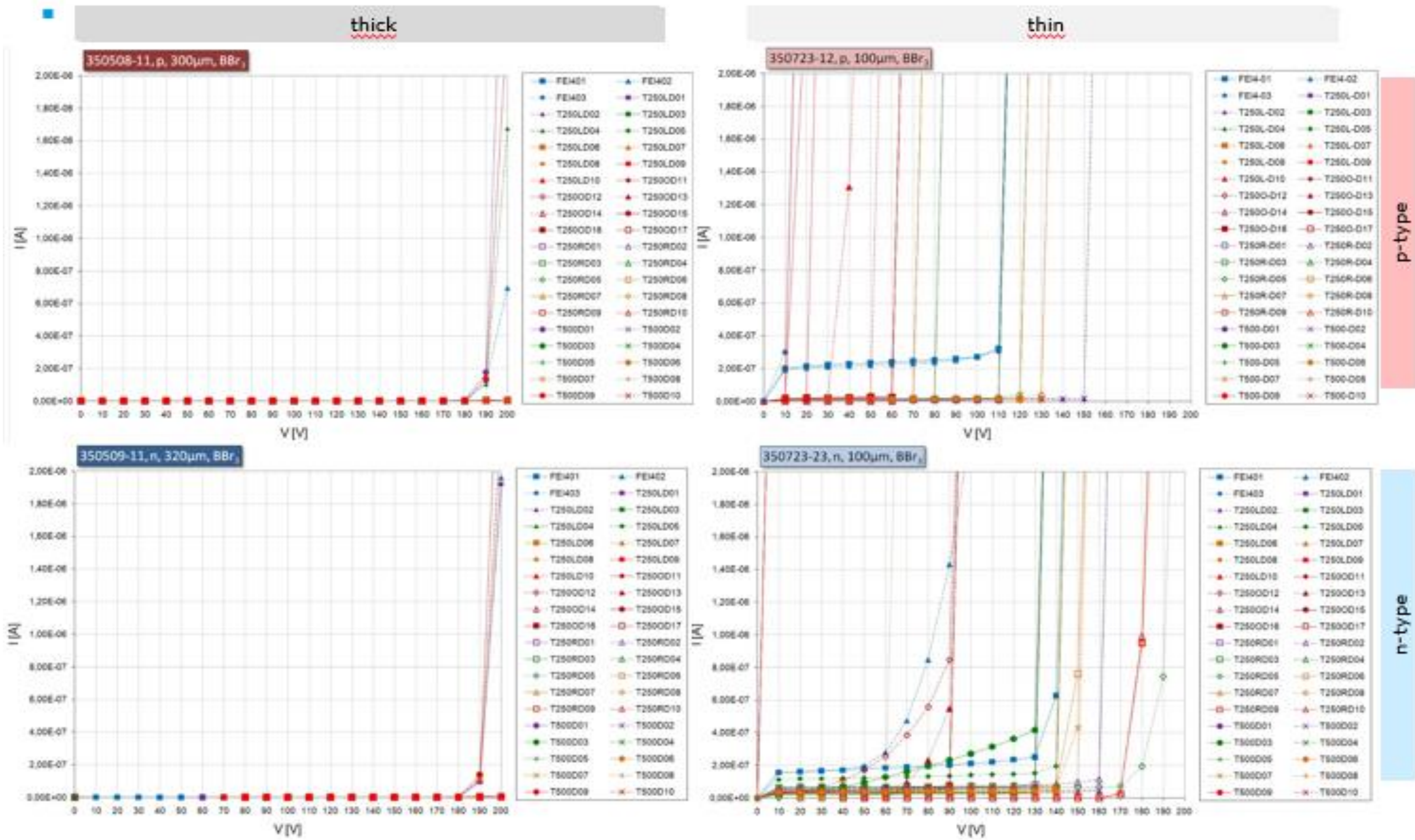
Boron tribromide difusion



slim edge
reduction of inactive sensor

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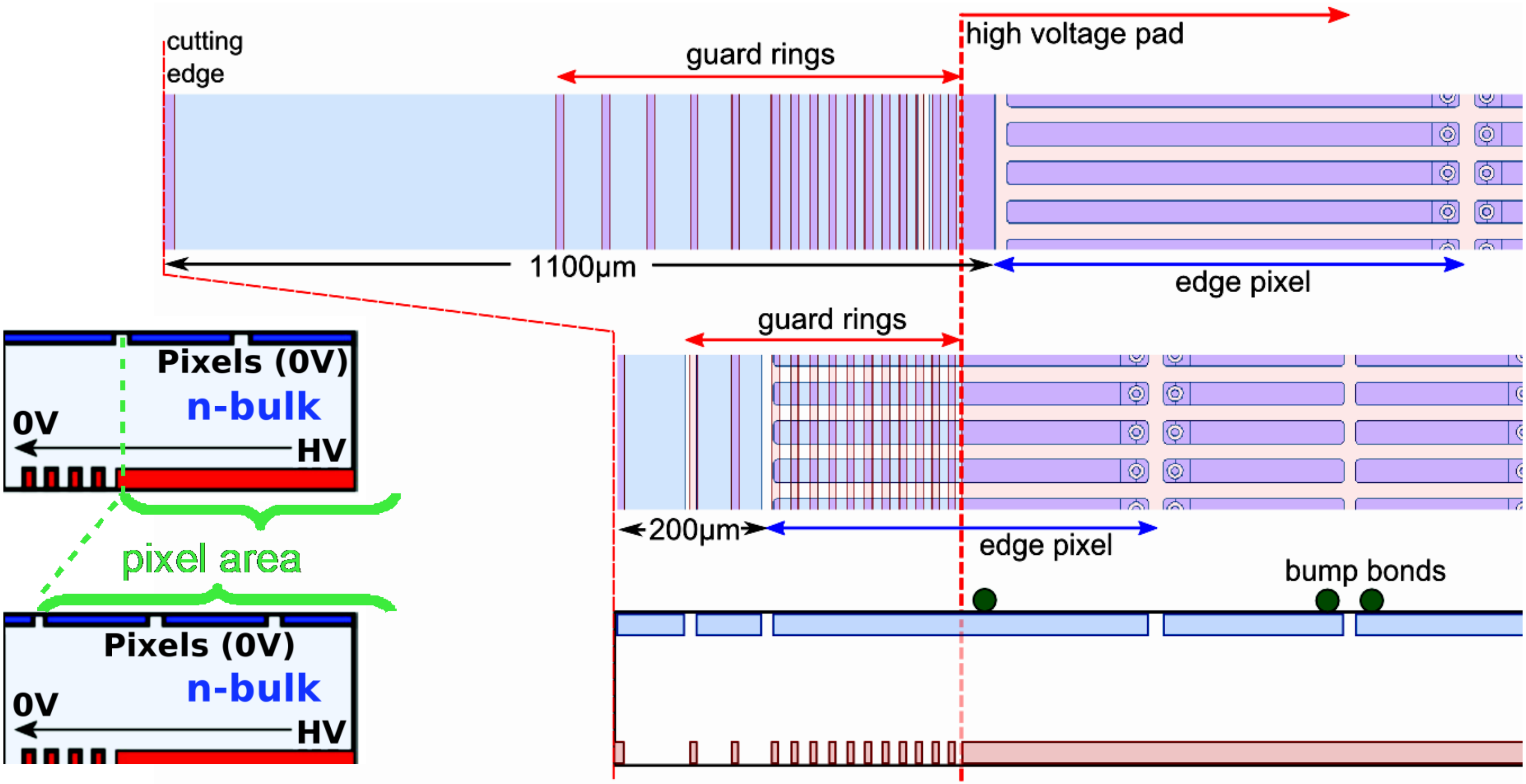
- in the past: ATLAS IBL design
- n-in-n, double sided, guard rings overlap the pixels



active edge sensors

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- only one side structured
- n-in-p as well as n-in-n sensors can be processed
- same masks can be used