



# Progress toward Cold Electronics for Pixelated Readout of the DUNE Near LArTPC

Dan Dwyer (LBNL)

ArgonCUBE Collaboration Meeting

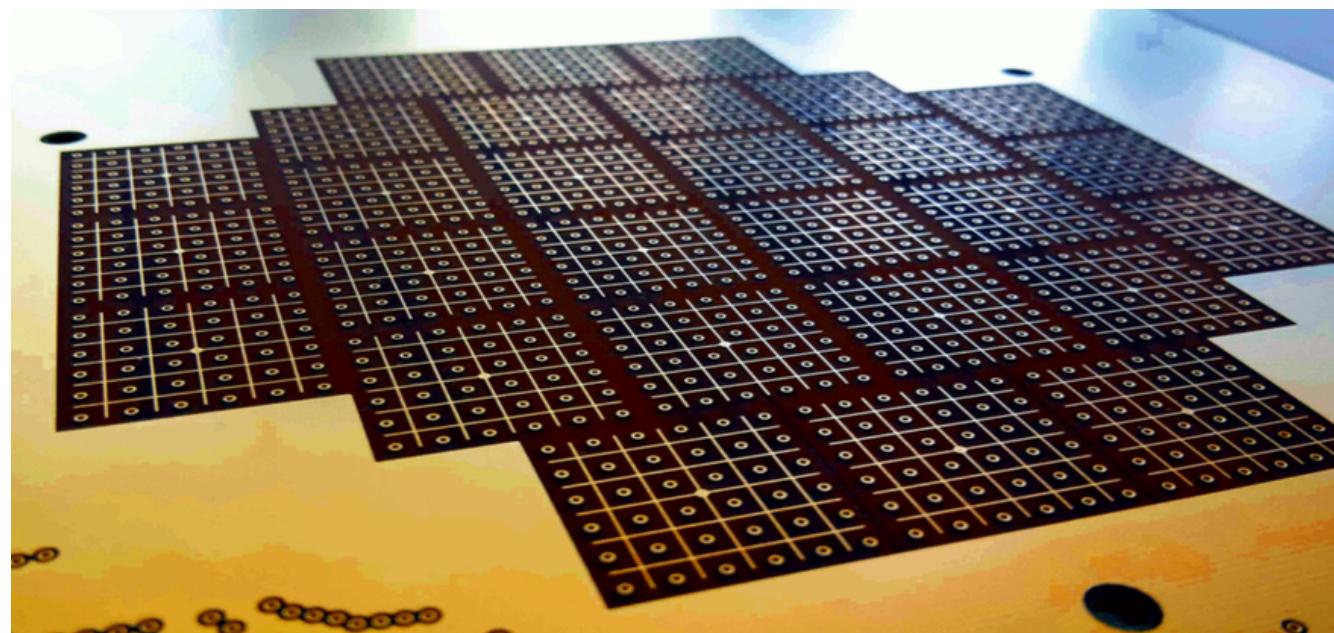
Oct. 17, 2017



# Pixel Sensor Development

## LHEP group at Univ. of Bern / ArgonCUBE:

- Demonstrated pixel sensor in LAr (Summer 2016)
- Need low-power electronics for large-scale use



*Pixel spacing: 3mm*





# Introduction

## Developing front-end ASIC for scalable LAr-TPC pixel readout

- True 2D readout: front-end channel for each ‘pixel’ (i.e. pad-based readout)
- Scalable: power use must be very low to avoid excess heat generation in LAr

## Recent Progress:

- LArPix v1 ASIC: wafers arrived LBNL this week
- Test PCBs: in production, delivery in ~1 week
- Control system: firmware and software written, now in testing.

## Initiating testing program:

### Electronics testing:

Initial tests on bench at room temp, in cold box, and at  $\text{LN}_2$  temperature

### In-situ testing:

Actual particle detection in small pixel demonstrator TPC provided by Bern

## Team:

D. Dwyer, C. Grace, M. Garcia-Sciveres, A. Krieger, D. Gnani, T. Stetzelberger, M. Kramer, S. Kohn, P. Madigan



# Prototype IC Targets

## v1 prototype considerations:

- Limit requirements in order to advance schedule, increase chance of success
- Focus on two critical aspects:
  - 1) Demonstrate low-noise low-power cryogenic amplifier
  - 2) Demonstrate MIP-track detection capability in test TPC

### Goal 1: Amplifier

**Noise:** < 1600 ENC

SNR of 9 to 1 for MIP signals

**Power:** < 50  $\mu$ W/channel

Total heat load: ~few W/m<sup>2</sup>

**Channel Density:** >= 16 ch / chip

Minimize system complexity, cabling

### Goal 2: MIP-track detection

**Multiplexed:** >= 100s of pixels per output

Achieve MIP detection with feasible # of feedthroughs.

**ADC LSB:** LSB < 1600 ENC

Digitization noise < amplifier noise

**ADC Range:** 6-bit range

Span MIP signal range

**ADC Time-resolution:** <= 2  $\mu$ s

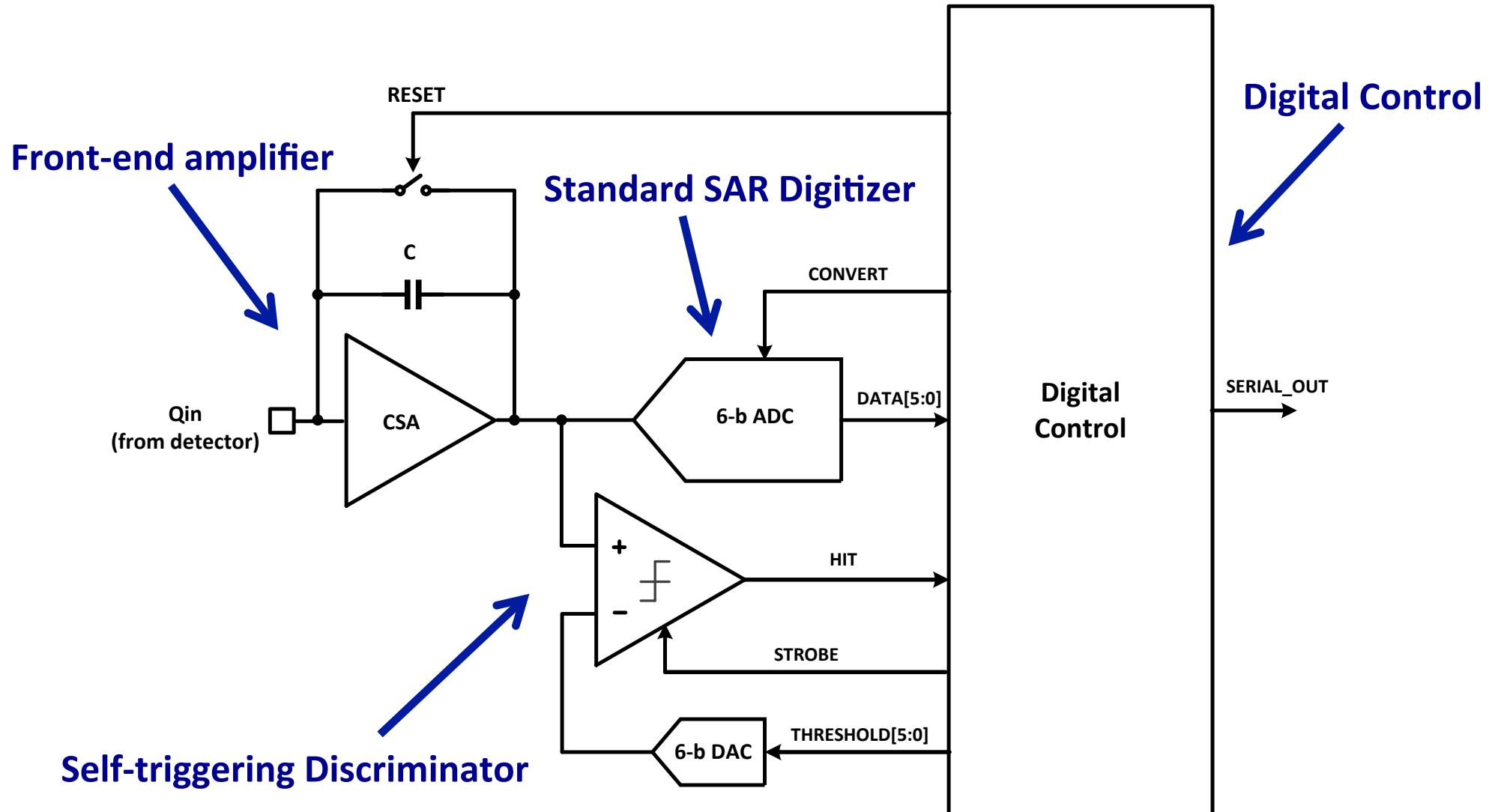
Equal or better than spatial resolution (3 mm)

**Deadtimeless:** Buffer > 1500 digitizations

Handle worst-case: track perpendicular to pixel

# LArPix v1: Design Concept

## Amplifier with Self-triggered Digitization and Readout



*Achieve low power: avoid digitization and readout of mostly quiescent data.*



# LArPix v1: Digital Core

## Digital Core:

Based around FIFO buffer,

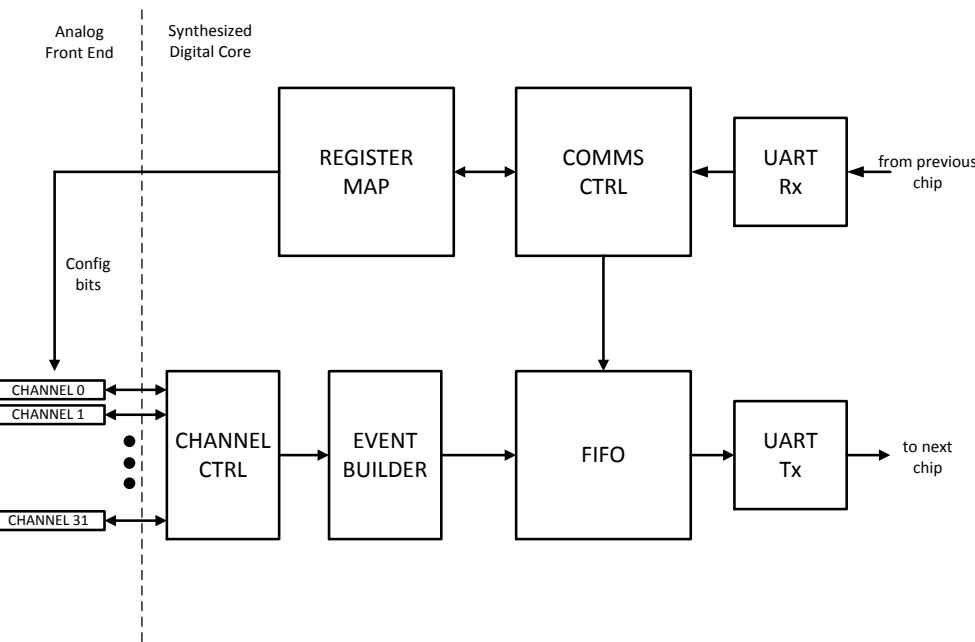
- shared by 32 channels on IC.

Digitized samples placed in FIFO

- sent out on UART Tx as available.

Incoming UART Rx data inspected:

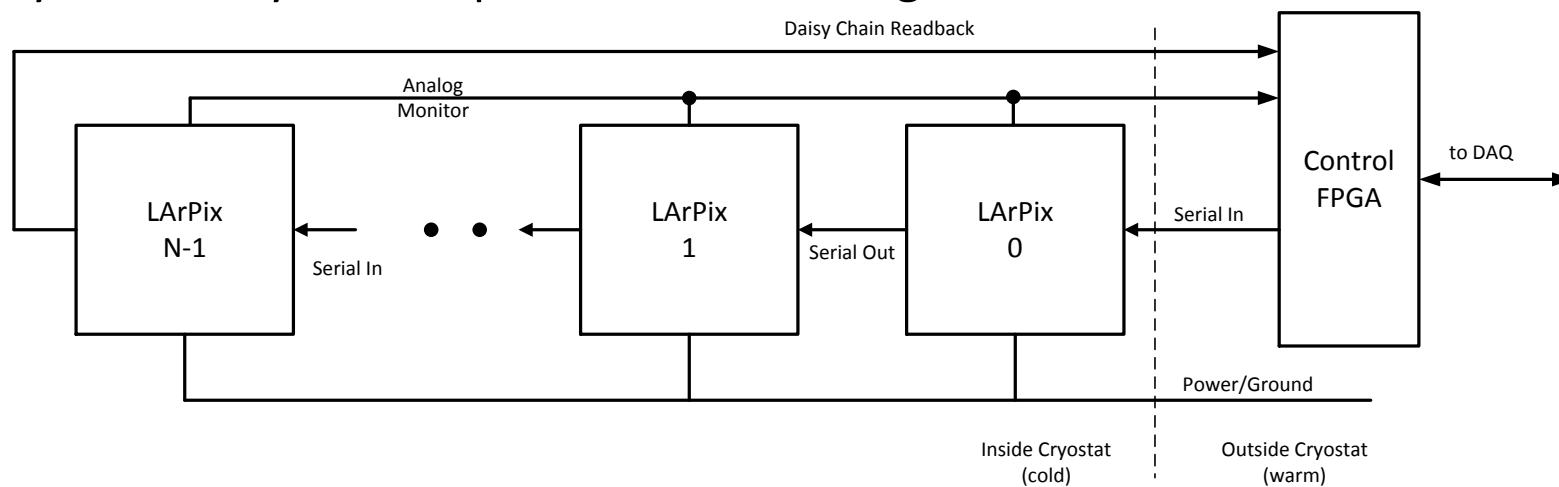
- If command for this IC, update register map.
- If not, put data in FIFO and pass to next IC.



## Daisy-chaining:

Minimize cryostat penetrations: Up to 256 ICs share two UART I/O lines

Selectively attach any CSA output to shared analog monitor line.



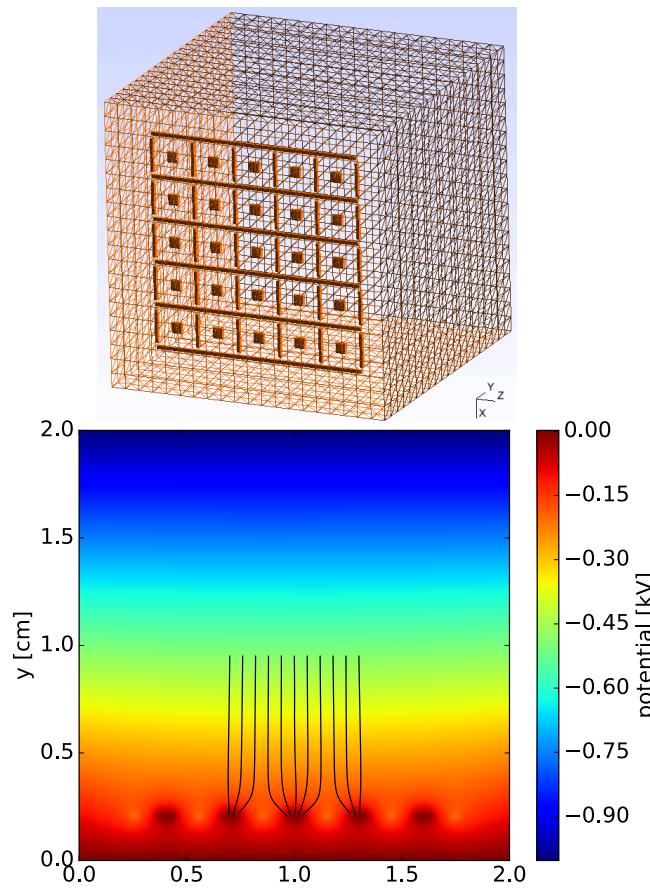
(Digital Power: ~25μW per channel, with multiple potential routes for reduction.)



# Design Tools

Developed a set of tools to assess TPC readout design

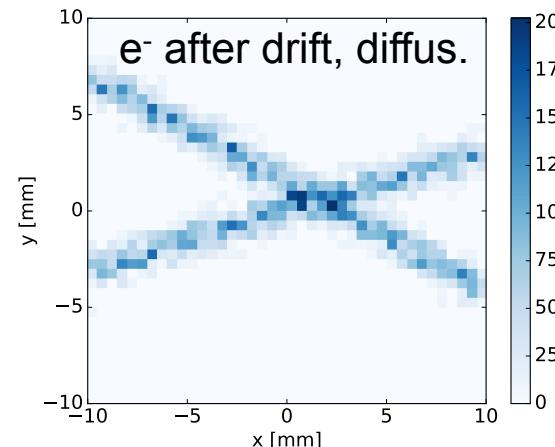
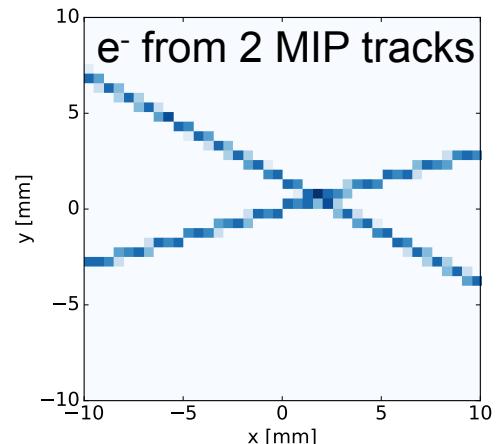
Sensor model in 3D



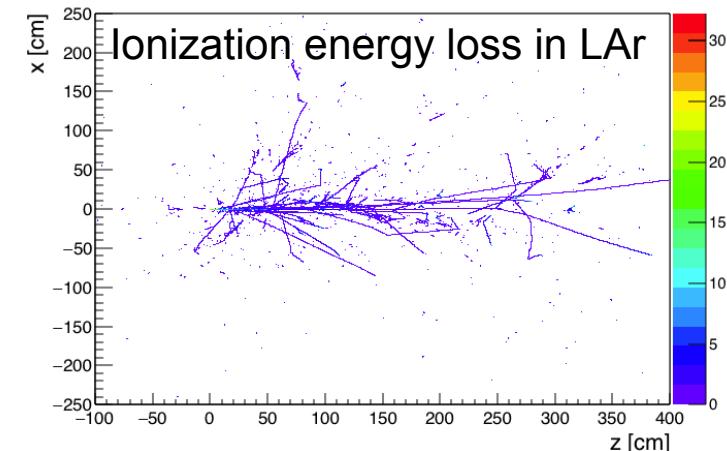
3D drift field, pix response

→ Thanks to B. Viren for intro to BEM tools

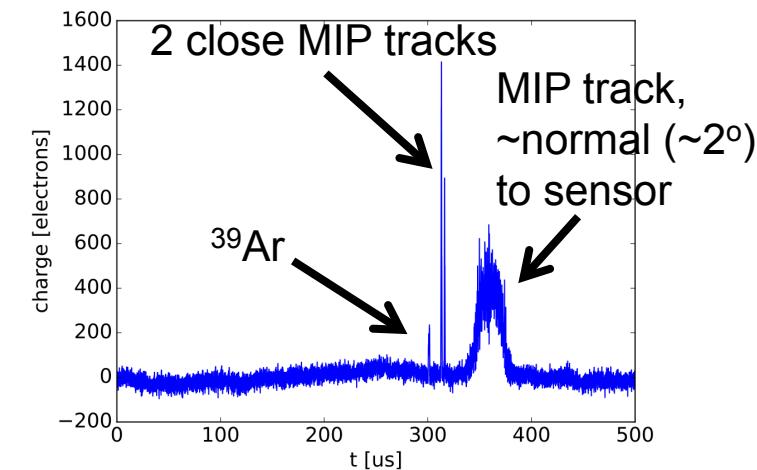
Ionization, recomb.,  
drift loss, diffusion



Fast primitive Geant4 sim.



Realistic signals (with noise)



Signals have been input to IC modeling program  
(Spice, Cadence) to assess IC design, performance.



# LArPix v1: Design Details

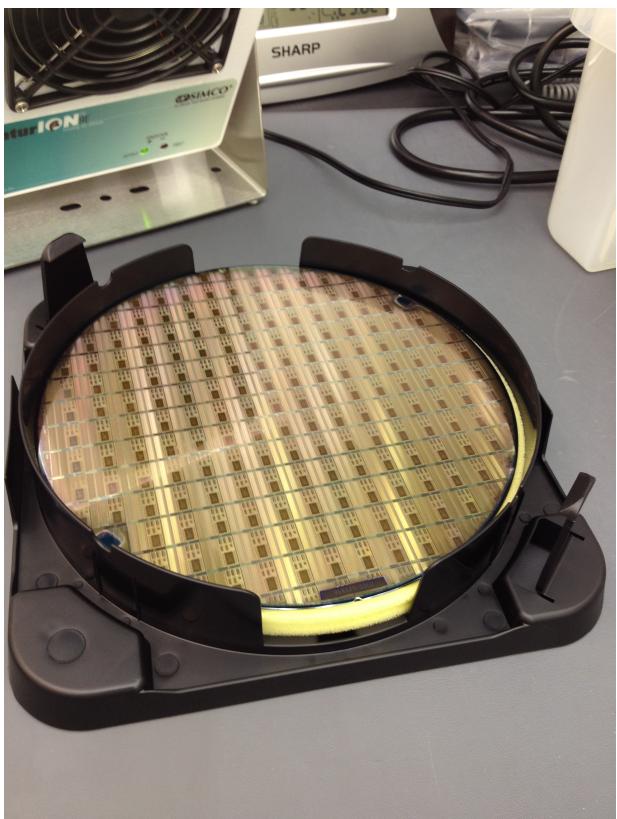
Specification	Value	Units	Note
<b>Number of Analog Inputs (channels)</b>	32 (single-ended)		160 $\mu\text{m}$ effective pitch
<b>Noise</b>	300 @ 88K 500 @ 300K	ENC, e-	Stipulated charge deposition is 15 ke- per MIP for a track in LAr
<b>Channel gain</b>	4 or 45	$\mu\text{V/e-}$	Digitally programmable
<b>Time resolution</b>	2	$\mu\text{s}$	with 10 MHz master clock rate
<b>Analog Dynamic Range</b>	~1300	mV	max signal ~ 250 ke-, minimum detectable signal ~ 600 e-
<b>ADC resolution</b>	6	bits	programmable LSB, 4 mV nominal (1 ke-)
<b>Threshold Range</b>	0 – 1.8	V	
<b>Threshold Resolution</b>	< 1	mV	nominal
<b>Channel Linearity</b>	1	%	
<b>Operating Temperature Range</b>	88 - 300	$^{\circ}\text{K}$	
<b>Event Memory Depth</b>	2048	memory locations	~8 ms without data loss in case of track normal to pixel plane
<b>Output Signaling Level</b>	3.3	V	
<b>Digital data rate</b>	10	Mb/s	with 20 MHz master clock
<b>Event readout time</b>	5	$\mu\text{s}$	



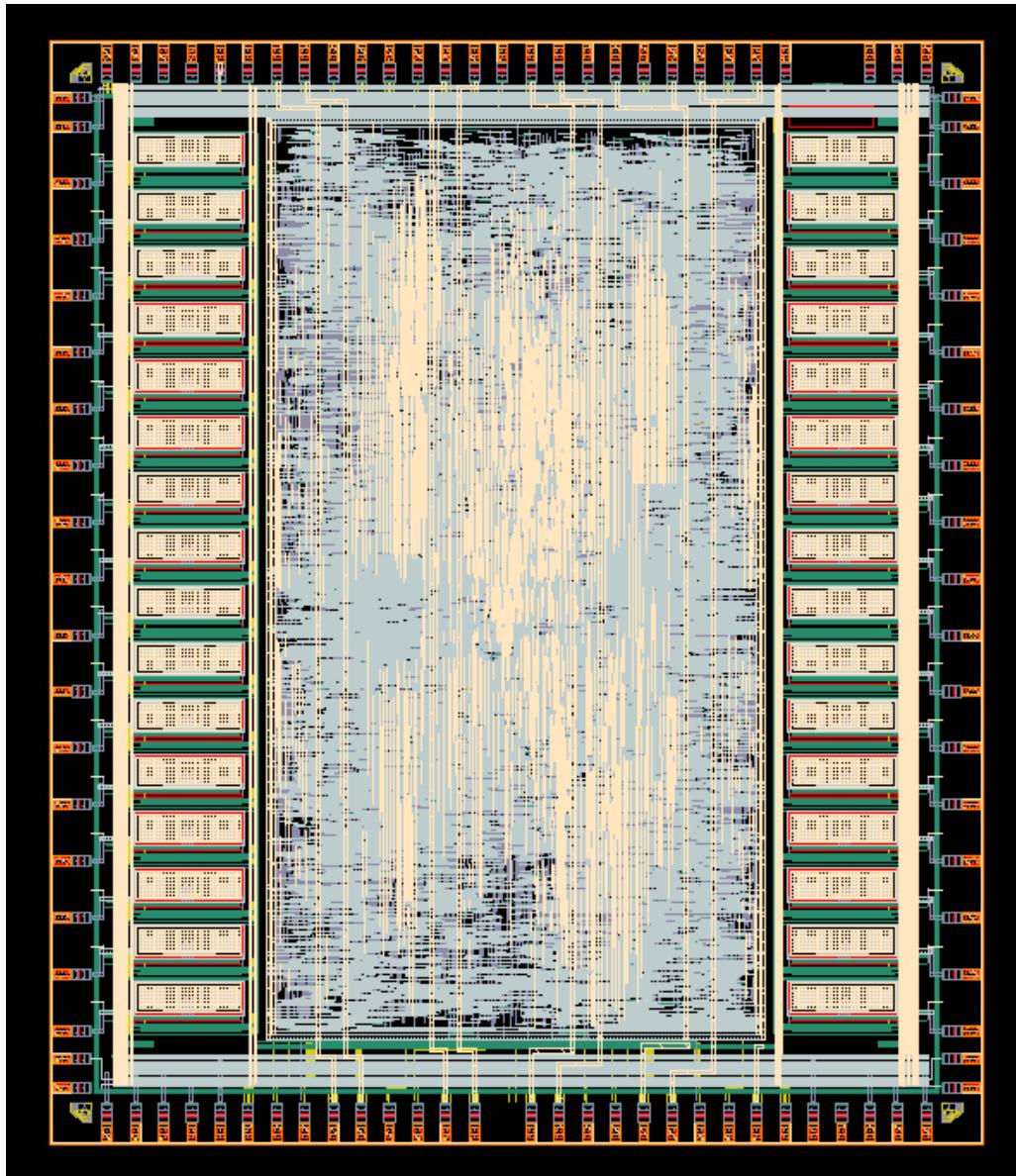
# LArPix Prototype Progress

## LArPix v1 ASIC:

- Dec. 2016: Design began
- May 2017: Design completed
- June 2017: Submitted for fabrication
- Oct. 2017: Wafers delivered to LBNL



Right now: ICs are being diced.



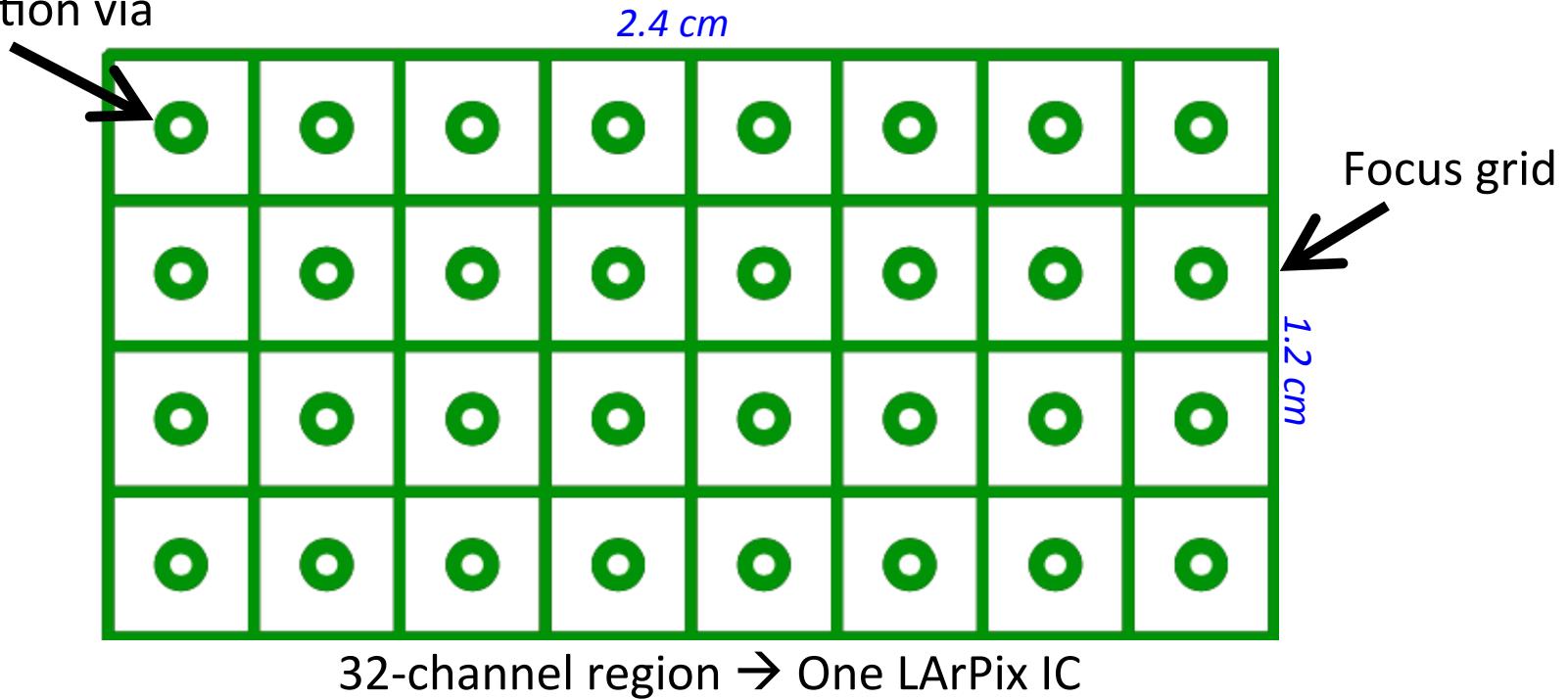
Process: TSMC 180nm

# TPC Signal PCB

## PCB as Sensor: Bottom side

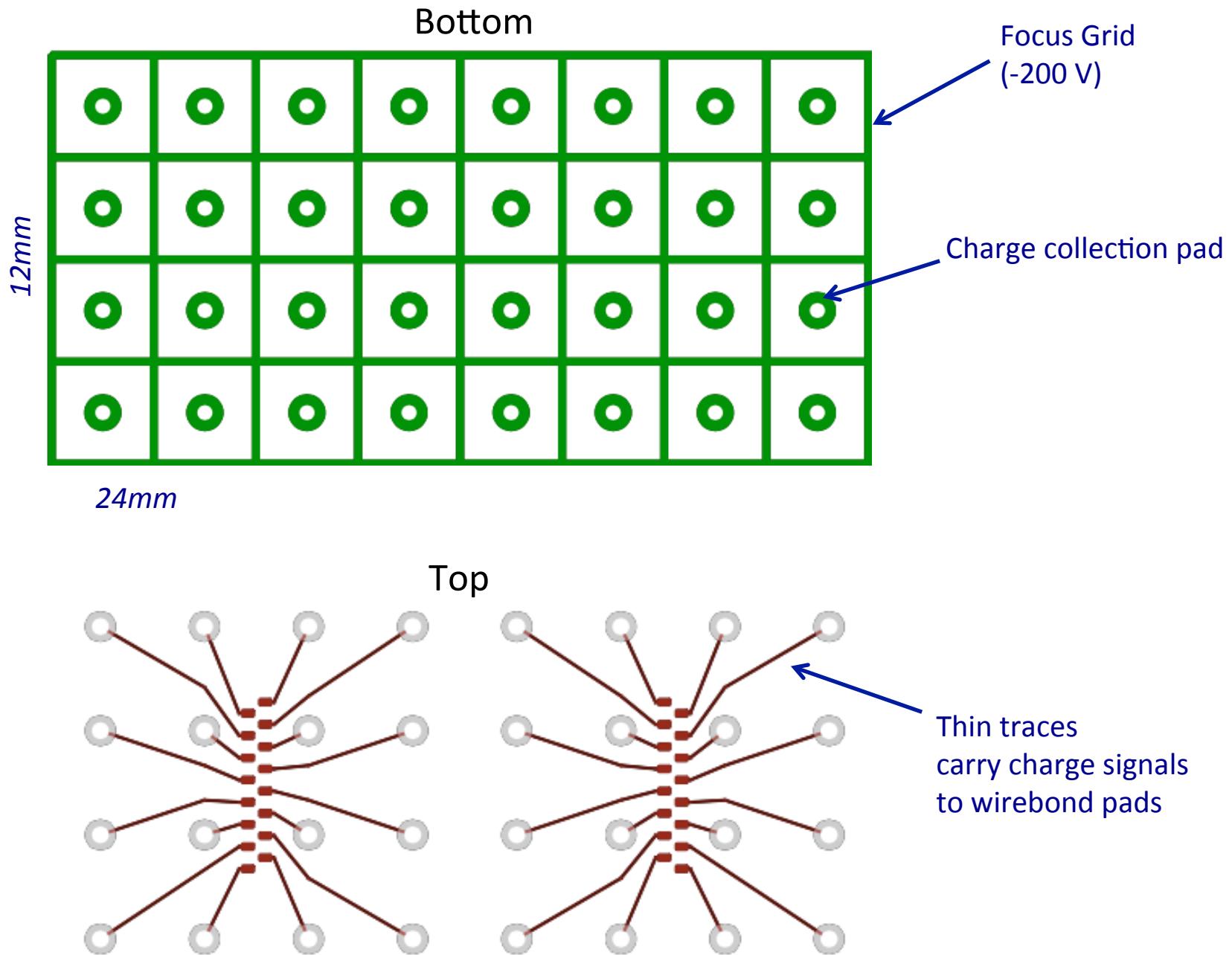
- Circular ~1mm pads collect ionization electrons produced in liquid argon
- Spacing between pads: 3mm
- Electric field in TPC volume (~200 V/cm to ~1 kV/cm) drifts  $e^-$  to sensor
- PCB grid (biased at ~-200 V) focuses  $e^-$  onto floating pads
- Key concern: keep sensor capacitance as low as possible (<4 pF)

Charge-collection via





# Signal PCB: 32-Pixel Region

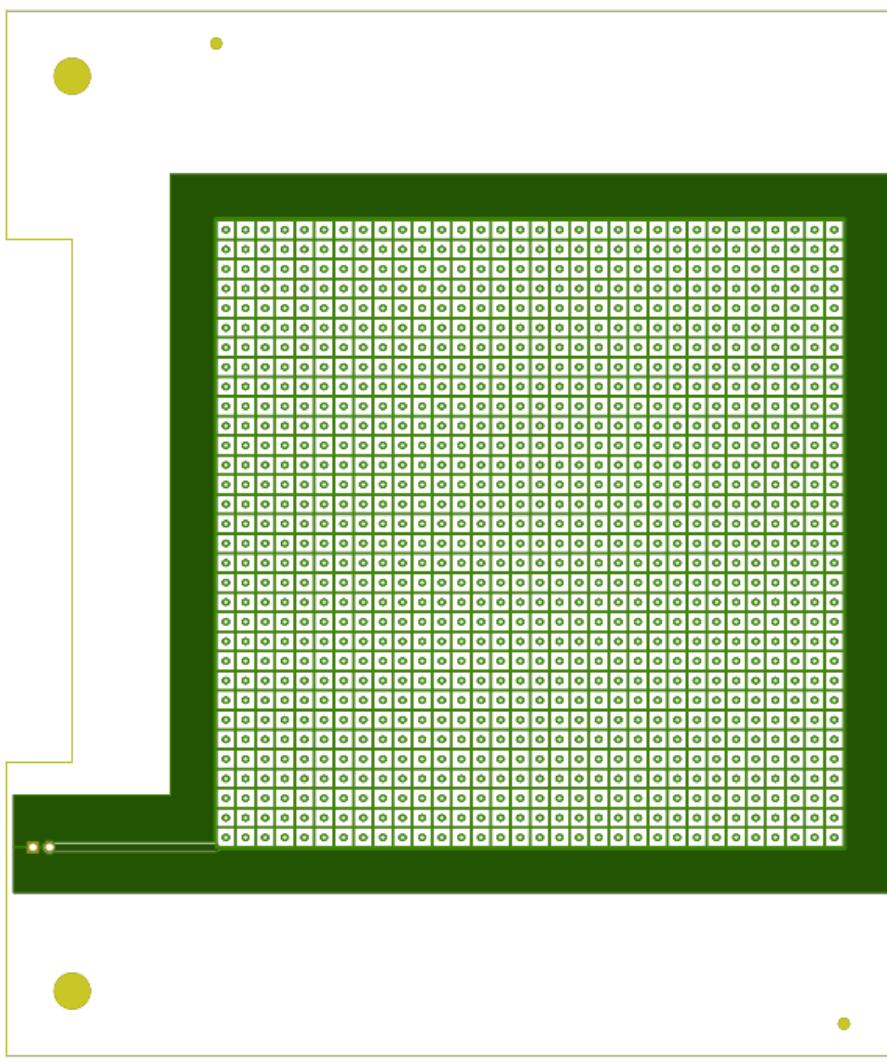




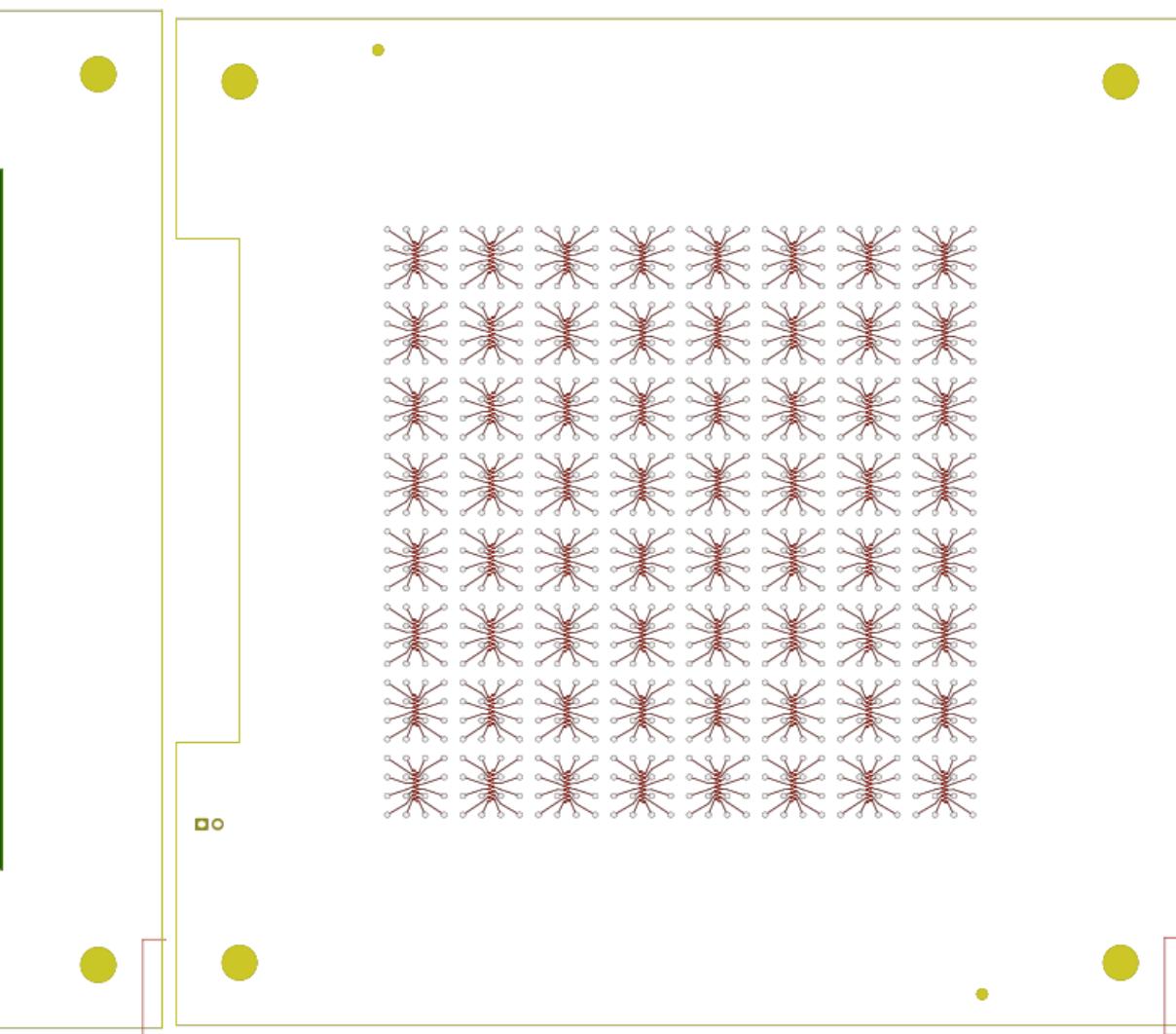
# Signal PCB: 4x8 LArPix

Designed as drop-in replacement for ArgonCube Pixel Demonstrator TPC

Bottom layer



Top layer





# LArPix v1 PCB Layout

## Modular 32-pixel PCB region:

- 2.4 cm by 1.2 cm (8 x 4 pixels)

## Top layer must fit:

- 1 LArPix v1 IC

- Routing of 12 power, ref, I/O traces

- 36 surface mount components

- 15 bypass circuits

- 4 external bias current circuits

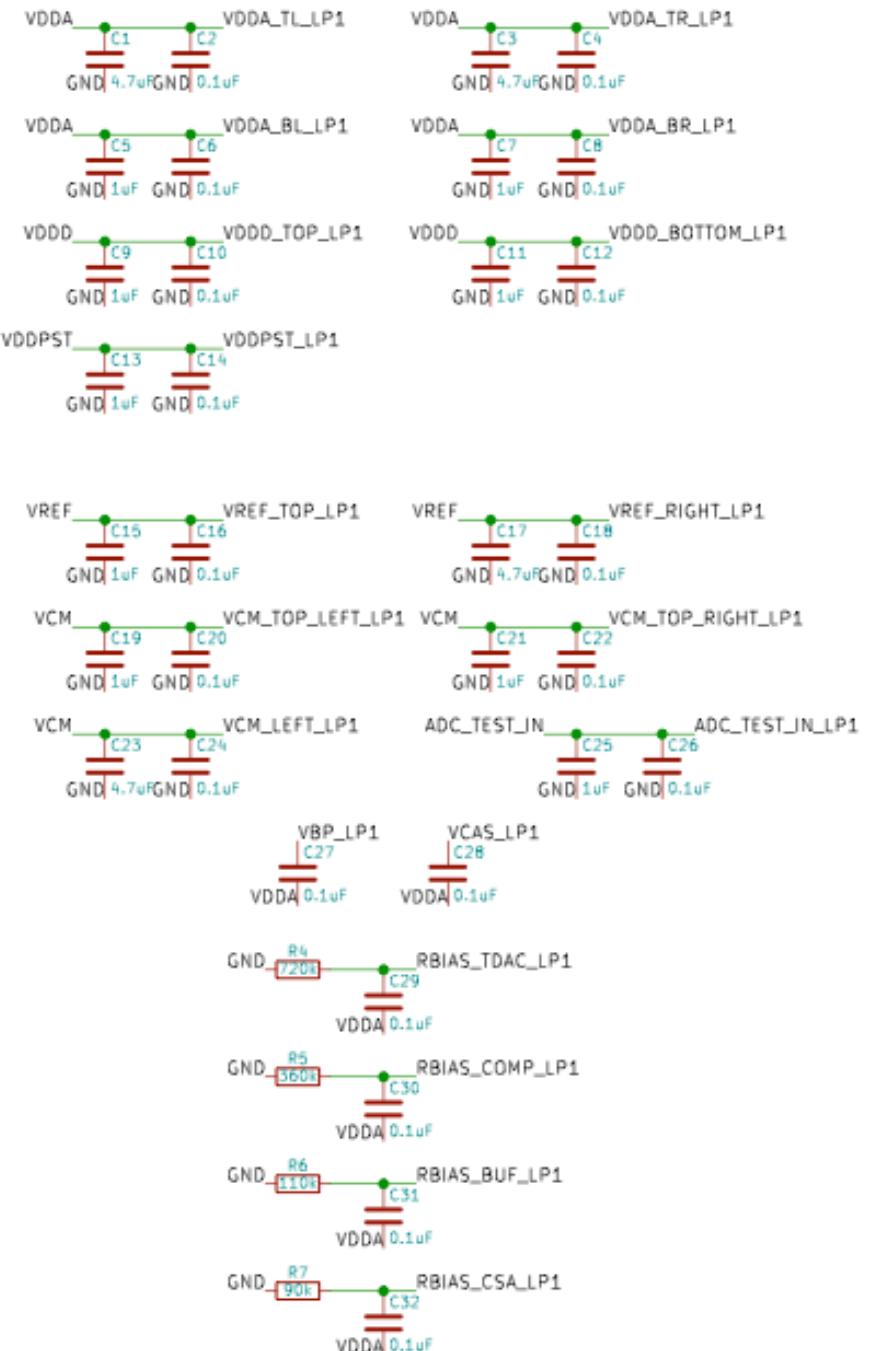
- 32 connections to input signals

## Design Constraints:

- Minimum via size: 0.5 mm (0.020")

- Minimum trace width: 0.1 mm (0.004")

- Minimum clearance: 0.1 mm (0.004")



# Current Approach

## 2 2-Layer PCBs:

**Data (Top) PCB:** 1/32" thin active PCB hosting LArPix, power, I/O

### 2-Layer PCB:



**Signal (Bottom) PCB:** 1/8" thick passive TPC sensor plane



### Issues:

- Insufficient space to route signal, power, I/O and host passive components.

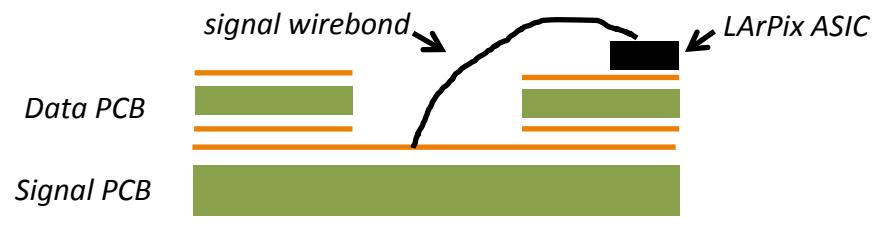
→ *Not viable for v1 prototype testing*

### Issue:

Route TPC signals from Signal PCB to Data PCB

### Solution:

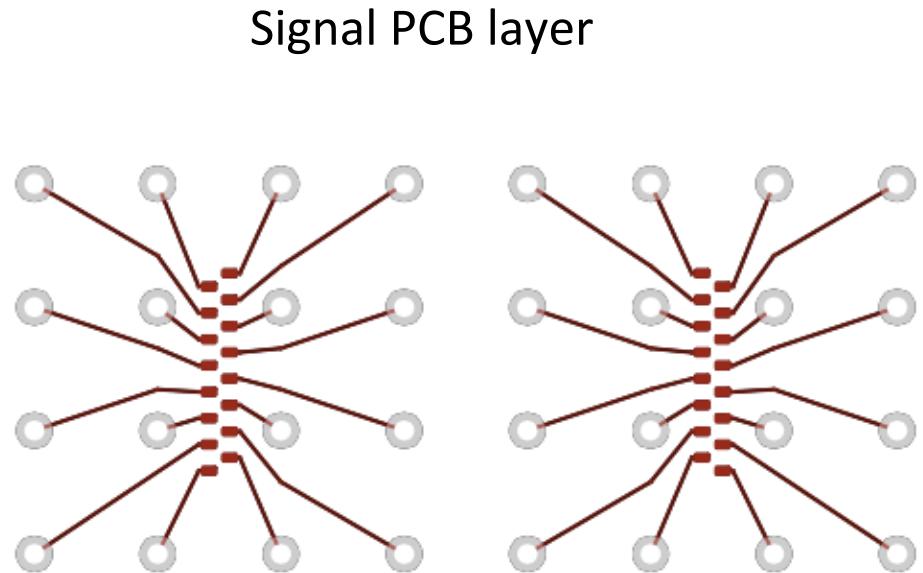
Wirebond through cavities in Data PCB



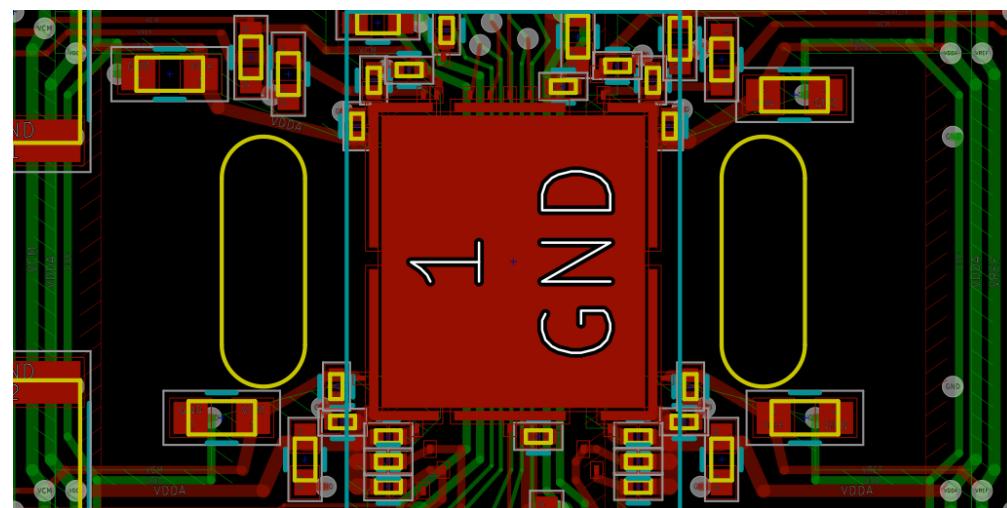
# Data PCB Layout

## Considerations:

- Power, ground, and I/O traces should avoid sensor PCB pixels and traces.  
(i.e. Traces should overlap ~2.2mm gaps between pixel blocks in sensor PCB)
- Segregate analog and digital regions of data PCB.
- Position bypass capacitors as close as possible to LArPix wirebond pads.
- Carefully consider ground returns; try to provide clear, low-impedance paths.



Single LArPix Region



Red and gold items: present on top layer  
Green items: present on bottom layer

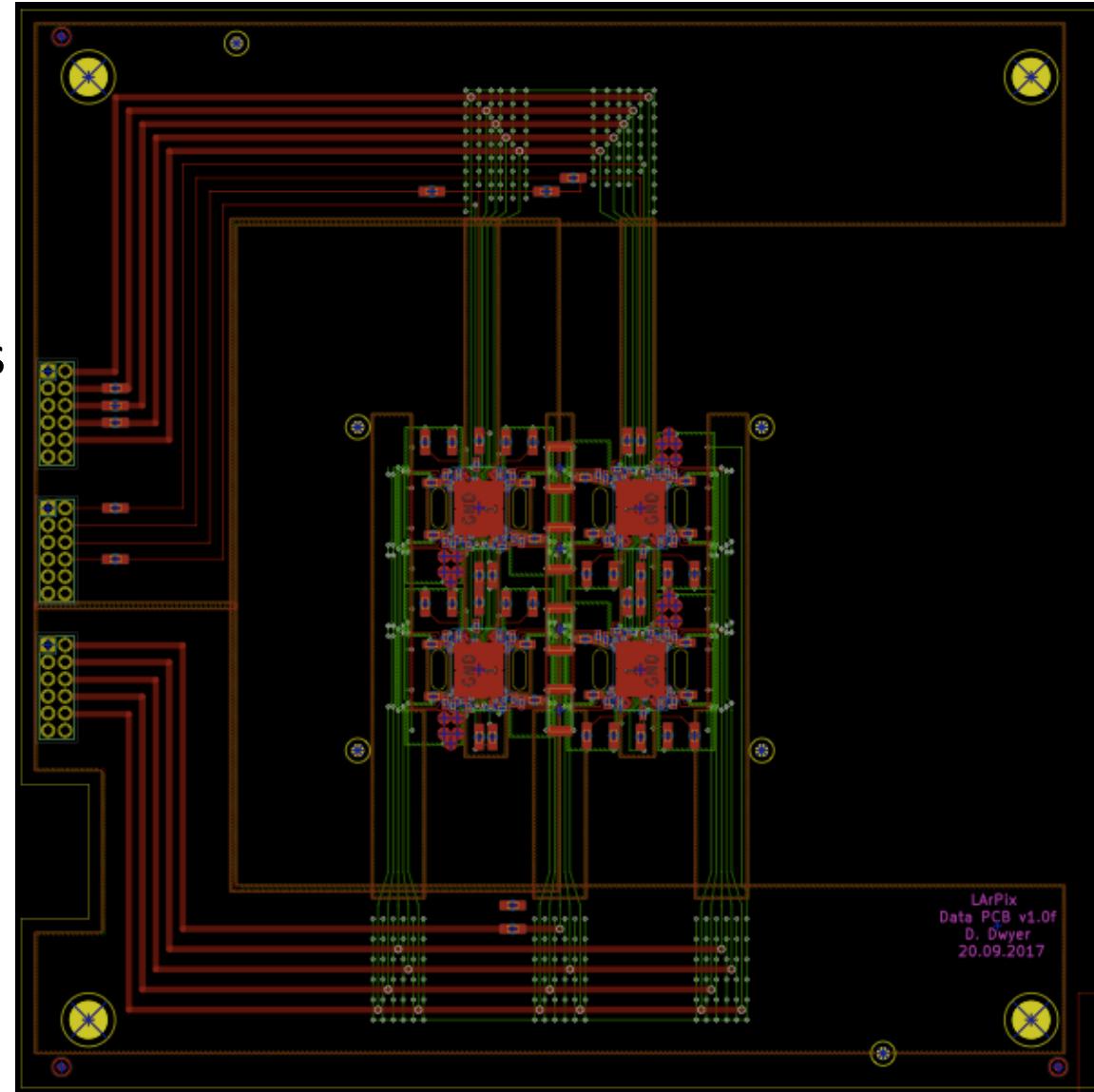


# LArPix Testing PCB

## Testing PCB for LArPix:

- Supports four LArPix v1 ASICs
- Adjustable in 1 or 2 daisy chains
- Allows bypass of any IC in chain
- Adjustable external bias networks
- Segregates digital and analog regions for lower-noise operation
- Compatible with use in Bern test TPC.
- Scalable layout for easy adaptation to full pixel plane

Submitted for production.  
Expect delivery in ~1 week.





# 2x2 Data PCB

## Step 1: Produce a 2x2 LarPix IC test board

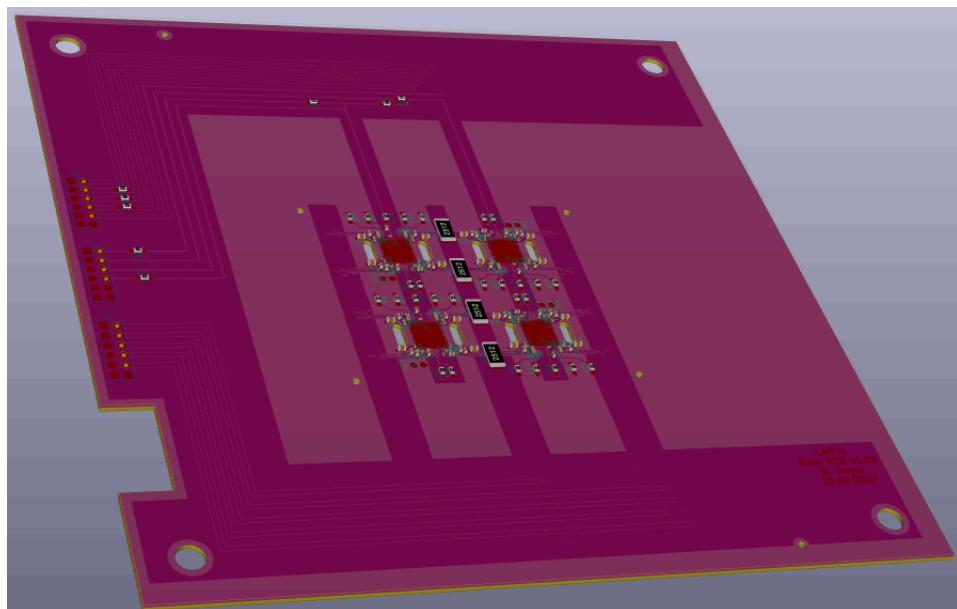
Use for initial LArPix bench-tests

Bias resistor circuit:

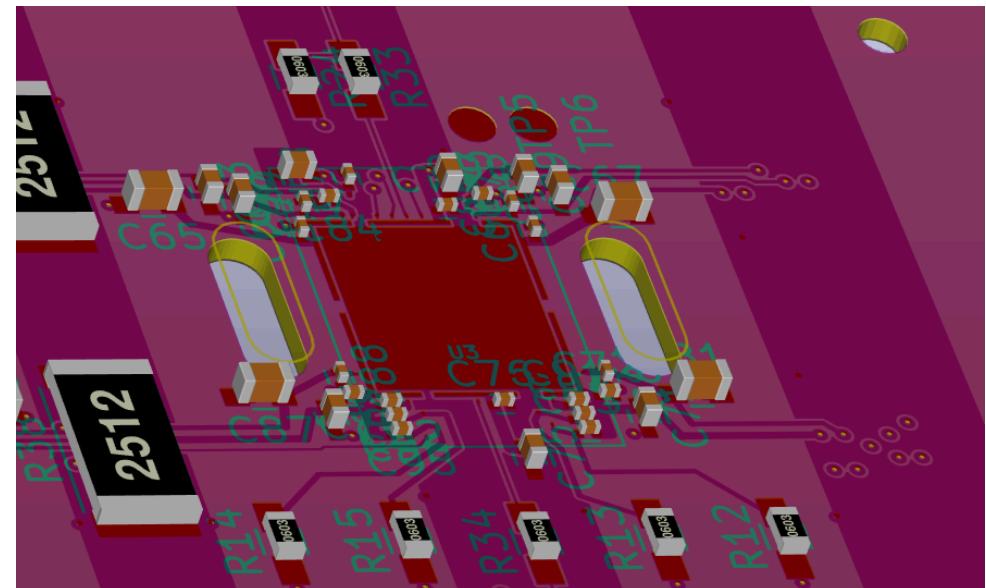
- Will need to be tuned during initial LArPix operation
- Increase size and expand layout of bias circuit, use 0805 resistors
- Allow easier modification of resistor value for initial bench tests

Revise full 4x8 Data PCB design based on lessons learned

- e.g. Can we reduce the number of bypass capacitors in the 4x8 PCB?



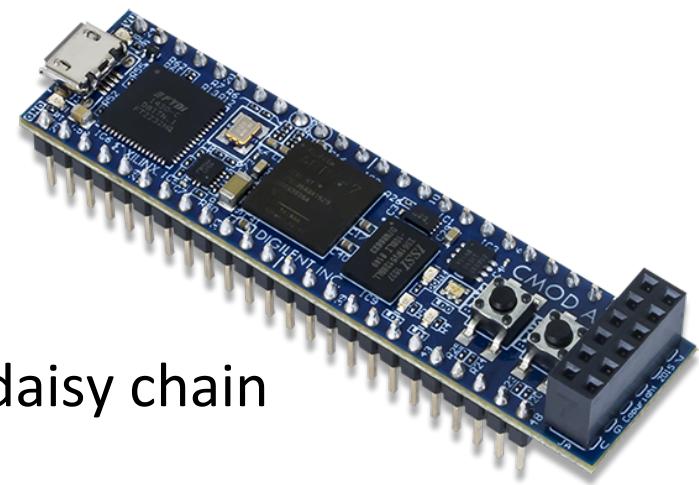
4 ASIC Test Board



0805 SMD bias resistors.  
Easier to manually remove, replace



# LArPix Control



## Digital Control System:

- Uses off-the-shelf module:  
Digilent Cmod A7 Artix-7 FPGA Module
- Module provides clock and digital I/O for LArPix daisy chain
- FPGA firmware:
  - formats configuration command packets going to LArPix chain
  - parses signal data packets returning from LArPix chain
- Software control:
  - high-level scripting to arrange LArPix configuration and data acquisition
  - communicates with FPGA module via USB
  - written in Python
- Firmware and software both written. Now in testing.

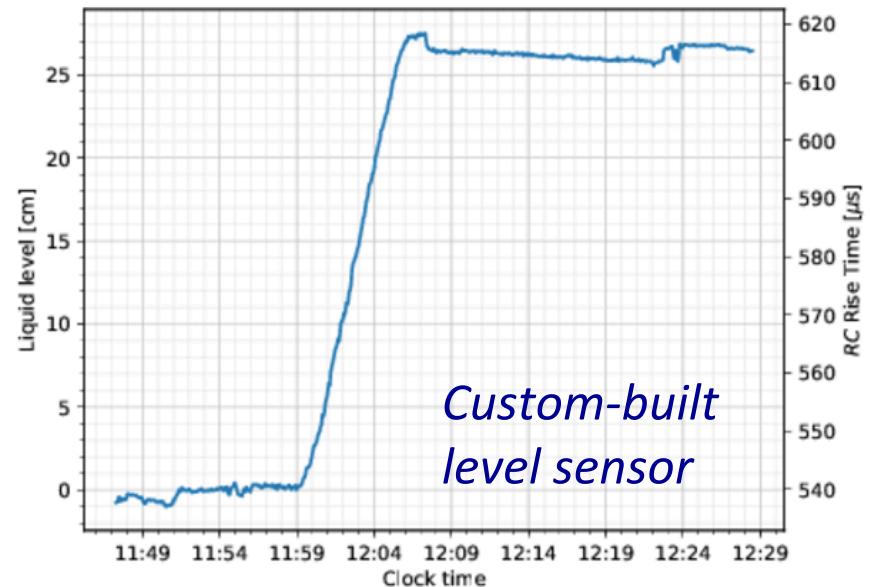
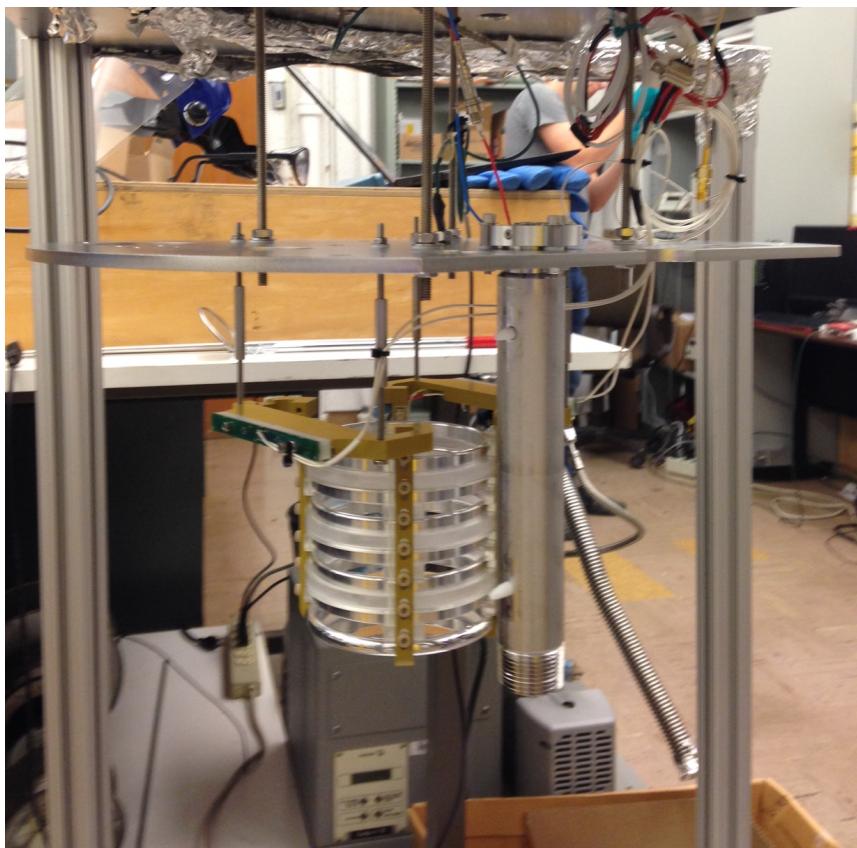




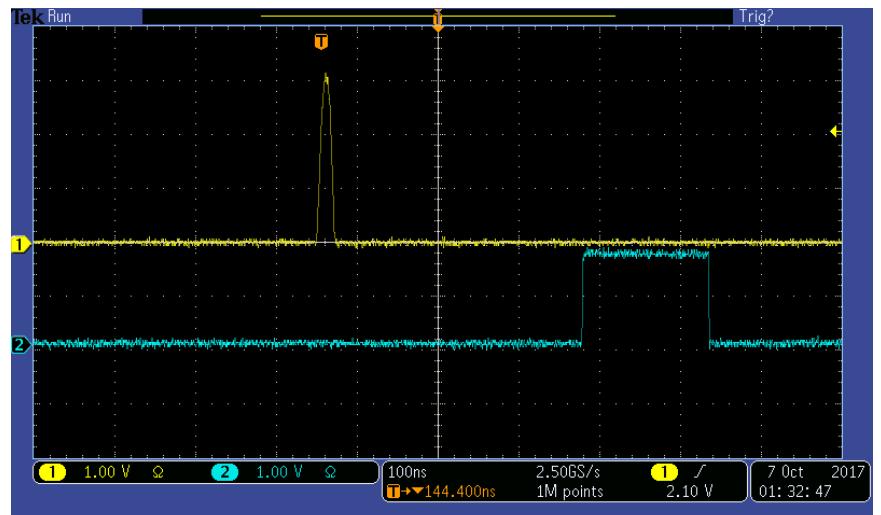
# Preparation for TPC Testing

## Initial test preparations using LUX/LZ high-purity LAr system:

- Single-pass LAr purification and cryostat
- Tested cool-down process, SiPM operation, LAr level monitoring
- Determined appropriate SiPM bias in LAr (-49 V)
- Refining system to reduce susceptibility to noise from lab environment.



UV LED pulse (yellow), SiPM coincidence trigger (blue)



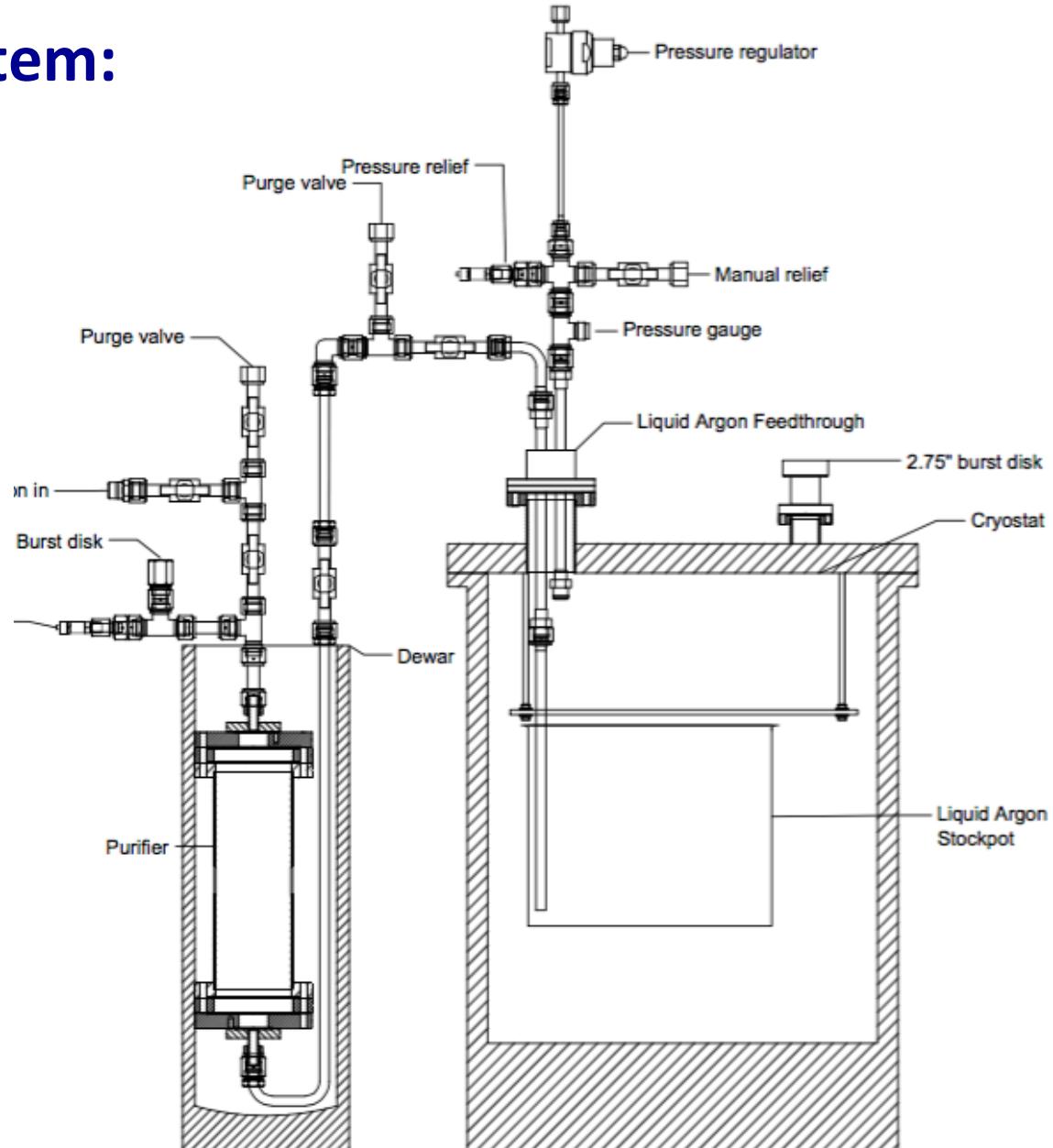
# Dedicated Testing System

## Preparing High-purity LAr system:

- Dedicated for LArPix TPC testing
- Modeled on LUX/LZ system
- LAr volume: up to ~120 liters

## Schedule:

- Design completed Summer 2017
- Final major component arrived last week (cryostat lid)
- Assembly and commissioning: Oct-Nov. 2017
- Target: ready for TPC testing in late November.





# Future Testing

**Next Steps, assuming initial tests of LArPix v1 go well:**

## 1) Fully-tiled LArPix sensor

- Produce fully-tiled (4 x 8) LArPix sensor board
- Test one copy in Small Pixel Demonstrator at LBNL
- Test one copy in Full-sized Pixel Demonstrator at Bern

## 2) LArIAT

- Layout and produce large sensor board (50cm x 50cm?, 40cm x 90cm?)
- Install in LArIAT TPC
- Characterize performance with well-known particle beam.

## 3) ArgonCube 2x2

- Design, produce sensor plane for ArgonCube 2x2 module



# Summary

## LAr-TPC Near Detector Module:

Hindered by signal pile-up from LBNF beam intensity.

ArgonCUBE prototype: demonstrated feasibility of 2D charge readout

Large-scale deployment requires low-power readout electronics

## LArPix v1 IC:

Dedicated IC for low-power 2D charge readout.

Chip production complete. Testing effort is now ramping up.

Aim to characterize noise & power performance soon.

## Working closely with Univ. of Bern / ArgonCUBE.

→ Glad to work with any others interested in 2D readout.