Development of a large pixel chip demonstrator in RD53 for ATLAS and CMS pixel upgrades

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2017 Topical Workshop on Electronics for Particle Physics – Sept. 11-14, Santa Cruz, CA

- Introduction
- Radiation qualification
- The RD53A demonstrator
  - Floorplan and design flow
  - Power
  - Analog front-ends
  - Digital matrix
  - Digital chip bottom
  - Analog chip bottom
  - RD53A verification
- Conclusion

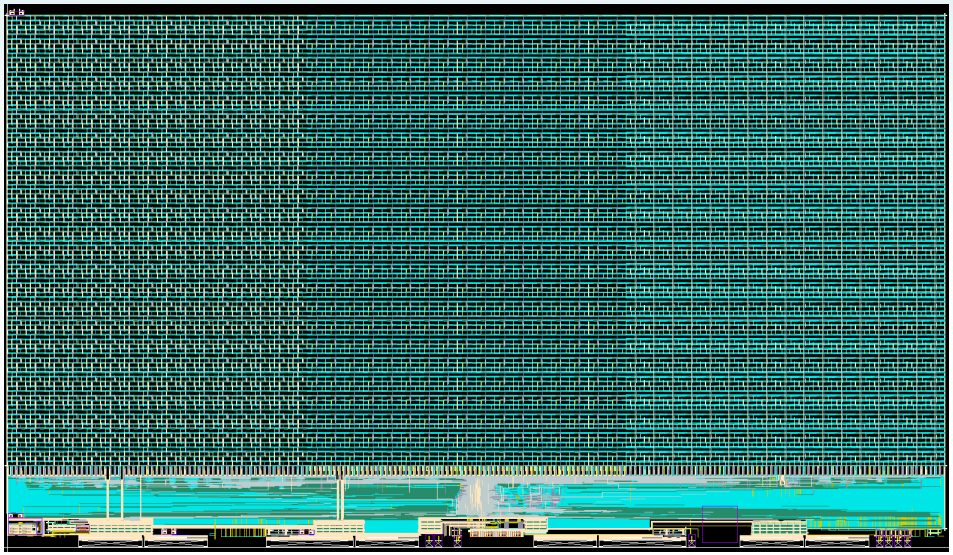
Next generation of silicon pixel detectors for phase-2 upgrade of ATLAS and CMS experiments at HL-LHC (~2024-26) sets unprecedented design requirements

- High granularity → small pixels (50x50 μm^2 / 25x100 μm^2)
- Large chips (~2x2 cm^2, ~10^9 transistors)
- High occupancy (pileup ~200) → 3 GHz/cm^2 hit rate
- Radiation tolerance for innermost layers: 2x10^{16} n_{eq}/cm^2, 1 Grad TID

RD53 Collaboration*: focused R&D developing pixel chips for ATLAS/CMS upgrades (baseline technology: 65 nm)*

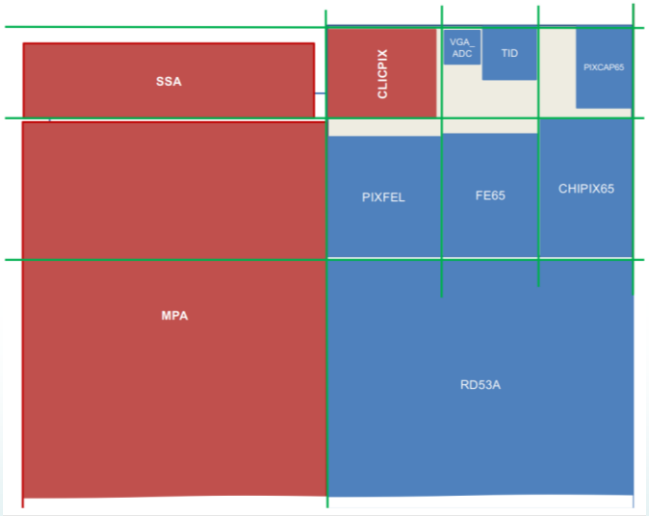
- Extensive radiation testing to determine how best to obtain sufficient radiation hardness
- Tools and methodology to efficiently design large complex mixed signal chips
  - dedicated simulation and verification framework
- Developed and tested many test structures, building blocks and small pixel arrays
  - shared rad-hard IP library (*analog front-ends, calibration circuit, bandgap, DAC, ADC, PLL, serializer, cable driver, serial I/O, serial power regulator, on-chip monitoring*)
  - radiation test structures (*transistor arrays, analog circuits, digital libraries*)
  - two small scale (64x64) prototypes: ***FE65-P2*** (*see presentation by Timon Heim*), ***CHIPIX65*** (*see presentation by Luca Pacher*)
- Design and characterization of full scale demonstrator pixel chip: **RD53A**

- RD53A is intended to demonstrate in large format IC the suitability of the chosen 65nm CMOS technology for HL-LHC upgrades of ATLAS and CMS
  - radiation tolerance
  - stable low threshold operation
  - high hit and trigger rate capabilities



- RD53A size: 20 x 11.8 mm^2
  - → 400 columns x 192 rows, 50 x 50 μm^2 pixels

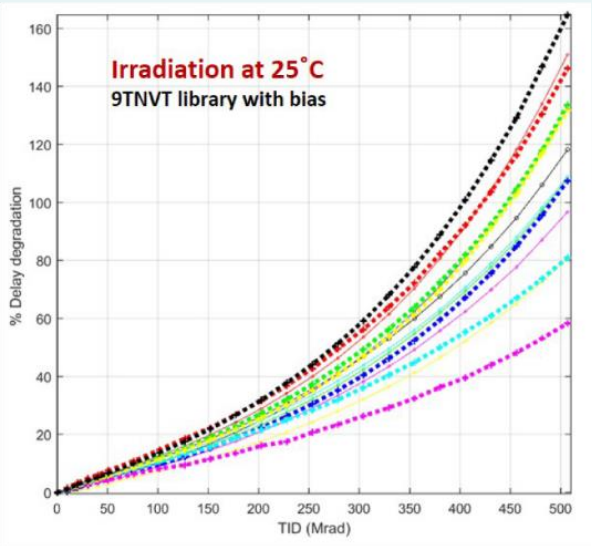
- RD53A is not intended to be a final production chip for use by the experiments
  - contains design variations for testing purposes
  - wafer scale production will enable prototyping of bump bonding assembly with realistic sensors in new technology
    - → performance measurement
  - forms the basis for production designs of ATLAS and CMS: architecture designed to be easily scalable to a full scale chip

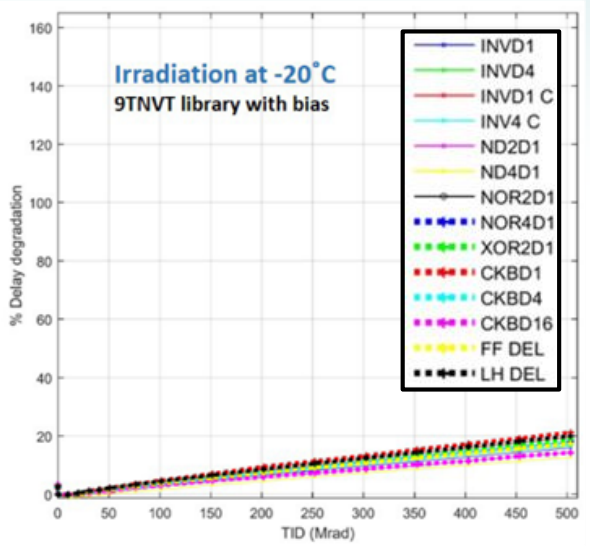


- Submitted: end of August 2017 (shared engineering run with CMS MPA/SSA chips for cost sharing)

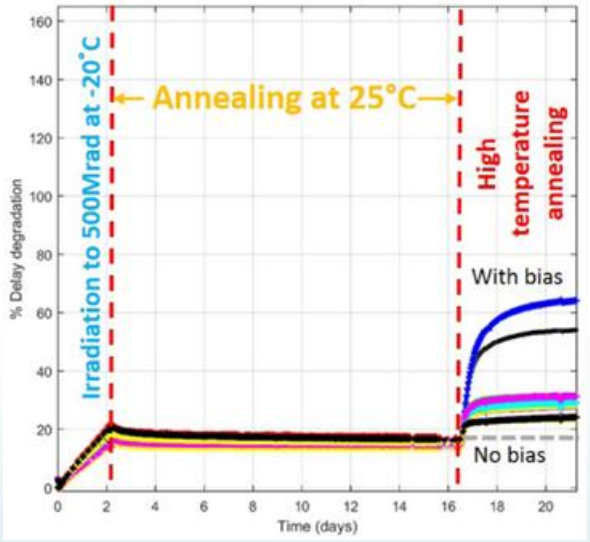
- Extensive irradiation campaign in past 3 years
  - transistor arrays
  - analog circuits
  - digital test chip

- Significant radiation damage above 100 Mrad
  - analog: transconductance, V_{th} shift
  - digital: speed degradation

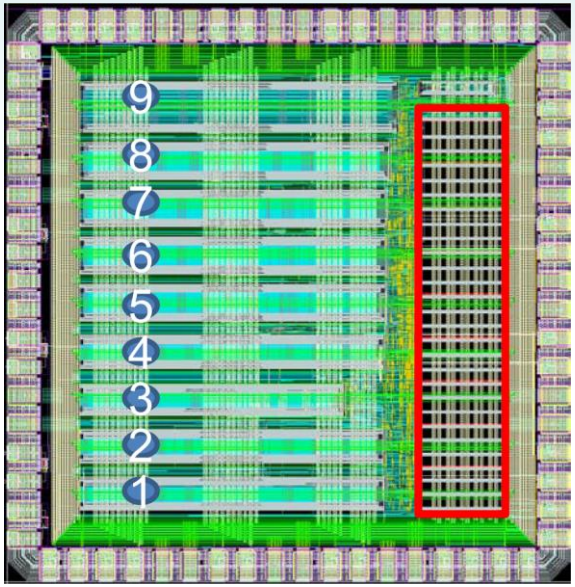


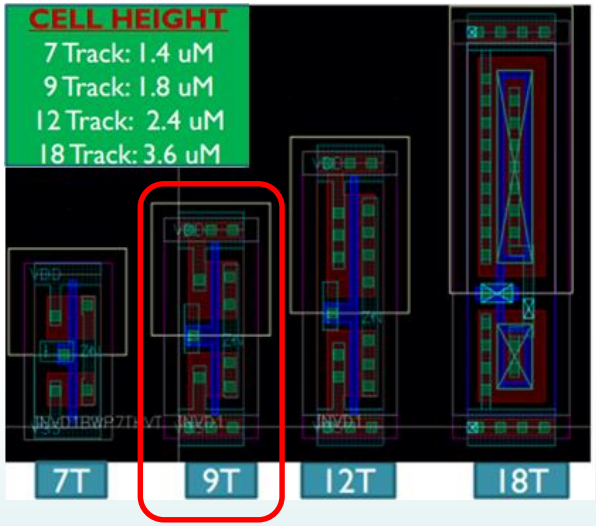


- Short and narrow channel effects (*RISCE*, *RINCE*)
  - strongly depend on temperature during irradiation and bias conditions of devices
  - less damage when irradiating at low temperature (-20 °C)
  - worst case bias : $V_{GS} = V_{DS} = 1.2$ V (diode connected)
  - some recovery observed at low and room temperature annealing but high temperature annealing with bias introduces high V_{th} shift



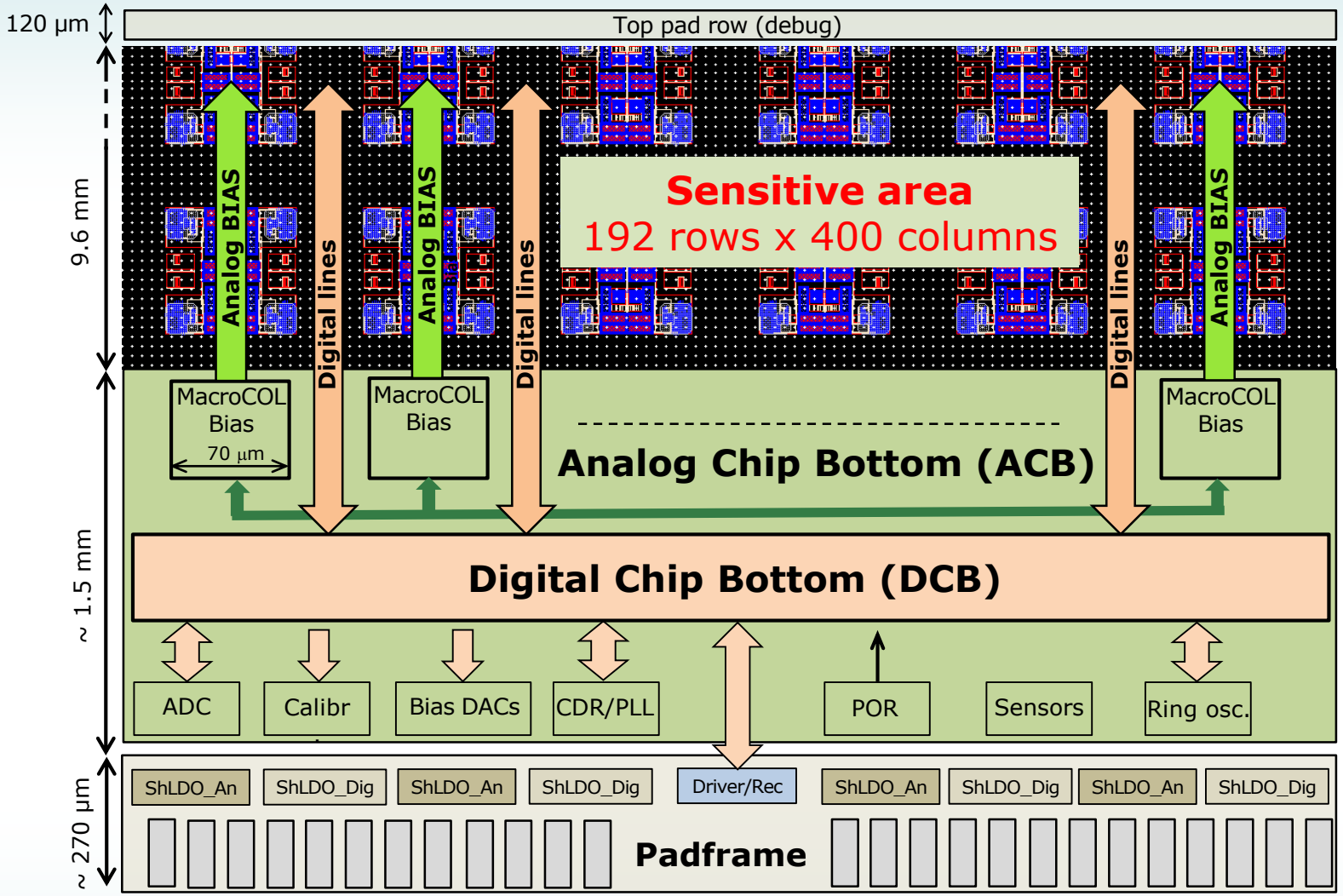
- Realistic to stand 500 Mrad with conservative design approach (inner barrel layer can be replaced after 5 yrs)
- Conservative transistor **simulation models** for behavior after 200 and 500 Mrad dose (worst case bias, irradiation at room temperature) for circuit simulations and optimizations
- Analog circuits appropriately designed (large transistors) and then simulated with 500 Mrad corner model
- Digital libraries: **DRAD chip** [*Jara Casas et al., JINST, 2017*]
  - study effect of radiation on digital standard cells in 65nm
  - test efficiency and validity of digital simulations with irradiation corner model
- Simulation results agree with irradiation tests but the model overestimates TID damage level
  - NOR gates should be avoided due to strong degradation
  - Large devices → better time margins
- Test results used to decide which timing corner to use for RD53A design





substrate contacts

RD53A specifications [CERN-RD53-PUB-15-001]	
Technology	65 nm CMOS
Pixel size	50 x 50 um^2
Pixels	192 x 400 = 76800 (50% of production chip)
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	< $600e^-$
In-time threshold	< $1200e^-$
Noise hits	< 10^{-6}
Hit rate	< 3 GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	Max 1 MHz
Trigger latency	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤ 1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	500Mrad, 1 x 10^{16} 1Mev eq. n/cm^2 at -15 ^oC
SEU affecting whole chip	< 0.05/hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1W/cm^2 including SLDO losses
Pixel analog/digital current	4 uA / 4 uA
Temperature range	-40^{o}C ÷ 40^{o}C



– RD53A metal stack: 9 metal layers + 28K AP layer

– RD53A uses standard V_t 9-track library (tcbn65lp)

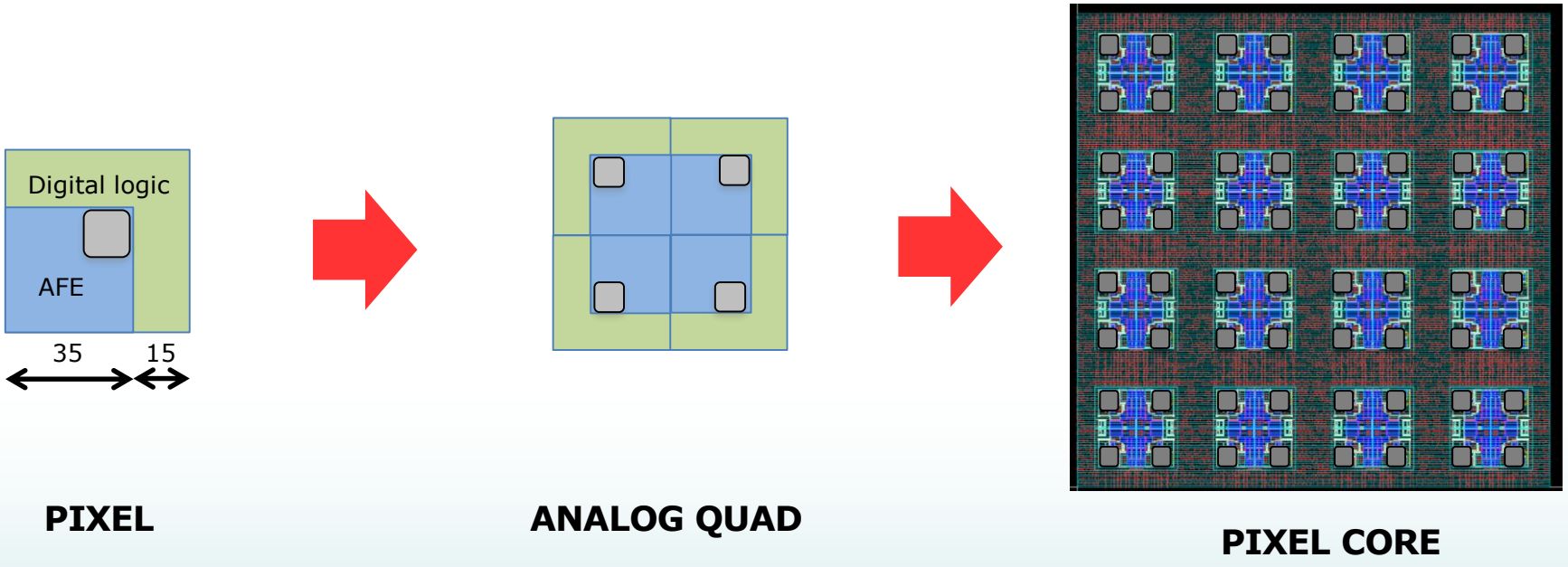
50x50 µm² pixel floorplan

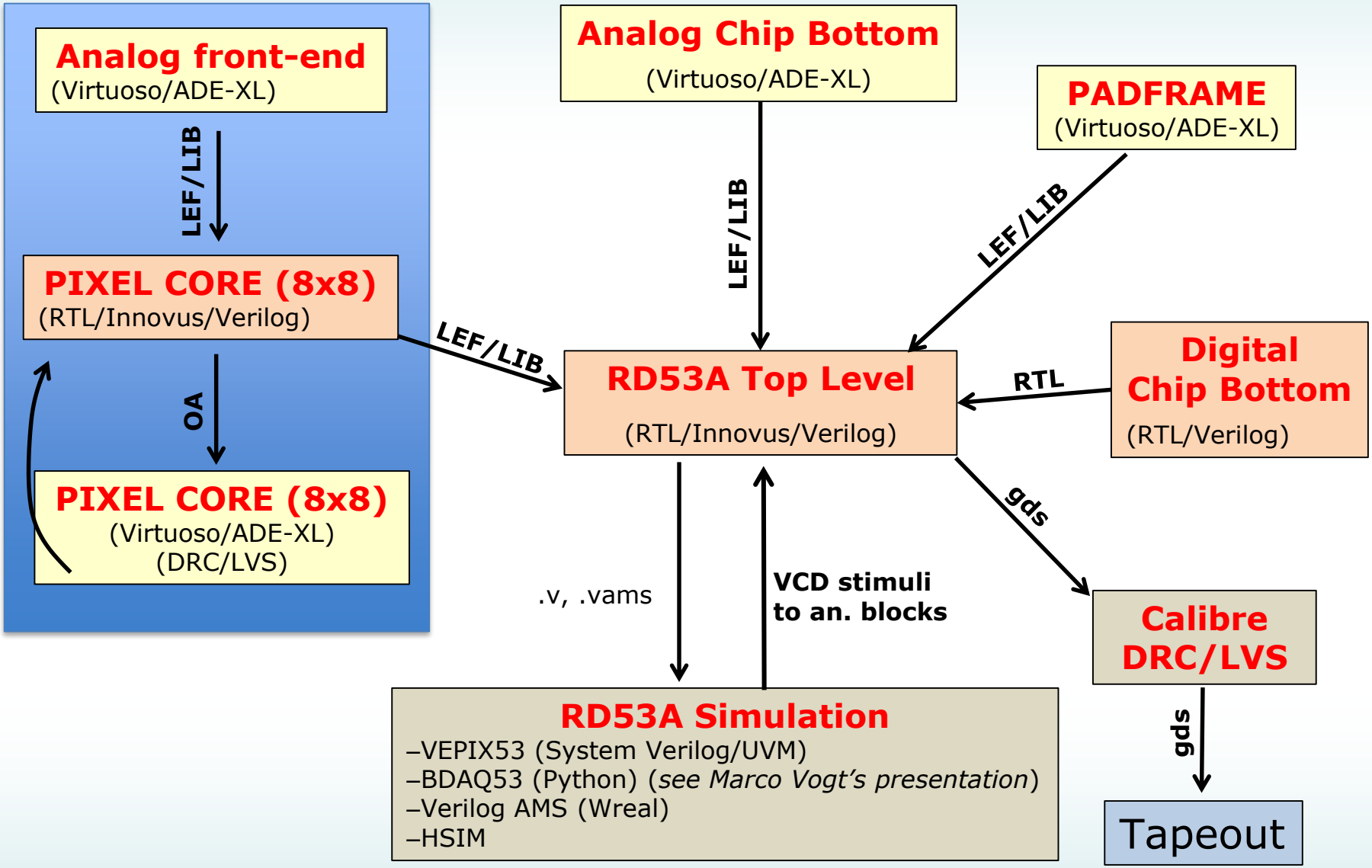
– 50% Analog Front End (AFE), 50% digital cells

– Pixel array built up of 8x8 pixel cores
→ 16 analog "islands" (quads) embedded in a flat digital synthesized "sea"

– A pixel core can be simulated at transistor level with analog simulator

– All cores (for each FE flavour) are identical
→ hierarchical verifications



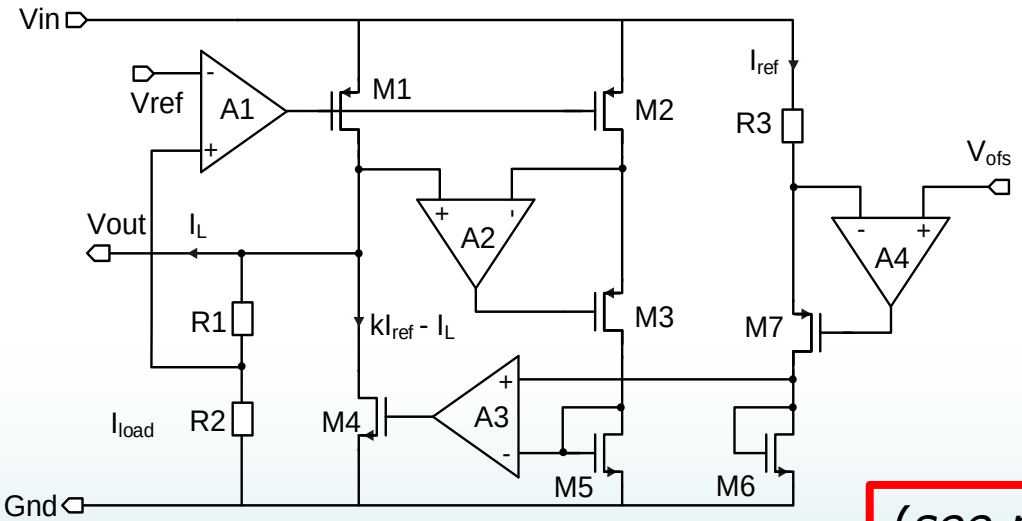

Analog front-end
(Virtuoso/ADE-XL)
LEF/LIB
PIXEL CORE (8x8)
(RTL/Innovus/Verilog)
OA
PIXEL CORE (8x8)
(Virtuoso/ADE-XL)
(DRC/LVS)
Analog Chip Bottom
(Virtuoso/ADE-XL)
PADFRAME
(Virtuoso/ADE-XL)
LEF/LIB
LEF/LIB
LEF/LIB
RD53A Top Level
(RTL/Innovus/Verilog)
RTL
Digital
Chip Bottom
(RTL/Verilog)
gds
.v, .vams
VCD stimuli
to an. blocks
Calibre
DRC/LVS
gds
Tapeout
RD53A Simulation
–VEPIX53 (System Verilog/UVM)
–BDAQ53 (Python) (see Marco Vogt's presentation)
–Verilog AMS (Wreal)
–HSIM

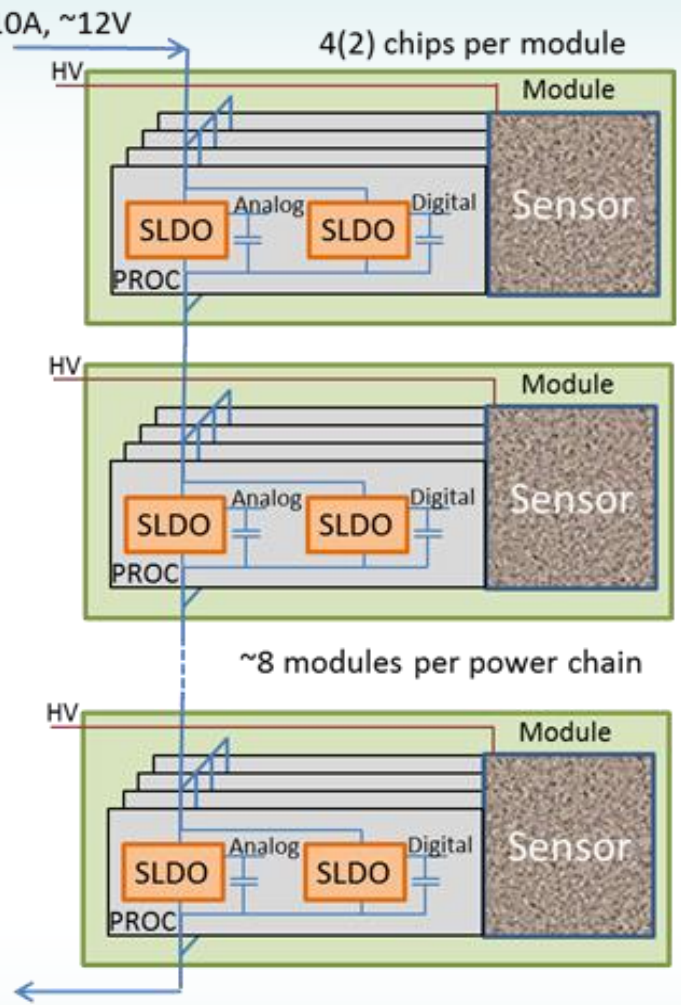
– RD53A designed to operate with **serial powering**
  → constant current to power chips/modules in series

– 2 internal voltage rails: analog (V_{DDA}) and digital (V_{DDD})

– Based on **ShuntLDO** regulator: Low Drop-Out linear voltage regulator + shunt regulator

– 2 ShuntLDOs (analog, digital internal rails) and 4 active pads associated with each

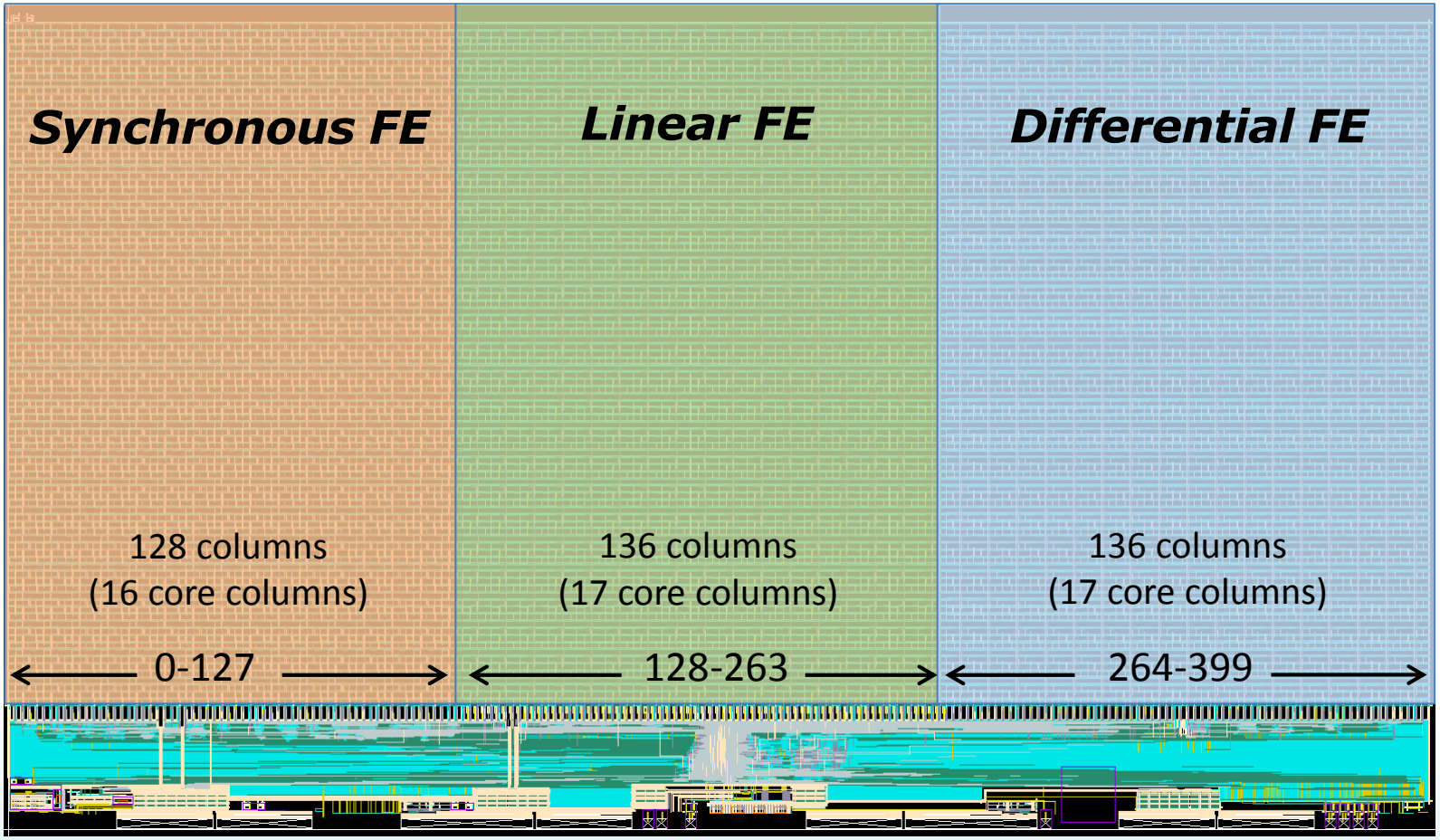




(*see presentation by Stella Orfanelli*)

3 different analog front-end designs for performance comparisons with same layout area

- Easily interchangeable on the pixel array
- Common calibration injection circuit for direct performance comparison



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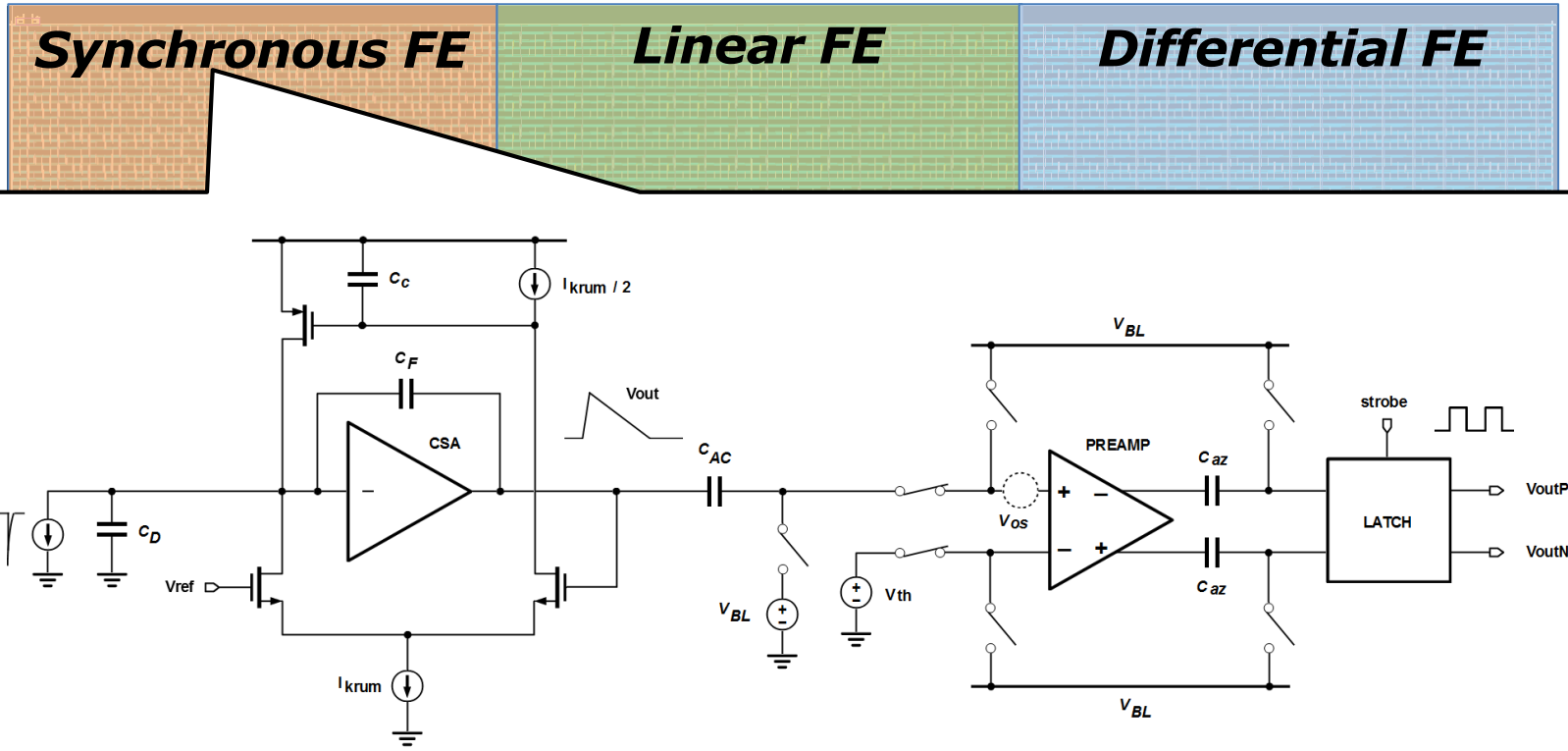
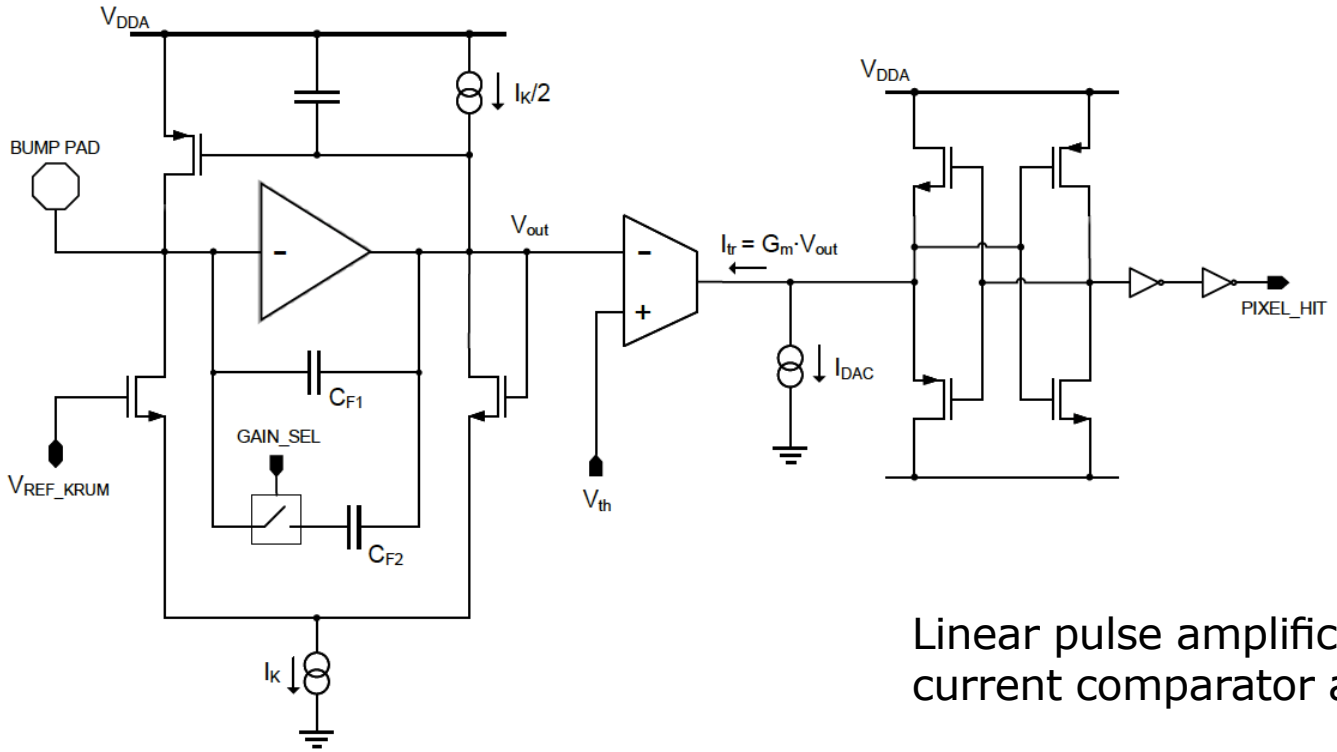


- Single stage Charge Sensitive Amplifier AC coupled to synchronous comparator
- Baseline "auto-zeroing" scheme → no threshold trimming needed
- Latch can be turned into local oscillator up to 800 MHz for fast ToT counting

3 different analog front-end designs for performance comparisons with same layout area

- Easily interchangeable on the pixel array
- Common calibration injection circuit for direct performance comparison

Synchronous FE | **Linear FE** | **Differential FE**

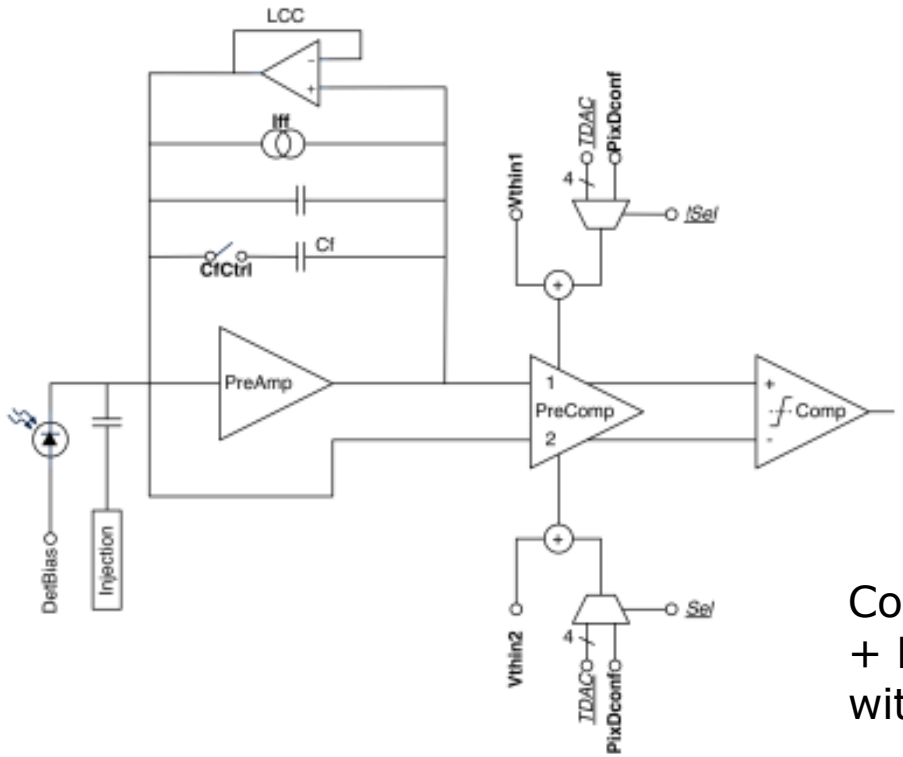


Linear pulse amplification stage with current comparator and ToT counter

3 different analog front-end designs for performance comparisons with same layout area

- Easily interchangeable on the pixel array
- Common calibration injection circuit for direct performance comparison

Synchronous FE | **Linear FE** | **Differential FE**

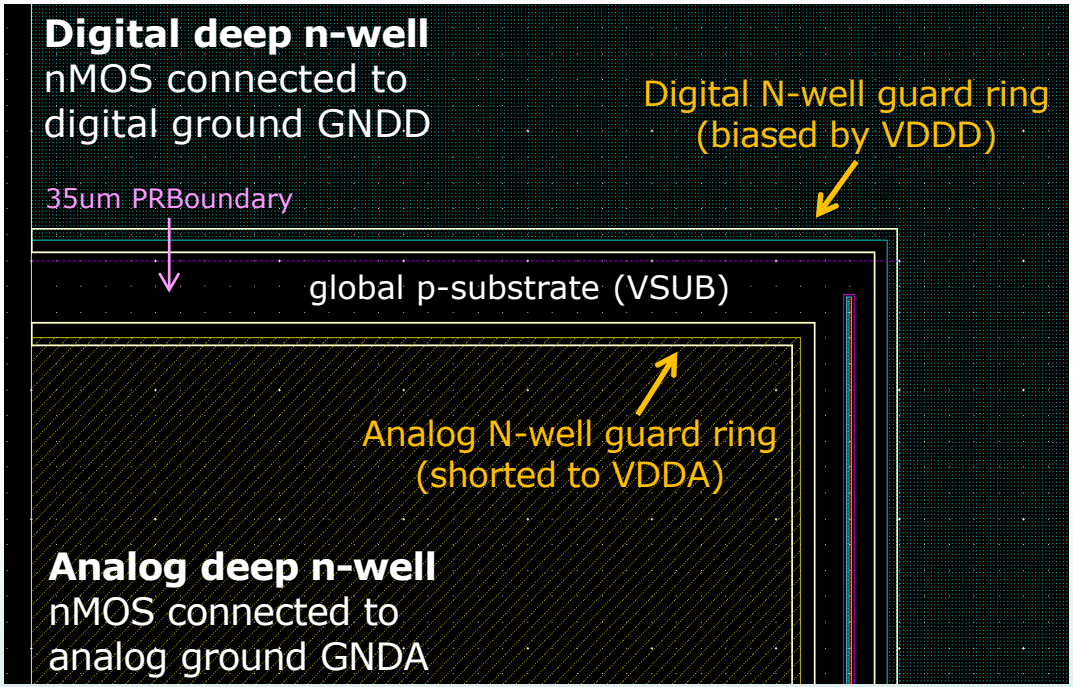


Continuous reset integrator first stage
+ DC-coupled pre-comparator stage
with differential threshold circuit

Analog front-ends main features	**Sync.**	**Lin.**	**Diff.***	**spec**
Charge sensitivity [mV/ke$^-$]	43	25	103	-
ENC rms [e$^-$]	67	83	53	<<126
Threshold dispersion $\sigma(Q_{th})$ rms [e$^-$]	93	32	20	<<126
$\sqrt{(ENC^2 + \sigma(Q_{th})^2)}$ [e$^-$]	115	89	54	≤126
In-time overdrive [e$^-$]	≤50	≤100	0	≤ 600
Current consumption [μA/pixel]	3.3[1]	4.3	3.5	≤ 4
Time over threshold [ns]	121	99	118	< 133

Post-layout simulations (*except Diff.: schematic level sim): C_D=50 fF, T=27 °C, Q_{th}=600 e$^-$

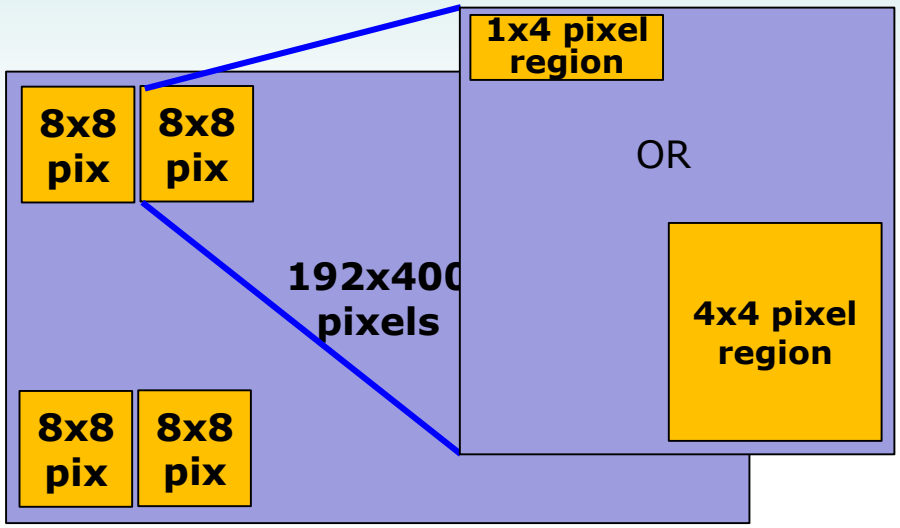
- In-time overdrive relative to Q_{in}=30 ke$^-$
- Time walk → Q_{in}=1200 e$^-$ (relative to a Q_{in}=30 ke$^-$)
- ToT → Q_{in} = 6 ke$^-$
- [1] 5.1 uA including latch

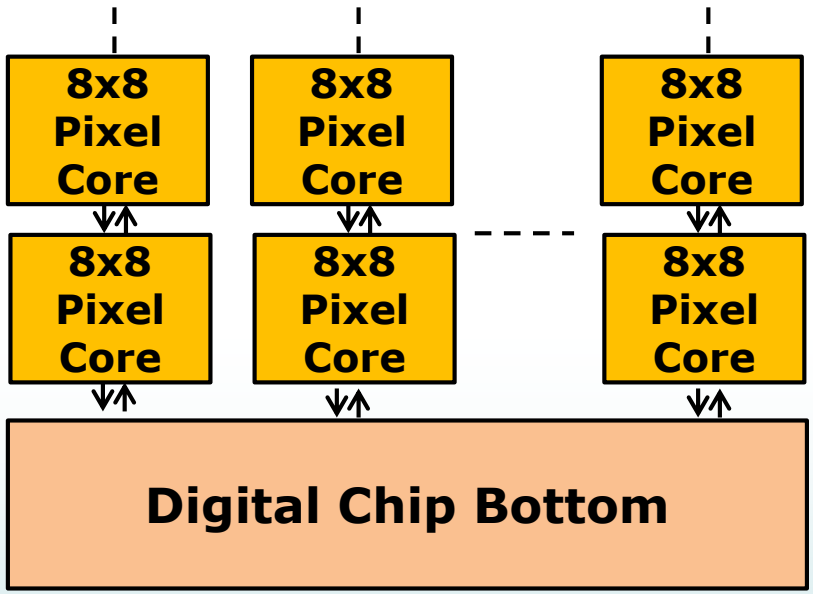


Digital n-well guard ring closed: analog quad isolated from "outside"

Pixel array logic organization

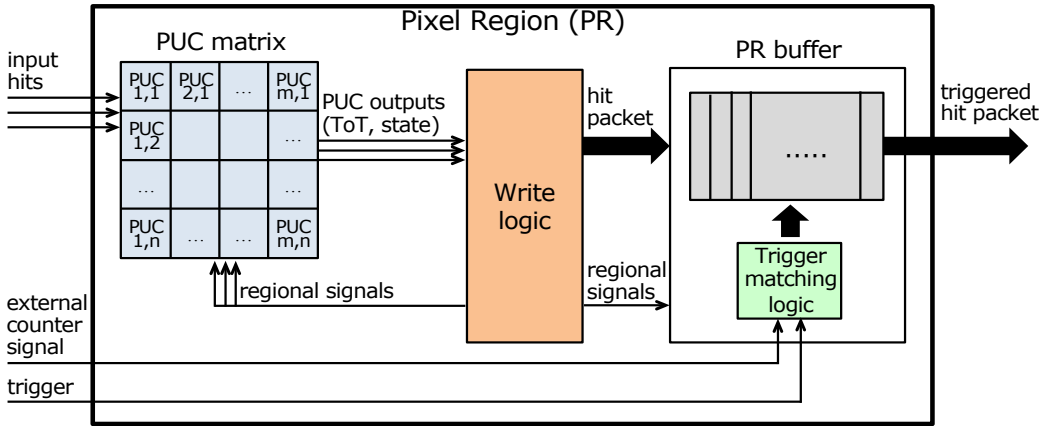
- Basic layout unit: 8x8 digital **Pixel Core**
  → synthesized as one digital circuit
- Pixel Core contains multiple **Pixel Regions** (PR) and some additional arbitration and clock logic
- Each Pixel Core receives all input signal from the previous core (closer to Digital Chip Bottom) and regenerates the signals for next core
- Timing critical clock and calibration injection signals are internally delayed within the core relative to the regenerated ones to have a uniform timing (within 1-2 ns)





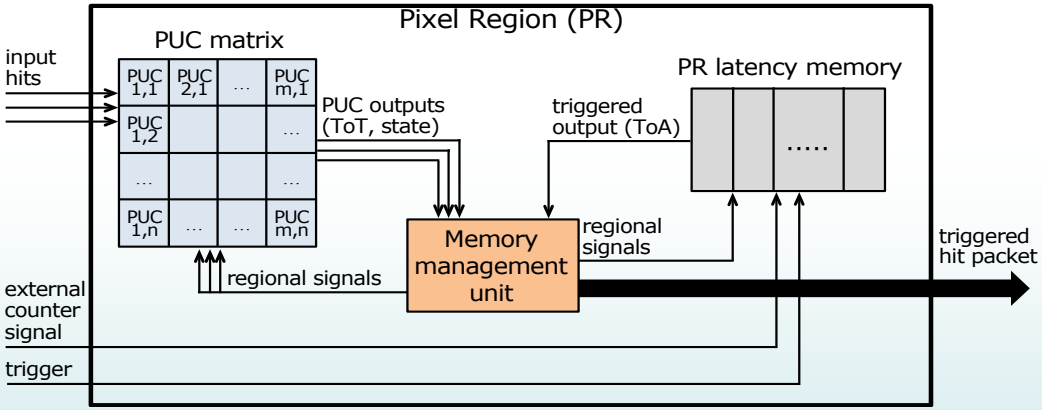
– Pixel Regions contain trigger latency buffering (most efficient architectural solution in order to handle very high hit rate)

– Architecture exploration from initial statistical study (2013) to *behavioral* parameterized pixel array model: two different buffering architectures (2014-2015), eventually implemented into small scale prototypes



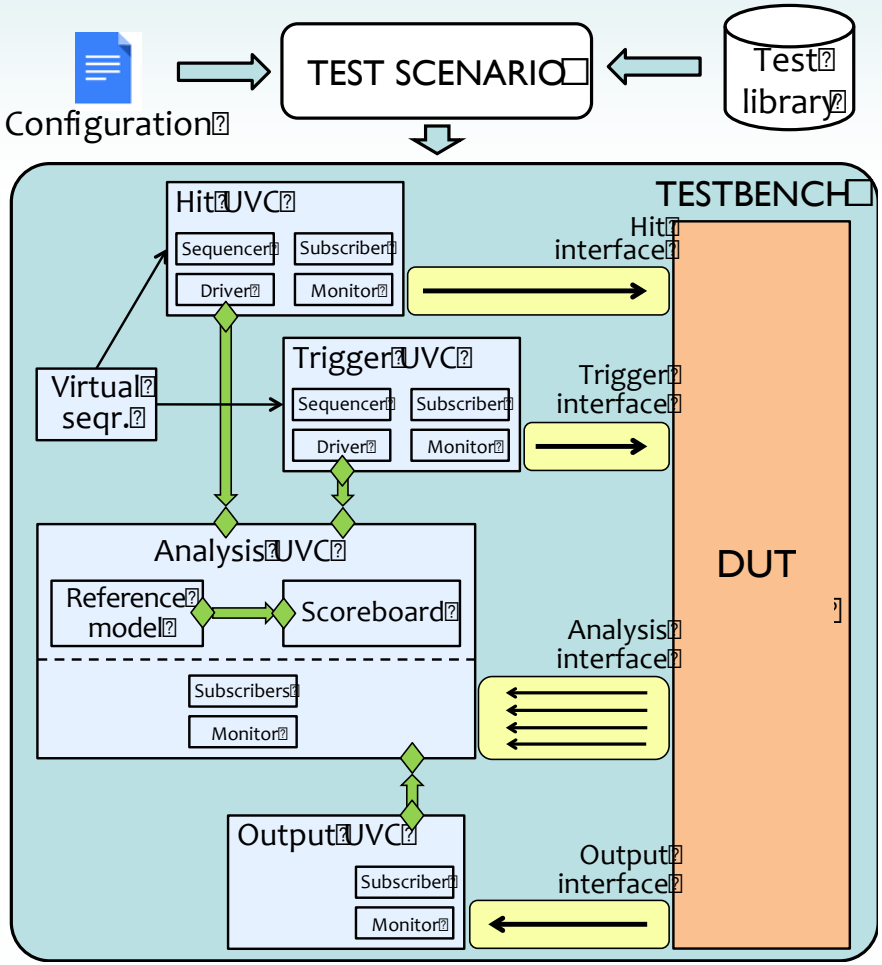
Centralized Buffering Architecture (CBA)

– 4x4 pixel region
– implemented into *CHIPIX65*



Distributed Buffering Architecture (DBA)

– 2x2 → 1x4 pixel region
– based on ATLAS FE-I4
– implemented into *FE65_P2*



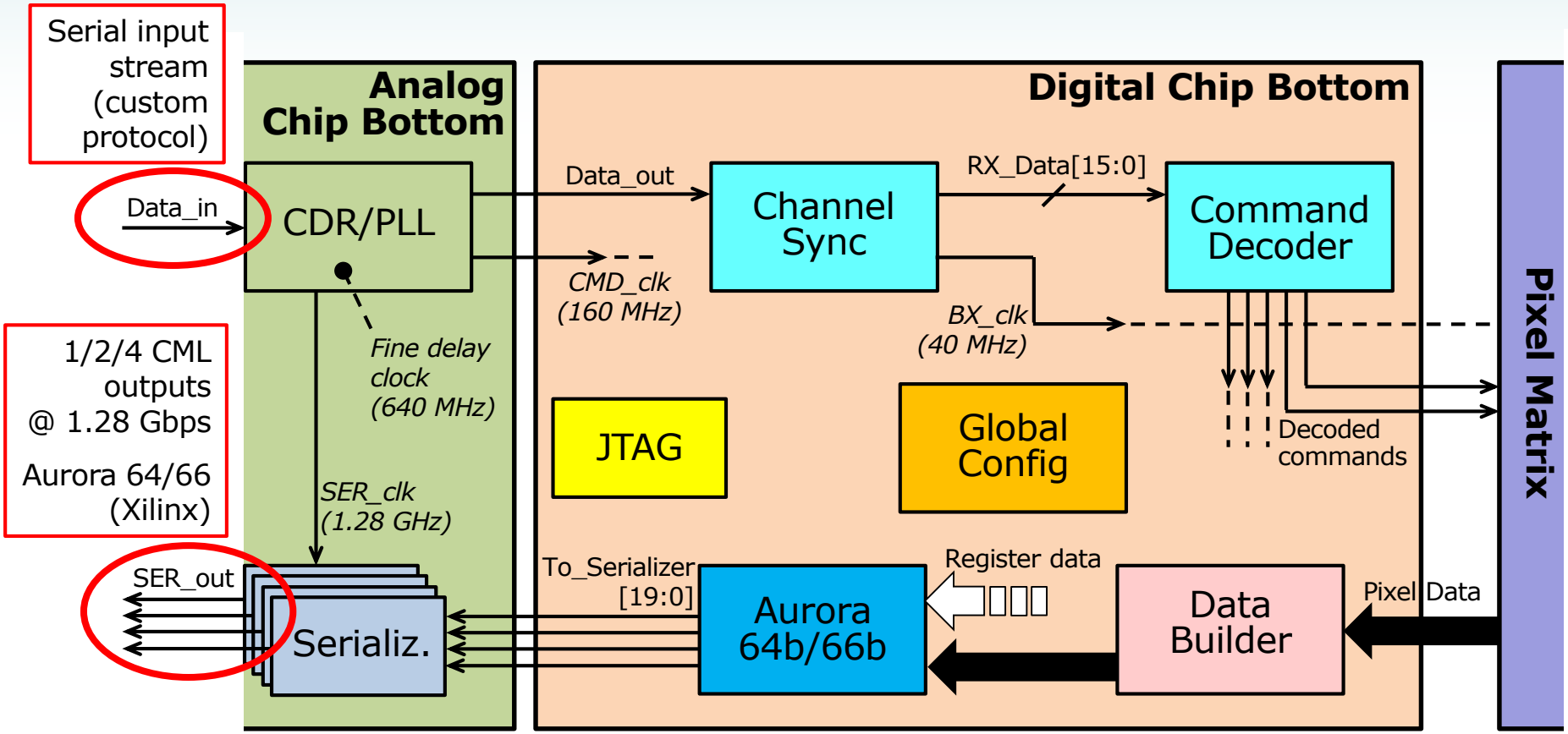
– ***VEPIX53***: simulation and verification environment (UVM) supporting design from initial architectural modeling to final verification
  – generation of different kinds of input stimuli (internally generated or from Monte Carlo)
  – automated verification features

– Pixel array architecture performance metrics: *hit loss* and *latency buffer occupancy*

– Comparative study DBA-CBA:
  – at behavioral level
  – at RTL from small scale prototypes

– *Comparable performance* found between CBA and DBA architectures in terms of buffer overflow hit loss

Result of the study motivated further optimizations implemented into RD53A addressing design limitations → all differences solved



Readout proceeds with column-parallel token chain one trigger at a time

Configuration: 9-bit address, 16-bit data

– *Global configuration*: 9-bit address, 16-bit data

– *Pixel configuration*: up to 8-bit data per pixel, R/W done on pixel pairs

SEU tolerance strategy

– SEU tolerant dual interlocked (DICE) latches with interleaved layout designed and irradiated: 9x more tolerant than single latch → not sufficient

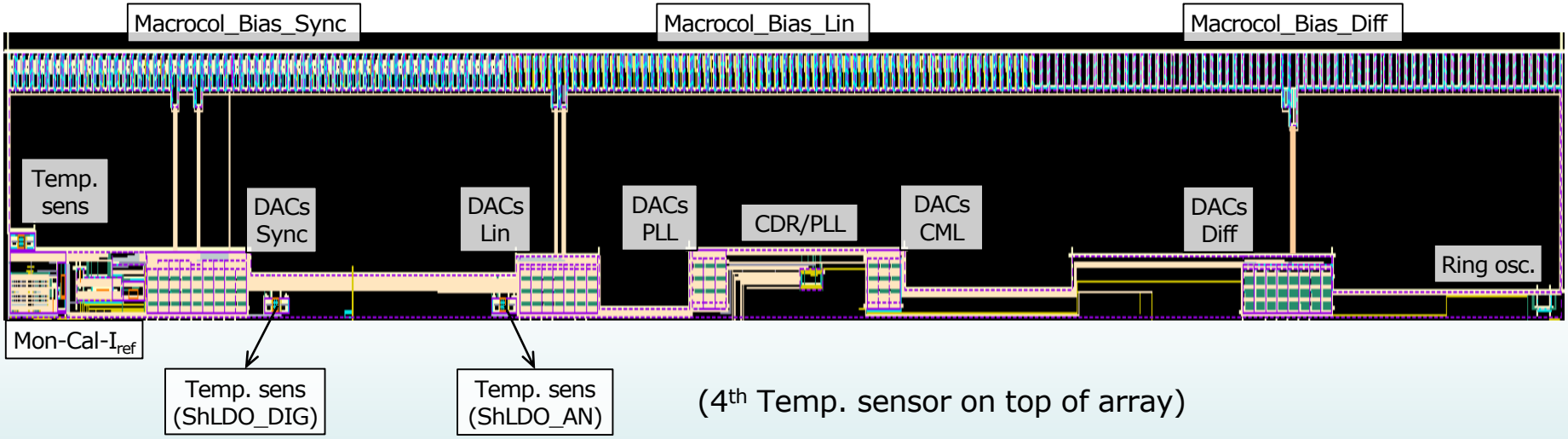
	Mean time between errors		**Area/bit** (without ctrl logic)
	Pixel config (1.28 Mbit/chip)	Global config (1 kbit/chip)	
Single latch	55 ms	71 s	5 um^2
DICE	0.5 s	639 s	11.6 um^2
TMR	209 s	74 h	700 um^2

– *Triple Modular Redundancy* (TMR) consumes area and not compatible for pixel configuration
→ used for global configuration

– Solution for pixel configuration: simple DFF with *trickle configuration* (frequent data refresh cycles)

– To be refined, extended and have SEU simulations for final chips

- Multi-purpose macroblock containing all analog IPs, assembled in analog environment (Virtuoso) and simulated with analog and mixed-signal simulator
  - Provides 4 µA current reference to current DACs, regulated in order to compensate for process variations
  - Monitors different quantities (temperature, total dose, currents/voltages) in different parts of the chip, digitized by 12-bit ADC
  - Provides global analog front-end bias and calibration circuit voltage levels
- All IPs previously thoroughly tested, also from the standpoint of radiation tolerance before integration in RD53A chip



(4th Temp. sensor on top of array)

VEPIX53 UVM verification components (UVC) allowing for reusability and automated verification functions

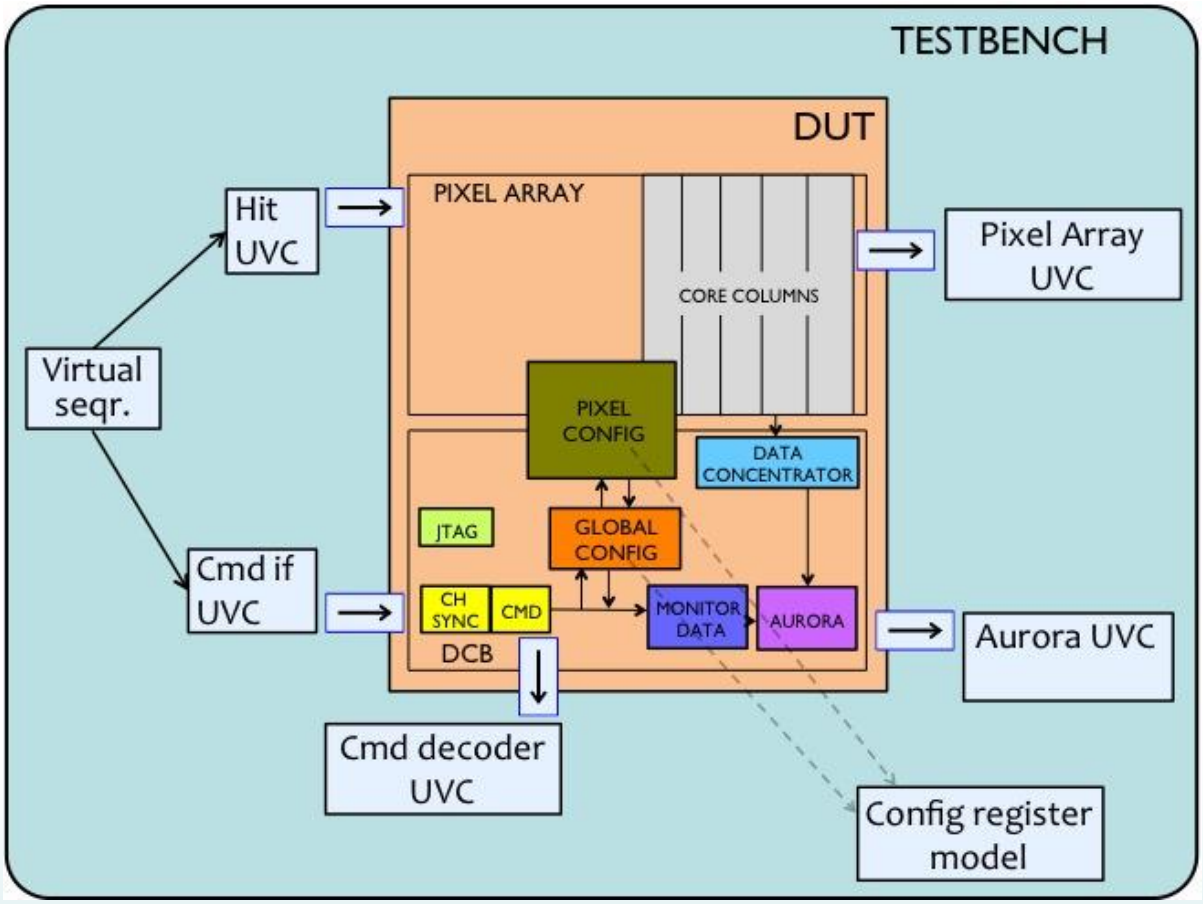
Also support directed test pattern generation

Interface verification components (UVCs):

- Hit (sensor pixel hit data)
- Command (custom input protocol for control and trigger)
- Aurora, HitOr (monitor pixel chip output)

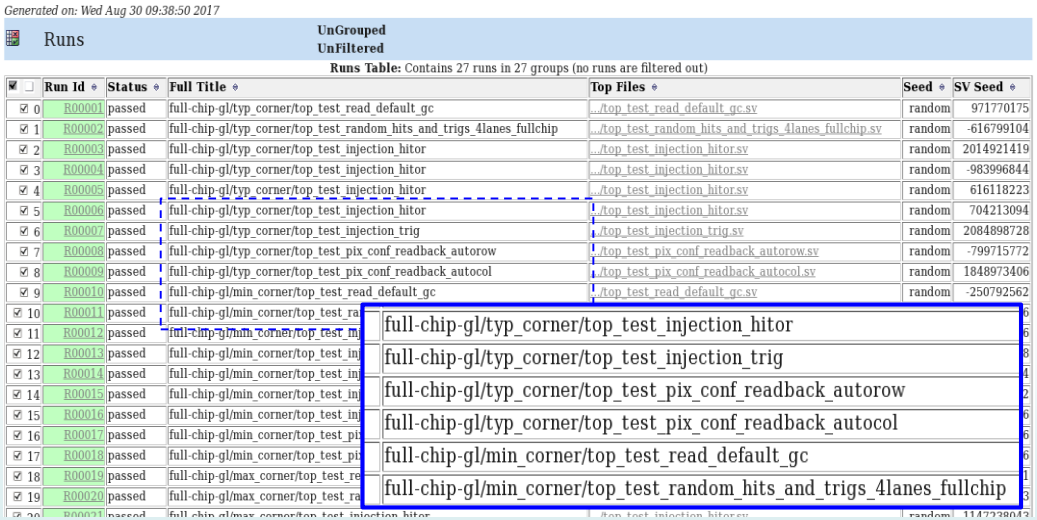
Module UVCs:

- Pixel array UVC (reference models, scoreboard, lost hits classifier)
- Channel Sync and Command Decoder UVC (monitor, checker)
- *Planned*: configuration register model (automatic configuration register verification), SEU injection



Verification approach:

1. *Constrained-random tests* → functional coverage collection
   - Based on generation of constrained-random inputs
   - Automated pixel array verification
2. *Directed tests* → specific test cases aimed to verify single functions and unlikely perturbations
   - Custom command sequences
   - Extreme hits/triggers
   - No extensive tests
   - So far tests checked manually (eManager logs and Simvision waveforms for debug)
3. *Generation of stimuli for analog simulations*



Example of test regression run at each design iteration (RTL and gate-level, 3 timing corners)

Block / Function	*Test type*
Global configuration readback	Directed
Hit or data path	Constrained-random
Triggered data path	Constrained-random
Calibration injection hits	Directed
Pixel configuration readback	Directed

The goal of the RD53A chip is to demonstrate feasibility of 65 nm technology with respect to the challenging requirements set by the future experiment upgrades at the HL_LHC

RD53A puts into practice guidelines elaborated by RD53 over the years (radiation tolerance, architecture exploration, floorplan, design flow, serial powering, verification) and used IP library developed, prototyped and tested

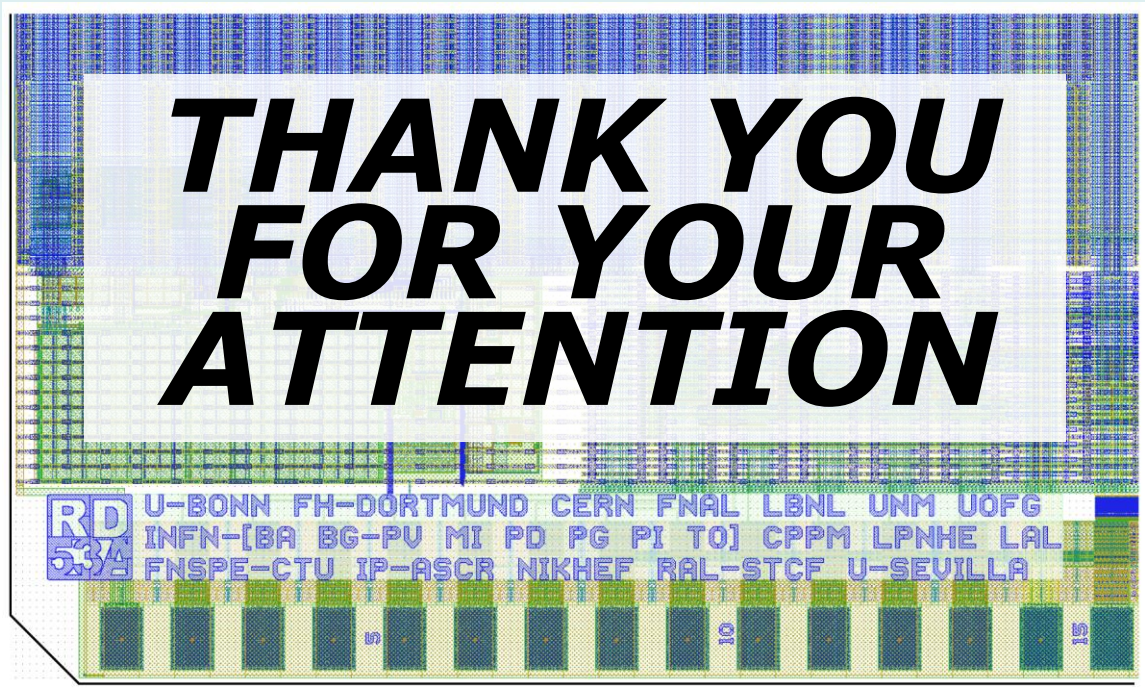
→ different analog front-end flavors and digital pixel array architectures coexisting on the same chip

RD53A submitted at end of August on shared engineering run, expecting delivery ~November

Preparation for chip testing already ongoing

RD53 in agreement with upgrade management of experiments is formally proposing to make final chips for ATLAS and CMS

– select front end variant, increase pixel matrix size, additional functionality according to experiment specs
– further optimization (power, architecture, SEU immunity)



The RD53 Collaboration

- Bonn
- CERN
- Marseille CPPM
- FNAL
- LBNL
- Paris LPNHE
- New Mexico
- INFN (Bari, Milano, Padova, Bergamo-Pavia, Pisa, Perugia, Torino)
- NIKHEF
- Prague IP-FNSPE-CTU
- RAL-STCF
- Seville

RD53A design team

- Flavio Loddo (Bari)
- Tomasz Hemperek (Bonn)
- Roberto Beccherle (INFN PI)
- Elia Conti (CERN)
- Francesco Crescioli (Paris)
- Francesco De Canio (INFN BG-PV)
- Leyre Flores (Glasgow)
- Luigi Gaioni (INFN BG-PV)
- Dario Gnani (LBNL)
- Hans Krueger (Bonn)
- Sara Marconi (CERN / INFN PG)
- Mohsine Menouni (CPPM)
- Sandeep Miryala (FNAL)
- Ennio Monteil (INFN TO)
- Luca Pacher (INFN TO)
- Andrea Paternò (INFN TO)

BACKUP

Corners for RD53A

	Typ Ro1	Typ Ro2	Typ Ro 3	Typ Op1	Typ Op2	Typ Op3	LV Op1	LVO p2	LV Ro1	LV Ro2	FF LT	FF HT	SS HT	SS LT	200 Mrad	500 Mrad
Model	TT	FS	SF	TT	FS	SF	FS	SF	FS	SF	FF	FF	SS	SS	200Mrad	500Mrad
VDD	1.2	1.2	1.2	1.2	1.2	1.2	1.08	1.08	1.08	1.08	1.32	1.32	1.08	0.9	1.2	1.2
T	27	27	27	-20	-20	-20	-20	-20	27	27	-40	40	80	-40	27	27

Only for digital

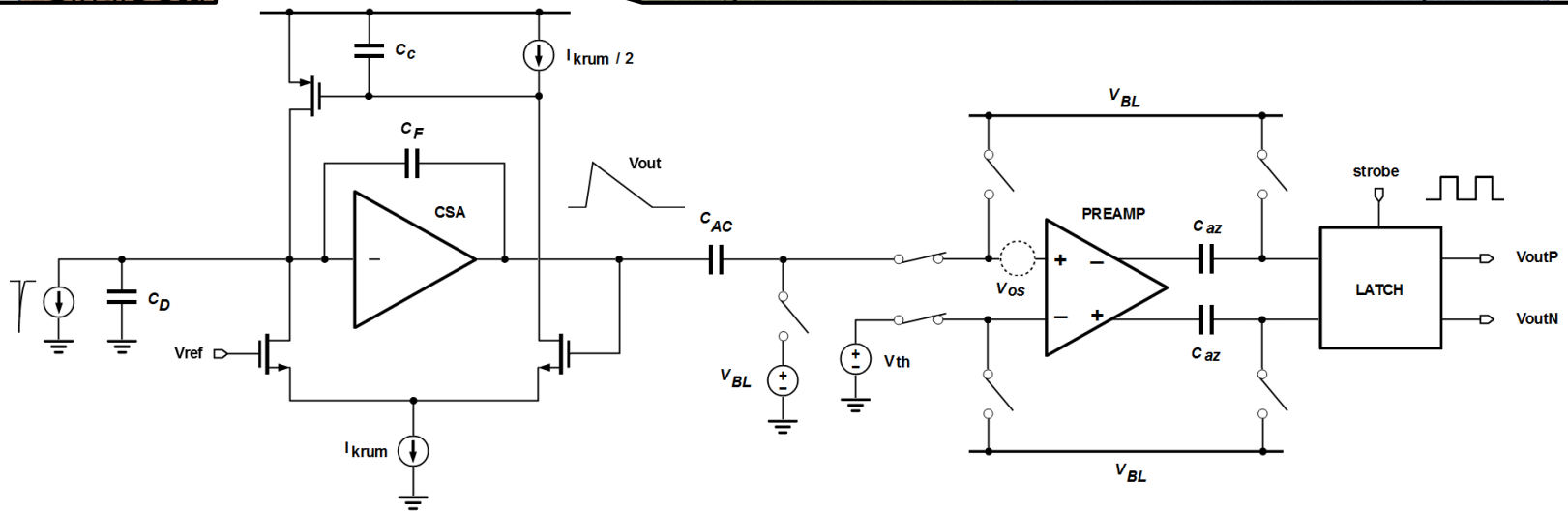
3 different analog front-end designs for performance comparisons with same layout area

– Easily interchangeable on the pixel array

– Common calibration injection circuit for direct performance comparison

Synchronous FE | **Linear FE** | **Differential FE**

Single stag | Single stage with current | Continuous reset integrator



– Single stage Charge Sensitive Amplifier with Krummenacher feedback AC coupled to synchronous discriminator (offset compensated Differential Amplifier (DA) + positive feedback latch)

– Baseline "auto-zeroing" scheme → no threshold trimming needed

– Latch can be turned into local oscillator up to 800 MHz using asynchronous logic feedback loop → Fast ToT counting

3 different analog front-end designs for performance comparisons with same layout area

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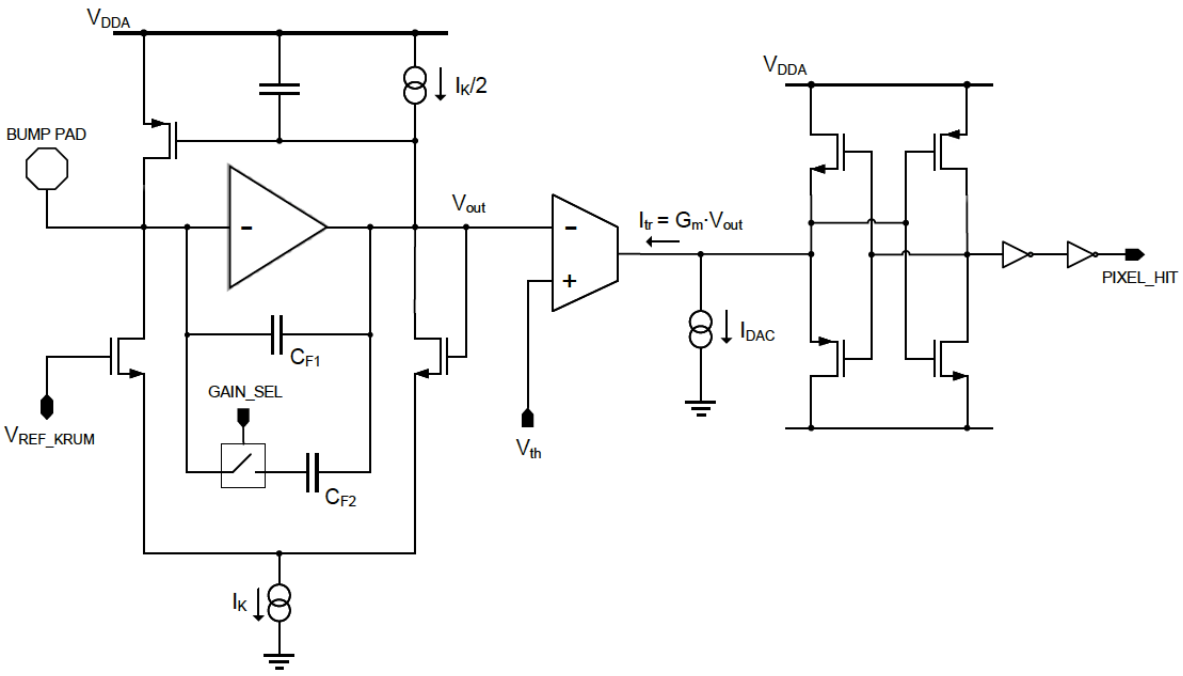
Synchronous FE | **Linear FE** | **Differential FE**

Single stage wit… | …stage with current | Continuous reset integrator



– Linear pulse amplification stage with current comparator and ToT counter

– Single amplification stage for minimum power dissipation

– Krummenacher feedback to comply with expected large increase in detector leakage current

– High speed, low power current comparator

– Selectable gain

– 30000 e^- maximum input charge, ~450 mV preamplifier output dynamic range

3 different analog front-end designs for performance comparisons with same layout area

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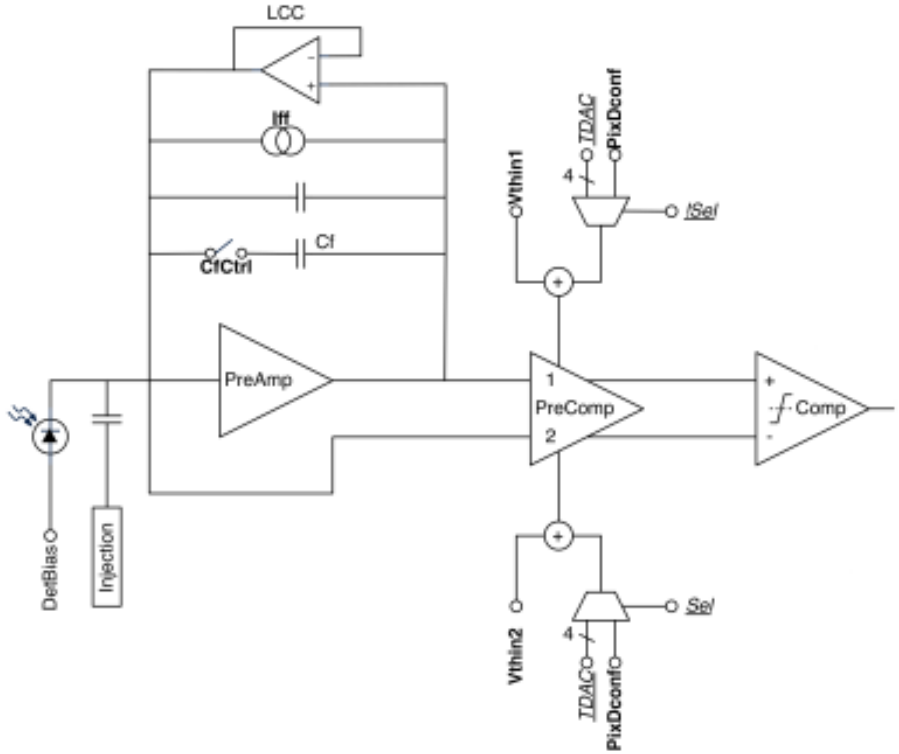
Synchronous FE | **Linear FE** | **Differential FE**

Single stage with SAR-like | Single stage with current | integrator



– Preamplifier: continuous reset and adjustable gain (two possible values of feedback capacitance), can operate at very low currents

– DC-coupled pre-comparator stage: additional gain and differential threshold circuit

– Global threshold adjustable through two distributed voltages, trimmed in each pixel using one 4-bit resistor ladder in each pre-comparator branch.

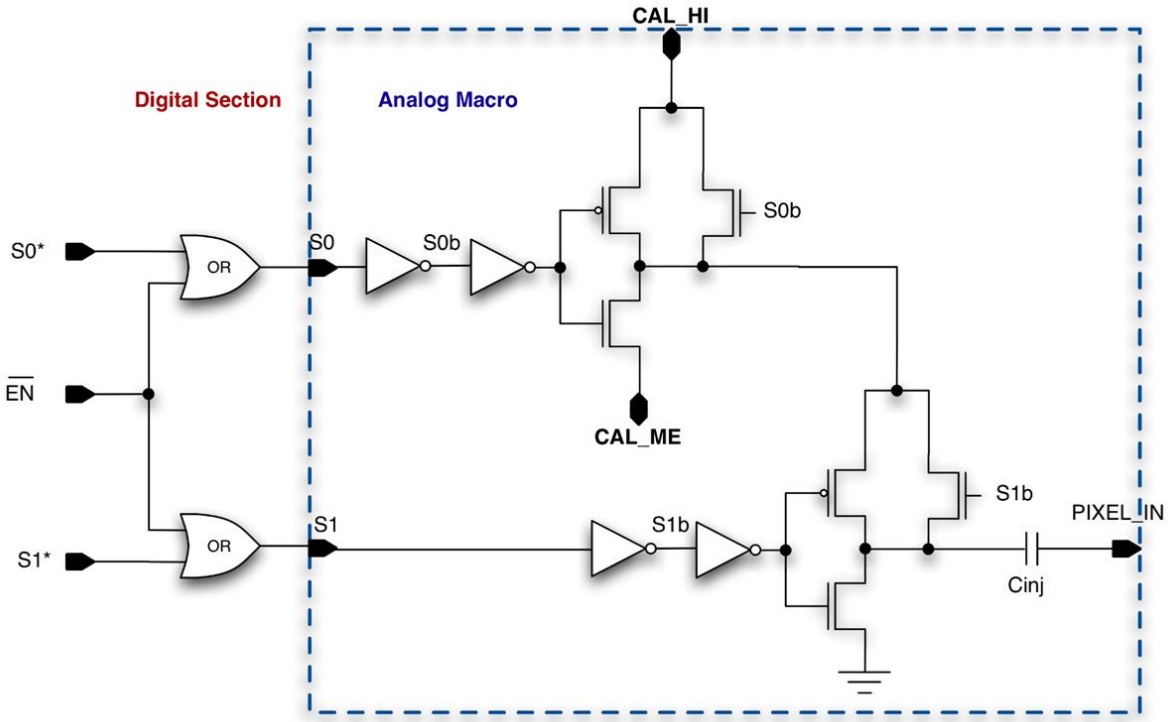
– Continuous time comparator stage with output connected to digital pixel region through logic gates

– Optimized for low-threshold operation (~500e$^-$)

– Current consumption: 4 μA/pixel at 50 fF detector load and 10 nA leakage current

3 different analog front-end designs for performance comparisons with same layout area

- Easily interchangeable on the pixel array
- Common ***calibration injection circuit*** for direct performance comparison



- Local generation of analog test pulse from 2 defined DC voltages (CAL_HI, CAL_ME) distributed to all pixels and a 3rd level (local gnd)
- Two operation modes allowing to generate 2 consecutive signals of same polarity or to inject different charges in neighboring pixels at same time
- Control signals S0 and S1 generated in digital domain and can be phase shifted with fine delay (global for the whole chip)

3 different analog front-end designs for performance comparisons with same layout area

- Easily interchangeable on the pixel array
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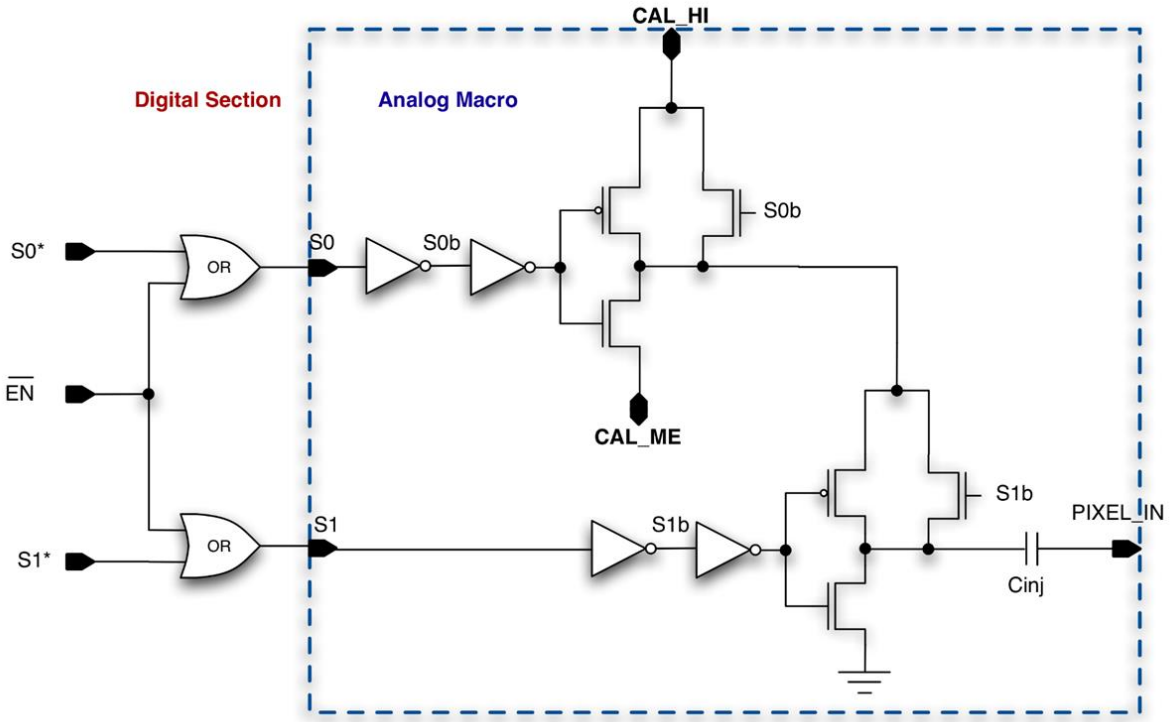

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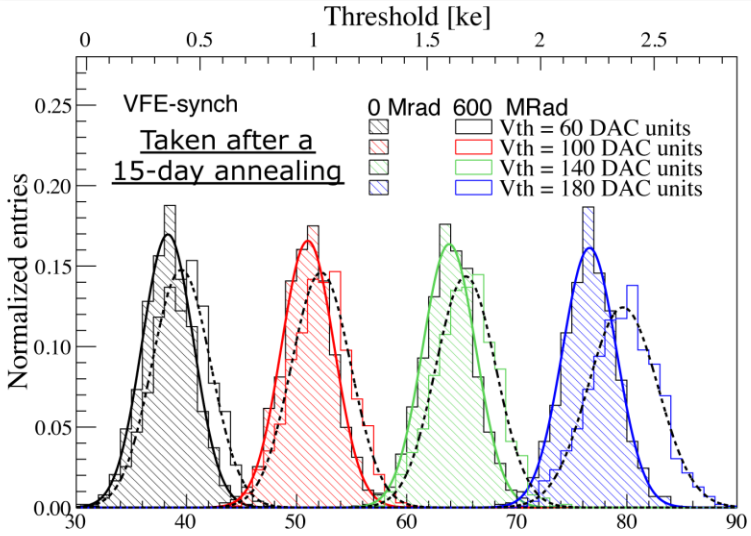
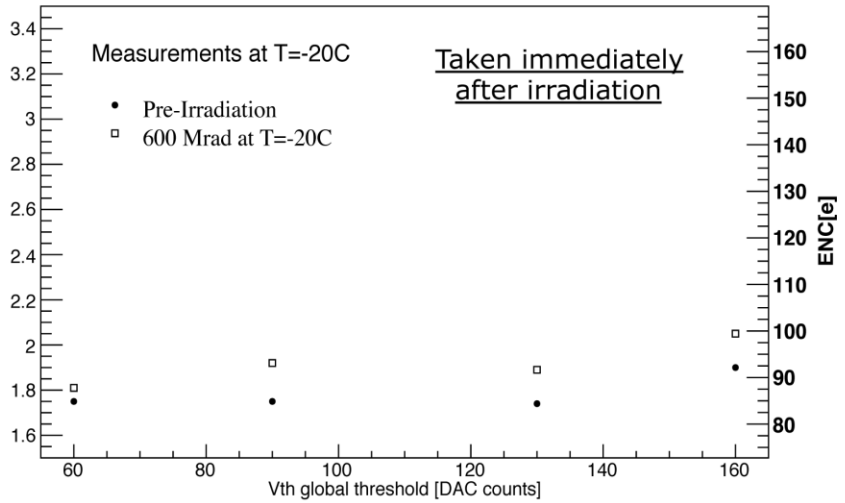
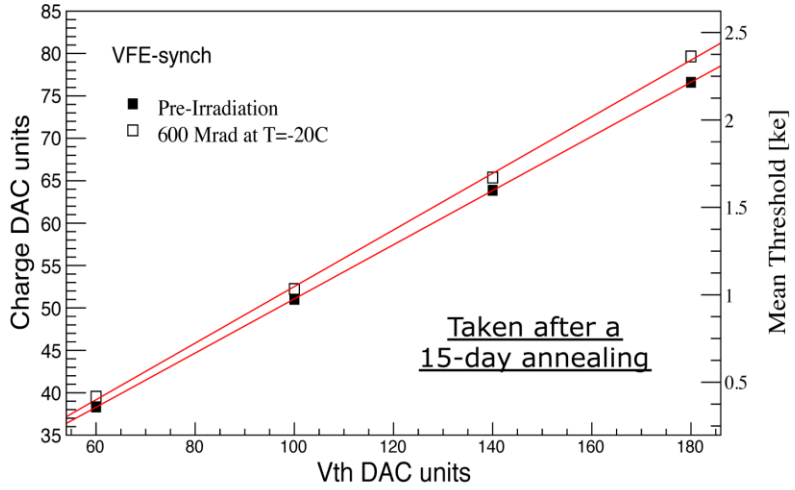
- Fast ToT counting with local oscillator

AFE irradiation campaign at -20°C

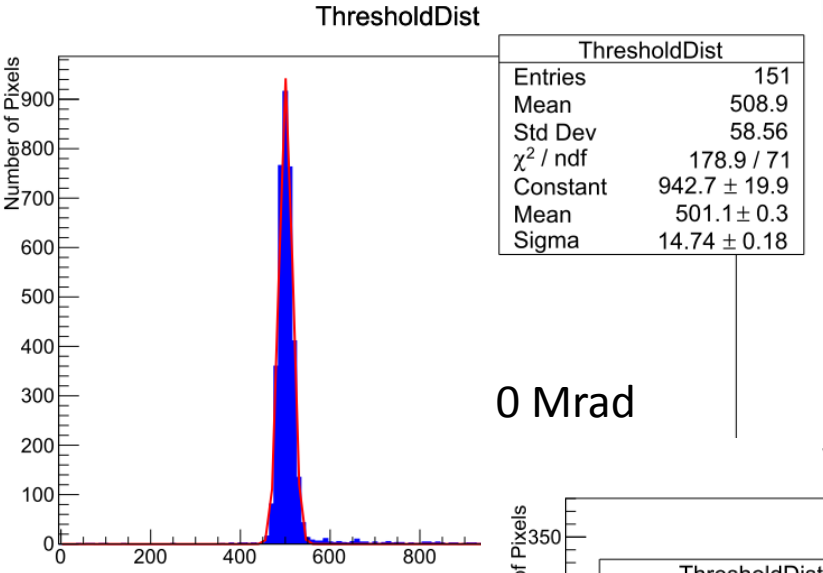


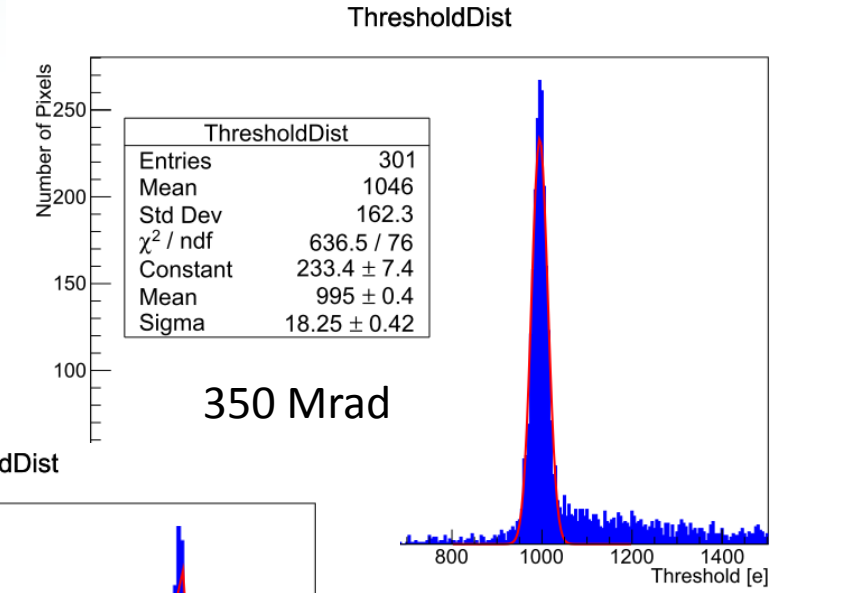


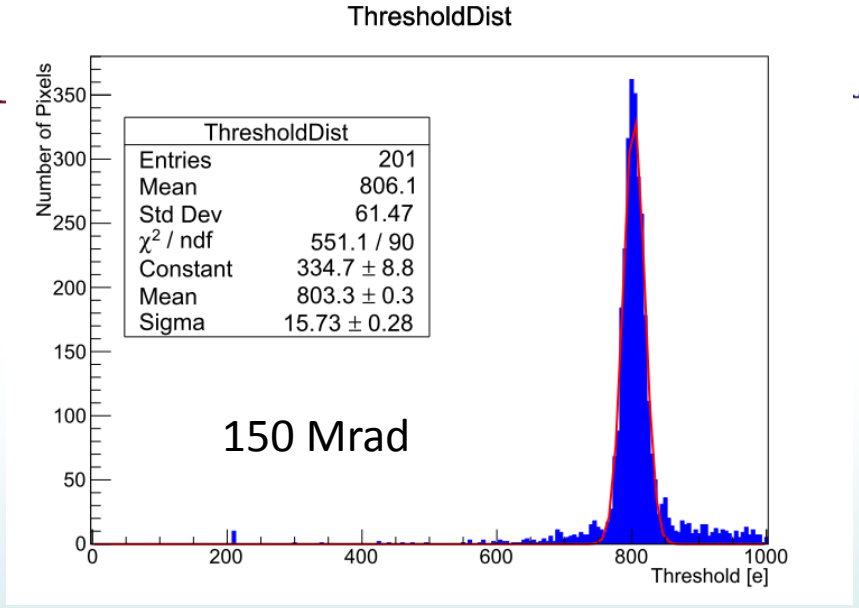


- The threshold mean value increases slightly with radiation
- Threshold dispersion increase is higher for thr > 1ke; in the region of interest below 1 ke the increment is limited to around 10%
- The ENC experiences a 10% increase at 600 Mrad

- The AFE prototype in FE65_P2 shows significant degradation of its threshold tuning capabilities



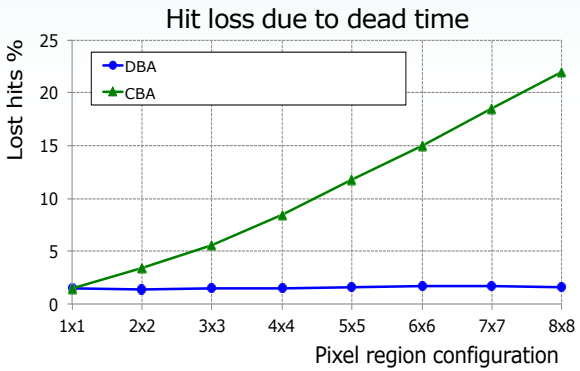


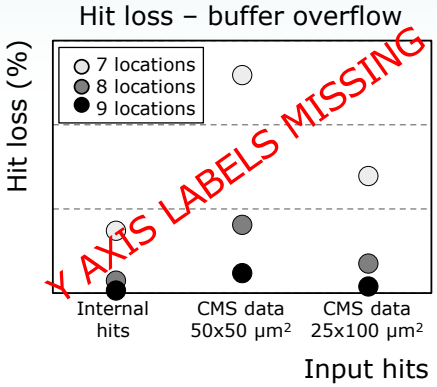


– Pixel array architecture performance metrics: hit loss and latency buffer occupancy

– Comparative study DBA-CBA:
  – at behavioral level
  – at RTL from small scale prototypes

– DBA to be preferred at behavioral level



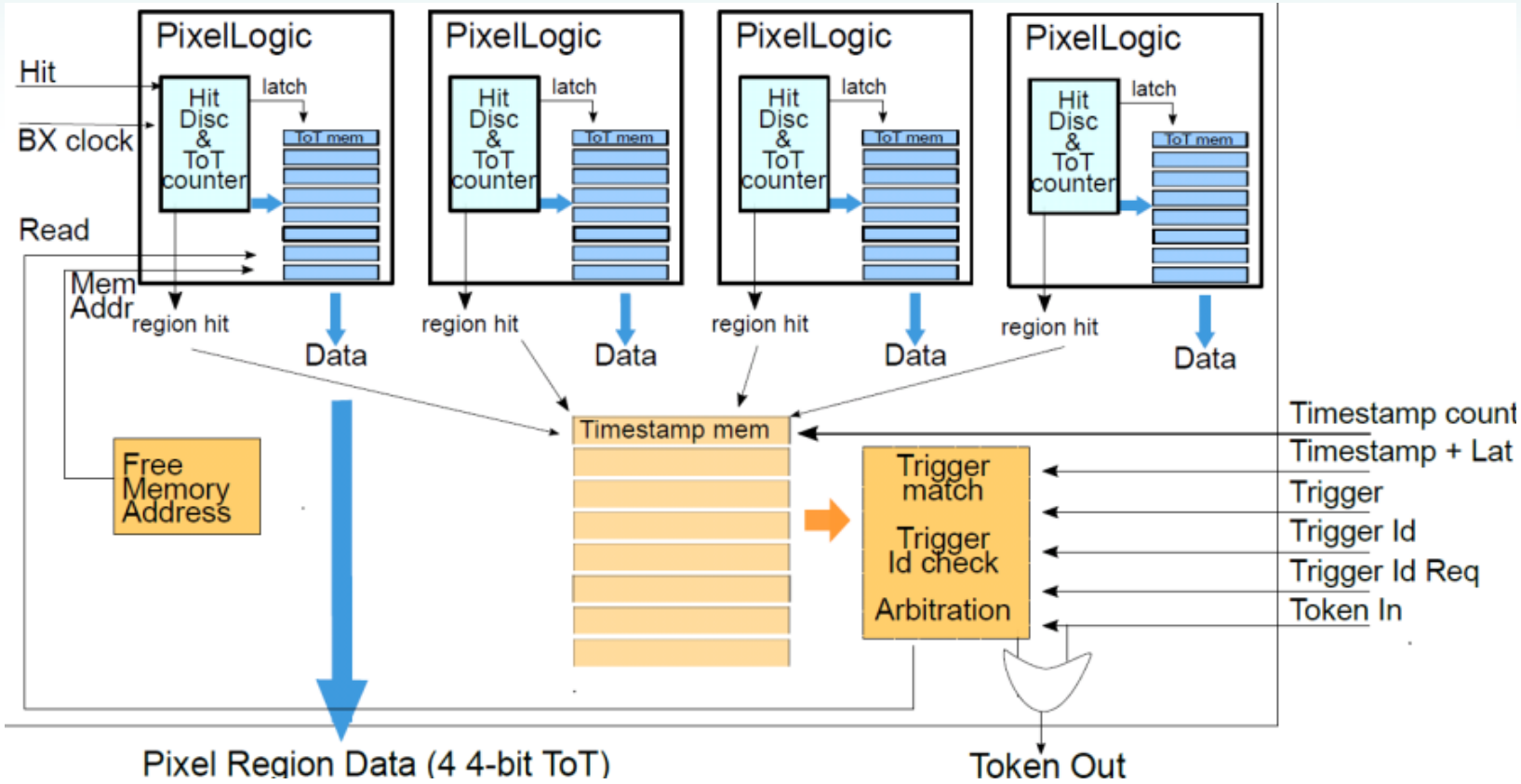


– Comparable performance found between CBA and DBA architectures in terms of buffer overflow hit loss

– Result of the study motivated further optimizations implemented into RD53A

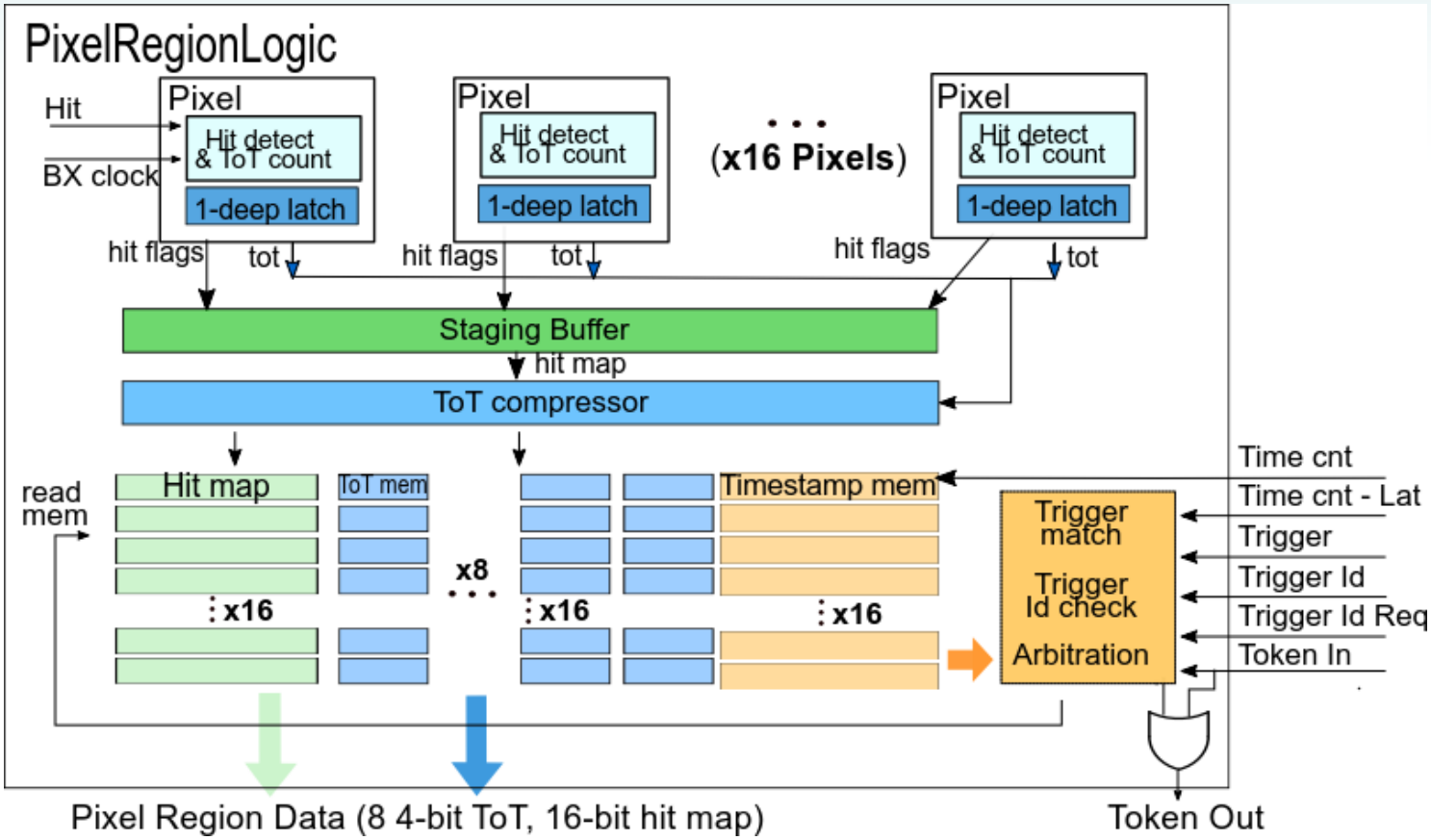
Metrics		**CBA (CHIPIX65)**	**DBA (FE65_P2)**
Hit loss (%)	*analog dead time*	3.19	0.72
	buffer overflow	*15 loc.*: 0.59 *16 loc.*: 0.24	*8 loc.*: 0.74 *9 loc.*: 0.27
Total hit loss (%)		*15 loc.*: 3.79 *16 loc.*: 3.44	*8 loc.*: 1.46 *9 loc.*: 0.99
ToT loss (%)		0.10	–

Implemented DBA architecture



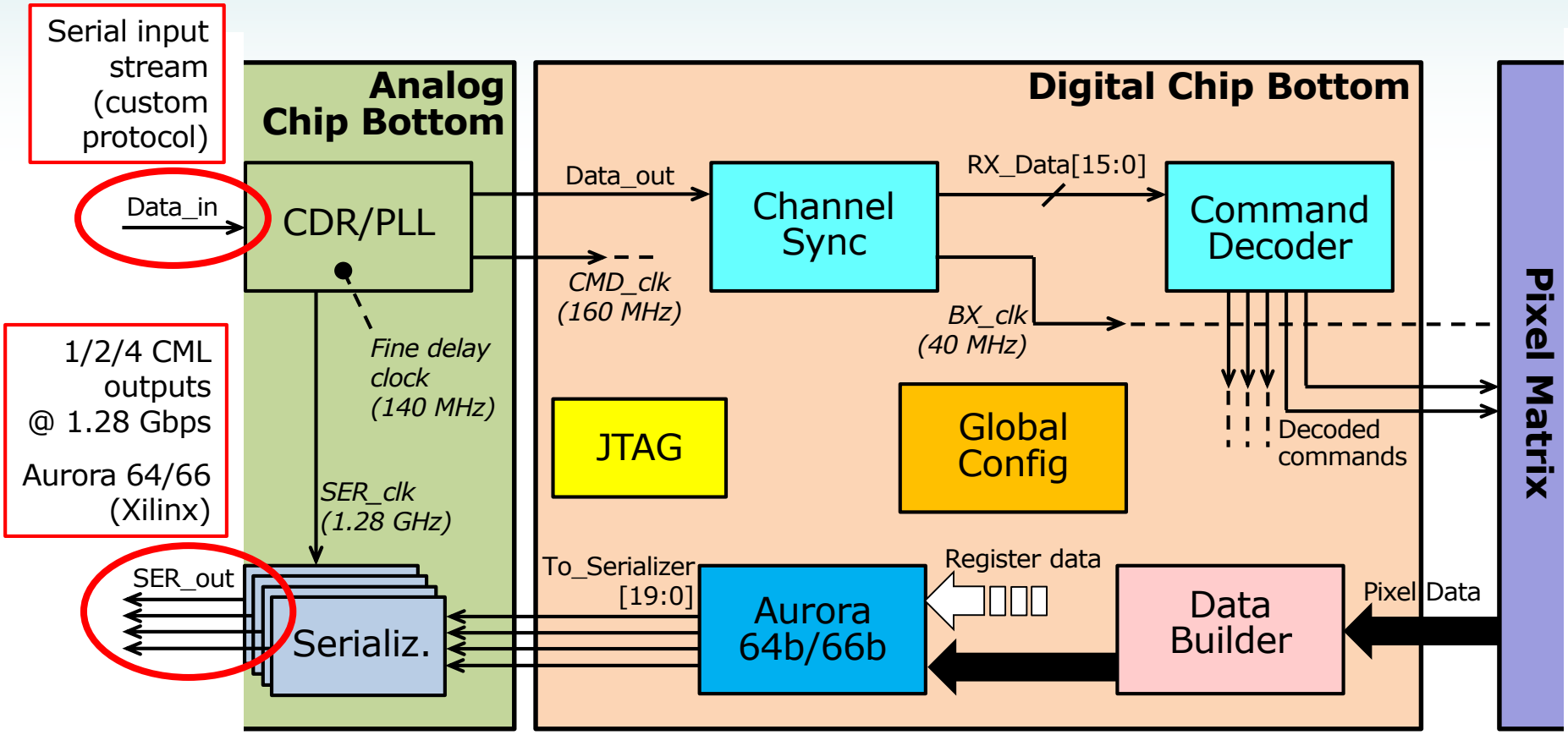
- Shared hit time buffer (latency counters)
- Independent hit charge buffer in each PUC
- 8 memory locations
- 1x4 elongated shape more convenient for buffer occupancy

Implemented CBA architecture

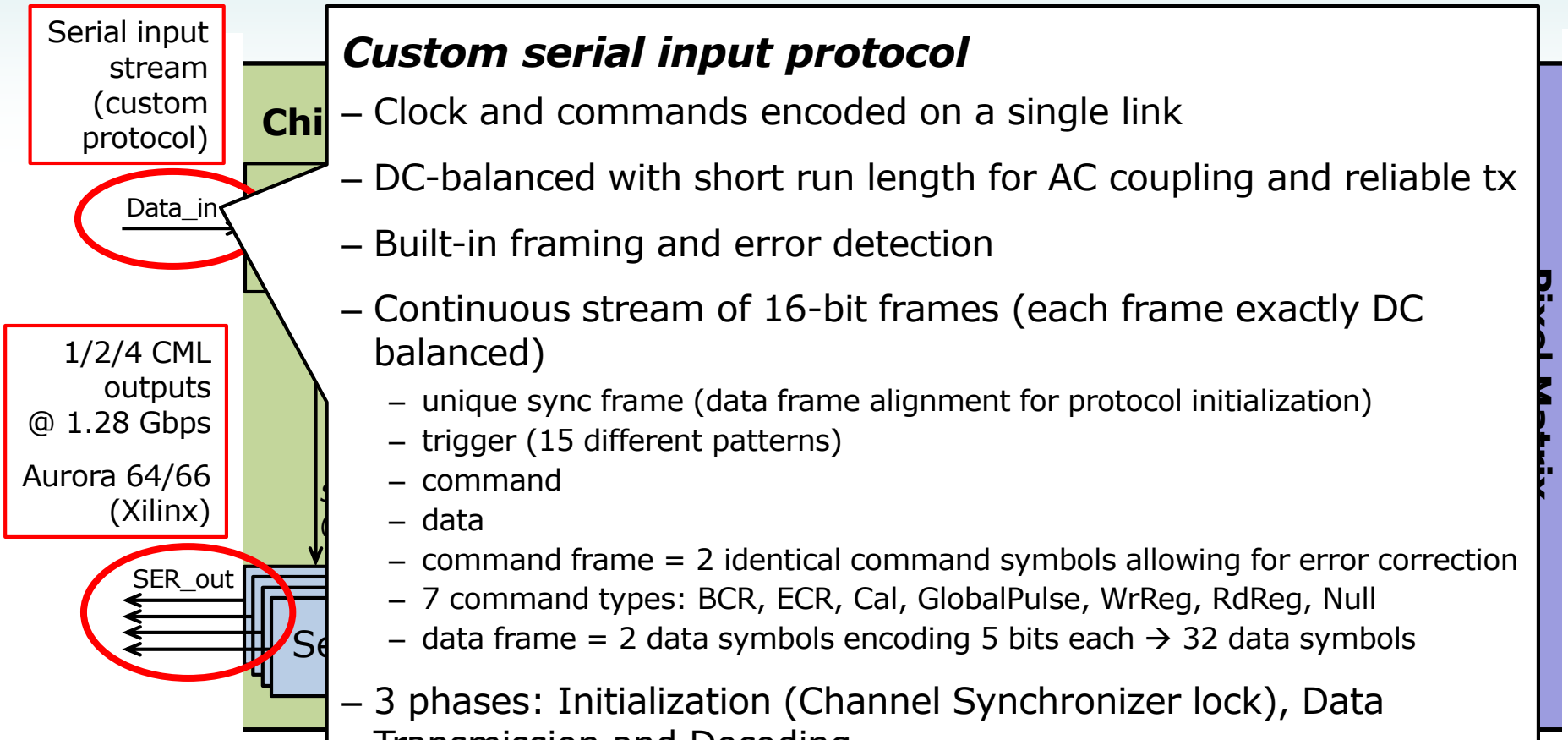


- Pixels have a latch-based single-row buffer
- Staging buffer delays hit map for Sync time Clock Cycles (2 rows deep)
- TOT Compression maps 16 TOTs into 8 slots
- 16 rows deep timestamp buffer

- Integrated with Sync analog front-end (Fast ToT)



- Different reset procedures for different parts of the chip
- Data path logic reset with ECR command
- Active low Power-On Reset (POR) generator powered from digital power internal rail (no brown-out detection)
- Asynchronous reset for Global Config register, synchronized with CMD_CLK for all other blocks

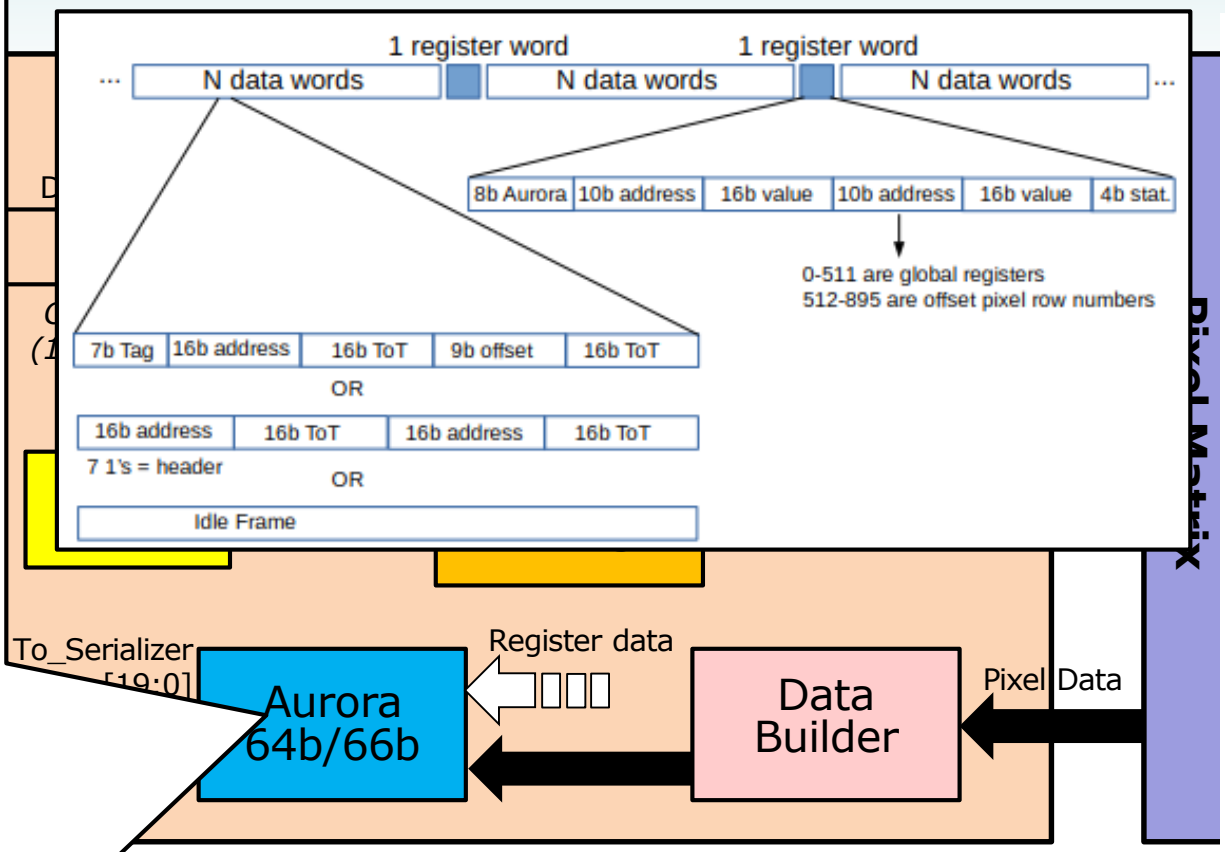


Custom serial input protocol

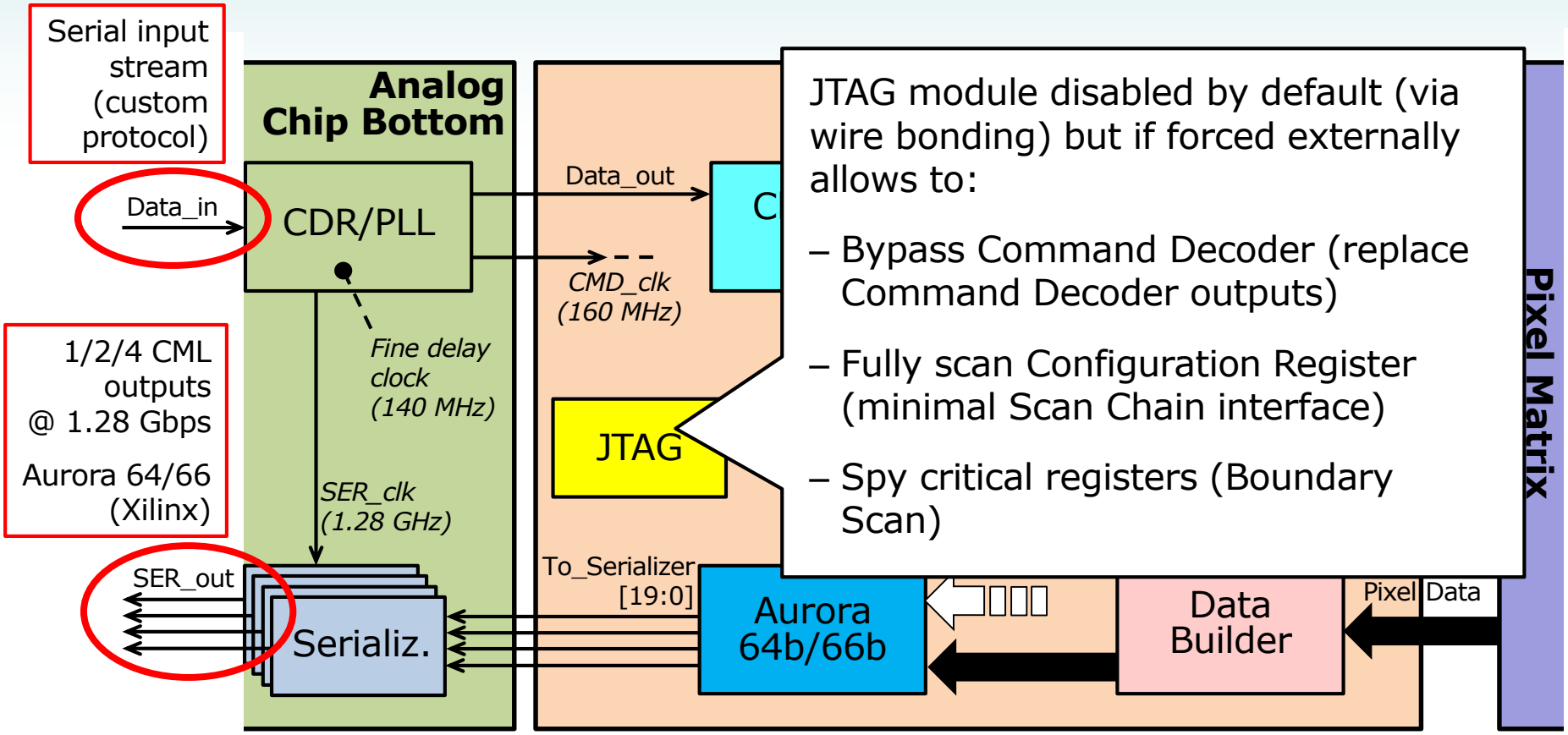
- Clock and commands encoded on a single link
- DC-balanced with short run length for AC coupling and reliable tx
- Built-in framing and error detection
- Continuous stream of 16-bit frames (each frame exactly DC balanced)
  - unique sync frame (data frame alignment for protocol initialization)
  - trigger (15 different patterns)
  - command
  - data
  - command frame = 2 identical command symbols allowing for error correction
  - 7 command types: BCR, ECR, Cal, GlobalPulse, WrReg, RdReg, Null
  - data frame = 2 data symbols encoding 5 bits each → 32 data symbols
- 3 phases: Initialization (Channel Synchronizer lock), Data Transmission and Decoding
- ChipID associated to commands with data frames: command executed only by the chip with matching geographical address (3 wirebond pads)

Output protocol: Aurora 64b66b

- All data, messages, and configuration readback serialized with the Aurora protocol and transmitted on 1 to 4 parallel lanes (1.28 Gbps each, programmable)
- Multilane Aurora protocol using strict alignment: all lanes send same type of Aurora frame (66-bits long)
- Output stream: N_D data frames + 1 register/service frame (N_D:1 ratio programmable)

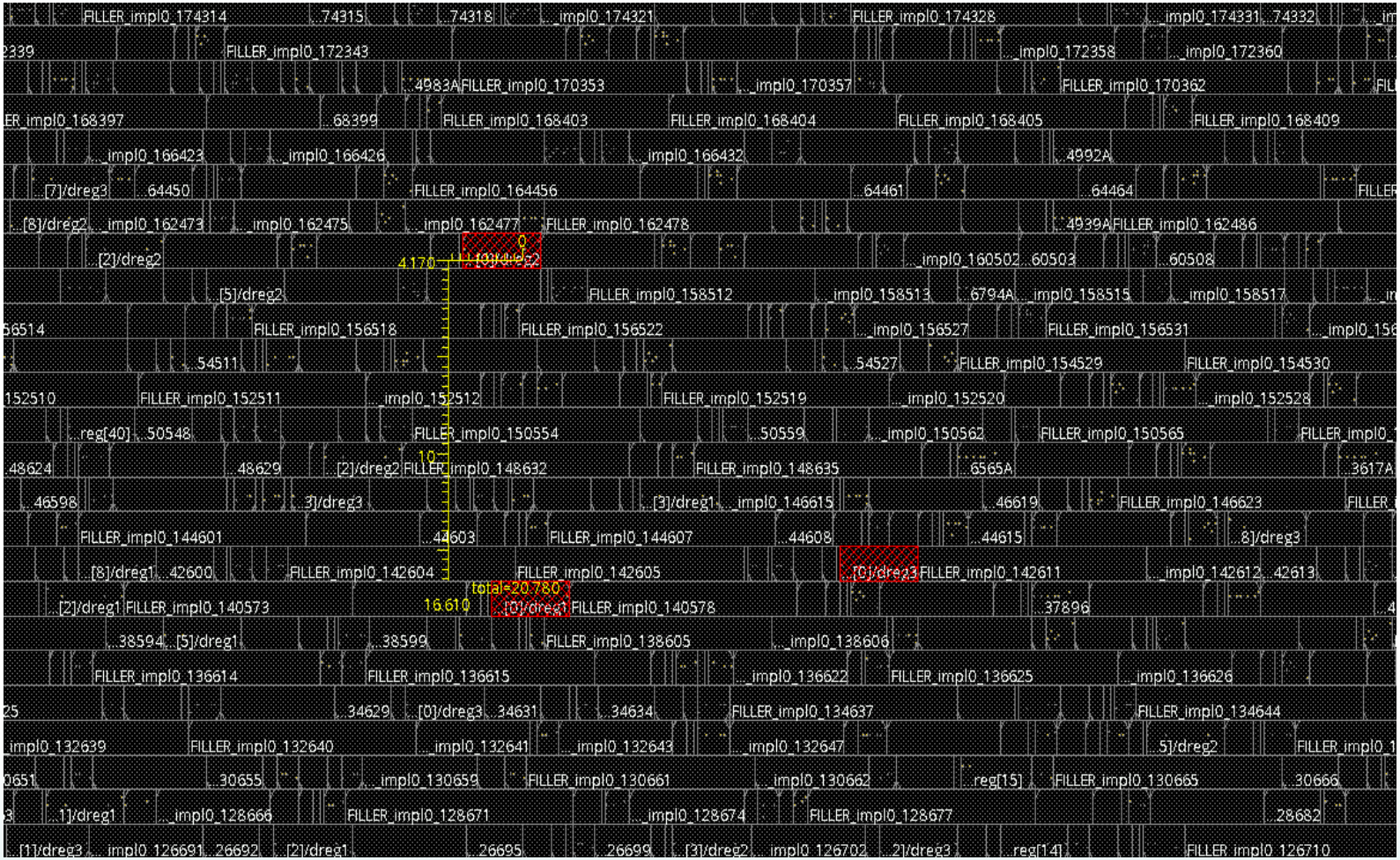


parallel token chain one trigger at a time



– We need to have a working chip even in case of malfunctioning blocks
  → we must be able to completely bypass critical blocks
– CMD_CLK and SER_CLK can be externally bypassed

SEU: TMR placement



(*see Sandeep Miryala's presentation*)

Analog front-end bias

2-stage structure:

1. Global V/I provided by 10-bit current steering DACs in ACB
2. After current scaling biases are distributed to MacroColumnBias cells where final bias is distributed in parallel to 384 pixels (768) of two adjacent columns

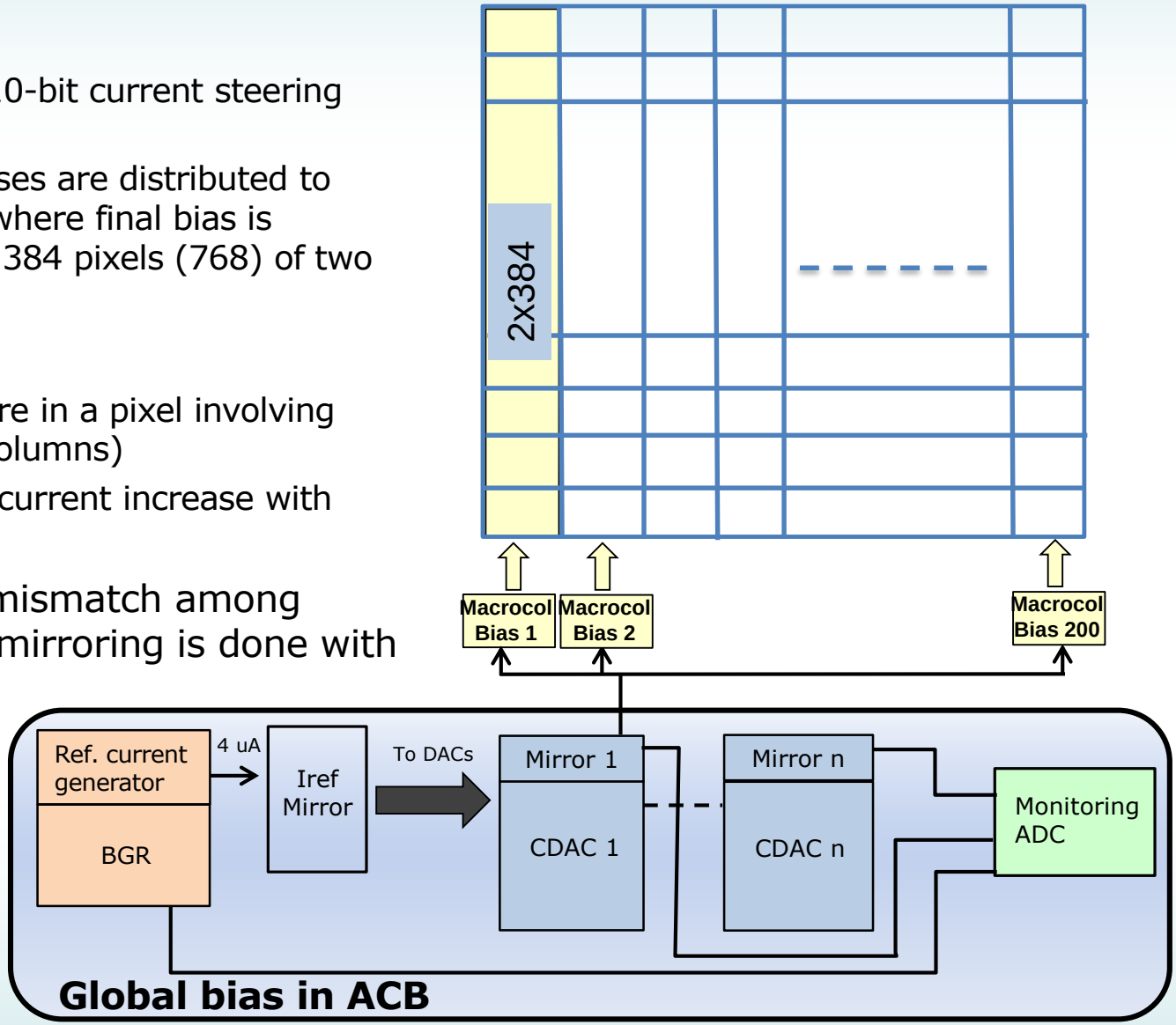
Advantages:

– Improved reliability (failure in a pixel involving bias lines affects only 2 columns)

– Limited effect of leakage current increase with radiation

Drawback: increase of mismatch among pixels, (but 1st current mirroring is done with large transistors)

All DACs currents can be read back from Monitoring block



RD53A test preparation

- RD53A test working group preparing testing
  - Chips will come in November
- Test systems being prepared:
  - A. PC plug-in Hardware:
    - Commercial PCI-E FPGA card
    - Custom FMC adapter card
  - B. Standalone custom card: Ethernet
  - Single chip card with standardized interface:
    - Command/clock line and Readout link(s) on standard display port cable
    - Power prepared for serial powering
  - Multi-chip hybrids: In the pipeline for later tests
  - Firmware,
  - Software
  - Based on previous experience with FEI4 test systems
- Pixel sensors being produced in both ATLAS and CMS.
- Bump-bonding being prepared
  - RD53A dummy wafers and sensors for initial trials
  - 300mm wafer handling in HEP community and BB compa
    - Community getting equipped with 300mm wafer probers
- Radiation testing
- Many systems will be used in ATLAS/CMS pixe community